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Optimizing Throughput for Limited Receiver Circuit Power

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Abstract—Maximizing the battery life time of mobile devices and sensor nodes increasingly becomes a challenge, and receiver power consumption tends to become more problematic than delivering adequate transmit power. We address the challenge of achieving the highest possible throughput per Watt of receiver circuit power. Our results show that optimum and adaptive tuning of the front-end parameters of the receiver can result in substantial power savings, compared to the common practice of a design for worst case conditions. We obtain a closed form solution for maximum throughput and the corresponding optimal overall system specifications. We confirm that handling the interference from nearby channels has a large influence, and our analysis concludes that adaptive control of the IP3 performance has an overarching impact. We further describe how the adaptive overall system settings can be translated into optimum gain and IP3 specifications of each of the individual stages that form the receiver cascade, considering both the accumulation of circuit noise and distortion products. The example of a WLAN system is elaborated to illustrate our method.

I. INTRODUCTION

In current mobile receivers, such as laptops and cell phones, the radio frequency (RF) signal processing is a major factor that influences battery life time. In the absence of disruptive new approaches, we expect this trend will continue for the foreseeable future. Currently, mobile users spend more and more time downloading data. Therefore, the receiver power consumption becomes a more prominent power consuming part of the battery limited side of the transceiver chain.

The aim of our analysis is to find an appropriate operation point for each of the analog stages of a power-constrained receiver, such that its user data throughput is maximized.

For our analysis we restrict ourselves to a commonly used receiver architecture. A broad band signal is processed at radio frequency (RF) by the analog front end, where the wanted signal only occupies a small portion of the front-end bandwidth. The analog front end amplifies, down-converts, and filters the desired signal from the received broadband signal and presents the signal to the ADC.

Therefore, the first stages of our receiver need to handle a broadband signal which usually contains strong adjacent channel interferers, with a priori not fully known statistical properties [1]. These signals need to be handled with adequate linearity to avoid excessive distortion spill-over into the band of the desired signal [2]. Typically, a higher linearity requirement leads to a higher power consumption of the analog circuit. Commonly, the linearity is specified for the highest power of the interference at which the receiver should still operate. This results in an overly linear design at all lower values of the interference power, which is a waste of energy and reduces battery lifetime unnecessarily.

Commonly, an RF design is based on a set of system specifications, determined by standardization [2], which may include packet error rates, sensitivity and modulation. An RF designer strives to achieve the lowest power design possible, for a fixed overall specification target [3], [4]. However, we address the converse, given an available receiver circuit power budget we determine the maximum throughput. To achieve this optimum we do not define the system requirements a priori. Rather, we assume the key system settings are variable. This optimum might seem to depend on a large number of independent variables, but since we are designing at the minimum power consumption in a given IC process it is known from theory that several variables can be linked in this minimum [5]. This reduces the number of independent variables which determine the optimum of the throughput.

A main contribution of this work is that we reduce the optimization of the throughput to one variable from which all other variables can be derived and that this optimum is unique. Furthermore, the result shows that by far the most dominant factor in power consumption for low power designs is the linearity requirement. This is graphically shown by varying the interference power relative to the wanted signal power and plotting the subsequent throughput versus power consumption.

II. MODELING SYSTEM THROUGHPUT

To determine which variables are dominant in low power design we strive to optimize the throughput $T$ for a given receiver circuit power budget $P_r$, according to

$$\hat{T} = \max T.$$  \hfill (1)

Here the maximum is taken over all possible settings of the RF stages, provided that the total consumed power does not exceed $P_r$. We further use the capacity expression as a measure of achievable throughput $T$ for the modeled AWGN system.

$$T = \log_2 \left(1 + \frac{S}{N_{\text{tot}}}\right)$$ \hfill (2)
where $S$ is the input signal power. The total noise plus distortion, relative to power levels at the input, is

$$N_{\text{tot}} = N_{\text{th}} + \frac{N_r}{G_{\text{tot}}} + \frac{N_d}{G_{\text{tot}}},$$

(3)

where $N_{\text{th}}$ is the noise in the channel, $N_r$ the electronics noise added by the analog circuits of the receiver, and $N_d$ is the distortion caused by an interferer. Other noise sources such as LO leakage, DC leakage and images are not considered, since they are related to the architecture, topology and layout, which are beyond the scope of this paper. The AWGN noise in the channel is given by

$$N_{\text{th}} = kT B,$$

(4)

where $k$ is Boltzmann’s constant, $T$ is the temperature and $B$ is the bandwidth of the desired signal. Further, $G_{\text{tot}}$ is the total maximum power gain of the analog receiver given by

$$G_{\text{tot}} = \prod_{m=1}^{M} G_m,$$

(5)

where $G_m$ is the gain of the $m^{th}$ stage in the cascade (Figure 1). We now need a more detailed model of $N_d$ and $N_r$.

A. Distortion and Noise

We obtain the distortion power $N_d$ in (3) via the third order input referred intercept point $IP3$. The $IP3$ is a measure of the linearity of the analog circuits in the receiver [2]. Total $IP3$, $IP3_{\text{tot}}$, is defined as

$$IP3_{\text{tot}} = P_{\text{int}} \sqrt{\frac{P_{\text{out}}}{N_d}}$$

(6)

where $P_{\text{out}}$ is the output power in the channel of the interferer due to the received channel interference power $P_{\text{int}}$. $IP3_{\text{tot}}$ corresponds to the extrapolated input power at which $P_{\text{out}}$ and $N_d$ are equal. For an analog receiver the output power is $P_{\text{out}} = G_{\text{tot}}P_{\text{int}}$, with $P_{\text{int}}$ the input power. Therefore we can substitute $P_{\text{out}}$ in (6) by $G_{\text{tot}}P_{\text{int}}$. The distortion can now be expressed as

$$N_d = \frac{G_{\text{tot}}^3 P_{\text{int}}}{IP3_{\text{tot}}}.$$  

(7)

We simplify our model by assuming that after further channel selectivity filtering, Nyquist sampling and A/D conversion, the baseband processing engine of the receiver has no further knowledge of this distortion signal, and experiences it as AWGN. The total worst case $IP3$ of $M$ stages can be calculated via [5]

$$IP3_{\text{tot}} = \left( \sum_{m=1}^{M} \prod_{j=1}^{m-1} G_j \right)^{-1},$$

(8)

under the worst case assumption that all distortion components are in-phase. Here $IP3_{\text{m}}$ is the third order intercept point of the $m^{th}$ stage.

Next to the distortion signals, the analog front end adds noise $N_r$ to the desired signal. This addition of noise is modeled via the noise figure (NF), and is defined as $NF = 10 \log_{10}(F_m)$. Here, the noise factor $F_m$ is defined as:

$$F_m = \frac{SNR_m}{SNR_{m+1}},$$

(9)

where $SNR_m$ is the SNR at the input, and $SNR_{m+1}$ is the SNR at the output of the $m^{th}$ stage in a cascade. Note that the noise figures do not model the contribution by distortion. The total noise-factor of $M$ stages in a cascade, $F_{\text{tot}}$, can be calculated via Friis formula

$$F_{\text{tot}} = 1 + \sum_{m=1}^{M} \frac{F_m - 1}{\prod_{j=1}^{m-1} G_j},$$

(10)

where $F_m$ the noise-factor of the $m^{th}$ stage and $G_j$ the gain of the $j^{th}$ stage. Moreover, the total noise factor must satisfy

$$F_{\text{tot}} = 1 + \frac{N_r}{G_{\text{tot}}N_{th}},$$

(11)

where $G_{\text{tot}}$ is the total gain of the analog circuit and $N_r$ is the variance of the electronics noise added by all analog circuits weighed with the partial gains. Note that the distortion noise does not contribute to the noise figure. The electronics noise can now be expressed as

$$N_r = (F_{\text{tot}} - 1) N_{th} G_{\text{tot}}$$

(12)

By combining (3) (7) and (12), the total noise plus distortion, normalized to power levels present at the input, is now given by

$$N_{\text{tot}} = F_{\text{tot}} N_{th} + \frac{P_{\text{int}}^3}{IP3_{\text{tot}}},$$

(13)

while achieving $IP3_{\text{tot}}$ using (8) and $F_{\text{tot}}$ using (10). Figure 1 now depicts how the receiver is modeled, every individual stage has variable gain ($G_1$, · · · , $G_M$) and $IP3$ ($IP3_1$, · · · , $IP3_M$), thus allowing for variable $IP3_{\text{tot}}$ and variable $F_{\text{tot}}$ of the receiver cascade.

B. Optimum Throughput

Our aim is to optimize the power budget $P_r$ over the various stages such that throughput $T$ is optimum under the constraint of a given technology, a given received power $S$, total gain $G_{\text{tot}}$ needed to drive the ADC and channel parameters $N_{th}$ and $P_{\text{tot}}$. The optimization is done in a two staged approach by using $F_{\text{tot}}$ and $IP3_{\text{tot}}$ as an intermediate design variable.

Section II-C.1 first addresses how for a chosen $F_{\text{tot}}$ and $IP3_{\text{tot}}$ one can optimize the power budget $P_r$ by optimally distributing the gains ($G_1$, · · · , $G_M$) and $IP3$'s
Optimization (MPCO) solves:

\[ P_{\text{min}} = \min \left( \sum_{m=1}^{M} P_m \right) , \quad (14) \]

where \( P_m \) is the power dissipation of circuit block \( m \), for a given technology, as will be covered by (18). Section II-C extends the MPCO by further optimizing \( P_{\text{tot}} \) and \( IP_{3\text{tot}} \) to satisfy our end goal of maximizing the throughput per unit of consumed circuit energy, thus searching for

\[ \hat{T} = \max_{F_{\text{tot}}, IP_{3\text{tot}}} (T) , \quad (15) \]

where the available receiver circuit power \( P_r \), satisfies \( P_r = P_{\text{min}} \), as in (14). By substituting (2) and (3) in (15), we can show that maximizing (15) corresponds to

\[ \hat{N}_{\text{tot}} = \min_{F_{\text{tot}}, IP_{3\text{tot}}} (N_{\text{tot}}) . \quad (16) \]

A main contribution of this paper is that we can reduce the minimization of (16) to one variable. This is achieved by expressing the power optimal \( IP_{3\text{tot}} \), called \( IP_{3\text{tot}}^* \), as a closed form function (22) of the figure of merits related to the used IC design process, the available receiver circuit power \( P_r \), the power optimal total noise factor \( F_{\text{tot}} \) and total gain \( G_{\text{tot}} \). Therefore, we can write \( N_{\text{tot}} \) as a function of \( F_{\text{tot}} \) and the available receiver circuit power \( P_r \). Our claim is that in the end (16), for a given power budget \( P_r \), is equal to

\[ \hat{N}_{\text{tot}} = \min_{F_{\text{tot}}} \left( N_{\text{tot}}(IP_{3\text{tot}}^*) \right) . \quad (17) \]

We will call this an Minimum Throughput Cascade Optimization Method (MTO).

C. Minimum Power Cascade Optimization Method

1) Linearity Factor Model: Traditionally, designers aim at achieving the system specifications for \( IP_{3\text{tot}}, F_{\text{tot}}, \) and \( G_{\text{tot}} \) at minimal power dissipation. This, justifies the use of an equivalent figure of merit (EFOM) [5], such as

\[ P_m = \frac{f_m G_m}{\kappa_m} IP_{3\text{tot}}^*, \quad (18) \]

where \( f_m \) is the power limiting bandwidth and \( \kappa_m \) is the power linearity factor of the \( m^{th} \) stage. The most appropriate parameter to choose for \( f_m \) highly depends on the circuit functionality. For LNAs with a dominant pole, the bandwidth is an appropriate choice. By using an EFOM, \( P_m \) theoretically does not depend on the noise figure \( F_m \).

2) Dual Lagrange Optimization Method: So,

\[ P_{\text{min}} = \min \left( \sum_{m=1}^{M} \frac{f_m G_m}{\kappa_m} IP_{3\text{tot}}^* \right) \quad (19) \]

while achieving the \( G_{\text{tot}} \) using (5), \( IP_{3\text{tot}} \) using (8), and \( F_{\text{tot}} \) using (10). In this optimization process, the \( f_m, \kappa_m, \) and \( F_m \) of a cascade are taken as constant. The individual \( F_m \) is kept constant because the \( F_m \) is fundamentally limited by the topology and used technology. A closed form expression can be derived [5] for the minimal analog signal conditioning (ASC) power dissipation as a function of the overall noise factor \( F_{\text{tot}} \),

\[ P_{\text{min}} = IP_{3\text{tot}} \left( \sqrt{\frac{f_m G_m}{\kappa_m}} + \frac{F_w}{(F_{\text{tot}} - F_1)} \right)^2 . \quad (20) \]

where the "weighed excess noise factor" \( F_w \) is defined as

\[ F_w = \left( \sum_{m=1}^{M-1} \sqrt{\frac{f_m}{\kappa_m}} (F_m + 1) \right)^3 . \quad (21) \]

D. Maximum Throughput Cascade Optimization Method

Whereas (20) gives the minimum power \( P_{\text{min}} \) needed to satisfy a required \( IP_{3\text{tot}} \), we can conversely claim that the best \( IP_{3\text{tot}} \) that one can achieve for a given available \( P_r \) equals

\[ \text{IP}_{3\text{tot}} = P_r \left( \sqrt{\frac{f_m G_m}{\kappa_m}} + \frac{F_w}{(F_{\text{tot}} - F_1)} \right)^2 . \quad (22) \]

Now, we can rewrite the total noise (3) as a function depending on \( F_{\text{tot}}, P_{\text{min}} \) and \( P_{\text{min}} \),

\[ N_{\text{tot}} = F_{\text{tot}} N_{\text{th}} + \frac{P_{\text{th}}^2}{P_r^2} \left( \sqrt{\frac{f_m G_m}{\kappa_m}} + \frac{F_w}{(F_{\text{tot}} - F_1)} \right)^4 . \quad (23) \]

The noise factor is a real positive number which is \( F_{\text{tot}} \geq F_1 \).

1) Maximizing Throughput: By combining (1), (2), (3), and (23), we can maximize \( T \) by minimizing \( N_{\text{tot}} \). We require that

\[ \frac{dN_{\text{tot}}(F_{\text{tot}})}{dF_{\text{tot}}} \mid_{F_{\text{tot}} = \hat{F}_{\text{tot}}} = 0 \quad (24) \]

and obtain \( \hat{F}_{\text{tot}} \) as \( \hat{F}_{\text{tot}} = \\

\[ F_1 + \frac{4F_w}{\sqrt{\frac{f_m G_m}{\kappa_m}} + \sqrt{\frac{f_m G_m}{\kappa_m} + 25/3 \left( \frac{F_w N_{\text{th}} P_r^2}{P_{\text{tot}}} \right)^{1/3}}} \quad (25) \]

Applying this value of \( \hat{F}_{\text{tot}} \) means that (12) turns into

\[ N_{\text{tot}} / G_{\text{tot}} = \\

\[ (F_1 - 1) N_{\text{th}} + \left( \sqrt{\frac{f_m G_m}{\kappa_m}} + \sqrt{\frac{f_m G_m}{\kappa_m} + 25/3 \left( \frac{F_w N_{\text{th}} P_r^2}{P_{\text{tot}}} \right)^{1/3}} \right) 2 . \quad (26) \]

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TABLE I: Typical design choices for cascades in an ASC (LNA [6], Mixer [7], and Output buffer [8]). Where, numbers denoted in italics are considered as variable in this paper.

<table>
<thead>
<tr>
<th>Block</th>
<th>LNA</th>
<th>Mixer</th>
<th>Buffer</th>
</tr>
</thead>
<tbody>
<tr>
<td>NF [dB]</td>
<td>16</td>
<td>9.5</td>
<td>10.7</td>
</tr>
<tr>
<td>Gain [dBm]</td>
<td>4</td>
<td>10.2</td>
<td>19</td>
</tr>
<tr>
<td>P_{in} [mW]</td>
<td>765.10^4</td>
<td>178.10^8</td>
<td>1.22.10^9</td>
</tr>
<tr>
<td>f_m [MHz]</td>
<td>100</td>
<td>2500</td>
<td>22</td>
</tr>
</tbody>
</table>

![Fig. 2: Throughput for different values of CIR, versus receiver power P_r for a WLAN system.](image1)

![Fig. 3: Bits per Joule for different values of CIR, versus receiver power P_r for a WLAN system.](image2)

and (7) turns into \( N_d/G_{tot} = \)

\[
\frac{P_{tot}}{P_r} \left( \sqrt{\frac{1}{\kappa_{lat}} G_{tot}} + \sqrt{\frac{1}{\kappa_{lat}} G_{tot} + 2^{9/3} \left( \frac{F_i N_d P_0}{P_{int}} \right)^{1/3}} \right) ^4 \tag{27}
\]

which we insert in (2) and (3). We now have found an analytically closed form solution which maximizes the throughput for a given circuit power budget \( P_r \). We also found closed form solutions for \( F_{tot} \) and \( IP^3_{tot} \) that achieve the optimum throughput, respectively (25) and (22) with (25) inserted. The individual gain \( (G_1, \ldots, G_M) \) and \( IP^3 (IP^3_1, \ldots, IP^3_M) \) per stage follow from (5).

III. NUMERICAL RESULTS

Figure 2 and 3 show the results for the system specifications, \( S/N_{th} = 30 \text{ dB}, k = 1.38 \times 10^{-23}, T = 295K, B = 22 \text{ MHz}, \) and \( G_{tot} = 65\text{ dB} \), when using the EFOM of the building blocks of Table I. The considered technology is 90nm CMOS. The characteristic frequencies \( f_m \) are chosen to satisfy the frequency requirements of an IEEE802.11b system in the 2.4 GHz band. Therefore, \( f_m \) is for the LNA \( f_1 = 100 \text{ MHz}, \) the mixer \( f_2 = 2500 \text{ MHz}, \) and the output buffer \( f_3 = 22 \text{ MHz}. \) Channel to interference ratio (CIR) is defined as, \( \text{CIR} = S/IP_{int} \). The closed form solution for optimum throughput as a function of available receiver power, using (2), (3), (26) and (27), is depicted in figure 2. For large available receiver power the throughput approaches the throughput for a signal 30 dB above thermal noise, and LNA with noise figure \( F_1 = 1.7 \text{ dB} \). At small available receiver power \( N_r \) and \( N_0 \) become dominant. The figure shows that when the CIR is decreased, the power needed to achieve a certain throughput is increased. A relation between CIR and power consumption was reported earlier [1]–[5], but we now have formalized this relation.

The closed form solution for maximizing throughput can be extended to express bits per Joule as a function of available receiver power \( BT/P_r \), using (1), (2), (3), (26) and (27). The result is depicted in figure 3. When the CIR is decreased, the efficiency in bits per joule for a given available receiver power is decreased as well.

IV. CONCLUSIONS

An analytically closed form solution has been presented which maximizes the throughput for a given available receiver circuit power. From the maximized throughput all other receiver system specifications such as \( IP^3 \) and \( F \) can be derived. In turn, these derived system specifications allow us to derive the specification of the individual stages which form the receiver cascade. Furthermore, the closed form solution allows us to formalize the relation between interference power and achievable throughput for a given available receiver circuit power budget.

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