Technology exploration for adaptive power and frequency scaling in 90nm CMOS

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Technology Exploration for Adaptive Power and Frequency Scaling in 90nm CMOS

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ABSTRACT
In this paper we examine the expectations and limitations of design technologies such as adaptive voltage scaling (AVS) and adaptive body biasing (ABB) in a modern deep sub-micron process. To serve this purpose, a set of ring oscillators was fabricated in a 90nm triple-well CMOS technology. The analysis hereby presented is based on two ring oscillators running at 822MHz and 93MHz, respectively. Measurement results indicate that it is possible to reach 13.8x power savings by 3.4x frequency downscaling using AVS, ±11% power and ±8% frequency tuning at nominal conditions using ABB only, 22x power savings with 5x frequency downscaling by combining AVS and ABB, as well as 22x leakage reduction.

Categories and Subject Descriptors
B.7.1 [Integrated Circuits]: Types and Design Styles – advanced technologies, algorithms implemented in hardware, VLSI (very large scale integration).

General Terms
Measurement, Performance, Design.

Keywords
CMOS, adaptive voltage scaling, adaptive body bias, performance optimization, low power, leakage.

1. INTRODUCTION
In recent years the application of adaptive techniques to control either or both power supply (V_{DD}) and threshold voltage (V_{th}) has gained increased attention. This stems from the fact that modern electronics are hampered by the variation of fundamental process and performance parameters such as threshold voltage and power consumption. Design technologies such as AMD’s PowerNow! [1], Transmeta’s LongRun [2], Intel’s Enhanced SpeedStep [3], to mention some instances, are vivid examples of commercial ICs that use power management based on power supply scaling. In addition to these commercial accomplishments, chip demonstrators with V_{DD} and V_{th} scaling capabilities have also been reported in the literature archival [4]-[8]. Other reported uses of V_{DD} and V_{th} scaling, besides power management in processors, are in testing [9], product binning [10], and yield tuning [11].

As the benefits of V_{DD} and V_{th} scaling have already been proved, in this paper we concentrate on quantitative pointers for using such know-how in deep sub-micron technologies. In particular, we want to find what the expected power savings are, what power-delay tradeoffs can be made, understand present static and dynamic power consumption trends, and investigate how far can process-dependent performance spread be tuned. To give answers to the previous concerns, we have implemented a clock generator unit (CGU) consisting of seven ring oscillators in a triple well 90nm CMOS technology with a nominal power supply of 1V. The CGU unit consists of 1620 transistors in total. The design was laid out with a commercial place-and-route tool using constrained-area routing features. The ring oscillators use minimum sized inverters as delay elements, a 2-input NAND gate for enabling control, and a divide-by-2 circuit for duty cycle recovery. The ring oscillators have independent bias control over their PMOS and NMOS transistors by properly adjusting the N-well and P-well voltages, respectively. Measurements were performed using an Agilent 93K SoC test system in a controlled temperature (25degC) environment enabled by a Tempronic thermostat. The fastest measured oscillator has a frequency of 822MHz, while the slowest runs only at 93MHz. In the remainder of this paper, we will refer to the former ring oscillator as “ringo-1” and to the latter as “ringo-7”.

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Figure 1. Power supply and body bias scaling.

Section 2 introduces the voltage conventions we used for AVS and ABB. In section 3 we will focus on frequency scaling as well as frequency tuning. Section 4 presents current trends of both static and dynamic power consumption; section 5 deals with the use of AVS and ABB for reduction of power demand. Section 6 explores the potential of AVS and ABB for online performance compensation.
2. SCALING OPERATIONS

We will now briefly introduce the adaptive voltage scaling (AVS) and the adaptive body bias (ABB) schemes. Figure 1 shows a graph of frequency vs. power as a function of either or both AVS and ABB. The thick line shows the nominal trend as \( V_{DD} \) is varied from its maximum to its minimum value. An AVS operation consists in sweeping the power supply while maintaining the body bias constant. ABB is essentially the contrary approach: \( V_{DD} \) is kept constant and the body bias is swept. Here, it holds that frequency and power have an almost linear negative dependence on the threshold voltage. The result is a “cloud” of frequency-power points at a given \( V_{DD} \) operating point. Finally, AVS+ABB is the case when both body biasing and power supply are swept. Table 1 presents the voltage ranges we have employed during our measurements. Observe that the wells were forward biased for at most 0.5V and reverse biased by 1V, independently of the power supply value. Forward biasing is constrained by the turn-on voltage of the transistors’ body-to-source junction diode. Essentially, reverse biasing is unconstrained, but for high reverse biasing voltages it results in increased (junction) leakage. We will now illustrate how these techniques can be used to alter the performance of integrated circuits. For this purpose, we have focused our attention on ringo-1 and ringo-7. Observe that in the next sections we will use the term ringo to refer to any of the two ring oscillators when not differently stated.

<table>
<thead>
<tr>
<th>Operation</th>
<th>Description</th>
<th>Variable</th>
<th>Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>AVS</td>
<td>Adaptive Voltage Scaling</td>
<td>( V_{DD} )</td>
<td>([0.5, 1.0])V</td>
</tr>
<tr>
<td>ABB</td>
<td>Adaptive Body Biasing</td>
<td>( V_{pwell} )</td>
<td>([-1.0, 0.5])V</td>
</tr>
<tr>
<td>AVS+ABB</td>
<td>Adaptive Voltage and Body Biasing</td>
<td>( V_{DD} )</td>
<td>([0.5, 1.0])V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_{pwell} )</td>
<td>([-1.0, 0.5])V</td>
</tr>
</tbody>
</table>

3. FREQUENCY SCALING AND TUNING

Let us first investigate the dynamic range of the ring oscillators. To a first order approximation the frequency can be calculated as \( f = \frac{k}{\mu C_{ox}} (V_{DD} - V_{th})^\alpha \) [12], where \( f \) is the operating frequency, \( k \) is a proportionality factor, \( \mu \) is the carrier mobility and \( \alpha \) is a process dependent parameter that takes into account velocity saturation. In the case of velocity saturated devices, \( \alpha \) is close to 1. Because of the low \( \alpha \) factor, it follows then that frequency scales almost linearly with \( V_{DD} \). Figure 2 shows the ringo frequency as function of power supply. Observe that the frequency increases by 3.4x when \( V_{DD} \) is scaled up from 0.5V to 1V.

We can now analyze the impact of ABB as a frequency tuning mechanism at each \( V_{DD} \) point. Notice from Figure 2 that the relative tuning range is not the same for all \( V_{DD} \) values. In particular, we measured frequency spans of approximately ±14% at \( V_{DD} = 0.5V \) and ±8% at \( V_{DD} = 1V \) w.r.t. their nominal frequencies. This unbalance is because the effective gate drive of the transistors is smaller at low \( V_{DD} \) values.

The contour plot in Figure 3 displays the range for frequency tuning when using ABB at \( V_{DD} = 1V \). The horizontal and vertical axes show the N-well and P-well voltage bias, respectively. The upper left corner shows the highest frequency, and the frequency bands are spaced at 10MHz intervals. For the measured silicon, ABB gives an absolute tuning range of 131MHz for the chosen well voltages. Observe also that it is possible to change the \( V_{th} \) of the PMOS and NMOS transistors independently and still attain the same frequency. Obviously, the choice of \( V_{th} \) has a significant impact on static power consumption as we will show later in section 4.

In general, the ringo-1 and ringo-7 show the same frequency scaling and tuning trend, except of course for absolute differences.

Figure 4 shows measurement results of the ringo frequency as a function of temperature and power supply. The relative temperature dependence at \( V_{DD} = 1V \) and nominal body bias is about -1.2%/°C. When \( V_{DD} > 0.6V \), the frequency decreases linearly as temperature increases, but when \( V_{DD} < 0.6V \), the frequency increases linearly as temperature increases. To understand the varying frequency behavior as a function of
temperature, recall that frequency is dependent on the transistor’s threshold voltage $V_{th}$ and carrier mobility $\mu$. To a first order approximation \[13][14] this dependence can be expressed as
\[
\frac{dV_{th}}{dT} = -\chi \mu(T) = \mu(T_0) \left(\frac{T}{T_0}\right)^b
\]
where $\chi$ is a constant, $\mu(T_0)$ is the carrier mobility at a reference temperature $T_0$ and $b$ is a constant. In turn, $V_{th}$ decreases with temperature, while $\mu$ is inversely related to temperature. When $V_{DD} > 0.6V$, the carrier mobility is the dominant parameter. However, observe that both parameters, $V_{th}$ and $\mu$, balance out each other at $V_{DD} = 0.6V$ as the frequency remains more or less constant, i.e. it is independent of temperature. For $V_{DD} < 0.6V$, $V_{th}$ becomes a dominant factor and frequency increases for increasing temperatures.

\[V_{th} = \frac{K}{T}\]

\[
\mu(T) = \mu(T_0) \left(\frac{T}{T_0}\right)^b
\]

When comparing power values of ringo-1 and ringo-7, one can see that the CGU-static power consumption at nominal $V_{DD}$ is approximately the same whether the ringo oscillates at a high or low frequency. Notice however, that if ringo-1 is operated at $V_{DD} = 0.5V$, its running frequency is around 100MHz, close enough to the nominal frequency of ringo-7, but its power consumption is about 7x lower than the one of ringo-7. This shows the advantageous impact of using AVS.

Leakage power is one of the main concerns in deep sub-micron technologies. In fact, AVS and ABB are often used for leakage reduction purposes. Figure 7 shows the impact of AVS and ABB on the leakage current for our CGU. The plot shows measurements of leakage current as a function of power supply. For the measured silicon, leakage reduces by 5x when $V_{DD}$ is scaled down from 1V to 0.5V. When using ABB alone at $V_{DD} = 1V$, leakage decreases only by 1.2x. This low impact of ABB is probably because of a high level of gate leakage. On the other hand, the combination of AVS with ABB renders a leakage reduction of 22x. Notice that, while the exact numbers may not be characteristic given the maturity level of the technology, it is clear that ABB alone has only a small impact on leakage reduction.
downscaling using AVS over half of the entire VDD range. The ringo-1 indicates a 13.8x power savings by 3.4x frequency tuning range control of AVS and ABB. Measurement results of the plot of Figure 8 puts us in state to evaluate power savings and the line joining clouds indicates the nominal trend. Frequencies of the combined use of AVS and ABB.

The ultimate goal of the AVS and ABB schemes is performance tuning with performance being the optimal combination of frequency and power, i.e. the lowest power for a fixed frequency. Figure 8 presents a plot of frequency as function of the total power, e.g. both CGU-static and dynamic power consumption of ringo-1. In this plot we have used the same conventions as before, i.e. each cloud is associated to a unique VDD value, each dot in a cloud corresponds to a unique N-well and P-well combination, and the line joining clouds indicates the nominal trend.

The plot of Figure 8 puts us in state to evaluate power savings and tuning range control of AVS and ABB. Measurement results of ringo-1 indicate a 13.8x power savings by 3.4x frequency downscaling using AVS over half of the entire VDD range. The use of ABB at VDD = 1V results in ±11% power and ±8% frequency tuning w.r.t the nominal operating point. The combination of AVS and ABB yields 22x power savings with 5x frequency scaling from the highest possible frequency (minimum Vth) to the lowest one (maximum Vth). These results show the strength of the combined use of AVS and ABB.

5. POWER AND FREQUENCY TUNING

This is essentially due to the impact that both forward and reverse ABB have on leakage current levels.

Let us now explore possible performance tradeoffs by using AVS and ABB. Figure 10 shows a zoom-in of Figure 8 at VDD = 1V. If AVS and ABB are applied such that the nominal VDD becomes 0.9V instead of 1V, and the Vth’s are pulled to their minimum value as indicated by the arrow in Figure 10, we see that it is possible to achieve a 19% power savings w.r.t. the nominal conditions at a penalty of only 4% in frequency reduction. A more aggressive VDD downscaling to 0.8V results in 45% power savings at 19% frequency penalty. It is clear, thus, that AVS+ABB can lead to significant power savings without serious performance penalty.

Figure 11 puts in perspective both the ring oscillators. The left axis shows the frequency of ringo-7, the right axis is associated to ringo-1, and the horizontal axis shows the total power consumption. The plot also shows two arrows labeled as “A” and “B”, respectively. Arrow “A” indicates a constant power trend. It basically indicates that for the same power figure, ringo-1 runs still 5x faster than ringo-7. Arrow “B” indicates that for the same speed (actually ringo-1 runs at 10% higher speed than ringo-7) ringo-1 consumes 7x less power. The implication of this latter observation can be quite significant. Is it possible, for instance, to

For the sake of completeness, Figure 9 shows a plot of both CGU-static and dynamic ringo-power consumption against frequency. Worth seeing here is the spread of the static power consumption.
synthesize a circuit for a higher speed and then through AVS reduce the power supply to reach the target speed with the additional benefit of significant power reduction.

6. PERFORMANCE COMPENSATION

As the variation of fundamental parameters such as channel length, threshold voltage, thin oxide thickness and interconnect dimensions goes well beyond acceptable limits, “on the fly” performance compensation is becoming necessary. While process spreads are tightly controlled, their impact on circuit design and behavior is higher and higher. For instance, while before a $V_{th}$ variation of say 50mV on a nominal $V_{th}$ of 450mV was not that crucial, in deep sub-micron technologies with a nominal $V_{th}$ of 250mV this variation can make circuit operation quite difficult.

![Figure 11. Frequency vs. total power of both ringo-1 and ringo-7.](image)

Figure 11. Frequency vs. total power of both ringo-1 and ringo-7.

Observe that the frequencies of both axes are different, e.g. the clouds lie above the 45-degree line. What is notorious from this plot is the fact that it is possible to tune the “fast” sample to the “typical” one by using AVS and ABB. Notice also that the tuning is continuous for all frequencies. Namely, when both AVS and ABB are used, the frequency range of the “fast” ringo is $170\text{MHz} < f_{\text{fast}} < 892\text{MHz}$ while the one of the “typical” ringo is $85\text{MHz} < f_{\text{typical}} < 815\text{MHz}$.

![Figure 12. Frequency spread and performance tuning.](image)

Figure 12. Frequency spread and performance tuning.

Figure 12 shows an example of performance spread in which frequency is plotted against power supply for eleven different samples. Additionally, frequency tuning using ABB for three selected samples is shown as well. Samples were selected as “fast”, “typical” and “slow” with nominal frequencies of $822\text{MHz}$, $713\text{MHz}$, and $640\text{MHz}$, respectively. The total frequency spread of the limited sample set of ringo-1 is $180\text{MHz}$. Despite this spread, it is possible to tune its frequency to the “typical” ringo. This gives basically a 100% parametric yield improvement. Let us investigate now up to what extent the frequency spread can be compensated. Figure 13 shows a frequency correlation between sample “fast” and sample “typical”. Each cloud is associated to a unique $V_{DD}$ value and each point in the cloud corresponds to a unique N-well and P-well bias combination.

![Figure 13. Frequency correlation between "fast" and "typical" ringos.](image)

Figure 13. Frequency correlation between “fast” and “typical” ringos.

![Figure 14. “Fast” to “typical” ringo performance compensation.](image)

Figure 14. “Fast” to “typical” ringo performance compensation.

As an example we use AVS and ABB to lower the nominal frequency of the “fast” sample to the one of the “typical” sample as indicated by the arrow in Figure 14. The nominal $V_{DD}$ of the “fast” sample becomes 0.9V instead of 1V, while several combinations of $V_{th}$s can provide the required frequency of 713 MHz.
7. CONCLUSIONS
We presented measurement results that show the extent to which adaptive power supply and adaptive body bias are useful in a state-of-the-art CMOS technology. Although the results were obtained from this particular 90nm CMOS technology, they are well suited as indices for reference purposes.

This paper shows that AVS renders a wide frequency-scaling control and significant power savings. The index factors are ~14x power savings by ~3x frequency downscaling. While the frequency and power tuning range of ABB may look limited (index factors ±11% power and ±8% frequency tuning @ VDD = 1V), the frequency tuning range proves to be effective for process-dependent performance compensation. In fact, we observed a continuous frequency tuning despite the wide frequency spread. With AVS and ABB together it is possible to attain 22x power savings with 5x frequency downscaling. These indices show that the combined use of AVS and ABB offers significant performance control. Contrary to the belief that high Vth has a considerable impact on leakage power reduction, we showed that reverse-bias ABB alone reduces leakage only by 1.2x. However, the combination of AVS and ABB yields an index factor of ~22x leakage reduction.

More work is needed to qualify this design technology in deep sub micrometer technologies, e.g. to assess the implications of VDD and Vth scaling on circuit activity, noise margins, power supply noise among other parameters. While the work hereby presented relates to ring oscillator measurements, it is a first step towards understanding the limitations of power and frequency scaling given the constraints imposed by the semiconductor process.

8. ACKNOWLEDGMENTS
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9. REFERENCES