Equivalent-circuit modeling of ferroelectric switching devices

D. B. A. Rep a)

Department of Applied Physics, Materials Science Center, University of Groningen, Nijenborgh 4, 9747 AG Groningen, The Netherlands

M. W. J. Prins b)

Philips Research Laboratories, Prof. Holstlaan 4, 5656 AA Eindhoven, The Netherlands

(Received 2 November 1998; accepted for publication 24 February 1999)

A compact equivalent-circuit model for ferroelectric switching devices is derived from a general model for local charge displacements. The general model consists of a matrix of repeat units describing local dissipationless charge displacements (electrostatic channel), as well as dissipative charge displacements (electrochemical channel), the channels being coupled due to the electrical charge of the moving species. The derived model for ferroelectric charge displacements is used to simulate both hysteresis and transient characteristics, and applied to two devices: (i) a ferroelectric capacitor and (ii) a ferroelectric memory field-effect transistor. The circuits are programmed in SPICE-derived analysis software. We find that experimental hysteresis data obtained on Pb(Zr,Ti)O₃ ceramic capacitors and on thin-film transistors with a SnO₂:Sb semiconductor and a Pb(Zr,Ti)O₃ ferroelectric insulator can be reproduced and interpreted with the equivalent-circuit models. © 1999 American Institute of Physics. [S0021-8979(99)02011-3]

I. INTRODUCTION

Ferroelectric material, once electrically polarized, remains polarized even in the absence of an electric field. This is due to hysteresis in the polarization response of the ferroelectric material to electric fields. Two remnant polarizations are available, of opposite polarity but equal magnitude. Data-storage devices with a ferroelectric component make use of these states. The two possible remnant polarizations are related to a logic “0” and “1”, memory states that can be stored without needing a supply voltage or cyclic refreshing. The ferroelectric component can also offer a low programming voltage, radiation hardness, and nondestructive read out. Owing to these properties, ferroelectric memory devices such as ferroelectric random-access memories¹ and ferroelectric memory field-effect transistors (FEMFETs, see for example Refs. 2–4) are being developed.

Ferroelectric device models can be used to support the process of integration of devices such as FEMFETs within complicated circuitry, as well as provide deeper understanding of the device physics. In the absence of an analytical description of ferroelectric switching, models that approximate (part of) the switching process have been developed in the past.³ Some models⁶,⁷ consist of a set of physics-based operation equations to be evaluated by means of mathematical software. Other, so-called behavioral models⁸–¹¹ translate experimentally observed ferroelectric switching behavior into an equivalent circuit for device simulation. Here, we present a model that combines a phenomenological equivalent circuit with physics-based operation equations. Programmed by means of SPICE-derived device-simulation software,¹² the model is compact and requires minimal mathematical efforts. As examples we will show that the model can be used to reproduce the electrical characteristics of a ferroelectric capacitor and of a FEMFET.

II. CHARGE-DISPLACEMENT MODEL

In this section we explain the conceptual origin of our compact model for ferroelectric switching. It starts with the observation that the movement of charge in a material is partly accompanied by energy dissipation and partly dissipationless. For example, the polarization of core electronic states is dissipationless, while the hopping of free carriers or migration of ions involves the dissipation of energy. In a one-dimensional model the dissipationless charge movement is described by a serial arrangement of capacitors [Fig. 1(a)]. Nodal point i between capacitors Cᵢ₊₁ and Cᵢ defines the electrostatic potential Vᵢ at point xᵢ. The displaced charge per unit area Qᵢ displaced in capacitor Cᵢ depends on the drop of electrostatic potential Vᵢ₋Vᵢ₋₁.

Dissipative charge transport of particles of species s (e.g., electrons) is described by a serial arrangement of resistors [Fig. 1(b)]. At the nodal points i the electrochemical potential Vᵢ of species s at position xᵢ is defined, assuming local thermal equilibrium. The current flowing through resistor Rᵢ depends on the local drop of electrochemical potential Vᵢ₋Vᵢ₋₁. The channel for dissipative transport of species s (Rᵢ) is coupled to the electrostatic backbone (Cᵢ) when species s carries electrical charge. The coupling strength—in our model given by C_DOS,s—is proportional to the local density of states per unit energy [see Fig. 1(c)].¹³ For unit-charge particles C_DOS,s=є²×DOSₛ, where DOSₛ is the density of states for species s (units m⁻³J⁻¹).

The equation describing the charge displaced in capacitors and the current flowing through resistors can be a linear as well as nonlinear function of the potentials, depending on

---

a)Electronic mail: rep@phys.rug.nl
b)Electronic mail: prins@natlab.research.philips.com
**III. FERROELECTRIC MODEL**

Ferroelectric materials are characterized by bistable charge-displacement characteristics. The bistability is generally caused by off-centered ions in the atomic unit cell each of which can flip from one off-center position to the other when it has sufficient energy to overcome the energy barrier in between the two positions. Thus, in its simplest form, the charge displacement in ferroelectric material involves the dissipative transport of one species of charge (i.e., ions) within the atomic unit cells. In Fig. 2 we propose a system of ferroelectric model units that represent atomic unit cells. The dissipative movement of ionic charge within unit cell is modeled by resistor \( R_i \). The ions can cross the unit-cell boundaries; the interaction with neighboring cells is of a dissipative nature. A bistable system is created when the resistors \( R_i \) have a strongly nonlinear current–voltage characteristic.

An isolated unit of Fig. 2 allows for parallel transport of charge through the capacitor describing electrostatic charge displacement \( (C_i) \) and through the serial arrangement of two nonlinear capacitors \( (C_i\text{DOS,ion} \text{ and } C_i\text{DOS,ion}) \) and a nonlinear resistor \( (R_i) \). This arrangement is summarized in Fig. 3, where \( R_i \) is denoted as \( R_{FE} \) and \( C_i\text{DOS,ion} \text{ and } C_i\text{DOS,ion} \) are represented by \( C_{FE} \). The voltage across \( R_{FE} \) is given by \( V_1 \), the voltage across \( C_{FE} \) by \( V_2 \). Capacitor \( C_i \) is denoted as \( C_{\text{die}} \). This set is summarized by the symbol on the right, a ferroelectric capacitor with voltage drop \( V_{FE} = V_1 + V_2 \).

Next we will choose functionalities for the three components of the ferroelectric model unit. This choice will involve smooth (analog) charge-displacement and energy-dissipation characteristics, although in principle the polarization states of a single atomic unit cell are discrete. In our model the smooth curves represent the average displacement; this average is the same for time averaging or ensemble averaging. Capacitor \( C_{\text{die}} \) is a linear dielectric capacitor. We base our choice for the functionality of \( R_{FE} \) on the picture of bistable ions flipping at a threshold field. Thus, the switching current through \( R_{FE} \) should rapidly increase for \( |V_1| \) above a threshold value \( V_a \) (\( V_a > 0 \)). As an example, we take

**FIG. 1.** Equivalent-circuit model of dissipationless (a) and dissipative (b) charge movement along a direction designated as the \( x \) direction. At \( x = x_i \), an electrostatic potential \( V_i \) is defined at node \( i \) and an electrochemical potential \( V_{i+1} \) at node \( i+1 \) for every species \( s \) of moving charge. The two types of charge movement channels (a) and (b) are combined in panel (c). The capacitors \( C_i^{\text{DOS,s}} \) relate to the local density of \( s \)-particle states in the material. When using this circuit to describe a one-dimensional system, the unit of \( C_i \) and \( C_i^{\text{DOS,s}} \) is Farad. For a three-dimensional system the unit is F/m².

**FIG. 2.** Equivalent circuit for the ferroelectric-type movement of a single species of (ionic) charge. \( R_{FE} \) describes dissipative charge movement. The capacitors \( C_{i\text{DOS,ion}} \text{ and } C_i\text{DOS,ion} \) define how this movement affects the local electrostatic potential. Dissipationless charge displacement is modeled by capacitor \( C_{i\text{DOS,ion}} \).

**FIG. 3.** Equivalent-circuit model for the charge displacement and energy dissipation in ferroelectric material, based on the model unit of Fig. 2. The two DOS capacitors are combined in \( C_{FE} \) while the dissipative-charge displacement resistor is denoted as \( R_{FE} \). Both components are nonlinear. Electrostatic charge displacement is modeled by a linear dielectric capacitor, denoted as \( C_{\text{die}} \) (cf. Fig. 2). The circuit is summarized by the hysteretic capacitor shown on the right.

---

It seems there might be some formatting issues with the text, especially with the diagrams. If you need further assistance or have questions, feel free to ask!
I0 is a normalization parameter. Parameter \( \alpha (\alpha > 0) \) controls the abruptness of ferroelectric switching at \( V_1 = \pm V_a \). In case \( \alpha \) is very close to zero, charge transport through \( R_{FE} \) can only occur if \( V_1 \) equals \( \pm V_a \), so that the charge displaced in the ferroelectric cell is given by \( Q_{FE}(V_1) = Q_{FE}(V_2 = \pm V_a) \). Consequently, the simulated hysteresis loop consists of two \( Q_{FE}(V_2) \) loops shifted along the voltage axis by \( \pm V_a \). For larger values of \( \alpha \) the transport of charge through \( R_{FE} \) also occurs for voltages that deviate from \( \pm V_a \); this phenomenon corresponds to ferroelectric depolarization. For the functionality of \( C_{FE} \) we choose

\[
R_{FE} : I_{FE} = I_0 \frac{\sinh \left( \frac{V_1}{\alpha V_a} \right)}{\sinh \left( \frac{1}{\alpha} \right)}. \tag{1a}
\]

\( I_0 \) is a normalization parameter. Parameter \( \alpha (\alpha > 0) \) controls the abruptness of ferroelectric switching at \( V_1 = \pm V_a \). In case \( \alpha \) is very close to zero, charge transport through \( R_{FE} \) can only occur if \( V_1 \) equals \( \pm V_a \), so that the charge displaced in the ferroelectric cell is given by \( Q_{FE}(V_1) = Q_{FE}(V_2 = \pm V_a) \). Consequently, the simulated hysteresis loop consists of two \( Q_{FE}(V_2) \) loops shifted along the voltage axis by \( \pm V_a \). For larger values of \( \alpha \) the transport of charge through \( R_{FE} \) also occurs for voltages that deviate from \( \pm V_a \); this phenomenon corresponds to ferroelectric depolarization. For the functionality of \( C_{FE} \) we choose

\[
C_{FE} : Q_{FE} = \text{sign}(V_2) \times Q_{SAT} \times \tanh \left( \frac{|V_2|}{2 \delta} \right), \tag{1b}
\]

These expressions stem from Miller’s model equations of ferroelectric capacitors and their specific form is chosen for mathematical convenience and applicability to the experimental data of Sec. IV. \( Q_{SAT} \) represents the saturation value of the ferroelectric charge displacement and \( Q_R \) the value at \( V_2 = V_a \). An idealized, square hysteresis loop has \( n \approx 0 \) and \( \alpha = 0 \) with \( V_a \) equal to the coercive voltage and \( Q_R \) to the remnant polarization. For larger values of \( \alpha \), the hysteresis loop deviates from the shape of \( Q_{FE}(V_2) \) and the apparent coercive voltage and remnant polarization are no longer equal to \( V_a \) and \( Q_R \), respectively. Such deviations also occur when increasing the time needed for measuring one hysteresis loop (so, by decreasing the sweep frequency).

**IV. SIMULATION RESULTS**

**A. Ferroelectric capacitor**

In Fig. 4(a) experimental data are shown of a ferroelectric capacitor. Figure 4(b) presents a simulation for the serial arrangement of a nonlinear resistor \( R_{FE} \) and a nonlinear capacitor \( C_{FE} \), neglecting the dielectric contribution \( (C_{dil} = 0) \). This is to show that the serial arrangement of these two components gives rise to hysteresis behavior with a nonzero coercive voltage, a nonzero remnant polarization, and to a saturating behavior at high applied voltages. The addition of the dielectric contribution [Fig. 4(c)] reproduces the experimentally observed characteristic. The sharpness of the switching-current onset at \( V_1 = \pm V_a \), described by parameter \( \alpha \), is closely related to the retention of ferroelectric polarization in the absence of an external electric field \( V_{FE} = 0 \); low values of \( \alpha \) relate to material that retains its polarization effectively, high values give depolarization in time. This is illustrated in the retention graph of Fig. 5, where the decrease of polarization is shown for our model ferroelectric unit at \( V_{FE} = 0 \) over 16 time decades.
The influence of \( \alpha \) on the \( Q(V_{FE}) \) graphs is particularly notable for voltage sweeps with an amplitude that is insufficient to drive the ferroelectric polarization into saturation, so-called inner hysteresis loops or subsaturation loops. Figure 6(a) shows a set of experimental \( Q-V \) curves including subsaturation loops. The loops have a dissimilar derivative \( dQ_{FE}/dV_{FE} \) for given \( V_{FE} \) (the experimental observation that this derivative is similar among different subsaturated loops is described for example in Ref. 6). In fact, for simulations with a low value for \( \alpha \) and \( C_{diel}=0 \) [Fig. 6(b)], the derivative is either that of the outer loop or zero. This is due to the fact that no charge is being displaced when the voltage across \( R_{FE} \) is lower than \( V_{\alpha} \). When a \( C_{diel}>0 \) is added, the zero-derivative sections turn into sections with a \( (n=1) \) and simulation results.

Two ferroelectric modules with different \( \alpha \)-values (\( n=1 \)) and simulation results. The correspondence with the experimental results, especially in those sections, is improved when two dissimilar model units are combined as can be appreciated from Fig. 6(c) in which two units with a different value of \( \alpha \) are combined. Possibly, nonuniformities in the material and effects like domain-wall movement and pinning generate the need for dissimilar model units. The use of two \( \alpha \)-modules also results in two decay characteristics in the retention graph, one giving rise to fast decay of the polarization (\( \alpha =0.2 \)) and one relating to a more slowly decaying component (\( \alpha =0.02 \)). We note that the data of Teowee and co-workers\(^{17} \) for Ti/Pb(Zr,Ti)O\(_3\)/Pt and Ti/Pb(Zr,Ti)O\(_3\)/Zn capacitors are similar to the retention simulations of Fig. 6(c). The origin of the complex decay behavior may be the presence of nonuniform fields inside the capacitor (e.g. due to space-charge region near the interface or due to nonswitching layers) or structural inhomogeneities. The influence of depolarization in time is also seen when the measurement of a hysteresis loop is performed more slowly, resulting in a decrease of the apparent coercive voltage and a decrease of the apparent remnant polarization for decreasing sweep frequencies. This well-known property of ferroelectrics is reproduced by our simulations as well (not shown).

### B. Ferroelectric transistor

We will next describe how a thin-film ferroelectric field-effect transistor, shown in Fig. 7 and described in detail in Ref. 3, can be simulated with a compact equivalent-circuit model such as shown in Fig. 1. We treat the case of small source-drain voltages, so that we only need to derive the equations for charge displacement in the ferroelectric material and the semiconductor layer along the normal of the semiconductor/ferroelectric interface (i.e., along the \( x \) axis). For the ferroelectric gate insulator we use the model of Fig. 4(c). A description of the band bending and charge accumulation/depletion in the semiconductor layer of thickness \( t \) must satisfy the Poisson equation\(^{18} \)

\[
\frac{\partial^2 \Phi}{\partial x^2} = \frac{\rho(x)}{\varepsilon}.
\]

\( e\Phi(x)=E_c(x)−E_F \) denotes the position of the conduction band edge \( (E_c) \) with respect to the Fermi level \( (E_F) \), \( \rho(x) \) the associated charge density, and \( \varepsilon \) the dielectric constant of the semiconductor. We base our equivalent-circuit description of the \( n \)-type semiconducting material on the general model of Fig. 1(c). One moving charge species is involved, viz. electrons. No current is flowing in the \( x \) direction, so that the resistors in the electrochemical channel can be replaced by shorts. The nodal points \( t \) are at zero electrochemical potential, corresponding to the Fermi level of the semiconductor material. This yields the model displayed in Fig. 8(a). Parameter \( t \) is the thickness of the thin-film semiconducting layer. As is shown explicitly in the Appendix, the array
solves Poisson’s equation for \( N \) equidistant points \( x_i \) when we define for \( Q_i \) (on \( C_i \)) and \( Q_i^{\text{DOS},e} \) (on \( C_i^{\text{DOS},e} \))

\[
Q_i = \frac{e}{\Delta x} [\Phi(x_i) - \Phi(x_{i-1})],
\]

\( i = 1, 2, \ldots, N \)

\[
Q_i^{\text{DOS},e} = -e\Delta x \int_{-\infty}^{\infty} f(E)D(E - e\Phi(x_i))dE + q_0,
\]

with \( f(E) \) the Fermi-Dirac distribution function and \( D(E) \) the density of electron states (in \( \text{m}^{-3}\text{J}^{-1} \)) in the semiconductor. Parameter \( q_0 \) ensures charge neutrality for zero gate voltage. Since we are using a degenerately doped semiconductor material\(^{19} \) we choose \( q_0 \) such that the Fermi level lines up with the conduction band edge at \( \Phi = 0 \). We assumed that the influence of the source-drain voltage on the band bending is negligible, so that we can approximate the source-drain conductivity (\( \sigma \)) by counting the electrons in states above the conduction band edge (\( n_{\text{cond}}(x) \)) and calculating

\[
\sigma(x) = n_{\text{cond}}(x) \times e \times \mu \quad \text{[see Fig. 8(b)]}
\]

\[
\sigma(x) = e \mu \int_{e\Phi(x)}^{\infty} f(E)D(E - e\Phi(x))dE,
\]

for \( n \)-type conduction with electron mobility \( \mu \). We assume that the conduction band shape is parabolic, i.e., \( D(E) \sim (E - E_c)^{-1/2} \). To model the grain boundaries in the polycrystalline semiconductor material a constant density of grain-boundary states (\( D_{gb}(E) = D_g \) for all energies) is added to the DOS. Grain-boundary states with an energy inside the semiconductor energy gap are assumed to have zero mobility; states above the gap are assumed to be part of the conduction band. The sheet conductance (\( G \)) of the transistor finally follows from

\[
G = \int_0^L \sigma(x)dx \approx \sum_1^N \sigma(x_i)\Delta x.
\]

This summation is performed by an array of resistors, see Fig. 8(b), each having a conductance equal to \( \sigma(x_i)\Delta x \).

So far, the model does not take into account charge injection into the insulating layer, which may occur in the presence of high electric fields. In our device the charge displacement is of the order of 0.1 C/m\(^2\), which gives rise to electric fields of the order of \( 10^9 \) V/m at the semiconductor/ferroelectric interface. These very high fields are expected to yield charge injection into localized states near the interface (see Ref. 21 for a discussion on charge injection into ferroelectric material). This effect modifies the transistor characteristics. The injected charge is localized and does not contribute to conduction along the semiconducting channel. Furthermore, the process of charge trapping and detrapping causes hysteresis in the conductance of the source-drain channel as a function of the displaced charge in the gate insulator. We model the interfacial trapping region by an interfacial insulating layer of thickness \( t_{\text{inter}} \) (see Fig. 9). The local density of trap states across the interfacial layer is described by capacitance \( C_{\text{trap}} \) (unit F/m\(^2\)). Since the interfacial layer is an insulator the capacitors describing the density of nontrapped states may be neglected in this region. \( R_{\text{trap}} \) controls the threshold behavior and rate of trapping/detrapping of charge carriers, in a similar fashion as \( R_{\text{FE}} \) does in our ferroelectric model unit. We choose for the functionality of \( R_{\text{trap}} \) expression (1a) in which fit-parameter \( \alpha \) is replaced by \( \beta, \) and switching-threshold \( V_{\alpha} \) by trap/release-threshold \( V_{\beta} \). To model the complete ferroelectric field-effect transistor, a single ferroelectric module\(^{22} \) is connected to the interfacial region as shown in Fig. 9.

Let us now compare the experimental results [Fig. 10(a)] to our simulation results from the ferroelectric/semiconductor model [Fig. 10(b)]. The charge displacement curves (a1 and b1) have an apparent coercive voltage of 2 V. This voltage results from the coercivity of the ferroelectric layer and the coercivity of the charge trapping across the interfacial layer. The apparent remnant polarization \((-0.08 \, \text{C/m}^2\) is a factor of two smaller than the value of \( Q_R \). This reduction is caused by the band bending in the semiconductor layer, giving a partial depolarization of the ferroelectric material at zero externally applied voltage (see for example Ref. 3). The sense of rotation of the transfer characteristic (panels a2 and b2) indicates what mechanism determines the memory effect in the semiconductor layer. When the ferroelectric polarization dominates, the sign of the induced charge in the semiconductor upon voltage application is the same as the sign of the remnant charge when the voltage is
of charge into the interfacial layer between the semiconduc-
tor and the ferroelectric material.

In panels a3 and b3, the $Q-V_G$ and $I_D-V_G$ curves are combined to a curve of the conductance of the source-drain channel ($G$) versus the charge density displaced in the gate insulator. The slope of the $G-Q$ curve in the high-
conductivity (or accumulation) regime determines the elec-
tron mobility in the semiconducting channel; the deduced
value ($1.3 \times 10^{-4} \text{ m}^2/\text{Vs}$) is in agreement with measure-
ments of the Hall mobility in the same material.\textsuperscript{19} The slope of the $G-Q$ curve at low conductivity (depletion or sub-
threshold regime) is given by the density of grain states $D_{gr}$
and the effective semiconductor layer thickness $t_{eff}$. These
parameters cannot be deduced independently from the mea-
sured curve. However, the semiconductor band bending
required for the displacement of a given amount of charge
increases for increasing $t_{eff}$ because the band bending in the
semiconductor should be smaller than the applied gate volt-
age minus the voltage required for ferroelectric switching,
we can deduce an upper limit for $t_{eff}$ (so also a lower limit
for $D_{gr}$). The deduced value is about 2.5 nm, which is of the
same order as the Fermi wavelength of the charge carriers\textsuperscript{19}
and smaller than the nominal thickness of 10 nm. We attri-
bute this difference to the granular nature of the semicon-
ducting material\textsuperscript{19} and to depletion effects near the
semiconductor/capping interface. The fact that several na-
nometers of the film thickness do not contribute to the con-
duction is in agreement with our experience that laser-
ablated thin films of SnO$_2$ with a nominal thickness below 10
nm show a strongly reduced conductivity compared to films
of only slightly larger thickness. The fitted value of the den-
sity of grain-boundary states is $8.5 \times 10^7 \text{ F/m}^3$, corre-
sponding to a state density of $1.8 \times 10^{20} \text{ cm}^{-3}$.\textsuperscript{25} This value is in
the expected range for polycrystalline material.\textsuperscript{26,19} Finally,
we observe hysteresis in panels a3 and b3 with a clockwise
sense of rotation. This is caused by charge trapping in the
interfacial layer between the semiconductor and the ferro-

electric material. From comparison of experimental and
simulation results, no precise value for $C_{trap}$ could be con-
cluded. The similarity between the $G-V_G$-curves for both
 sweep directions suggests that charge injection into the trap-
ing layer occurs only at high gate voltages. Due to leakage
currents in the same regime, it is difficult to estimate values
for $V_B$, $I_B$, and $C_{trap}$. Thus, we have chosen them as to
yield a sharp transition from zero trapping to complete trap-
ing of all additional charges when $|V_G| \sim 3 \text{ V}$, indicated for
example in panel b3 of Fig. 10.

V. SUMMARY AND DISCUSSION

This article describes a model for the electrical switching
characteristics of ferroelectric material in devices such as
 capacitors and field-effect transistors. The model is based on
a compact modeling concept of charge displacement as a
function of position in a material, distinguishing dissipative
and dissipationless currents. Dissipative transport is de-
scribed by a channel of resistors; the current that flows

---

FIG. 10. Experimental graphs (a) and simulation results (b). Panel a1 and b1 show ferroelectric-type charge displacement per unit area ($Q$) as a function of gate–voltage ($V_G$). Panels a2 and b2 show the transistor transfer characteristics (drain-current $I_D$ vs $V_G$). The source is at zero potential and $V_D=1 \text{ V}$. The curves are combined in panels a3 and b3, showing the semiconductor sheet-conductance ($G$) vs $Q$ for the measured data and simulation, respectively. The simulation curves were obtained with the following model parameters: $V_T=2.2 \text{ V}$, $I_s=10^8 \text{ A/m}^2$, $n=0.02$, $Q_{sat}=0.22 \text{ C/m}^2$, $n=0.4$, $Q_{gr}=0.17 \text{ C/m}^2$, $C_{air}=0.02 \text{ F/m}^2$, $F=1.3 \times 10^{-4} \text{ m}^2/\text{Vs}$, $D_{gr}=8.5 \times 10^7 \text{ F/m}^3$, $t_{eff}=2.5 \text{ nm}$, $t_{inter}=5 \text{ nm}$, $t_{inter}=50 \text{ nm}$, $V_D=1.3 \text{ V}$, $I_D=1 \text{ A/m}^2$; $\beta=0.01$, $C_{trap}=1 \text{ F/m}^2$, and $N=31$. Note the hysteresis in $G$ due to trap-
ing. Gate leakage currents dominate the conductance at negative gate voltages ($V_G \leq -2 \text{ V}$). The experimental graphs were obtained on a thin-film transistor with a 144 nm PbZr$_{0.3}$Ti$_{0.7}$O$_3$ ferroelectric layer and a 15 nm polycrystalline SnO$_2$ layer, doped with $4 \times 10^{19} \text{ cm}^{-3}$ Sb forming the tran-
sistor channel, passivated by a capping layer of 10 nm BaZrO$_3$. Panel 1a was
determined with a Sawyer–Tower circuit (see Ref. 16) swept at 100 Hz.
More details on the transistor fabrication can be found elsewhere (see Refs.
2, 3, 23, and 24).
through the resistors depends on the drop of electrochemical potential inside the material. The dissipationless transport occurs in a channel of capacitors across which a drop of the electrostatic potential is present. The two channels are coupled by capacitors that relate to the local DOS inside the material. The model is used to derive a resistor/capacitor unit that reproduces the ferroelectric switching behavior of an atomic unit cell (Fig. 3). A serial arrangement of a capacitor of saturating nature and a resistor with an exponential current–voltage behavior yields ferroelectric-type charge-displacement characteristics. Important in this model unit is the degree of nonlinearity of the resistor (described by parameter $\alpha$) which determines the sharpness of the onset of switching and the time-dependent depolarization of the material. A combination of fast and more slowly decaying polarization components (experimentally observed in Ref. 17 for example) can be simulated by utilizing multiple model units with differing values for $\alpha$. Good agreement is obtained between experimental characteristics (i.e., charge displacement and transfer characteristics) of ferroelectric thin-film transistors and simulations based on our ferroelectric model combined with a model for the semiconductor and for the ferroelectric/semiconductor interface. The latter two models are derived from the same modeling concept that generated the ferroelectric unit. Charge displacement in the semiconductor channel is calculated along one dimension, sufficient to describe the linear regime of transistor operation ($V_{SD} \ll V_G$). The model can be straightforwardly extended to describe displacements in two or three dimensions by extending the network of Fig. 1. From the comparison between experiment and our model we conclude that at the most 25% of the nominal 10 nm thickness of the SnO$_2$:Sb layer (the transistor channel) is conductive. This we attribute to the granularity of and depletion effects in the semiconductor thin film.

In this work we have developed models describing ferroelectric-type, semiconductor-type, and injection-type charge displacement from a single concept model. This model takes into account fundamental material parameters such as the intrinsic DOS, the dielectric behavior, and dissipative charge transport. Therefore, it appears to be a versatile vehicle for modeling a variety of materials. Inhomogeneities in the material call for dissimilar model units to be connected to each other. As an example, several model units placed in a matrix will allow the study of multicell ordering phenomena such as ferroelectric domain wall movement. The existence of inhomogeneities does in principle endanger the compactness of the model. This situation occurs in highly disordered systems where charge transport is determined for example by percolation (the principle of which is a random matrix of dissimilar resistors) or by variable-range hopping.28 When sufficiently compact units can be defined, as in the case of our ferroelectric devices, compact modeling can be of great importance to simulate the behavior of the devices when embedded in larger electronic circuits, like for example in sensor systems or in memory chips.

**ACKNOWLEDGMENTS**

The authors thank Sjoerd Zinnemers for providing the experimental data discussed in this article and Harry van Esch, Ben Giesbers, and Hans Cillessen for preparing the devices.

**APPENDIX: THE CHARGE-DISPLACEMENT MODEL SOLVING POISSON’S EQUATION**

Referring to Fig. 8, charge conservation yields

$$\Phi(x_j) - \Phi(x_{j+1}) = C_{j+1}^{-1}\left(\Phi(x_j) - \Phi(x_{j-1})\right)$$

$$\times C_j^{-1} + \left[\Phi(x_1) - \Phi(x_0)\right]$$

$$\times C_1^{-1} + \left[\Phi(x_N) - \Phi(x_N-1)\right] = 0.$$  \hspace{1cm} (A)

From (3b) we have

$$\Phi(x_i)C_{i}^{\text{DOS}} = \rho(x_i)\Delta x$$  \hspace{1cm} (B)

so that

$$-\Phi(x_{i-1}) + 2\Phi(x_i) - \Phi(x_{i+1}) = \frac{\rho(x_i)}{C_i}\Delta x.$$  \hspace{1cm} (C)

Here, the left-hand side corresponds to minus the second derivative of $\Phi(x)$ at $x = x_i$. $C_i$ is defined by Eq. (3a) as $e/\Delta x$ so that Eq. (C) yields a discretization of the Poisson equation, Eq. (2).

---

1MRS Bull. 21, 7 (1996).
12SPICE = Simulation program with integrated-circuit emphasis; for a recent overview of the history and features of SPICE-based simulation software, see e.g., A. Vladimirescu, *The Spice Book* (Wiley, New York, 1994).
13A familiar example of a DOS capacitor is the local charge density in a semiconductor conduction band; the formula $n = n_i \exp(q(\phi - \phi_0)/k_BT)$ describes how the local charge density depends on the difference between the local electrostatic potential ($\phi$) and the local electrochemical potential ($\phi_0$, the quasi-Fermi level for electrons), for the case that the Fermi level is situated several times $k_BT$ below the conduction band edge.14
18 Note the sign of the left-hand side of the equation, which differs from what is commonly used, because of our definition of \( \Phi(x) \).
20 The integrals involving \( D(E)/(E-E_c)^{1/2} \) cannot be solved analytically. We have used both an approximation to the integrals valid for \( \Phi > \delta T \)
and a discrete set of points from a numerical solution in between which the circuit-analysis software interpolates. The results were sufficiently close to each other.
22 Because subsaturation characteristics of the ferroelectric transistor are not included in the experimental data, the model contains for simplicity only one ferroelectric unit.
25 \( D_p \) is expressed in F/m\(^3\) so that \( D_p/e \) (\( e \) being the electron charge in m\(^2\)eV\(^{-1}\)) by assuming an energy gap width of 3 eV this is converted into m\(^{-3}\).