Phase-Shifted Full Bridge Converter Featuring ZVS over the Full Load Range

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Abstract— A new full-bridge circuit which can achieve zero voltage switching (ZVS) for all the primary side switches over the full load range and a wide input voltage range is proposed. The ZVS is achieved by the energy stored in the auxiliary inductor and the magnetizing inductance of the transformer. Because the leakage inductance is relatively small, there is no severe duty ratio loss or severe voltage ringing across the output rectifier. As the assistant current for achieving ZVS is almost the same for any duty ratio, the conduction losses at light load are reduced. The principal operation of the converter is described, and the optimal design is discussed. Finally, the operation of the converter is verified on a 1kW prototype.

I. INTRODUCTION

The zero-voltage switching (ZVS) phase-shift full-bridge (PSFB) converter has been widely used in medium- or high-power application [1]-[3]. It has several desirable features, such as low component stresses, low EMI, constant switch frequency and soft switching for all switching devices by utilizing the parasitic capacitor of the power MOSFET and the leakage inductor. In a conventional PSFB, ZVS of the leading leg can only be achieved over a limited load range, and attention must be spent on the leakage inductance. A large leakage inductance, which can extend the ZVS range, has several drawbacks such as duty cycle loss, high voltage ringing across the rectifier diodes and large circulating current [4].

A number of techniques have been proposed to improve the performance of the ZVS PSFB converter [5]-[7]. In [8] and [9], the ZVS range of the PSFB is extended and no output inductor is needed by using series-connected two transformers. In [9], the conduction losses are reduced by adding a boost capacitor. However, the duty cycle loss is still serious. In the approaches proposed in [10]-[16], full-range ZVS of primary switches is achieved by utilizing adaptive energy stored in inductive components of an auxiliary circuit. The energy stored in the auxiliary circuit is adaptive according to the phase shift i.e. the load condition, so circulating energy is reduced. As the auxiliary inductor does not appear in the power-transfer path, it does not cause serious duty cycle loss or voltage ringing. However, at critical continuous condition, the operation duty ratio is still large while the reflected load current is nearly zero, so the inductance of the auxiliary circuit must be small enough to ensure enough assistant current to achieve ZVS. As a result, the conduction losses are large at light load.

Fig. 1 shows the proposed circuit topology which can be divided into two independent parts: one is the standard PSFB converter with a smaller magnetizing inductance \( L_m \), the other is the transition auxiliary circuit including a transformer \( TR_x \) and an inductor \( L_x \).

II. OPERATION PRINCIPLE

The primary side of the power transformer \( TR \) is connected between the leading leg output \( A \) and the lagging leg output \( B \). A small capacitor \( C_b \) is inserted on the primary side of \( TR \) for blocking dc voltage unbalance. \( L_k \) is the leakage inductance of \( TR \), which is much smaller than that in a conventional PSFB. The secondary side of the \( TR \) is connected to a full-wave rectifier. Other types of rectifiers can also be used.

In order to achieve ZVS over the full load range, the primary side of an auxiliary transformer \( TR_x \) is connected between the leading switch leg output \( A \) and the center-tap of the a capacitive divider in the DC bus. One of the terminals
of the secondary winding of \( TR_x \) is also connected to the capacitive center-tap. The other secondary output is connected in series with an inductor \( L_x \) which, by its turn, is connected to the lagging leg output \( B \). The inductance of \( L_x \) is designed to have a same value with the magnetizing inductance of the transformer \( TR \). A small DC blocking capacitor may need to be inserted between the terminal of \( L_x \) and the lagging leg output \( B \), which is not drawn for simplicity.

To simplify the analysis, it is assumed that each switch device is ideal with a fixed output capacitor value. The auxiliary transformer is assumed to be ideal with a turn ratio of \( n_{TR} = 1 \). The turn ratio of the transformer \( TR \) is \( n_{TR} = N_p/N_s \). \( N_p \) and \( N_s \) are the numbers of primary-winding turns and secondary-winding turns of \( TR \), respectively. The DC bus capacitors \( C_{di} \) and \( C_{d2} \) are assumed to be large enough to achieve a constant voltage equal to \( V_{in}/2 \) across each capacitor.

Fig. 2 illustrates representative waveforms of the circuit in Fig. 1. The voltage across the auxiliary inductor \( L_x \), \( v_{BD} = V_{BD} - V_{BZ} \), is illustrated in Fig. 2. Generally, the voltage second products of the transformer \( TR \) and the auxiliary inductor \( L_x \) both depend on the phase shift between the turn-on instants of the corresponding switches in the bridge legs, and the sum of them is almost constant. Therefore, the sum of the two current \( i_x \) and \( i_m \) is almost constant at the transition of leading leg for any duty ratio.

Fig. 3 shows the equivalent circuits of the operation stages in half switching cycle.

**Stage 1 (t0-t1):** Before \( t1 \), switch \( S_1 \) and \( S_3 \) are conducting, and the voltage across the primary-winding of \( TR \) is almost equal to \( V_{in} \). The magnetizing current \( i_m \) increases with the rate \( V_{in}/L_m \). \( D_R \) is off, and \( D_{R2} \) conducts the current \( i_m \) to the load. Because the voltage across the auxiliary inductor \( L_x \) is nearly zero, the current of \( L_x \) keeps at \(-i_x\) during this stage, as shown in Fig. 2. The value of \( i_x \) can be expressed as follow:

\[
I_x = \frac{V_{in}(1-D)}{4f_L}.
\]  

**Stage 2 (t1-t2):** At \( t1 \), \( S_4 \) is turned off, the output capacitors \( C4 \) and \( C3 \) are charged and discharged linearly by currents \( i_x \) and \( i_m \) until the voltage across \( C4 \) reaches \( V_{in} \), where \( i_x \) is the sum of reflected filter inductor current \( i_L/2\) and the magnetizing current \( i_m \). As the energy is from the output filter \( L_x \), the magnetizing inductance \( L_m \) and the auxiliary inductor \( L_x \), the charging and discharging is easily completed before dead time ends. The voltage across the primary-winding of the power transformer \( v_{AB} \) remains positive during this stage, so \( D_{R1} \) is still off, and \( D_{R2} \) conducts the output current.

**Stage 3 (t2-t4):** At \( t2 \), \( C4 \) is fully charged to \( V_{in} \), and the body diode \( D3 \) conducts naturally. Then \( S3 \) is turned on with zero voltage switching after dead time ends at \( t3 \). The equivalent circuit is shown in Fig. 3(c). The outputs of the two legs are shorted by switch \( S1 \) and body diode \( D3 \), and the voltage across the primary-winding falls to zero. The primary current \( i_p \) decreases with the rate given by

\[
\frac{di_p}{dt} = \frac{d}{dt} \frac{V_{in}}{n_{TR}L_f} = -\frac{V_{in}}{n_{TR}L_f}.
\]  

At this stage, the voltage across the auxiliary inductor \( L_x \) is \( V_{in} \). Therefore, current \( i_x \) increases with the slope \( V_{in}/L_x \) until it reaches its maximal value \( I_{cap} \) at \( t4 \).
Fig. 3. Equivalent circuits of the operations stages in half switching cycle: (a) Stage 1 (t0-t1), (b) Stage 2 (t1-t2), (c) Stage 3 (t2-t4), (d) Stage 4 (t4-t5), (e) Stage 5 (t5-t6), (f) Stage 6 (t6-t7).

Stage 5 and Stage 6 (t5-t7): At t5, after the body diode D2 conducts, S2 is turned on at zero voltage, as shown in Fig. 3(f). The input voltage is applied on $L_{lk}$, so $i_p$ decreases with the slope $V_i/L_{lk}$ until it changes direction, and then DR2 turns off. The output current $i_o$ flows through DR1, and $V_i$ is applied on the magnetizing inductor of TR. This stage ends when S3 turns off at t7, and then the second half cycle starts, which is similar to the first one.

III. DESIGN CONSIDERATION

To achieve ZVS over the full load range, the leakage and magnetizing inductance of TR and the auxiliary inductance should be designed properly.

A. ZVS Range for the Lagging Leg

The charging and discharging of the output capacitor $C_4$ and $C_3$ is achieved by the energy stored in output filter inductor $L_s$, magnetizing inductor $L_m$ and auxiliary inductor $L_a$, all of which can be seen as constant current source. Further simplified equivalent circuit at this transition time is shown in Fig. 4(a). The equivalent capacitor $C_s = C1+C2$ is charged.
by two current sources. From Fig. 2, the value of $I_x$ and $I_p$ can be described by (2) and (5).

$$I_p = \frac{I_o + \Delta I_o / 2}{n_{TR}} + \frac{DV_o}{4f_{s}L_s} \tag{5}$$

$L_o$ is the average output current, and $\Delta I_o$ given by (6) is the current ripple of the output filter inductor $L_f$. To achieve ZVS for the lagging leg, equation (7) must be satisfied, where $t_d$ is the dead time illustrated in Fig. 2.

$$\Delta I_o = \frac{V_o(1 - D)}{2L_s f_{s}} \tag{6}$$

$$\frac{(I_o + I_p)_{d}}{C_s} \geq V_{in} \tag{7}$$

### B. ZVS Range for the leading leg

Fig. 4. Simplified transition equivalent circuits: (a) the lagging leg and (b) the leading leg

The charging and discharging of output capacitors $C_1$ and $C_2$ is achieved by the energy stored in the leakage and magnetizing inductance of TR and the auxiliary inductor $L_x$. The further simplified equivalent circuit of the leading leg at the transition time is shown in Fig. 4(b). $L_f$ resonates with $C_s$ during the transition period with the initial current $I_{rest}$ and resonant period $T_c$, which are given in (8) and (9) respectively.

$$I_{rest} = (I_o - \Delta I_o / 2) / n_{TR} \tag{8}$$

$$T_c = 2\pi \sqrt{C_s L_{f}} \tag{9}$$

There are three different cases for the transition of leading leg, according to the value relationship between $I_{rest}$ and $I_{out}$ which is shown in Fig. 5 [13], [15].

Assuming the dead time to be $T_c / 4$, we can get the voltage across the output capacitor $C_s$ at the end of dead time for different leakage inductance, magnetizing inductance and auxiliary inductance. Fig. 6 and Fig. 7 show the results without considering the input voltage clamp. At the end of dead time, if voltage $V_{Cs}$ is higher than the input voltage ($V_{in} = 400$V), ZVS can be achieved.

A conclusion can be drawn from Fig. 6 and Fig. 7 that if ZVS cannot be achieved, either a larger leakage inductance or a smaller auxiliary inductance should be used. Compared with the converters presented in [10] and [13], there’s no large redundant assistant current at light load, so the conduction losses at light load is reduced.

![Fig. 6. Voltage across the parasitic capacitor $C_s$ at the end of the transiting period versus load current $I_o$ at different leakage inductance $L_{Lk}$ ($L_x = 410 \mu H, L_f = 26 \mu H$ and $V_{in} = 400$V).](image)

From the above analysis, larger leakage inductance and smaller auxiliary inductance is helpful to achieve ZVS. On the other hand, with smaller leakage inductance, duty cycle loss and voltage ringing can be reduced. So a compromise must be reached between conduction losses and duty cycle loss and voltage ringing.
IV. EXPERIMENTAL RESULTS

An 1kW/100kHz (Input: 300-400 VDC; Output: 50V/20A) prototype is built to verify the operation. The main components and some key parameters are listed in Table I. To damp the ringing between the rectifier diodes and the leakage inductor, a RCD-snubber circuit is employed.

<table>
<thead>
<tr>
<th>Components</th>
<th>Parameters</th>
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<tbody>
<tr>
<td>Vin (Input voltage)</td>
<td>300 V-400V</td>
</tr>
<tr>
<td>Vout (Output voltage)</td>
<td>50 V</td>
</tr>
<tr>
<td>Pout (Maximum output power)</td>
<td>1000 W</td>
</tr>
<tr>
<td>f_s (Switching frequency)</td>
<td>100 kHz</td>
</tr>
<tr>
<td>L_f (output filter inductor)</td>
<td>26 μH</td>
</tr>
<tr>
<td>n_TR (Turns ratio of transformer)</td>
<td>19/4</td>
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<tr>
<td>L_m (magnetizing inductance)</td>
<td>420μH</td>
</tr>
<tr>
<td>L_A (auxiliary inductance)</td>
<td>381 μH</td>
</tr>
<tr>
<td>L_{lk} (Leakage inductance)</td>
<td>12.1 μH</td>
</tr>
<tr>
<td>S (Power MOSFETs)</td>
<td>IXFH24N50</td>
</tr>
<tr>
<td>D_R (Diodes)</td>
<td>MBR20200</td>
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<tr>
<td>t_d (dead time)</td>
<td>160ns</td>
</tr>
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<td>C (Output capacitor of MOSFET)</td>
<td>510pF</td>
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<tr>
<td>Controller</td>
<td>UC3895</td>
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Table I: Utilized Components and Parameters of the Prototype

Fig. 8 and 9 represent the voltage and current waveforms of TR and L_x at 50% load. It is shown that the voltage waveforms across TR and L_x are complementary, and the current i_x changes when i_p stays the same, which verifies the operation of the converter.

The ZVS operation waveforms of the leading leg and lagging leg at full load and 5% load are shown in the Fig. 10, respectively. As seen in all these waveforms, the drain voltage falls to zero before the rise of the corresponding gate voltage. ZVS operation is well achieved for all primary switches over the full load range.

In order to illustrate the efficiency improvement, another similar converter is built, which only does not utilizing the magnetizing current. Because the magnetizing inductance of this converter is much larger than the auxiliary inductance, the auxiliary inductance must be much smaller than that in the proposed converter to ensure full load range ZVS. Fig. 11 shows the overall efficiency of the two similar converters, compared to a conventional PSFB converter utilizing a large leakage inductance. At high load the efficiencies of the two
similar converters are almost the same, and are both about 2% higher than the conventional one. However, at light load the proposed converter has a much higher efficiency than that without utilizing the magnetizing current, because the assistant current increases considerably when duty ratio is small in the converter without utilizing the magnetizing current. The efficiency higher than 90% is achieved from 20% load to full load, and the efficiency of 95% is achieved at full load for the proposed converter.

![Efficiency Comparison](image_url)

**Fig. 11. Efficiency comparison.**

V. CONCLUSION

A new phase-shift full-bridge circuit featuring ZVS over the full load range and a wide input voltage range is proposed in this paper. The ZVS is achieved using adaptive power stored in an auxiliary inductor and the magnetizing inductance of the power transformer. As the leakage inductance is much smaller compared to that of conventional phase-shift full-bridge converters, the duty cycle loss is reduced. Because the assistant current for achieving ZVS is almost the same for any duty ratio, there is no large redundant assistant current and the conduction losses are reduced at light load. The operation is verified on a 1kW prototype, and the overall efficiency is improved more than 2% with respect to the conventional PSFB converter.

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REFERENCES


