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Optimal Transmission Rate for Ultra Low-Power Receivers

J.H.C. van den Heuvel∗, J.P.M.G. Linnartz† and P.G.M. Baltus∗
∗Eindhoven University of Technology, Dept. of Electrical Engineering
Den Dolech 2, Eindhoven, the Netherlands
Email: J.H.C.v.d.Heuvel@tue.nl
†Philips Research, High Tech Campus, Eindhoven, the Netherlands

Abstract—In many wireless systems, the energy consumed by the receiver is significantly larger than the energy consumed by the transmitter, possibly even by orders of magnitudes. This paper derives an analytical solution to maximize the throughput per unit of available receiver circuit power. Adaptive control of the IP3, to handle the time-varying adjacent channel interference level, can substantially improve the power efficiency, compared to the common practice of design for worst case. There appears to be an optimum throughput at a specific (non zero) power consumption level. For large SNR, the optimal throughput per Joule of receiver circuit power occurs for a modulation rate of 2.3 bits/s/Hz, irrespective of interference power level. If the receiver has less power available than the optimum setting requires, a duty cycling scheme can still achieve optimum operation.

I. INTRODUCTION

The motivation to optimize throughput for a receiver with a limited availability of battery power is two-fold. In many applications, the mobile user spends significantly more time receiving data than transmitting. Often, the energy consumed in receiving mode is several orders of magnitude larger than the energy consumed in transmit mode [1] [2], even if the transmitter circuit power consumption is larger than the receiver circuit power consumption when switched on. Secondly, in a short range link, the transmit power can be relatively small. So the transmit power amplifier is no longer the main power consumer. Yet, the receiver front end often needs to recover a weak signal in the presence of strong adjacent channel interference, which requires highly linear, thus power hungry RF designs. In the absence of disruptive new approaches, we expect that this trend will continue for the foreseeable future.

The aim of our analysis is to extend our work in [3] and to find an appropriate operation point for each of the analog stages of a power-constrained receiver, such that its user data throughput is maximized per Joule of receiver circuit power spent. The optimum appears to depend mainly on the strength of adjacent channel interference. Too low receiver circuit power would lead to a highly non-linear receiver, hence strong distortion and low throughput. Too high values of receiver circuit power would create an unnecessarily linear receiver, which cannot be exploited because of the finite signal-to-channel-noise ratio of the received signal. Yet even with very large signal-to-noise ratios, it appears to be more energy efficient to use a receiver with modest linearity. There appears to be an optimum choice of the distribution of gain, noise figure and linearity along the cascade, which yields the highest throughput per unit of receiver circuit power. For very low available receiver circuit power, our results imply that a duty cycle strategy is more efficient than continuous operation. The receiver is proposed to operate in bursts.

A commonly used direct-conversion receiver architecture is used in our analysis. In most receivers a broad band signal is processed at radio frequency (RF) by the analog front end, where the desired signal only occupies a small portion of the front-end bandwidth. To present the desired signal to the baseband (BB) ADC, the analog front end amplifies, downconverts, and filters the received RF broadband signal. Therefore, the first stages of our receiver usually contains strong adjacent channel interferers, with a priori not fully known statistical properties [4]. These signals need to be handled with adequate linearity to avoid excessive distortion spill-over into the band of the desired signal [5]. Generally, a higher linearity requirement leads to a higher power consumption of the analog circuit. In conventional RF designs the linearity is fixed and specified for the highest power of the interference at which the receiver should still operate. Thus results in an overly linear design at all lower values of the interference power, reducing battery lifetime unnecessarily. Most RF designs are based on a set of system specifications, determined by standardization [5], such specifications may include packet error rates, sensitivity and modulation. An RF designer than strives to design a receiver at the lowest power possible, for this target [6], [7].

Conversely, we want to determine the maximum throughput efficiency possible in terms of bits per unit of available receiver circuit power budget. To formulate this optimum we do not a priori fix the system specifications, such as the modulation constellation. Rather, we assume that the key RF receiver specifications, IP3, gain, and noise figure, are adaptive. The optimum throughput efficiency might seem to depend on a large number of independent variables, but for a given IC process, several design performance indicators have known achievable values [8]. This reduces the number of independent variables which determine the optimum of the throughput [3]. We conclude that at large SNR, the most power-efficient receiver (in terms of Joule/bit) will operate near 2.3 bits/s/Hz. We give an expression for its power consumption in (34).
II. MODELING SYSTEM THROUGHPUT EFFICIENCY

To operate a wireless network at the highest efficiency possible, in terms of bits per second per unit of receiver circuit power, we strive to find the receiver circuit power $P_r$ at which the throughput $T$ is maximized using

$$\bar{P}_r = \arg \max_{P_r} \left( \frac{T}{P_r} \right).$$

That is, we search the most efficient receiver circuit power budget. The inner optimization for a given receiver circuit budget with $\sum P_m = P_r$ is given by

$$\bar{T} = \max T | \sum P_m = P_r,$n

here $P_m$ is the power allocated to the $m^{th}$ stage of a receiver circuit. The maximum is taken over all possible settings of the RF stages, provided that the total consumed power does not exceed $P_r$. We use the capacity expression

$$T = \log_2 \left( 1 + \frac{S}{N_{tot}} \right)$$

as a measure of achievable throughput $T$. Here $S$ is the input signal power. Yet, $T$ should not be interpreted as the Shannon capacity of the system in information theoretic sense: if the sampling and ADC circuits are allowed to capture the entire band, including the interference signal, the distortion can be predicted by the BB DSP and its effect can be eliminated, at least from an information theoretical perspective. Hence one could design a receiver that has higher throughput than the value found in (3). However, such a receiver architecture would be at odds with our ambition to minimize the receiver circuit power consumption. Lacking a better model, we define the throughput $T$ as in (3). The total noise plus distortion, relative to power levels at the input, is

$$N_{tot} = N_{th} + N_r + N_d = \frac{N_r}{G_{tot}} + \frac{N_d}{G_{tot}},$$

where $N_{th}$ is the noise in the channel, $N_r$ the electronics noise added by the analog circuits of the receiver, and $N_d$ is the distortion caused by an interferer. Other RF impairments such as LO leakage, DC leakage and images are not considered, since they are related to the architecture, topology and layout, which are beyond the scope of this paper. The AWGN noise in the channel is given by $N_{th} = kTB$, where $k = 1.38 \times 10^{-23}$ is Boltzmann’s constant, $T$ is the temperature and $B$ is the bandwidth of the desired signal. Further, $G_{tot}$ is the total maximum power gain of the analog receiver given by

$$G_{tot} = \prod_{m=1}^{M} G_m,$n

where $G_m$ is the gain of the $m^{th}$ stage in the cascade (Figure 1). We now need a more detailed model of $N_d$ and $N_r$.

A. Distortion and Noise

The distortion is expressed as [3]

$$N_d = \frac{G_{tot} P_{int}^3}{IP3_{tot}^3}.$$ (6)

Here $IP3_m$ is the third order intercept point of the $m^{th}$ stage. We simplify our model by assuming that, after further channel selectivity filtering, Nyquist sampling and A/D conversion, the baseband processing engine of the receiver has no further knowledge of this distortion signal, and experiences it as AWGN [9]. The total worst case $IP3$ of $M$ stages can be calculated via [8]

$$IP3_{tot} = \left( \sum_{m=1}^{M} \prod_{j=m}^{M-1} G_j \right)^{-1},$$ (7)

under the worst case assumption that all distortion components are in-phase.

Next to the distortion signals, the analog front end adds noise $N_r$ to the desired signal. This addition of noise is modeled via the noise figure (NF), and is defined as $NF = 10 \log_{10}(F_m)$. Here, the noise factor $F_m$ is defined as:

$$F_m = \frac{SNR_m}{SNR_{m+1}},$$ (8)

where $SNR_m$ is the SNR at the input, and $SNR_{m+1}$ is the SNR at the output of the $m^{th}$ stage in a cascade. Note that the noise figures do not model the contribution by distortion. The total noise-factor of $M$ stages in a cascade, $F_{tot}$, can be calculated via Friis formula

$$F_{tot} = 1 + \sum_{m=1}^{M} F_m - 1 \prod_{j=m}^{M-1} G_j,$n

where $F_m$ the noise-factor of the $m^{th}$ stage and $G_j$ the gain of the $j^{th}$ stage. Moreover, the total noise factor must satisfy

$$F_{tot} = 1 + \frac{N_r}{G_{tot} N_{th}}$$ (9)

where $G_{tot}$ is the total gain of the analog circuit and $N_r$ is the variance of the electronics noise added by all analog circuits weighed with the partial gains. The electronics noise can now be expressed as

$$N_r = (F_{tot} - 1) N_{th} G_{tot}.$$ (10)

By combining (4) (6) and (11), the total noise plus distortion, normalized to power levels present at the input, is now given by

$$N_{tot} = F_{tot} N_{th} + \frac{P_{int}^3}{IP3_{tot}^3},$$ (12)

where $IP3_{tot}$ follows from (7) and $F_{tot}$ from (9). Figure 1 now depicts the receiver model, where every individual stage has variable gain $(G_1, \cdots, G_M)$ and IP3 $(IP3_1, \cdots, IP3_M)$, thus allowing for variable $IP3_{tot}$ and variable $F_{tot}$ of the receiver cascade.
C. Minimum Power Cascade Optimization Method

1) Linearity Factor Model: A commonly used equivalent figure of merit (EFOM) [8] is

\[ P_m = \frac{f_m G_m IP3_m}{\kappa_m}, \]  \hspace{1cm} (16)\]

where \( f_m \) is the power limiting bandwidth and \( \kappa_m \) is the power linearity factor of the \( m^{th} \) stage. The most appropriate parameter to choose for \( f_m \) highly depends on the circuit functionality. For LNAs with a dominant pole, the bandwidth is an appropriate choice. By using an EFOM, \( P_m \) theoretically does not depend on the noise figure \( F_m \). By using structure independent transforms (SIT), it is possible to trade IP3, gain and power dissipation, to transform a chosen topology for each circuit block to a circuit with the optimal specification [10]. Creating a topology that can also change IP3 adaptively and still meet (16) is a topic of current IC design research.

2) Dual Lagrange Optimization Method: So,

\[ P_{\text{min}} = \min_{G_1, \cdots, G_M} \left( \sum_{m=1}^{M} \frac{f_m G_m IP3_m}{\kappa_m} \right), \]  \hspace{1cm} (17)\]

while achieving the \( G_{\text{tot}} \) using (5), \( IP3_{\text{tot}} \) using (7), and \( F_{\text{to}} \) using (9). In this optimization process, the \( f_m, \kappa_m \) and \( F_m \) of a cascade are taken as constant. The individual \( F_m \) is kept constant because the \( F_m \) is limited by the topology and used IC process technology. A closed form expression [8] for the minimal analog signal conditioning (ASC) power dissipation as a function of the overall noise factor \( F_{\text{to}} \) is,

\[ P_{\text{min}} = IP3_{\text{tot}} \left( \sqrt{F_e} + \sqrt{\frac{F_w}{F_{\text{tot}}-F_1}} \right)^2, \]  \hspace{1cm} (18)\]

where the "weighed excess noise factor" \( F_w \) is defined as

\[ F_w = \left( \sum_{m=1}^{M-1} \frac{f_m}{\kappa_m} (F_m - 1) \right)^3. \]  \hspace{1cm} (19)\]

Here the excess noise factor of the final stage is

\[ F_e = \frac{f_m}{\kappa_m} G_{\text{tot}}, \]  \hspace{1cm} (20)\]

which is a fixed value.

D. Maximum Throughput Cascade Optimization Method

While (18) gives the minimum power \( P_{\text{min}} \) needed to satisfy a required \( IP3_{\text{tot}} \), we can conversely claim that the best \( IP3_{\text{tot}} \) that one can achieve for a given available \( P_r \) equals

\[ IP3_{\text{tot}} = P_r \left( \sqrt{F_e} + \sqrt{\frac{F_w}{F_{\text{tot}}-F_1}} \right)^{-2}. \]  \hspace{1cm} (21)\]

Now, we can rewrite the total noise (4) as a function depending on \( F_{\text{tot}}, P_{\text{int}} \) and \( P_r \)

\[ N_{\text{tot}} = F_{\text{tot}} N_{\text{th}} + \frac{IP3_{\text{tot}}}{F_e} \left( \sqrt{F_e} + \sqrt{\frac{F_w}{F_{\text{tot}}-F_1}} \right)^4 \]  \hspace{1cm} (22)\]

B. Optimum Throughput

In [3] our aim is to optimize the power budget \( P_r \) over the various stages such that throughput \( T \) is optimum under the constraint of a given technology, a given received power \( S \), total gain \( G_{\text{tot}} \) needed to drive the ADC and channel parameters \( N_{\text{th}} \) and \( F_{\text{int}} \). In [3] we first addressed how for a chosen \( P_{\text{tot}} \) and \( IP3_{\text{tot}} \) one can optimize the power budget \( P_r \) by optimally distributing the gains \( (G_1, \cdots, G_M) \) and \( IP3 \)’s \( (IP3_1, \cdots, IP3_M) \) over the cascade. In fact, this is a mathematical formalization of a commonly encountered design problem in RF design, of optimizing each circuit block to meet a given spec for the receiver. In [8] a double Lagrangian tool is proposed for this exercise, to solve the distribution of the gains and \( IP3 \) for the cascade. Paper [7] summarizes [8] for \( M = 2 \). This Minimum Power Cascade Optimization (MPCO) solves:

\[ P_{\text{min}} = \min \left( \sum_{m=1}^{M} P_m \right), \]  \hspace{1cm} (13)\]

where \( P_m \) is the power dissipation of circuit block \( m \), as will be covered by (16). In [3] we extend the MPCO by further optimizing \( P_{\text{tot}} \) and \( IP3_{\text{tot}} \) to satisfy our end goal of maximizing the throughput, thus searching for

\[ \hat{T} = \max_{F_m, IP3_{\text{tot}}} (T), \]  \hspace{1cm} (14)\]

where the available receiver circuit power \( P_r \), satisfies \( P_r = P_{\text{min}} \) as in (13). This is achieved by expressing the power optimal \( IP3_{\text{tot}} \), called \( IP3_{\text{opt}} \), as a closed form function (21) of the figure of merits related to the used IC design process, the available receiver circuit power \( P_r \), the power optimal total noise factor \( F_{\text{tot}} \) and total gain \( G_{\text{tot}} \). Therefore, we can write \( N_{\text{tot}} \) as a function of \( F_{\text{tot}} \) and the available receiver circuit power \( P_r \). Our claim is that in the end the maximization in (14), for a given power budget \( P_r \), is equal to minimizing the total noise according to

\[ \hat{N}_{\text{tot}} = \min_{F_m} \left( N_{\text{tot}} (IP3_{\text{tot}}(F_{\text{tot}})) \right). \]  \hspace{1cm} (15)\]

We call this a Maximum Throughput Cascade Optimization Method (MTCO).
By combining (2), (3), (4), and (22), we can maximize $T$ by minimizing $N_{tot}$. We require that

$$\frac{d N_{tot}(F_{tot})}{d F_{tot}} \bigg|_{F_{tot} = \hat{F}_{tot}} = 0,$$  

and obtain $\hat{F}_{tot}$ as $\hat{F}_{tot} = F_1 + \frac{4 F_{\text{th}}}{2^{2/3} (\sqrt{F_c + \sqrt{F_c + 2^{5/3} (F_{\text{th}} N_{th} F_{\text{int}}^2 \text{tot})^2/3})^2}.$

Applying this value of $\hat{F}_{tot}$ means that (11) turns into

$$(F_1 - 1) N_{th} + \frac{4 F_{\text{th}} N_{th}}{-\sqrt{F_c + \sqrt{F_c + 2^{5/3} (F_{\text{th}} N_{th} F_{\text{int}}^2 \text{tot})^2/3})^2} = 0,$$  

and (6) turns into $N_d/G_{\text{tot}} =$

$$\frac{P_{\text{int}}}{2^{3/4}} \left( \sqrt{F_c + \sqrt{F_c + 2^{5/3} (F_{\text{th}} N_{th} F_{\text{int}}^2 \text{tot})^2/3})^2} \right)^4,$$

which we insert in (3) and (4). We now have found an analytically closed-form solution which maximizes the throughput for a given circuit power budget $P_r$. We also found closed-form solutions for $\hat{F}_{tot}$ and $\hat{F}_{3\text{tot}}$ that achieve the optimum throughput, respectively (24) and (21) with (24) inserted. The individual gain $(G_1, \ldots, G_M)$ and $IP_3$ ($IP_{31}, \ldots, IP_{3M}$) per stage follow from [8]. In Section III we give an example of MPCO to motivate our search for the MTCO, calculating the efficiency in terms of bits/Joule for a target $NF_{\text{tot}} = 2$ dB, with first $IP_{3\text{tot}} = -40$ dBm, and secondly $IP_{3\text{tot}} = -20$ dBm. Surprisingly, in our scenario, the efficiency at $IP_{3\text{tot}} = -40$ dBm is more than an order of magnitude larger than at $IP_{3\text{tot}} = -20$ dBm, namely 4.4 Gbit/Joule and 0.3 Gbit/Joule, respectively. The difference in $P_r$ is 8 dBm (5.9 mW) versus 28 dBm (590 mW), respectively.

**E. Variable Third Order Intercept Point**

With increasing interference power $P_{\text{int}}$, both the second and third noise term in (4) will increase. The second term increases, because to mitigate a more powerful interferer, more linearity is required so noise figure often is sacrificed. The third noise contribution increases as a function of $P_{\text{int}}$, because a more powerful interferer means more distortion. The only option to meet target specifications is to make more receiver circuit power available. Conversely, a weaker interferer can be handled with less power in the analog circuits.

In conventional RF design, the total $IP_3$ is determined by a worst case channel to interference ratio (CIR) as defined by the standard, where

$$\text{CIR} = \frac{S}{P_{\text{int}}}.$$  

An example of a common value for the CIR in the IEEE 802.11b standard at which the receiver should still operate in standardization is -30 dB. This implies that a conventional design wastes power to achieve a certain linearity, when the actual value of the CIR is lower than the worst case.

A variable $IP_3$ setting in the receiver adds an additional degree of freedom and allows the power consumption of the receiver to lower. The receiver can now adapt itself to the instantaneous value of the CIR, instead of to the worst case required by the standard. In the MTCO the optimal throughput of the system as a function of the available receiver and interference power is calculated. Figure 2 shows the simulation results for the system specifications of Table I, $S/N_{th} = 30$ dB, $k = 1.38 \times 10^{-23}$, $T = 295$ K, $G_{\text{tot}} = 65$ dB, and $B = 22$ MHz. In Figure 2 it can be seen that a reduction of the CIR of 20 dB allows for a reduction of the power consumption of 30 dB for a given target rate. The factor $\frac{3}{2}$ relation between CIR and $P_r$ follows from (6). This implies that a receiver with adaptive $IP_3$ could opportunistically scale back the $IP_3$, in the absence of large interferers, to operate in a substantially lower power mode, potentially orders of magnitudes. We recognize that this can be challenge in IC design as changing the $IP_3$ typically also changes in and output impedances of receiver stages which can lead to a power mismatch, which can reduce the aforementioned benefits. A relation between CIR and power consumption was observed earlier [4]-[8], but in this paper we have quantified this relation.

**F. Maximum Throughput Efficiency**

The throughput efficiency observes an optimum, as depicted in Figure 3. The location of the optimum is technology-dependent and directly relates to the linearity factors $\kappa$. The optima as in Figure 3 are depicted in Figure 4 for different values of CIR. These form a straight line on a logarithmic scale, with an angle of the line being $\alpha = -\frac{3 \text{dBm}}{2 \text{dB}}$, due to (6). Therefore, we only need to find one optimum to calculate all other optima for different CIR. This relation can be expressed as

$$P_{\text{opt}} = P_{\text{opt}, 0 \text{dB}} - \alpha \text{CIR},$$

where $P_{\text{opt}, 0 \text{dB}}$ is the optimum at $CIR = 0 \text{dB}$ and $P_{\text{opt}}$ is expressed in dBm and CIR in dBs.

We now derive the throughput related to the maximum in Figure 3, the throughput $T$ corresponding to

$$\tilde{T}_{MT} = \max_{P_r} \tilde{T}$$

The corresponding value of $T$ is now called the maximum throughput $\tilde{T}_{MT}$. Results are plotted in Figure 5. As can be observed in Figure 5, $\tilde{T}_{MT}$ converges to an upper limit for high values of the SNR. For large values of SNR we can simplify Equation (25) to

$$\lim_{SNR \to \infty} T = \log_2 \left( 1 + \frac{S P_r^2}{P_{\text{int}}^2 (\frac{1}{2} - G_{\text{tot}})^2} \right).$$

We are interested in finding $\tilde{T}_{MT}$. Thus solving

$$\frac{\delta}{\delta P_r} \left( \log_2(1 + \alpha P_r^2) \right) = 0.$$
where

\[ \alpha = \frac{S}{P_{\text{int}}^3 (f_n G_{\text{tot}})^2}, \tag{32} \]
yields,

\[ 2\sigma - (1 + \alpha) \ln(1 + \sigma) = 0, \tag{33} \]
where \( \sigma = \alpha P_r^2 \).

A numerical approximation for \( \sigma \) yields \( \sigma = 3.9 \), and the limit of \( \tilde{T}_r \) at large SNR is \( \tilde{T}_r = 2.3 \) bits/s/Hz. The \( P_r \) corresponding to \( \tilde{T}_r \) at large SNR, \( \tilde{P}_r \), is given by

\[ \tilde{P}_r = \sqrt{\sigma} \sqrt{P_{\text{int}}^3 (f_n G_{\text{tot}})} \tag{34} \]

A conclusion is that we showed the most power efficient receiver in terms of Joule/bit at large SNR will operate near 2.3 bits/s/Hz and its power consumption has been calculated in (34).

We believe this result is significant. A system designer can fix the modulation and coding method to 2.3 bits/s/Hz irrespective of the channel and interference conditions. Moreover the transmitter does not need to know the IC technology used for the transmitter, because the optimum is independent of IC technology. The receiver than adapts \( G, IP3 \), but there is no need to adapt transmitter settings. By fixing the throughput to 2.3 bits/s/Hz we are generally well below the available channel capacity for high SNR \((\log_2(1 + S/N_{th}))\). Therefore, we effectively exchange excess transmit power of for example a mains powered base station for maximal receiver circuit efficiency in a hand held device. An additional argument is that for most wireless network applications, mobile users spend only a short amount of time transmitting. Thus the energy consumed for receiving is orders of magnitudes larger than for transmitting [1] [2]. From this perspective it makes sense to focus at reducing the receiver circuit energy consumption.

G. Duty Cycling

A strategy to operate at the optimal efficiency and to achieve lower average power consumption is duty cycling. The receiver operates at the optimal efficiency and switches on and off according to the available circuit power. Via (3), (4), (25), and (26) the throughput which corresponds to the maxima of the curves in Figure 3 is calculated, results are shown in Figure 5. Interestingly, the optimum throughput is independent of the CIR. However, the receiver circuit power required to achieve this throughput is not (Figure 4). At large SNR this relation is given by (34).

However, in systems with very short duty cycles, the overhead for short packages can be prohibitive. In such cases there exists a tradeoff between the delay for merging packets versus the optimal power consumption. Furthermore, at the right hand side of the optimum, the throughput \( T \) expressed in bit/s/Hz can increase by making more circuit power available. However, the throughput \( BT/P_r \) expressed in bits/Joule cannot increase if a more power consuming circuit is used. Designing for better linearity than, to accommodate a crude modulation of 2.3 bit/s/Hz, does not pay off.
reduction in CIR requirements results in a 30 dB reduction in receiver circuit power consumption. For large SNR the optimal throughput per unit of receiver circuit power is 2.3 bits/s/Hz, irrespective of interference power level. This result has interesting consequences for new standards and can aid in the design of new standards and wireless networks to extend battery lifetime, since in typical applications most energy in mobile devices is consumed by the receiver chain. Therefore, a duty cycling strategy at low power consumption levels results in a higher system throughput. Interestingly, our analysis can be used as a method to determine whether duty cycling is a good design strategy for low power fixed receivers in a given technology.

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