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A Low-Power, High-Sensitivity Injection-Locked Oscillator for 60 GHz WPAN Applications

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Abstract — This article presents a 60 GHz low-power injection-locked oscillator in TSMC 65 nm technology. By using the frequency sweeping technique, a simulated 7 GHz total locking range is achieved, which covers the entire 60 GHz ISM band. The simulated settling time is less than 2 ns for each sweeping step with -60 dBm injection power. The DC power consumption is 1 mW of the oscillator core, and 5 mW in total for the input and output buffers, which are mainly used for the matching purpose.

Index Terms — 60 GHz, WPAN, Low Power, CMOS, injection locking, self-demodulating.

I. INTRODUCTION

The wireless personal area network (WPAN) is a wireless network that interconnects communication devices in a short range, e.g. within 10 meters. It gains momentum recently with the rapid evolution of wireless technologies and begins to play a crucial role in people’s daily life and business. One example is Bluetooth system, which transmits data with 1 to 3 Mbps within 100 meters. The IEEE 802.15 task group has been making several WPAN standards to fulfill different application requirements, shown in Fig. 1 [1] [2].

Recently, the 60 GHz WPAN draws a lot of attention because of its 7 GHz unlicensed spectrum and versatile applications. Besides, it also has some attractive features, such as small electronics feature size, inherent suitability to directional antennas, high security and high frequency reuse factor. However, the power consumption of an RF front-end at such high frequencies is often too large to make it attractive to be used for small mobile devices like a PDA or an MP4 player. Duty-cycled or wake-up radios are helpful to save power compared to always-on devices. Besides, direct conversion structure and constant envelope modulations of radios are also widely used to reduce the power consumed by the local oscillator (LO) or system linearity requirements, which are normally power-hungry. However, a duty-cycled radio still suffers from the turn-on power consumed for settling the oscillator, i.e. stabilizing the phase-locked-loop (PLL) even for simple direct conversion receiver. It turns out to be even worse when the radio is turned on and off quite frequently, e.g. in WPAN applications [3].

Based on the discussion above, a self-demodulating concept is proposed in this paper, which is especially suitable for on-off keying (OOK) modulation. Instead of using the combination of a voltage-controlled-oscillator (VCO) and a PLL, an injection-locked oscillator (IJLO) is used to capture the RF signal frequency and produce a large output voltage to drive the mixer. The RF and the oscillator signals will be mixed and produce baseband DC signals directly. When input RF amplitude is high, the mixer output DC level will be high and recognized as, e.g. “1”. Conversely, when the RF amplitude is low, the DC level will be low and will be recognized as, e.g. “0”.

The IJLO theory, trade-offs, design methodology and circuits are discussed and verified in sections II and III. Simulation results are given based on all these theories and models in section IV and conclusions will be given in V.

II. THEORETICAL ANALYSIS

Basic IJLO theory and system trade-offs will be discussed in this section.

A. Injection Theory and Locking Range

The injection locking phenomenon is well described in [4]. The oscillator can be conceptually modeled as a gain stage with a positive feedback and an L-C tank load. When injecting a current into the tank, a phase shift $\phi$ will be created between the injection current $I_{inj}$ (reference) and oscillation current $I_{osc}$. In order to compensate this phase
shift and maintain a closed loop phase shift of \(2\pi\), the oscillation current will shift its frequency to the frequency of the injection current. The double-side locking range \((\omega_L)\) is shown to be

\[
\omega_L = \frac{\omega_0}{Q} \frac{l_{inj}}{l_{osc}} \sqrt{\frac{1}{l_{osc}^2} - \frac{l_{inj}^2}{l_{osc}^2}}
\]

where \(\omega_0\) is the resonating frequency, \(Q\) is the quality factor of the L-C tank. If \(l_{inj} < l_{osc}\) the double-side locking range is approximately \(\omega_L = \frac{\omega_0}{Q} \frac{l_{inj}}{l_{osc}}\) [4].

**B. Trade-offs and Discussions**

As discussed in I, typical duty-cycled or wake-up radios have significant turn-on power which is a problem if they are switched on and off frequently. So, for a self-demodulating receiver front-end, the main research questions are “is the IJLO settling fast enough to save power”, and: “what is the relationship among sensitivity, locking range and locking time”?

The time-varying phase difference between injected and oscillation signals are solved in:

\[
\theta(t) = 2 \arctan\left(\frac{1}{\sin \alpha} - \cot \alpha \tanh\left(\frac{\omega_0 \cos \alpha}{2} (t - t_0)\right)\right)
\]

where \(\alpha\) is the steady state phase shift between injected signal and oscillation signal and \(t_0\) is integration constant depending on the initial condition. When approaching the steady state, \(\theta(t)\) will converge to \(\alpha\), which can be solved by \(\alpha = \sin^{-1}\left(\frac{\omega_0 - \omega_{inj}}{\omega_{inj}}\right)\) [5].

If \(\omega_{inj}\) is sufficiently close to the center of the locking range \(\omega_L\), \(\alpha\) will be very small and the locking time will be sufficiently short for all possible initial phase within \([-\pi, \pi]\), see the Fig. 2 (the curves are symmetrical by x-axes if phases are negative). This condition can be achieved by tuning the central frequency of the oscillator in the time domain, and carefully choosing the tuning resolution. The resolution should be sufficiently small to get a fast convergence of the phase between injection and oscillating signals while it also should be large enough to make sure the frequency sweeping time is not too long compared to the payload transmission time.

For example, if the frequency tuning resolution is 45 MHz, the maximum \(\omega_{inj} - \omega_{inj}\) will be eventually smaller than 22.5 MHz. If the locking range is 250 MHz, the maximum steady state phase difference will be about \(5^\circ\), which is small enough for a fast convergence according to (2).

From the above discussions, smaller frequency tuning resolution and larger locking range means faster locking for each step, but it will increase the total step number over the entire 7 GHz band and reduce the system sensitivity. A trade-off should be made between the frequency tuning resolution and the single-point locking range.

In this work, the injection current ratio \((I_{inj}/I_{osc})\) is chosen as 4% to obtain a single-point locking range as 250 MHz and to keep -60 dBm sensitivity at 1 mA bias current. To lock on this signal, the resolution of the tuning module should be finer than 250 MHz. We choose a small resolution as 45 MHz (\(\alpha = 5^\circ\)). In Fig. 2, for every possible initial phase difference, the locking time is smaller than 20 ns. Let’s choose 20 ns as the tuning step. In the worst case, frequency sweeping starts from the lowest edge, but the injected signal frequency lies in the highest edge, the total sweeping and locking time will be around 3112 ns. In the best case, it will be only 20 ns, i.e. only one step of sweeping. When OOK signal is applied, the IJLO may lose its locking condition as if data is “0”. However, the next locking process will be ultra fast due to the small initial phase difference between the injected and oscillating signals. In this case, long series of “0” must be avoided with proper coding.

In the 60 GHz WPAN applications, the package length is on the order of several Mb to Gb and the data rate is above 2 Gbps, so the worst-case locking overhead is 6224 bits and it is only 0.6224% of a 1 Mb data package. Moreover, with the co-design among network, MAC and PHY layers, the worst case scenario can be avoided.

**III. CIRCUIT AND LAYOUT DESIGN**

The oscillator core is configured with cross-coupled common-source stages loaded by an L-C tank. The finger width of transistors is chosen as 2 um to increase the unity-gain frequency [6] and the number of finger is 1.

The bias current is chosen as 1 mA. This value is low enough to keep a 250 MHz locking range under 24 uA injection current, but high enough to provide sufficient negative conductance for the oscillator to start-up.

Frequency sweeping is realized two MOS varactors. By tuning the control voltage, the central frequency of the

![Fig. 2 Locking Time vs. initial phase difference.](image-url)
tank varies from 57 to 64 GHz. A DC detector is added at the output of the IJLO to mix the input and output signals and sense their difference. The detector is built by a passive mixer and a low-pass filter (LPF). When the IJLO is locked with the input signal, the output of the detector will be a large DC voltage. In the frequency locking phase, the transmitted signal should be modulated by “1” only.

A 156-step (7 GHz/45 MHz) control voltage is kept on sweeping and changing the central frequency of the oscillator. Let’s assume a RF signal with frequency $f_1$ is injected to the IJLO. The sweeping voltage tunes the tank resonating at $f_2$ and the locking range is $f_1$ to $f_2$. If $f_2 < f_1 < f_3$, i.e. the incoming frequency lies within the locking range, the oscillator will lock to the injected RF signal and shift its resonating frequency to $f_1$. As a result, a pure DC signal will be produced at the output of the detector and the detector will send back a control signal to stop frequency sweeping immediately.

Current-reuse technique is applied on the input cascode buffers to increase the current-gain and to compensate for the loss introduced by the matching network. By adding a series inductor $L$ at the gate of the upper transistor, the drain node of MOS transistor $M_1$ will be coupled to the gate of $M_2$, as shown in Fig. 3. As a result, the drain current of $M_2$ will hold a relation as in (2). In other words, the cascode stage is then transferred into a cascade stage. The current gain is squared while the DC power consumption is kept the same.

Therefore, we can calculate the drain current by

\[
I_{d2} = g_{m2} \cdot V_{gs2} = \frac{g_{m2} \cdot I_{d1}}{\alpha C_{gs2}} \cdot \frac{I_{d1}}{\omega} = \frac{\omega I_{d2}}{\alpha} \cdot \frac{I_{d1}}{\omega} \quad (2)
\]

where $I_{d1}$ and $I_{d2}$ are the drain currents of $M_1$ and $M_2$ respectively, $g_{m2}$ is the transconductance of $M_2$, $V_{gs2}$ is the gate-source voltage of $M_2$, $C_{gs2}$ is the gate-source capacitor, $\omega$ is the operating angular frequency, and $\omega_{C2}$ is the angular cut-off frequency of $M_2$ [7].

The complete circuit of IJLO is shown in Fig. 4. Since the mixer and filter at the output are fully passive, they do not consume extra power. A phase shifter is inserted in the input path to add more freedom if smaller initial phase difference and shorter locking time is needed.

Therefore, we can calculate the drain current by

\[
I_{d2} = \frac{g_{m2} \cdot \omega}{\alpha C_{gs2}} \cdot \frac{I_{d1}}{\omega} = \frac{\omega I_{d2}}{\alpha} \cdot \frac{I_{d1}}{\omega} \quad (2)
\]

where $I_{d1}$ and $I_{d2}$ are the drain currents of $M_1$ and $M_2$ respectively, $g_{m2}$ is the transconductance of $M_2$, $V_{gs2}$ is the gate-source voltage of $M_2$, $C_{gs2}$ is the gate-source capacitor, $\omega$ is the operating angular frequency, and $\omega_{C2}$ is the angular cut-off frequency of $M_2$ [7].

The layout of the IJLO is shown in Fig. 5. The input and output of the IJLO is connected to the bondpads with four pieces of co-planar waveguide (CPW) 50 Ohm transmission line. The differential inductor at the input is separated into two single-ended inductors (the middle two medium-sized in Fig. 5) to make layout more compact.

IV. SIMULATION RESULTS

The simulation results are shown in this section. The start-up behavior of the IJLO is shown in Fig. 6.
When sweeping the tuning voltage, the central frequency of the L-C tank is shifted from 57 to 64 GHz, shown in Fig. 7. A single point sensitivity curve is illustrated in Fig. 8. When the tuning voltage is 1, the tank is resonating at about 60 GHz. This curve will show up 156 times (tuning steps) in the entire 7 GHz bandwidth, and the trade-off between sensitivity and locking range can be observed too.

\[ EFOM = 10 \log \left( \frac{f_{RF}}{P_{DC}} \cdot LR \right) \cdot \text{Sensitivity} \]  

The performance of different IJLO's then can be compared in the following table.

<table>
<thead>
<tr>
<th></th>
<th>( f_{RF} ) (GHz)</th>
<th>( P_{DC} ) (mW)</th>
<th>Sensi (dBm)</th>
<th>LR (GHz)</th>
<th>EFOM</th>
</tr>
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<td>50</td>
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<td>15</td>
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</tr>
<tr>
<td>[10]</td>
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<td>15</td>
<td>-20</td>
<td>0.1</td>
<td>242.6</td>
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<tr>
<td><strong>This Work</strong></td>
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<td>1</td>
<td>-60</td>
<td>7</td>
<td>326</td>
</tr>
</tbody>
</table>

V. CONCLUSIONS

A 60 GHz frequency sweeping injection-locked oscillator with 7 GHz locking range is demonstrated. The power consumption of the oscillator core is 1 mW while the sensitivity for each sweeping point is better than -60 dBm, shown in Table I. The total IJLO settling time varies from 20 ns to 3 μs depending on the carrier frequency difference between the transmitter and the receiver. The IJLO is quite low-power and fast-settled compared to the PLL-based LO system whose settling time is typically in a range of 40 to 300 μs and the power consumption is in the level of tens to hundreds of milliwatt [8].

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