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Continuous deep reactive ion etching of tapered via holes for three-dimensional integration

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Abstract

A continuous SF₆/O₂ plasma process at room temperature has been used to etch tapered through-silicon vias using a DRIE-ICP tool. These features (10–100 μm in diameter) are aimed for applications in 3D integration and MEMS packaging. The effects of various process parameters such as O₂ flow rate, platen bias, pressure and substrate temperature on the via profile (depth, slope angle and aspect ratio) development are investigated. The etching mechanism was also studied and x-ray photoelectron spectroscopy (XPS) analysis reveals a SiO_x passivation layer of the order of ~ 2 nm on the via sidewall and a substantial temperature dependence. Both tapering and anisotropy of etching depend on this passivation layer formation. Finally, suitable tapered vias with an aspect ratio of ~ 5 and a slope angle of $\sim 83^\circ$ are obtained by properly balancing the etching regimes. In this condition, a maximum etch rate of $7 \mu\text{m min}^{-1}$ is achieved.

1. Introduction

3D integration is an emerging technology to overcome RC delay for submicron technology and to allow heterogeneous integration of chips, also known as the ‘System-in-Package’ concept [1]. These 3D stacked chips make use of vertical interconnects, i.e. vias that are passing completely through the silicon wafer to provide the electrical connection between the stacked wafers. Compared to the conventional wire-bonding technology, these through-silicon vias (TSV) provide the shortest interconnect length with the highest density. Moreover, TSVs enable the 3D stacking of MEMS devices and IC components to realize the miniaturization and the heterogeneous integration of microsystems [2, 3]. One possible route to fabricate TSVs consists of blind via etching, liner deposition (isolation layer, barrier and seed layer) and via filling. Physical vapor deposition (PVD) to deposit the liner stack including the seed layer and electroplating to fill the vias is the two preferred techniques due to low cost and

high throughput. However, PVD in high aspect ratio vias (AR > 4), especially straight vias, has limited step coverage [4]. In the case that there is no or insufficient seed layer at the bottom, vias will close during electroplating, leaving a void inside. A tapered via can facilitate a more conformal deposition because it increases the incident angle of the precursor species at the via bottom corner while decreases it at the top corner thereby improving the step coverage. However, the introduction of tapering slightly decreases the interconnection density due to the larger opening (undercut) of the vias. A typical slope angle between 80° and 85° is expected to be a good trade-off with respect to the seed layer deposition and top area opening [5, 6].

An overview on the various plasma-etching techniques for TSVs was published recently [7]. Amongst all techniques, the well-known Bosch process originally developed for MEMS fabrication has been used most extensively for etching straight vias [8, 9] and other features with high aspect ratio (AR > 10). But for the etching of tapered vias, a modified Bosch process

should be developed. A possible approach is to take advantage of the parameter ramping capability of the etching system. Burkett *et al* reported a slope angle of 80.4° by using a seven-module method with a continuously increased passivation time [10]. Another method is to insert an isotropic step subsequent to the Bosch process [11, 12]. The sidewall tapering depends mainly on the extra isotropic etching time, but is only effective at the top part of the vias. Furthermore, this latter process is only applicable when there are no other devices on the wafer. Since all these processes are based on the Bosch etching, they have the disadvantages of long process duration and scallop formation.

A continuous process of silicon etching using a SF_6/O_2 plasma is another promising alternative to make tapered vias. Continuous etching with the SF_6/O_2 plasma, but mainly in the cryogenic regime in order to obtain straight vias, has been reported [13, 14]. Continuous etching at room temperature has been demonstrated both for etching straight [15] and tapered [12, 16] vias, but with a limited aspect ratio. However, no extensive study has been reported so far. In this paper, we present an optimized process to create tapered vias and trenches with a continuous etching at room temperature in a commercially available deep reactive ion etching—inductively coupled plasma (DRIE-ICP) tool. The process window, the different regimes and the obtained results will be discussed in view of the applications in the 3D integration and MEMS packaging field.

2. Experimental setup and definition

The tool used for the tapered via etching experiments is an ASE etching tool from Surface Technology Systems, which is originally designed for the DRIE Bosch process. The system is equipped with a single ceramic process chamber for wafers with up to 200 mm diameter and an ICP plasma source. The maximum RF coil power is 3000 W and the frequency is 13.56 MHz. During processing, the wafer is electrostatically clamped to the chuck, and helium cooled. Another RF power signal (called platen power) is fed to the chuck to vary the bias potential of the wafer with respect to the plasma, thus separately controlling the energy of the incident ions. A throttle valve controls the pressure in the chamber in combination with a turbomolecular pump. Standard 150 mm (100) p-doped ($20\text{--}30\ \Omega\ \text{cm}$) silicon wafers were used. Patterns of via chains ranging from $10\ \mu\text{m}$ to $100\ \mu\text{m}$ in diameter in steps of $10\ \mu\text{m}$ are transferred to a $3\ \mu\text{m}$ thick thermal SiO_2 hard mask for etching (a total open area of 0.19%). The use of thin SiO_2 as the etch mask can avoid the via profile deviation due to a thick photoresist mask, and the redeposition of the resist inside the via as the contamination. Alternatively, low-temperature PECVD oxide can also be used as the hard mask and is compatible with the CMOS back-end process. The process parameters investigated in this work are the O_2 flow rate, platen bias, pressure and substrate temperature. The settings of each parameter are shown in table 1. When a certain parameter is investigated, the settings of other parameters are directly taken from the baseline recipe.

Figure 1. Schematic picture of the obtained tapered vias, with via parameter definition (local bowing, undercut, slope angle and depth).

Table 1. Baseline etching recipe with parameter variations.

Parameters	Investigation values	Baseline
Coil power (W)	2000	2000
SF_6 flow (sccm)	75	75
C_4F_8 flow (sccm)	5	5
O_2 flow (sccm)	45, 60, 75	60
Platen bias (W)	5, 15, 25	15
Pressure (mTorr)	20, 40, 60	40
Platen temperature ($^\circ\text{C}$)	$-10, 0, 10, 20, 25, 30$	10

After etching, the results are usually evaluated according to several profile parameters such as the etch rate, slope angle and via sidewall roughness. The definition of the obtained tapered via profile parameter is illustrated in figure 1. The requirements for a good tapered via shape are small undercut, constant sidewall slope around 83° , smooth surface and no local bowing.

3. Results and discussion

3.1. Effect of the $\text{O}_2/(\text{SF}_6+\text{O}_2)$ ratio and platen bias power

The addition of O_2 to the SF_6 gas flow in a plasma is known to drastically increase the F-radical concentration in the plasma. At a certain O_2 partial pressure, the F-radical concentration reaches a maximum before it starts decreasing due to dilution [17]. Similarly, the silicon etch rate increases due to a higher F-radical density and subsequently decreases because of a growing $\text{Si}_x\text{O}_y\text{F}_z$ film and F-radical dilution. This dominates the ion inhibitor regime of this process, i.e., the range of O_2 values which produce a growing film. Using the ratio of O_2 to the total gas flow $\text{O}_2/(\text{SF}_6+\text{O}_2)$ to control the sidewall angle in trenches has been previously shown [15, 18]. An increase of the ion bombardment energy can overcome the passivation process and modify the etching regime. The SEM images in figure 2 show via cross sections with the amount of additional O_2 gas flow varying from 37.5% (45 sccm) to 50% (75 sccm) and with a platen power from 5 to 25 W. The etch rate, undercut and slope angle as a function of the O_2 flow rate and platen

Figure 2. SEM cross-section images of vias from the nine recipes with different O_2 flow rates and platen bias power. Etch time: 20 min; mask opening: 90 μm diameter.

bias are plotted in figure 3. At low bias power (5 W) and high O_2 gas flow (75 and 60 sccm), the ions do not have enough energy to remove the local passivation $\text{Si}_x\text{O}_y\text{F}_z$ film. Therefore, the via walls are over-passivated, which results in a very low etch rate, anisotropic profile and a very rough surface with spikes. The high oxygen ratio is well known to lead to etching instabilities ('random spiking' [19]) in cryogenic etching. The vias are not tapered, and some peculiar shapes are observed with no measurable slope angle. Here, the etching is physically limited since the ion bombardment is too low. A reduction of the O_2 gas flow (45 sccm) improves the overall via shape, since at 5 W the ion bombardment becomes strong enough to remove the passivation layer. But at the same time, the etching tends to be more isotropic. As a result, the undercut increases dramatically, while the roughness remains significant in the low power bias-etching recipe.

Keeping the flow rate constant (45 sccm), an increase in the platen bias power (25 W) leads to even larger isotropic etching (bottom right in figure 2). In addition to the large undercut, the bowing here also becomes significant. The etch rate (i.e., the via depth) does not increase, but the total volume of the etched silicon is larger (+30%) due to lateral etching. This suggests a depletion of fluorine radicals in the vias from the top down to the bottom of the vias and thus a chemically limited regime. Between the two extremes (5 W, 75 sccm and 25 W, 45 sccm), intermediate etching regimes are observed, which leads to tapered vias within specifications. The 15 W, 60 sccm recipe is particularly interesting. In this case, the competition between the passivation and the ion bombardment seems to lead to a smooth via wall, a limited undercut, a tapering slope of 82.5° and a high etch rate. This suggests that above a certain slope angle, the incoming ions have a limited action on the passivation layer covering the via walls, whereas at the via bottom, efficient passivation layer etching is achieved. It is therefore possible to balance the passivation

and the etching within one continuous recipe. The 15 W, 60 sccm recipe has been identified as an optimized recipe to etch tapered vias. The slope angle can be tuned by varying the O_2 flow around 60 sccm, and/or varying the platen power around 15 W. Additionally the Si/SiO₂ etch selectivity is high (>100) for all the experiments except for the 5 W, 75 sccm recipe, while selectivity for the 15 W, 60 sccm recipe is ~ 190 .

3.2. Via width and aspect-ratio-dependent etching (ARDE)

In order to assess the ARDE effect, vias with different nominal widths ranging from 10 μm to 100 μm have been etched with this optimized recipe. Figure 4 shows SEM images of the cross sections for three relevant widths and figure 5 depicts the obtained aspect ratio versus the nominal width for a 20 min etch time. The aspect ratio is defined as the ratio between the via depth and the actual width of the via opening after etching. The first striking result is that the via shape is maintained regardless of the via width. The via slope remains in the range of 82.5° – 83° , while the undercut varies linearly with the nominal width. The ARDE is very moderate compared to the standard Bosch process for similar conditions [20]. Knudsen transport limitation does not seem to be as critical as in straight vias, since the large opening alleviates the diffusion conditions. The via depth shows a limited variation ($\sim 10\%$) over the width range, ensuring a significant aspect ratio increase above 3. This limited width dependence suggests that the etching mechanism remains the same regardless of the via size, and the slope angle depends only on the balance between etching and passivation.

3.3. Time dependence etching

After investigating the basics of the continuous etching with O_2 and SF_6 , the etch time has been increased up to 35 min in order to investigate how the etch rate and the via shape change with

Figure 3. Etch rate, slope angle and undercut versus platen bias for different O_2 flow rates.

time. Another reason to increase the etch time is to increase the aspect ratio of vias in view of TSV applications. The optimized 15 W, 60 sccm recipe from the previous experiments has been used for 35 min and the corresponding SEM pictures of 80 μm wide vias are shown in figure 6.

Figure 5. Depth and aspect ratio of vias etched with the optimized 15 W, 60 sccm recipe for different nominal widths. The aspect ratio has been calculated with the actual via width. Etch time: 20 min.

The via profile after 20 min of etching is indicated by the dashed line in the figure. Both the undercut and the depth increase almost linearly with time for all via sizes. The increasing undercut means that the sidewall passivation layer is continuously eroded during the etching. It suggests that the passivation layer does not completely protect the silicon from etching during the processing, but only decreases the lateral etch rate. The final via width increases much less with time than the final depth does, resulting in a larger aspect ratio of the vias.

3.4. Effect of pressure

Pressure is another important parameter in DRIE etching since it can efficiently change the ion flux, ion energy and the concentration of the F radicals in the plasma as well. In order to study the different parameters independently, the total gas flow was throttled [19]. The etching system can automatically adjust the automatic pressure control (APC) to keep the pressure constant. In this case, there is almost no change of the ion and radical density, but the ion mean free path is inversely proportional to pressure. In the meantime, the F-radical concentration increases with pressure. The purpose of this experiment is to understand how the pressure can change the anisotropic characteristic and the other profile parameters of etched vias, such as undercut and local bowing. Two experiments with a lower pressure of 20 mTorr and a higher pressure of 60 mTorr were conducted and the results were compared with the baseline recipe (15 W, 60 sccm) at

Figure 4. SEM cross-section images of vias with different initial widths etched with the optimized 15 W, 60 sccm recipe. Etch time: 20 min; mask openings: 90, 50 and 20 μm diameter.

Figure 6. Comparison of nominally 80 μm wide vias after 20 and 35 min of etching with the 15 W, 60 sccm recipe.

Figure 7. Via profiles for different pressures: 20, 40 and 60 mTorr. Etch time: 35 min; mask opening: 90 μm diameter.

40 mTorr. In figure 7, an illustrative comparison among the profiles is given.

At low pressure, the F-radical density is low while the ion energy is high, so the etching is limited by the isotropic etching of the F-radicals. It translates into an anisotropic-like etching with a steep via wall (88°) and a limited etch rate. With increasing pressure (up to 40 mTorr), more F-radicals are available from the plasma system, and the etch rate increases. The vias become more tapered and show a smaller local bowing. The continuous increase of the undercut with the pressure proves again that the undercut formation is dominated by the chemical etching of F-radicals. At high pressure (60 mTorr), the ion energy decreases considerably and the etching is limited by the ion sputtering of the passivation layer. From the SEM picture, we can clearly see the rough bottom, which is the evidence for the over-passivation that cannot be removed by the ions. High pressure corresponds to a physical-reaction-limited regime.

The results show that the slope angle decreases with pressure. This is similar to the results in work of Gomez *et al* who observed that the sidewall slope is determined by the F/O ratio [15]. The etch rate increases with the pressure in the chemical-reaction-limited regime and decreases in the physical-reaction-limited regime. The highest etch rate can be obtained at the transition point of the two regimes. A pressure of 40 mTorr produces the best result for the tapered via etching in our case. This value is maintained in the following experiments.

3.5. Effect of substrate temperature and passivation layer

The substrate temperature during etching is generally kept at 10°C (283 K) upon using the Bosch etch process as well as for some of the continuous etch processes. However, the effect of temperature on the via profile is not well understood yet. Tezcan *et al* [20] did some experiments and they found that the undercut is larger at 20°C than at 10°C , but the etch depth and etch rate are higher at 10°C . However, no explanation was given in their paper. Ranganathan *et al* indicate that the etch rate and the local bowing increase with increasing temperature [12]. We performed experiments at six different temperatures: $-10, 0, 10, 20, 25$ and 30°C . Figure 8(a) shows the corresponding SEM pictures and the close-ups of the via bottom at 0, 10 and 25°C are also shown in figure 8(b). At -10°C , huge spikes and roughness on the sidewall appear. At 0°C , the spikes become smaller and decrease even further at 10°C . At temperatures above 20°C , both the sidewall and the bottom become smooth and no spikes can be found. In addition to roughness change, the via shape varies with temperature as well. Although the etch rate remains constant throughout the entire temperature range, the undercut increases almost four times from -10 to 25°C as shown in figure 9(a). This suggests a more isotropic etching process and a decrease of the slope angle at higher temperature. The corresponding Arrhenius plot for the undercut is also shown in figure 9(b). It follows the equation $y = y_0 e^{-\frac{E_a}{kT}}$ with E_a being the activation energy of the process, which suggests that the top part via formation (i.e., the undercut part) is a thermally excited reaction. Deeper

Figure 8. (a) SEM pictures of vias etched with different temperatures from -10°C to 30°C ; (b) the roughness of the via bottom etched at 0, 10 and 25°C . Etch time: 35 min; mask opening: $90\text{ }\mu\text{m}$ diameter.

Figure 9. (a) Undercut and etch rate for $100\text{ }\mu\text{m}$ diameter vias at different temperatures; (b) Arrhenius plot of the undercut versus temperature.

in the via, a changing slope along the sidewall is observed. At low temperatures, the slope angle changes toward more positive tapering at the bottom of the vias. At 10°C the change becomes smaller and above 20°C , the slope change is reversed toward the negative tapering. It seems that the temperature can induce a transition from the physical-reaction-limited regime to the chemical-reaction-limited regime.

This can be due to a different passivation layer formation versus substrate temperature. In order to investigate the formation of a passivation layer in more detail, an x-ray

photo-electron spectroscopy (XPS) analysis was performed. XPS inspection was carried out with a $10\text{ }\mu\text{m}$ (nominal) spot on samples etched at three different temperatures: 0, 10 and 25°C . The atomic surface concentration of various elements (C_{1s} , F_{1s} , O_{1s} , Si_{2p}) was measured at three positions on the via sidewall (top, middle and bottom). The results are shown in figure 10.

In all measured samples, the amount of F remains very low and decreases from the top (6–8 at%) to the bottom (3–4 at%) of the via (see figure 10(a)). The same trend can

Figure 10. XPS measurement results: (a) F_{1s}; (b) Si_{2p} at three different positions (top, middle and bottom) on the wall of 100 μm vias etched with the 15 W, 60 sccm recipe for three different temperatures: 0, 10 and 25 $^{\circ}\text{C}$.

also be found for the concentration of oxifluoridic silicon (see figure 10(b)). These observations indicate that the passivation layer is slightly thicker at the top than at the bottom, which is consistent with our expectation. However, the oxifluoridic silicon concentration is approximately the same in all the samples, indicating that the passivation layer thickness is more or less equal for all temperatures used and is in the order of ~ 2 nm. Therefore, we can conclude that the main component of the passivation layer is SiO_x, which is hardly sensitive to the temperature. Moreover, it suggests that the etching mechanism itself, rather than the passivation layer formation, is thermally activated.

As a conclusion, substrate temperature turns out to be a key parameter in the range from -10 to 30 $^{\circ}\text{C}$, especially for improving the via wall roughness and via profile. The main disadvantage of increasing the substrate temperature is the larger undercut formed in the process, which however remains controllable and small enough for most of the envisioned applications.

4. Conclusions

The O₂/(SF₆+O₂) ratio is found to be the most important parameter for the sidewall tapering and the undercut formation. It is also responsible for the sidewall roughness and the spike formation, especially when the ratio is high. Increasing the temperature can alleviate these problems, but it introduces much larger undercut. The platen bias and the pressure determine the energy of the incident ions, so both parameters are effective to tune the anisotropic characteristic of the via. As a final result, tapered vias with an aspect ratio of ~ 5 suitable for 3D interconnections and MEMS packaging have been obtained by properly balancing the etching regimes. A global dependence trend of all relevant via profile characteristics on the etching parameters is listed in table 2. This can be particularly useful for further developments and to reproduce these results with other DRIE tools and process approaches. In conclusion, conventional continuous etching with an ICP tool, at room temperature, is a promising and low-cost method to

Table 2. The trends of various profile parameters with increasing process parameters.

	Undercut	Etch rate	Slope	Bowing	Roughness
O ₂ flow	—	~	++	—	++
Platen bias	++	++	—	+	—
Pressure	+	~	—	—	+
Temperature	++	~	~	++	—

++: increase,
 —: decrease,
 +: slight increase,
 ~: almost constant.

fabricate tapered vias for 3D interconnections and/or MEMS packaging.

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