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Built-in Current Sensor for ΔI_{DDQ} Testing of Deep Submicron Digital CMOS ICs

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Abstract

This paper presents the implementation of a built-in current sensor that includes two recently reported new techniques for I_{DDQ} testing to take into account the increased background current of defect-free circuits and its increased variance due to process variations. These techniques are the correlation between speed and I_{DDQ} , and the ΔI_{DDQ} testing technique. The monitor has been manufactured in a 0.18 μ m CMOS technology and it is based on the principle of disconnecting the device under test from the power supply during the testing phase. The monitor has a resolution of 1 μ A for a background current less than 100 μ A or 1% of background currents over 100 μ A to a total of 1mA full-scale. The sensor operates at a maximum clock speed of 250MHz. The monitor has been verified in a test chip consisting of one "DSP like" circuit of about 250,000 transistors. Experimental results prove the usefulness of our approach as a quick and effective means for detecting defects.

1. Introduction

In spite of its usefulness, I_{DDQ} testing is troubled by the fact that the gap between the defective and the defect-free I_{DDQ} current is narrower due to the increasing background current and the increasing of its variance [5][6][15]. To deal with this problem, techniques such as reverse body biasing, low temperature, multi-threshold circuits, or disconnect the idle circuits, have been proposed [1][7].

On the other hand, new techniques such as clustering [8], neighbourhood [9], current ratios [10], Delta- I_{DDQ} [11][12] or exploiting the correlation between the circuit speed and current [5][6], have been used to minimize the impact of variability on the I_{DDQ} measurements and to improve defect detectability. Two features can be highlighted from these solutions:

- **Differential measurements.** The general approach consists of performing some type of *comparison* between two or more measurements and, depending upon the outcome of this comparison, to decide if the circuit is defective or not. All these methods use some type of *differential* measurements and the decision is taken after more than a single measurement is made.
- **Complexity.** It is assumed that the testing system is able to remember the measurements in a previous time or location, (or of a different parameter) than the performed in the present time or location (or parameter). Using a digital analogy, these new methods are "*sequential*" instead of the "old" "*combinational*" method based on a single PASS/FAIL threshold. Thus, they assume the existence of a *memory* and

a *processing unit* in the testing system to execute the algorithms of such methods.

In recent years several built-in current sensors (BICS) have been proposed, e.g. a sensor with a magnetic device [16], a sensor based on a voltage voltage at the power lines [13], sensors using current mirrors [17] or bypass transistors [2][3]. Off chip solutions are also available and many companies offer off-chip I_{DDQ} monitors included in their ATEs.

The following general conclusions can be extracted from the analysis of these sensors:

- Presently, non-invasive BICS solutions using magnetic sensors or voltage drops in the power wires are inherently low in robustness due to the extremely small signal provided for these sensors, noise and process variations. Of course, this situation can change in the future if more sensitive magnetic sensors are developed. For BICS, at this moment, a realistic point of view is to accept some degree of disturbance in the circuit power distribution due to a device in series with the power line, and to define a bound in the performance loss due to this disturbance.
- BICS are much more faster than off-chip sensors. It is thus more interesting to develop monolithic BICS to save test time, especially if complex I_{DDQ} algorithms need to be executed.
- The proposed implementations do not solve the new needs in I_{DDQ} testing. None of the BICS deal with the I_{DDQ} variance although a sensor that takes into account the increasing in background current was reported [18]. Most of the designs follow the "old" style: compare the measured I_{DDQ} against a fixed single threshold to generate a PASS/FAIL signal, and that's all. No implementation of the new techniques to improve I_{DDQ} testing exists. For the off-chip solution, the intrinsic programmability of the ATE makes relatively easy to implement complex algorithms as current ratios or ΔI_{DDQ} but at the expense of an additional reduction in speed.
- Only one BICS has been implemented in an industrial chip [4], and only a few BICS have been manufactured in test chips, the remaining implementations are checked by simulation. This fact is explained by the manufacturer scepticism about the behaviour of the proposed BICS in an industrial real environment. At the same time, this fact also reveals the great difficulties to satisfy the required features in the design of such sensors.

In this paper we present a new BICS for *delta* I_{DDQ} testing. The approach follows closely the conclusions drawn in this introduction to get a fast and reliable sensor that is able to detect defects that produce small increments in I_{DDQ} current. The paper is organized as follows: next section describes the proposed sensor, Section 3 describes its circuit implementation, Section 4

summarizes the experimental results, and Section 5 presents the conclusions.

2. Built-in current sensor for ΔI_{DDQ} testing

The main characteristics and specifications of such sensor are shown in Table 1 and will be described in more detail in the next subsections.

Table 1: **Summary of characteristics and specifications of the proposed built-in ΔI_{DDQ} monitor.**

Characteristics	Benefits
Combines multiple-parameter testing and ΔI_{DDQ} testing in one monitor	Suppress the high background current and decreases the I_{DDQ} variance
Based in the Keating-Meyer approach	Robust and fast if on-chip
Differential determination of PASS/FAIL	Robust despite of mismatches
Takes into account process variations	Self-adjust
Specifications	
Range of measurement	1 μA to 1 mA
Resolution	1 μA ($I_{DDQ} < 100 \mu\text{A}$) or 1% of the full range ($I_{DDQ} > 100 \mu\text{A}$)
Speed	Depends on CUT. Max. 2.5 Mvectors/s @ 0.18 μm technology test chip with maximum I_{DDQ}
Area overhead	<1% @ 0.18 μm technology
Loss of performance	Depends on switch size. <5 % in the test chip.

The proposed scheme combines the multiple-parameter current testing [6] and the ΔI_{DDQ} testing [11] approaches to obtain a current sensor able to detect defective currents, which are a small percentage of the background current. Our scheme uses a version of the Keating-Meyer approach for I_{DDQ} testing [2]. It includes an on-chip switch connected between the V_{DD} pin and the CUT. As this switch is integrated in the circuit, a faster sensor operation is possible because of the reduction of the circuit's loading capacitance C . Our scheme detects defective circuits by analyzing the differences between measurements of current consumption instead of using the absolute value of such measurements. For this reason it is not sensitive, in a first order analysis, to the variability of sensor parameters. Nevertheless, the proposed scheme takes into account the process variability by adjusting its range of measurement and its PASS/FAIL limit according to the impact of the manufacturing process on the circuit's maximum frequency.

Figure 1. **Sensor operation.**

Important subjects to test the feasibility of the proposed sensor are the sensor resolution and speed as well as the maximum size

of the CUT where the sensor is connected, and, as a consequence, the area overhead. Figure 1 summarizes the sensor's operation and helps to oversee the parameters involved in such subjects. Further, Figure 1 shows two curves corresponding to low and high leakage scenarios. After applying an input pattern to the CUT and after opening the switch, the supply pin voltage decreases until it reaches the reference voltage V_{REF} . The expression associated with this discharge is

$$I_{DDQ} = C \frac{\Delta V}{\Delta t} \quad (1)$$

where $\Delta V = V_{DD} - V_{REF}$, and C is the total circuit's capacitance including decaps. The time, Δt , that takes the decaying voltage to reach V_{REF} is measured by a counter, C1, as m periods of the clock frequency T_{CK} . By replacing Δt by $m \times T_{CK}$, we obtain the following expression:

$$m = \left(\frac{C}{I_{DDQ}} \right) \times \Delta V \times F_{CK} \quad (2)$$

That is, the number m of C1 counts is inversely proportional to I_{DDQ} and directly proportional to C , ΔV and F_{CK} . We use this formula as well as technology data to estimate the sensor resolution and speed. We define the resolution as the minimum amount of current that the sensor can distinguish. For a resolution of 1 μA for $I_{DDQ} < 100 \mu\text{A}$, or 1 % of full scale (10 μA), m has to be equal or greater than 100. As ΔV and F_{CK} are defined before testing, the only parameter that is not controlled is the fraction C/I_{DDQ} that depends on the technology and on the CUT itself. Notice that because of process variability C/I_{DDQ} fluctuates as well. Thus, for fixed ΔV and F_{CK} , and to ensure a 1% accuracy, the sensor has to be connected to a CUT with a value of C/I_{DDQ} well above a given threshold to reach the desired resolution. This figure of merit is easily achieved in present and future technologies.

The sensor speed is defined as the number of input patterns that can be applied to the CUT in a unit of time. The sensor works at its maximum speed when it works just with the prescribed resolution (that is when $m = 100$) at the maximum F_{CK} possible. The corresponding speed expression is

$$\text{speed [vectors/s]} = \frac{F_{CK}}{m} = \frac{1}{\frac{C}{I_{DDQ}} \times \Delta V} \quad (3)$$

For fixed ΔV and F_{CK} , the maximum speed is proportional to I_{DDQ} . The technology, the process corner and the temperature determine the size of the CUT checked by one sensor. Using a 1% resolution criterion, $I_{DDQ_{max}} = 1\text{mA}$, the off-state current (I_{OFF}) of the transistors and other parameters extracted from the SIA Roadmap [15], it is possible to calculate the circuit size for 180nm and 130nm for FAST, NOMINAL and SLOW process corners. For the worst case (FAST corner) the sensor is able to manage circuits with about $0.6 \cdot 10^6$ transistors (130nm) or $0.9 \cdot 10^6$ transistors (180nm). For circuits with greater size, thus consuming an I_{DDQ} higher than 1 mA, there are two possibilities: the first is to keep the same **relative** resolution at the cost of less **absolute** resolution. For instance, in a 180 nm circuit with $9 \cdot 10^6$ transistors

and $I_{DDQ_{max}} = 10$ mA, the relative resolution is 1 %, or 100 μ A of absolute resolution. The second possibility is to partition the CUT, adding one sensor to each partition. This solution preserves both, the relative and the absolute resolution. For example, a circuit with $9 \cdot 10^6$ transistors and $I_{DDQ_{max}} = 10$ mA needs 10 sensors in a 180nm technology node.

3. Circuit implementation

The proposed scheme has three blocks: the I_{DDQ} measurement block (MEAS), the control block (CTRL), and the ΔI_{DDQ} block (DELTA) which executes two testing algorithms, see Figure 2. The MEAS block converts a voltage drop proportional to the quiescent current into a digital word that is n bits long. It includes a switch to disconnect the device under test from the power supply during the testing phase. The DELTA block captures this word and applies the ΔI_{DDQ} algorithms to obtain a PASS/FAIL signal. The CTRL block extracts information of the CUT's actual silicon speed and uses it to define the time base needed by the MEAS block and the threshold level that the DELTA block needs to distinguish between defective and defect-free circuits.

Essentially, our ΔI_{DDQ} built-in current monitor comprises a counter which counts clock pulses during a time interval to obtain a counted number of clock pulses (MEAS block). The count period has a start determined by the start of the testing cycle which occurs at the instant the switch disconnects the power supply from the device under test. The node connected to the CUT is a "virtual" power supply node (VVDD). The voltage at this virtual node starts decaying due to the quiescent current that discharges the CUT's capacitance that is intrinsically present at the terminal.

The count period may start at the start of the testing cycle, or a predetermined delay time after the start of the testing cycle. The end of the count period is determined through a comparator that detects that the voltage at the input crosses a reference value. Unlike conventional approaches, we determine the quiescent current by counting the number of clock pulses which occur until the voltage at the virtual node drops below a reference voltage value.

Figure 2. Detailed implementation of ΔI_{DDQ} monitor showing delta block diagrams for both "max-min and "successive" implementations.

Basically, at the end of the count period, the count value of the counter is inversely proportional to the CUT's I_{DDQ} as shown in equation (2), if the capacitance of the CUT and the I_{DDQ} are assumed constant, which is an acceptable assumption in the range

of supply voltages in which the test is performed. A post-processing unit (DELTA block) processes the counted number and the outcome is compared with a reference number to determine whether a defect exists in the device under test. To improve the defect detection accuracy, a control circuit (CTRL block) controls the value of the reference number and the frequency of the counter clock signal in dependence on the particular process parameters of the circuit under test.

3.1. MEAS Block

The I_{DDQ} measurement block works as follows: assume that the CUT (which is symbolized in Figure 2 by the current source I_{DDQ} and the capacitance C) is in the quiescent state, then the switch is opened and the voltage in the virtual VDD node starts to decrease due to discharge of C . As long as this voltage is greater than a reference, the comparator enables counter C1, which counts the number of clock periods (the time) this voltage takes to reach V_{REF} . When the virtual VDD voltage reaches the reference voltage, counter C1 stops counting. At this moment, the output of C1 stores a value (coded in n bits) which is inversely proportional to I_{DDQ} . To prevent malfunctioning of the switch or comparator an overflow signal limits the maximum time that counter C1 is enabled.

The switch is basically a PMOS transistor that is connected between the power supply pin (VDD) and the CUT power ring (VVDD). This switch is actually not an integral part of the sensor design because it needs to be tailored specifically for each distinct CUT. In our test chip the switch channel resistance is 0.848 Ω . The monitor supply voltage is taken before the switch, thus being constant.

An analog comparator is used to compare the decaying VVDD voltage and the voltage reference V_{REF} . Variations in resolution, delay and offset voltage can be managed because a die-to-die variation in these parameters is not critical as long as it affects each measurement in the same manner. The comparator uses additional circuitry to compensate offset voltage. The ranges in temperature and supply voltage are -40 to 85 C and 1.6 to 2 V. In our 0.18 μ m test chip, the difference between V_{DD} (nominal value is 1.8 V) and V_{REF} is 300 mV which is small enough to guarantee that the CUT state does not change during the measurement process.

3.2. CTRL Block

As is known, the I_{DDQ} of a defect-free circuit may change by orders of magnitude due to process variations. Therefore, the clock frequency of counter C1 has not only to be very high to obtain enough precision in the measurement of high I_{DDQ} currents, but also n has to be large to measure the long time counted by C1 when I_{DDQ} is small. To handle these requirements, the CTRL block is divided into two subblocks (see Figure 2): the first, which is composed of a ring oscillator, the counter C2 and the blocks Freq. Scaler and Reg. AUX, improves the resolution of the I_{DDQ} measurement by adapting the clock frequency of C1 to the manufacturing process point in which the chip is fabricated. The proposed scheme takes advantage of the correlation between I_{DDQ} and chip speed [5] to reduce the expected range of I_{DDQ} variability that the sensor needs to take into account. Basically there is an quasi-exponential relationship between speed and leakage. Thus, a

measurement of the circuit speed is performed before the I_{DDQ} measurement starts, and this information is used to set the clock frequency of the counter C1 to a proper value. This solution reduces the size of counter C1 to obtain the required precision. The ring oscillator's frequency is measured in terms of the number of counts that counter C2 reaches in a known period of time. This number of counts is introduced in the Frequency scaler block, which selects the proper clock frequency for C1. The speed information is also used to set register AUX which stores the limit of the maximum ΔI_{DDQ} allowed for this CUT. The other subblock inside the **CTRL** block is labeled CONTROL. It supplies the control signals to the counters and registers of the sensor from an external clock (CK) and a Test signal to enable it.

3.3. DELTA Block

According to the previous description, we have for each test pattern a word that is n bits long, which conveys the measured I_{DDQ} for this pattern. If M test patterns are applied to the CUT, the test results are stored in a vector of M words of n bits. The **DELTA** block is a built-in implementation of the ΔI_{DDQ} technique that digitally processes this information. Two ΔI_{DDQ} algorithms have been implemented in the sensor: the *max-min* algorithm and the *successive* algorithm. The relative benefits of these approaches are analysed elsewhere [7] [14]. The (*max-min*) algorithm detects defective circuits by analyzing if the difference between the maximum and the minimum I_{DDQ} of the CUT is greater than a given threshold. It works as follows: First, the contents of registers Rmax and Rmin are initialized to 00...00 and 11...11, respectively. After each measurement, the contents of counter C1 is stored in register R. Then, this value is compared to the content of registers Rmax and Rmin. If $R > R_{max}$, the contents of R is stored in Rmax and if $R < R_{min}$, R is stored in Rmin. The difference $R_{max} - R_{min}$ is performed synchronously, and this result is compared to the threshold stored in AUX, thus supplying a PASS/FAIL signal. The second algorithm presented in Figure 2 is based on the calculation of the difference between successive test patterns (*successive*). It uses a register R to store the value of C1 in the previous test pattern, a circuit to calculate the absolute value of the difference between the contents of C1 and R, and a digital comparator that compares this difference to a threshold stored in AUX. The output of this comparator is a PASS/FAIL signal. The result of each ΔI_{DDQ} algorithm is presented at the internal signals *pnf_successive* and *pnf_maxmin*. One of them is selected to drive the output pin *passnfail*. The selection is made by a flip-flop, which is loaded during the initialization phase.

4. Experimental results

This section presents results obtained from measuring 24 samples of the ΔI_{DDQ} built-in sensor. Figure 3 shows a microphotograph of the monitor (0.09mm^2) along with the DSP-like core (0.8mm^2) used for testing. The area overhead in the test chip is about 10 %. However, the monitor is able to manage circuit at least 4 or 5 times greater, thus reducing considerable the overhead. We did not actually find any real defects from the test chips received. Also, the background current of the core was around $3\mu\text{A}$. Thus, to fully explore the capabilities of the sensor,

we artificially introduced defects and elevated the background current as well.

Figure 3. Die photo.

Figure 4 shows how did we test the sensor. R_{DEF} is a resistor used to introduce our artificial defect and R_{BACK} is the resistor used to vary the background current. C_{DDExt} is a decoupling capacitance needed when the background current is artificially increased by means of R_{BACK} . Further, Figure 4 shows a block diagram of the ΔI_{DDQ} sensor and the name of the main signals. Signal **test** starts the sensor operation, signal **test2** opens and closes the switch and signal **ck_tester** is the external clock signal supplied by the ATE. Signal **vvdd** is connected to the internal DSP power ring. There is no external load connected to this pin (except eventually an oscilloscope probe). The current source I_{DDQ} models the DSP quiescent current. Signal **tq1** is one of the DSP outputs. Thus a small “defective” current is produced only for the test vectors that make signal **tq1** at zero.

Figure 4. ΔI_{DDQ} monitor with circuit under test showing additional circuitry for simulating a large background current and defects

4.1. Analog comparator

By controlling signal **test2**, we can independently test the analog comparator by reading the time (proportional to the number of counts stored in register R) that signal **vvdd** needs to reach the **vref** voltage. The behavior of comparator is shown in Figure 5 for chip #1 for no load conditions in the **vvdd** signal.

As can be seen Δt changes when **VREF** changes, and the slope of the line is constant (except for noise measurement). This slope is

$\Delta t/\Delta V$, that is to say, C_{DD}/I_{DDQ} . All ΔI_{DDQ} measurements have been performed at $\Delta V = 0.3$ V.

Figure 5. Linearity of comparator

4.2. ΔI_{DDQ} measurements

To make clearer the meaning of the results described in this section we use Figure 6 as a reference. It shows the waveforms of the different signals as they are observed in an oscilloscope. The whole ΔI_{DDQ} test remains "inside" the **test** pulse, and each **test2** pulse corresponds to the ΔI_{DDQ} test for one DSP vector. The period while **test2** is at zero corresponds to the period of time the tester loads a new DSP vector. Signal **passnfail** is the error flag. It is normally at one and its activation is different depending on the ΔI_{DDQ} test performed. In ΔI_{DDQ} *successive*, there is a first pulse that corresponds to the difference between the initial value in register R (zero) and the first ΔI_{DDQ} measurement. As this difference is greater than the threshold defined, **passnfail** is activated. However, in a good chip this is the only activation of **passnfail**. If a second activation is produced (dashed line pulse in the figure) means that a defect is detected.

Figure 6. Functional behavior of ΔI_{DDQ} monitor

In ΔI_{DDQ} *max-min* mode, **passnfail** remains always at one if no defect is detected, and if it is activated for any measurement, it remains activated until the end of the whole ΔI_{DDQ} test. The following figures are real waveforms captured on a TDS440 digital oscilloscope when a test is executed with 16 DSP test vectors. Figure 7(left) shows the *successive* ΔI_{DDQ} test detecting four

ΔI_{DDQ} measurements above the threshold. Figure 7 (right) shows a *max-min* ΔI_{DDQ} test detecting a defect in the 9th DSP test vector.

Figure 7. Fault detection with successive and max-min algorithms.

4.3. Checking the sensor resolution and robustness

The capability to distinguish small defective currents on top of a high background current was measured to check the resolution and robustness of the sensor. The results were obtained as follows: forty measurements were made in a single chip with and without defect, and the histogram of such measurements was made. Results for three values of R_{DEF} (background current is about 49 μ A and defective current are 0.8 μ A and 1.6 μ A) are shown in Figure 8. As can be seen, defect-free and defective distributions are separated and the defective circuits can be properly distinguished from the defect-free ones.

To evaluate false detects, we measured the noise threshold plus the variations on I_{DDQ} vector to vector. The procedure is as follows. We know that the minimum defect current that can be detected is around 0.8 μ A, and that exactly four detects are flagged by the ΔI_{DDQ} -successive test. Then, to measure the noise threshold we lower the threshold stored in register AUX until we have more than four detects. Likewise, we raise the contents of register AUX until we have less than four detects. These are the lower and upper bounds of false detects.

Figure 9 shows the combined results. One can see that there is a wide margin between the erroneous and correct detection of the defect for all chips. Notice the logarithmic scale in the Y axis.

Figure 8. Histogram with three values of R_{DEF} .

5. Conclusions

Defect-free digital ICs of actual and future technologies have an increase in both, the absolute value and the variability of their quiescent current. Thus, the extra I_{DDQ} current due to a defect is a small percentage of the total current. As a consequence, the single PASS/FAIL current threshold approach to distinguish defective circuits is not feasible. Several solutions have been proposed to reduce the absolute value and variability of the I_{DDQ} current, thus lengthening the usefulness of the I_{DDQ} testing. All of them propose complex computations to distinguish defective circuits. To be useful and practical, sensors for current testing have to implement one or more of the previous solutions. Off-chip sensors can be more accurate than the on-chip ones, however they are inherently slower. Since the test speed is an important issue, an on-chip solution is more appropriate. We presented a built-in current sensor in a 0.18 μ m CMOS technology that correlates speed and I_{DDQ} for self calibration due to process variations. The sensor implements two ΔI_{DDQ} test algorithms, has a maximum speed of 2.5Mvectors/s at maximum I_{DDQ} = 1mA, and a resolution of 1 μ A/1% of full scale (max. 1 mA). The sensor is robust, fast, and presents a plausible solution for a built-in current sensor in present and future technologies.

Figure 9. Monitor's sensitivity to false detects.

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