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All-Optical Label Swapping of Scalable In-Band Address Labels and 160-Gb/s Data Packets

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Abstract—Scalability and photonic integration of packet switched cross-connect nodes that utilize all-optical signal processing is a crucial issue that eventually determines the future role of photonic signal processing in optical networks. We present a 1×4 all-optical packet switch based on label swapping technique that utilizes a scalable and asynchronous label processor and label rewriter. By combining N in-band labels at different wavelengths (within the bandwidth of the payload), up to 2^N possible addresses can be encoded. The proposed label processor requires only N active devices to process the 2^N addresses that makes this label processing technique scalable with the number of addresses. Experimental results showed error-free packet switching operation at 160 Gb/s. The label erasing and new label insertion operation introduces only 0.5 dB of power penalty. These results indicate a potential utilization of the presented technique in a multi-hop packet switched network.

Index Terms—Label processor, label rewriter, label swapping, optical packet switching, optical signal processing, semiconductor optical amplifier (SOA), wavelength converter.

I. INTRODUCTION

THE increase of the traffic in the access networks makes it likely that future all-optical metro and core networks should be capable to handle tens of Tb/s data traffic. Current networks are based on electronic circuit switching technology in combination with wavelength division multiplexing (WDM) technology. Despite the flexibility of the electronics for processing the packet addresses, a typical electronic circuit switch requires to implement electrical clock recovery, electrical de-multiplexing to scale down the line rate of the optical packets (typically >10 Gb/s) to a data rate compatible with the electronic speed (<622 Mb/s) for processing the labels, multiplexing the packets and switching the packets to the proper output port. With the increase of the data rate of the optical packet (above 40–100 Gb/s) and of the number of WDM channels to meet the capacity demand, electronic circuit switching may have fundamental limits due to the scalability of multi-racks electronic switching fabrics, and power consumption and dissipation required by the optoelectronic conversions [1], [2].

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All-optical packet switching has been proposed as a technology to solve the bottleneck between the fibre bandwidth and the electronic router capacity by exploiting high speed and parallel operation of all-optical signal processing. Moreover, photonic integration of the optical packet switch potentially allows a reduction of volume, power consumption and costs.

In all-optical packet switches the optical packets are routed based on the address information that is encoded by the attached labels. The optical packet is stored (delayed) in the optical domain for the time required to the label processor to process the address and provide a routing signal for routing all-optically the stored packet.

To exploit the benefit of photonic technology to miniaturize and decrease the power consumptions of the system, photonic integration of the all-optical packet switch depends on the capability to integrate the label processor and the optical delay related to the latency of the label processor. This imposes stringent constraints on the latency time of the label processor. Indeed, integrated delay lines using an InP photonic waveguides have around 2 dB/cm of optical losses. One centimeter of waveguide provides a delay of 100 ps. If the latency of the label processor is in the order of 1 nanosecond, integration of such delay exhibits a total waveguide loss of 20 dB, which is impractical. Therefore, high speed operation of the label processor (<100 ps) is a must to allow photonic integration of the packet switch system. Moreover, scalability of the label processor with the number of labels (or the number of label bits) is crucial too. Indeed, the number of active components that can be integrated in the label processor is limited by the thermal crosstalk and heat dissipation which can prevent photonic integration of the circuit. A method that has been introduced to minimize the number of active components in the label processor architecture is the all-optical label swapping (AOLS) [2]. In AOLS, only a few labels for routing the optical packet have to be processed at each node, thus leading to a considerable simplification of the label processor architecture.

Several solutions were presented to implement an all-optical packet switch node. In [1]–[5], the addresses were processed in the electrical domain while the payload is stored in the optical domain. The electrical label processing drives the optical switches for routing the optical packets. However, electronic label processing and new label rewriting requires no trivial optoelectronic per-packet based clock recovery, and introduces long processing latency in the order of tens of nanoseconds which prevents the integration of the system. All-optical packet switch employing all-optical label processor were investigated in [6]–[12]. Mainly these works employed optical correlators, which recognize the labels, and set/reset optical flip-flops to

store the information for the duration of the packet. However, as the number of addresses, of the WDM channels carried by each fiber, and of the packet data rate increase, photonic integration, high speed operation, low latency, and scalability of the label processor remain key-issues to be solved. Solutions employing 2^N optical correlators and 2^N optical flip-flop to process the addresses may prevent photonic integration.

Our research focuses on the realization of an all-optical packet switching system that is scalable and suitable for photonic integration. Recently, we have presented a 1×4 all-optical packet switch [13]. We used in-band labels as scalable labeling technique. We encode the addresses by combining the N in-band label wavelengths, therefore 2^N possible addresses can be encoded within a limited bandwidth. We introduced a scalable label processor that is able to process the 2^N addresses in parallel by means of only N optical switches. The capability to process in parallel N bits (2^N addresses) allows the realization of a large optical packet switched cross-connect out of $1 \times N$ optical packet switch. This will hugely reduce the amount of active components. Moreover, the label processor operates in asynchronous fashion, does not require optical flip-flops, and can handle packets with variable lengths.

In this work we present a 1×4 all-optical packet switch based on label swapping technique. In AOLS the old label, processed by the label processor, provides the local routing information, while the new label, generated by the label rewriter, is attached to the routed packet and determines the routing of the packet at the next node. We present a label processor for processing in-band labeling addresses and an all-optical label rewriting function that provides a new address according to the old one. The label processor and label rewriter processes ‘on the fly’ the optical labels, which results in low processing latency of few tens of picoseconds. Moreover, we investigate the cascability of the all-optical label erasing/rewriting function of the packet switch in two-cascaded nodes configuration.

This paper is organized as follows. In Section II, we present the all-optical packet switch architecture, introducing the main all-optical functions required to accomplish the AOLS. In Sections III and IV, we demonstrate the label processor and label rewriter functions, respectively. Finally, we summarize and discuss the main results in the conclusions section.

II. ALL-OPTICAL PACKET SWITCH ARCHITECTURE

Fig. 1 illustrates the all-optical packet switch based on label swapping technique. The input packet format is also reported in Fig. 1. The input packets consist of a 160-Gb/s payload, with a pulse duration of 1.6 ps making the 20-dB bandwidth of the payload to be 5 nm. The packet address information is encoded by in-band labels. With this we mean that the wavelengths of the labels are chosen within the bandwidth of the payload. We encode addresses by combining different labels. Each label is OOK encoded and has a binary value: the label value is ‘1’ if the label is attached to the payload, the label value is ‘0’ if no label is attached to the payload. Thus, by using N in-band label wavelengths, 2^N possible addresses can be encoded, which makes this labelling technique highly scalable within a limited bandwidth. Note that, by using filters with bandwidth narrower than

Fig. 1. All-optical packet switch configuration. At the bottom, the packet format represented in the time and spectral domain.

0.1 nm, more than ten labels can be allocated in the payload bandwidth, which means 2^{10} encoded addresses. Moreover, if the payload data rate increases above 160 Gb/s (i.e., 320 or 640 Gb/s), a larger number of labels can be allocated in the payload spectrum. Thus, the proposed labeling technique scales well with the packet data rate. Other advantages of the in-band labeling are that the labels can be extracted by passive wavelength filtering. Moreover, by using a label that has the same time-duration as the payload makes the use of optical flip-flops redundant, and allows to handle packets with variable lengths in an asynchronous fashion. In the experiment, we encode four addresses by using two in-band labels. Fig. 1 shows packets carrying different addresses and the corresponding representation in the spectral domain.

The all-optical packet switch is based on label swapping technique. In the label swapping technique, the input labels have only a local meaning. The input labels are used to provide the packet’s routing information. New labels should be generated and attached to the packet payload before that the packet outputs the switch. To perform the label swapping and routing of the packet, we utilize four all-optical functions as shown in Fig. 1: label extraction/erasing, label processing, label rewriting, and wavelength conversion. The packet address encoded by the in-band labels is extracted/separated from the data payload by the label extractor/eraser. The data payload is optically delayed for the time required to the label process to provide a routing signal, before being fed into the wavelength converter. The labels are all-optical processed by the label processor and label rewriter. The information carried by the input labels is used for self-routing of the optical packet. An example of self-routing table for addresses composed by two labels is reported in Fig. 2. Note that the routing table in Fig. 2 was adopted in the label swapping experiment in Section IV. Different routing table has been used in the label processor experiment in Section III. For

Old Label	'0 0'	'0 1'	'1 0'	'1 1'
Routing Signal	1547.7 nm	1560.6 nm	1538.2 nm	1542.9 nm
New Label	'1 1' 1546.1 nm 1549.3 nm	'1 0' 1558.9 nm	'0 0'	'0 1' 1544.5 nm
Optical spectral				

Fig. 2. Self-routing table employed in the label swapping experiments.

each input labels combination, a routing signal at distinct wavelength and a new combination of labels should be provided by the label processor and the label rewriter, respectively. The self-routing table reported in Fig. 2 is one of the possible mappings. The mapping between the input label, the routing signal and the new label is assigned once and is not dynamic. This means that, once the mapping has been assigned, the value of the old labels determines one output port (by setting the routing signal) and one new address.

Fig. 2 reports also the corresponding optical spectra of the routing signal and new labels for different input labels combination. Note that the wavelengths of the new labels should be within the 5 nm band of the payload. Thus, the label processor provides a routing signal according to the input labels. The routing signal at a unique wavelength has a time duration equal to the packet time. The wavelength of the routing signal represents the central wavelength at which the 160 Gb/s data payload will be converted by means of wavelength conversion. Simultaneously, the label rewriter provides the new labels, which have a time duration equal to the packet duration. Moreover, the wavelengths of the new labels are selected so that they are in-band with the bandwidth of the converted payload (as shown in Fig. 2). The new labels are attached to the wavelength converted payload (see Fig. 1). The packet with the new labels is routed by means of an AWG to distinct output ports of the packet switch, according to the central wavelength of the converted payload.

It is worth noting that, since the label processor and label rewriter operate “on the fly,” the time delay required to store the payload is very short. This may allow photonic integration of the whole packet switch system. Moreover, as the routing signal and the new labels produced by the label processor and label rewriter have a time duration equal to the packet time, the presented system can handle packets with variable length.

In the next sections we present the operation principle and experimental results of the label processor and the label rewriter. Scalability of these circuits with respect to the number of labels will be also discussed.

III. ALL-OPTICAL LABEL PROCESSOR

The schematic of the label processing system is illustrated in Fig. 3. The system consists of the label extractor/eraser and the label processor. The input optical packets have the same format

as the one discussed in the previous section. The input packet is firstly processed by the label extractor/eraser, which consists of (reflective) fiber Bragg gratings (FBG) centered at the labels wavelengths. While the labels are reflected by the FBGs, the packet payload can pass through the label extractor/eraser before to enter the wavelength converter. The continuous wave (CW) routing signal that is needed for wavelength conversion is provided by the label processor (see Fig. 1).

The optical power of the extracted labels is used to drive the label processor. The label processor receives also as input 2^N CW bias signals at different wavelengths $\lambda_1 \dots \lambda_{2^N}$. The wavelengths of the CW signals are chosen according to the self-routing table and represent the wavelengths at which the payload will be converted. The label processor consists of a cascaded of N pairs of periodic filter and optical switch. The periodic filter has one input and two outputs. The optical switch has two inputs and one output. The two outputs of the periodic filter have complementary wavelength transfer functions as shown in Fig. 3. Moreover, each of the N periodic filters has different period as also shown in Fig. 3. In particular the bandwidth (BW) of the i -th filter is equal to $BW_i = 2^{(i-1)} \times BW_{ch}$, with $i = 1, \dots, N$ and BW_{ch} , the bandwidth of the single CW signal. Each of the 1×2 periodic filter separates (in wavelength) half of the input CW-signal to output port 1 and the other half of the input CW signals at the output port 2. The 2×1 optical switch selects the CW signals of port 1 or port 2 based on the value of the label information. Therefore, the output of each pair of periodic filter and optical switch consists of half the number of CW signals. Thus, after the first stage, the 2^N CW signals becomes $2^N/2 = 2^{N-1}$. Therefore, after cascading N pairs in which each optical switch is driven by the corresponding label, a distinct CW signal is selected. This CW signal at distinct wavelength has a time duration equal to the packet time duration and represents the routing signal to which the payload will be converted. Note that the processing is performed entirely in the optical domain. By implementing the optical switches by means of very fast SOA-MZI devices, label processing with only tens of picoseconds of processing time can be possible. Moreover, as no synchronization is required in the scheme, and since the routing signal at the output of the label processor has the same duration as the packet payload, the system can handle packets with variable lengths.

The experimental set-up used to demonstrate the 1×4 all-optical packet switch employing two-labels address is shown in Fig. 4. Packet payload is generated by time-quadrupling a 40-Gb/s data-stream consisting of 1270 bytes of pre-defined return-to-zero bits at $\lambda_p = 1553.8$ nm up to 160-Gb/s data-stream using a passive fiber-based pulse interleaver. Each pulse has duration of 1.6 ps, making the 20-dB bandwidth of the payload to be 5 nm. The resulting packet payload consists of a 254 ns data burst. The packet-to-packet guard time is 2 ns, making the packet repetition rate 256 ns.

We encode addresses by combining using different wavelength labels. In the demonstration we used two labels that allow for encoding four addresses. The labels are at wavelengths $\lambda_{L1} = 1551.9$ nm and $\lambda_{L2} = 1552.5$ nm which are within the 20-dB bandwidth of the packet-payload. We processed four packets with two label bits with pattern “0 0,” “0 1,” “1 0,” and

Fig. 3. Schematic of the label processor. Details of the optical period filters employed in the device are shown at the bottom.

Fig. 4. Experimental setup employed to demonstrate the all-optical packet switch based on the label processor.

Fig. 5. Optical spectra of the packet recorded at (a) before the label extractor/eraser. Details of the FBGs filters employed to extract the labels are also visible in the picture. (b) Optical spectrum after the label extractor/eraser.

“1 1” to cover all possible combinations. The label extractor consists of two fiber (reflective) Bragg gratings (FBG) with a 3-dB bandwidth of 0.12 and 0.432 nm centered at λ_{L1} and λ_{L2} , respectively. The 20-dB bandwidths of the FBGs were of 0.8 nm and the insertion losses were 0.7 dB. The filter profiles and the optical spectrum of the packet are shown in Fig. 5(a). The filtered 160 Gb/s payload in Fig. 5(b). The label bits extracted by the FBGs are shown in Fig. 6(a) and (b). The two labels are fed in the label processor with an optical power of 1.5 dBm for label 1 and 0.3 dBm for label 2, respectively. The label processor is made of two cascaded SOA Mach-Zehnder In-

terferometers (SOA-MZIs), which act as wavelength selective switches that are optically controlled by the extracted labels. Continuous wave (CW) bias signals at wavelength λ_1 and λ_2 and wavelength λ_3 and λ_4 are fed into port 1 and port 2 of SOA-MZI1, respectively. The optical power of each input CW signals at the SOA-MZI1 was -2.5 dBm. The bias current of SOA-MZI1 was 204 mA and 216 mA for SOA1 and SOA2, respectively. In this configuration, if the value of label1 is “0,” the SOA-MZI1 is in bar-state and then the pair of signals (λ_1, λ_2) appears at the SOA-MZI1 output. However, if the label1 is “1,” the SOA-MZI1 is set in cross-state and thus

Fig. 6. Measured traces. (a), (b) Extracted labels. (c)–(f) Output traces of the label processor.

the signals (λ_3, λ_4) are switched at the SOA-MZI1 output. The dynamic extinction ratio was higher than 16 dB, and the efficiency was -2 dB. The measured OSNR at the SOA-MZI1 output was 37 dB. The insertion loss was 6 dB and the isolation between channels greater than 25 dB. An array-waveguide grating (AWG) and the 2×1 couplers are used as periodic filter to separate the pair of CW-signals (λ_1, λ_2) or (λ_3, λ_4) and coupled them into the input port1 (λ_2 or λ_4) and port 2 (λ_1 or λ_3) of SOA-MZI2, respectively. The SOA1 and SOA2 of the second MZI-SOA2 were driven by 259 mA and 282 mA of current, respectively. Thus, according to the value of label2, the SOA-MZI2 is set in bar or cross-state, selecting only one signal at distinct wavelength, which represents the routing signal to which the payload will be converted. The dynamic extinction ratio was 13 dB. The measured OSNR at the SOA-MZI2 output was 32 dB. The output power per channel (measured by using the OSA) after SOA-MZI2 was 0.2 dBm, which results in an amplification of 5 dB and thus losses compensation of the periodic demultiplexer. The output of SOA-MZI2 is coupled with the 160 Gb/s payload in the wavelength converter based on ultrafast chirp dynamics in a single SOA [14]. At the receiver side, the converted packets are demultiplexed by using an EAM to create a 5-ps switching window and then analysed.

Fig. 6(a) and (b) report the traces of the extracted label 1 and label 2, respectively. The measured extinction ratio was above 15 dB. Fig. 6(c)–(f) show the output of label processor. The output of the label processor for different old label combinations consists of a routing signal with time duration equal to the payload. Note that only for an address '00', the output trace shown in Fig. 6(d) presents also some pulses in correspondence of the packet guard-time. Those pulses, with a time duration equal to the packets' guard-time, are indeed generated during

Fig. 7. Measured traces after the wavelength conversion.

Fig. 8. Eye diagrams at different points of the system. (a) Input data payload. (b) Data payload after the label extractor/eraser. (c) After the wavelength conversion by using a CW signal. (d) After the wavelength conversion by using a routing signal provided by the label processor. Time scale is 2 ps/div.

the guard-time (which provides also a "00" combination). However, when the wavelength converted between the packet payload and the routing signal takes place, being those pulses in correspondence with the packet's guard-time and due to the non-inverting operation of the wavelength converter, those pulses will be suppressed. Fig. 7(a)–(d) shows the switched packets at different wavelengths for different label bits combination. For the visualization of the switched packets, we employed cross-gain modulation based wavelength converter and a tunable filter centered at each of the packet's wavelength routing in place of the AWG. Note that the pulses generating during the guard-time appear in Fig. 7(b) since the inverting operation of the wavelength conversion. Fig. 8(a)–(d) reports the eye diagrams in different point of the packet switch. Small degradation and broadening of the pulses is observed after the label extraction [Fig. 8(b)] with respect to the 160-Gb/s input payload pulses [Fig. 8(a)].

This is confirmed and quantified by the BER measurement reported in Fig. 9. The BER measurements were performed in static operation with noninverting wavelength conversion technique. The label extractor produces a penalty of less than 0.5 dB. After the wavelength converter, error-free operation was obtained with 5.5–7 dB of penalty compared to the input payload, and 1.5–3 dB of additional penalty if compared with the back-to-back 160 Gb/s wavelength converter payload. The extra penalty

Fig. 9. BER measurements at different points of the system.

can be ascribed to the pulse broadening after the label extractor which affects the wavelength converter performance and then produces cross-talk between adjacent time channels. This is also visible by comparing the eye diagrams in Fig. 8(c) and (d).

These results demonstrate error-free operation of 1×4 all-optical packet switch at 160-Gb/s data payload by all-optically processing two-labels address. The operation speed of the processor depends on the speed of the SOA-MZI. As the SOA-MZI in the switch configuration can operate up to 40 GHz, the latency introduced by the label processor is in the order of tens of picoseconds (including the few millimeters as the length of the device). Moreover, the SOA-MZIs and the AWGs are suitable for photonic integration. The label extractor/eraser may be implemented by using ring resonators with drop and pass through ports. Integration of the wavelength converter has been demonstrated in [15]. Therefore, the system can be potentially integrated in a single chip. The number of possible labels depends on the amount of switches that can be cascaded and the losses introduced by the periodic filters. Although the losses of the AWG (around 3–4 dB each one) can be compensated by the amplification provided by the SOAs in the MZI-switches, the optical signal to noise ratio (OSNR) degradation is finally the limiting factor. At each SOA-MZI, the OSNR degrades according to the noise figure of the SOAs. A reasonable number of cascaded switches is 5–6. This means that although 10 labels can be allocated in the payload spectrum and therefore 2^{10} possible addresses can be encoded, we can process up to 32–64 addresses, which is an acceptable number if label swapping technique is considered.

IV. ALL-OPTICAL LABEL REWRITER

To accomplish the AOLS technique, an all-optical label rewriter is also required. The label rewriter scheme is shown in Fig. 10.

The label rewriter has the same structure as the label processor discussed previously. The principle of operation of the

Fig. 10. Experimental setup employed to demonstrate the label rewriter.

label rewriter is similar to the label processor. In the case of label rewriter, the CW signals and the periodic filters are set to provide the new label combinations according to the self-routing table shown in Fig. 2. The wavelengths of the CW signals are set to be in-band with the switched payload (the central wavelength of the payload is set by the label processor). Thus, for a given old labels combination, the routing signal is provided by the label processor, and the new labels are provided by the label rewriter. Note that the case of new labels “0 0,” means that no optical signals at the labels wavelength, while in case of new labels “1 1,” the label rewriter should provide two CW signals at distinct wavelengths. As an example, if packet with labels “0 1” enters the packet switch (see self-routing table in Fig. 2), the payload is converted at 1560.6 nm and a signal at 1558.9 nm, in-band with the payload spectrum, that represents the new labels “1 0” is obtained at the label rewriter output. The new labels are coupled to the converted payload, so that, at the all-optical packet switch output, the switched packet contains the new in-band label information.

Similar to the label processor, the processing is performed entirely in the optical domain. By implementing the optical switches by means of very fast SOA-MZI devices, very fast processing time can be obtained. Moreover, the circuit operates in asynchronous fashion, and since the routing signal at the output of the label processor has the same duration as the packet payload, the system can handle packets with variable lengths.

We investigate the performance of the all-optical label erasing and rewriting functions of the packet switch emulating two-cascaded nodes configuration. Fig. 10 shows the experimental set-up employed to investigate the label erasing/re-inserting performance. Node 1 contains the 1×4 packet switch based on label swapping technique, while in Node 2 the new label inserted at node 1 is extracted by the label extractor and the effect on the payload is evaluated. We processed four packets with two labels with pattern of “0 0,” “0 1,” “1 0,” “1 1” to cover the all possible combinations. The packet format employed in the experiments is similar to the one used in the label processor experiment. We set the CW-signals according to the label swapping table reported in Fig. 2. The label bits extracted by the label extractor are shown in Fig. 11(a) and (b). In the experiment, we used two labels with the wavelengths of $\lambda_{L1} = 1551.9$ nm and

Fig. 11. Measured traces. (a), (b) Extracted labels. (c)–(f) Output traces of the label processor.

$\lambda_{L2} = 1552.5$ nm which are within the 20-dB optical bandwidth of the packet-payload. Fig. 13(b) shows the spectrum of the payload signal after label extraction. As compared with Fig. 13(a), the label was erased. Based on two-labels combination and according to the self-routing table, the label rewriter gave four sets of new labels. The label processor output traces are shown in Fig. 11(c)–(f), while the label rewriter output traces are shown in Fig. 12(c)–(f). It can be observed that for input labels combination “0 1,” the label processor produces the routing signal at 1560.6 nm [Fig. 11(c)], while the label rewriter produces the new labels ‘1 0’ represented by the signal at wavelength 1558.9 nm [Fig. 12(c)]. For the old label combination “0 0,” a routing signal at 1547.7 nm is obtained [Fig. 11(d)], and the new labels ‘1 1’ are represented by signals at wavelength 1546.1 nm and 1549.3 nm [Fig. 12(d) and (e)]. For the combination “1 1,” a routing signal at 1542.9 nm [Fig. 11(f)] and new labels “0 1,” represented by the signal at wavelength 1544.5 nm [Fig. 12(f)] was obtained. Finally the combination “1 0” produces a routing signal at 1538.2 nm [Fig. 11(e)] and a new label “0 0” that means no signals. The routing signal is used in the wavelength converter to route the packets in a wavelength routing switch configuration, while the new labels from the label rewriter were combined with the 160-Gb/s converted payload. Note that the wavelengths of the new labels are chosen to be in-band with the converted payload. To study the cascability of the proposed label erasing/rewriting functions, the switched packet at Node 1 output was fed into Node 2. At Node 2 the packet was processed by the label extractor/eraser, and the resulting 160-Gb/s payload was evaluated.

Fig. 14 shows the BER performance at different position of the two nodes system. The BER measurements were performed in a static operation by using a 160-Gb/s PRBS $2^{31} - 1$ data payload and fixing one address [old label “0 1,” see spectrum

Fig. 12. Measured traces. (a), (b) Extracted labels. (c)–(f) Output traces of the label rewriter.

in Fig. 13(a)]. The label extractor in Node 1 causes a penalty of less than 0.5 dB compared to the back-to-back payload. After the wavelength conversion, error-free operation was obtained with 5.5 dB of penalty. As reference we also reported the 160-Gb/s back-to-back wavelength converted, which has 4 dB of power penalty. The additional 1.5-dB penalty compared with 160-Gb/s back-to-back wavelength conversion can be ascribed to the pulse broadening by the label extractor which affects the wavelength conversion performance. The switched packet with the new label (1, 0) [see spectrum in Fig. 13(c)] was then fed into Node 2. The optical spectrum of the packet after the label extractor of node 2 is reported in Fig. 13(d). The power penalty after the label extractor is 0.5 dB. This results in a limited power penalty caused by the extraction/insertion of the new labels.

These results demonstrate the label rewriting function. Note that generally in the label rewriter the number of CW signals required is greater than in case of the label processor. For a large number of CW signals, the total optical power injected into the SOA-MZI should be decreased to avoid impairments due to the high saturation of the SOA. This results in a decreasing of the OSNR of the selected new labels. We have measured that the OSNR decreases from 38 to 32 dB when 4 or 16 CW signals were injected in the SOA-MZI, respectively. This means that the OSNR decreases with 3 dB after doubling the number of input CW signals. However, as new labels are rewritten at each node, the required OSNR of the new labels should be large enough only to guarantee the transmission between two nodes.

Similar to the label processor, the label rewriter operates in asynchronous fashion, is scalable with the number of addresses and can be potentially photonic integrated. Moreover, experiments performed in two-cascaded nodes configuration show that the label erasing and new label insertion operation introduces

Fig. 13. Optical spectra of the packet recorded at (a) before the label extractor/eraser of node 1. (b) After the label extractor/eraser of node 1. (c) Wavelength converted payload with attached the new label. (d) After the label extractor/eraser of node 2.

Fig. 14. BER measurements and eye diagrams at different points of the system. Time scale is 2 ps/div.

only 0.5 dB of power penalty. These results indicate a potential utilization of the presented technique in a multi-hops packet switched network.

V. CONCLUSION

We have demonstrated a 1×4 packet switch based on label swapping technique. All the required functions to switch the packets and to rewrite the new labels have been implemented

in all-optical manner. We employed a scalable labeling technique that by combining N in-band labels, which wavelengths are within the bandwidth of the payload, can encode up to 2^N possible addresses within a limited bandwidth. The label processing technique requires only N active devices to process “on the fly” the 2^N addresses, which makes this technique scalable with the number of addresses. Moreover, being the labels in-band and with a time duration equal to the packet payload, the label processor does not require all-optical flip-flop, operates in asynchronous fashion and can handle packets with variable lengths.

We have demonstrated the label processor by using semiconductor-based MZI optical switches that are suitable for photonic integration and can operate at data rate up to 40 Gb/s. This allows a total label processing time of few tens of picoseconds. This low latency time of the label processor is significant because it shortness the optical delay required to store the data payload, and thus allowing the photonic integration of the whole packet switch. The system was demonstrated with two labels. For a larger number of labels, a number of cascaded SOA-MZI switches and filters proportional to the number of labels are required. This will lead to an increasing in the chip size and an accumulated ASE noise for each SOA-MZI that can limit the scalability of the label processor and label rewriter. The typical length of SOA-MZI switch and the AWG is around 2.5 mm. This means that for each label the photonic chip increases in length of 2.5 mm. If we consider a medium-large size backbone network, a typical number of output links of the node are <32 ,

which can be addressed by using 5 labels. This leads to a length for the label processor and the label rewriter of less than 1.25 cm, which does not limit the capability to integrate the label processor and label rewriter. For what concern the scalability limit imposed by the OSNR degradation, since the losses of the AWG (around 3–4 dB) can be compensated by the amplification provided by the SOAs in the MZI-switches, the OSNR is expected to be reduced steeply after the first SOA-MZI switch, but after that it degrades gradually. The calculation depends on the amplifiers noise figure, the input optical power of the CW signals, and the gain of the amplifier [16]. As a reference, in a recirculation buffer containing 4 cascaded SOA [17] and with a totally compensated loop losses, an OSNR of 26 dB was measured after eight recirculation loops, which corresponds to 32-cascaded SOA.

We have presented experimental results that validate the operation of the packet switch by using two-labels address. Error-free packet switching operation at 160 Gb/s has been obtained with a limited penalty. This penalty was obtained with 2 label wavelengths. For a larger number of labels, the penalty depends on the spectral distortion due to the filtering process. Narrower is the bandwidth of the stop-band of the filter, less spectral distortion and then power penalty will occur. Therefore, for scaling the label extractor for larger number of labels, it is indispensable to properly designed filters with narrow bandwidth. Micro-ring resonators with drop and pass-through ports are potential candidates due their capacity to provide very narrow bandwidth and compactness.

To accomplish the label swapping operation, we used an all-optical label rewriter to demonstrate new labels insertion. The label rewriter is based on the same operation principle and thus has the same features of the label processor. We have experimentally measured that label erasing and new label insertion operation introduces only 0.5 dB of power penalty. These results indicate that the presented label swapping technique can be potentially utilized to devise a multi-hop packet switched network.

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