An ultra-low-energy/frame multi-standard JPEG co-processor in 65nm CMOS with sub/near-threshold power supply.
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Many digital ICs can benefit from sub/near-threshold operations that provide ultra-low-energy/operation for long battery lifetime. In addition, sub/near-threshold operation largely mitigates the transient current hence lowering the ground bounce noise. This also helps to improve the performance of sensitive analog circuits on the chip, such as delay-lock loops (DLL), which is crucial for the functioning of large digital circuits. However, aggressive voltage scaling causes throughput and reliability degradation. This paper presents SubJPEG, a state of the art multi-standard 65nm CMOS JPEG encoding co-processor that enables ultra-wide Vth scaling. With a 0.45V power supply, it delivers 15fps 640×480 VGA application with only 1.3pJ/operation energy consumption per DCT and quantization computation. This co-processor is very suitable for applications such as digital cameras, portable wireless and medical imaging. To the best of our knowledge, this is the largest sub-threshold processor so far.

The architecture of SubJPEG is shown in Fig. 8.1.1. The design is fully compliant with the JPEG encoder baseline standard [1]. Asynchronous FIFOs (AFIFOs) are located at the front-end of the data-path to enable an flexible interface to standard bus interfaces such as PCI/PCI-X/PCI-Express. For each frame, the external main CPU issues a command to the configuration register file of the JPEG processor. The command includes the source data start address/length, destination data start address, YUV sampling ratio, programmable quantization table coefficients, etc. SubJPEG accommodates two command slots in the configuration register file so as to minimize the inter-frame configuration latency. The JPEG data-path has three main stages: (1) 2D-DCT transformation, (2) Quantization, and (3) Huffman encoding. A pair of DCT and Quantization modules is denoted as an "engine". SubJPEG has 4 engines, each engine has 4 transform modules which can operate in parallel to mitigate throughput degradation. It exploits 2 supply voltage domains and 3 frequency domains. The configuration and interface operate with bus clock and VDDH, while the engines function with slow clock and VDDL. However, to reduce the I/O pads of this DMA processor, logic has been added to multi-plex busses for both clock domains and voltage domains so the driving capability is increased. The Monte-Carlo simulation for a critical path at VDD=0.4V shows that the standard deviation σ is reduced by 4.7× and the σ/µ is reduced by 3.6× when the configurable Vf balancer is used.

Our previous research has revealed that, Vf mismatch of paired transistors working in sub-threshold can be worse by a factor of two as compared to transistors working in the super-threshold region [3]. While Vf mismatch is always thought as notorius, an interesting observation is that the Vf mismatch between parallel transistors can be utilized to increase the sub/near threshold current drivability, as shown in Fig. 8.1.3. Therefore, wide sub-threshold power switches, such as S2 and S3 in the Vf balancer, are therefore preferably divided into narrow transistors. This is realized by utilizing a multiple-finger structured transistor. As a result, the drivability of power switches is significantly increased without increasing layout area.

A sub-threshold standard cell library has been developed to synthesize the engines. Compared to existing super-threshold libraries, in the sub-threshold library the standard cells are resized so as to pass Monte-Carlo simulation with high confidence. Besides, certain circuit structures are strictly prohibited, as illustrated in Fig. 8.1.4; cells with more than three parallel-transistors or more than three stacked transistors are avoided (only PMOS transistors are drawn for clarity). Also avoided are ratioed logic cells.

Also shown in Fig. 8.1.4 is the 2-stage level shift scheme used in subJPEG. The 1st stage level shifting is performed through simple buffers which are capable of pulling up signals from sub-threshold VDDL to VDDH (~VDDH+300mV). The 2nd stage level shifting is performed through feedback structured level-shifters from VDDL to 1.2V I/O pad.

The chip is fabricated in a 65nm 7-layer standard VDD CMOS process. A micrograph of the chip is shown in Fig. 8.1.7. The core area is 1.4×1.4mm 2 without pads. Fig. 8.1.5 shows the waveforms of some control signals from the logic analyzer. Also shown is the measurement result for the Vf balancer. Measurements of energy and speed performance are summarized in Fig. 8.1.6.

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References:
Figure 8.1.1: SubJPEG system block diagram.

Figure 8.1.2: Configurable VT Balancer.

Figure 8.1.3: Improving sub-threshold drivability by exploiting VT mismatch between parallel transistors.

Figure 8.1.4: Illustration of prohibited structures in sub-threshold library and 2-stage level shift scheme.

Figure 8.1.5: Waveforms from logic analyzer and VT balancer measurements from oscilloscope.

Figure 8.1.6: (a) Energy/operation for each engine, (b) Throughput for 4 engines and possible real-time image applications.
Figure 8.1.7: Die micrograph and core layout of SubJPEG test chip in 65nm CMOS.