An ultra-low-energy/frame multi-standard JPEG co-processor in 65nm CMOS with sub/near-threshold power supply.

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Many digital ICs can benefit from sub/near-threshold operations that provide ultra-low-energy/operation for long battery lifetime. In addition, sub/near-threshold operation largely mitigates the transient current hence lowering the ground bounce noise. This also helps to improve the performance of sensitive analog circuits on the chip, such as delay-lock loops (DLL), which is crucial for the functioning of large digital circuits. However, aggressive voltage scaling causes throughput and reliability degradation. This paper presents SubJPEG, a state of the art multi-standard 65nm CMOS JPEG encoding co-processor that enables ultra-wide \( V_{DD} \) scaling. With a 0.45V power supply, it delivers 15fps 640×480 VGA application with only 1.3pJ/opération energy consumption per DCT and quantization computation. This co-processor is very suitable for applications such as digital cameras, portable wireless and medical imaging. To the best of our knowledge, this is the largest sub-threshold processor so far.

The architecture of SubJPEG is shown in Fig. 8.1.1. The design is fully compliant with the JPEG encoder baseline standard [1]. Asynchronous FIFOs (AFIFs) are located at the front-end of the data-path to enable an flexible interface to standard bus interfaces such as PCI/PCI-X/PCI-Express. For each frame, the external main CPU issues a command to the configuration register file of the JPEG processor. The command includes the source data start frame, the external main CPU issues a command to the configuration register interface to standard bus interfaces such as PCI/PCI-X/PCI-Express. For each engine, this output is also fed back to the bulk of the VT balancing detector located at its corner. When the engines are set in super-threshold mode, the tri-state buffer is configured so that the power switches are configured so that the bulk of the VT balancer is configured to be in high impedance state. The bulk of the NMOS transistors is configured to be connected to GND. When the engines are configured to be in sub/near threshold mode, the tri-state buffer starts to function. Any fluctuation of the signal \( V_{out} \), which is generated from a process-corner \( V_{I} \) imbalance detector, is thus amplified and fed back to the bulk of the VT balancer. This output is also fed back to the bulk of the VT balancer. As the bulk controlling line is never higher than \( V_{DD} \), so the p-n junction diodes are prevented from turning on. The power switch transistors \( S_p, S_n \) and \( S_b \) are designed with NMOS transistors with their gate control voltage boosted to 1.2V, which is the VDDIO for pads, so the driving capability is increased. The Monte-Carlo transient time simulation for a critical path at \( V_{DD}=0.4V \) shows that the standard deviation \( \sigma \) is reduced by 4.7x and the \( \sigma \mu \) is reduced by 3.6x when the configurable VT balance is used.

Our previous research has revealed that, \( V_I \) mismatch of paired transistors working in sub-threshold can be worse by a factor of two as compared to transistors working in the super-threshold region [3]. While \( V_I \) mismatch is always thought as notoriuos, an interesting observation is that the \( V_I \) mismatch between parallel transistors can be utilized to increase the sub/near threshold current drivability, as shown in Fig. 8.1.3. Therefore, wide sub/threshold power switches, such as \( S_p \) and \( S_n \) in the \( V_I \) balancer, are therefore preferably divided into narrow transistors. This is realized by utilizing a multiple-finger structured transistor. As a result, the drivability of power switches is significantly increased without increasing layout area.

A sub-threshold standard cell library has been developed to synthesize the engines. Compared to existing super-threshold libraries, in the sub-threshold library the standard cells are resized so as to pass Monte-Carlo simulation with high confidence. Besides, certain circuit structures are strictly prohibited, as illustrated in Fig. 8.1.4; cells with more than three parallel-transistors or more than three stacked transistors are avoided (only PMOS transistors are drawn for clarity). Also avoided are ratioed logic cells.

Also shown in Fig. 8.1.4 is the 2-stage level shift scheme used in subJPEG. The 1st stage level shifting is performed through simple buffers which are capable of pulling up signals from sub-threshold \( V_{DDL} \) to \( V_{DDH} \) (~ \( V_{DDL}+300mV \)). The 2nd stage level shifting is performed through feedback structured level-shifters from \( V_{DDH} \) to 1.2V I/O pad.

The chip is fabricated in a 65nm 7-layer standard \( V_{DD} \) CMOS process. A micrograph of the chip is shown in Fig. 8.1.7. The core area is 1.4×1.4mm² without pads. Fig. 8.1.5 shows the waveforms of some control signals from the logic analyzer. Also shown is the measurement result for the \( V_I \) balancer. Measurements of energy and speed performance are summarized in Fig. 8.1.6.

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References:

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**Figure 8.1.1:** SubJPEG system block diagram.

**Figure 8.1.2:** Configurable V_T Balancer.

**Figure 8.1.3:** Improving sub-threshold drivability by exploiting V_T mismatch between parallel transistors.

**Figure 8.1.4:** Illustration of prohibited structures in sub-threshold library and 2-stage level shift scheme.

**Figure 8.1.5:** Waveforms from logic analyzer and V_T balancer measurements from oscilloscope.

**Figure 8.1.6:** (a) Energy/operation for each engine, (b) Throughput for 4 engines and possible real-time image applications.

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**Table:**

<table>
<thead>
<tr>
<th>Mode</th>
<th>VDDL (V)</th>
<th>VDDH (V)</th>
<th>Throughput (MB)</th>
<th>Possible Application</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sub-threshold</td>
<td>0.4</td>
<td>0.6</td>
<td>10 (2.5MHz clock)</td>
<td>Digital still image</td>
</tr>
<tr>
<td>Near-threshold</td>
<td>0.45</td>
<td>0.7</td>
<td>18 (4.5MHz clock)</td>
<td>VGA (640x480, 15fps)</td>
</tr>
<tr>
<td></td>
<td>0.5</td>
<td>0.8</td>
<td>40 (10MHz clock)</td>
<td>VGA (640x480, 30fps)</td>
</tr>
<tr>
<td>Super-threshold</td>
<td>0.6</td>
<td>0.9</td>
<td>100 (25MHz clock)</td>
<td>SXGA (1280x1024, 15fps)</td>
</tr>
<tr>
<td></td>
<td>0.7</td>
<td>1.0</td>
<td>160 (40MHz clock)</td>
<td>UXGA (1600x1200, 15fps)</td>
</tr>
</tbody>
</table>
Figure 8.1.7: Die micrograph and core layout of SubJPEG test chip in 65nm CMOS.