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A Novel Series-Resonant Converter Topology

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Abstract—A converter topology based on the principles of series-resonant (SR) power conversion is described in which the input and output of this converter have one terminal in common, and the transformer is omitted. Both the underlying theory and associated waveforms are presented. The converter is suitable for dc–dc as well as for dc–ac conversion. Special attention is given to operation in the region where the input voltage is approximately equal to the output voltage \( q \approx 1 \). Test results of a 700-W multi-quadrant dc–dc and/or dc–ac converter are shown.

I. INTRODUCTION

The principles of operation of series-resonant power converters (SR converters) have already been discussed by numerous authors [1]–[4]. The advantages of converters of this type, due to the high internal frequency and relatively low switching losses are well known. In many applications, a high-frequency transformer is used for voltage scaling and/or galvanic isolation. However, quite a few applications do not need these features and would find a common (ground) terminal for input and output acceptable. In the “standard” half-bridge or full-bridge configuration as described in [5] and [6], the omission of the transformer will lead to high-frequency common-mode voltages on the output terminals of the converter. Therefore the question arises as to whether there exists a transformerless power network in which the benefits of SR converters are maintained. This paper presents the power network and the associated switching modes and formulates the concepts of series-resonant power conversion in a generalized way, such that both the standard and the new SR converter can be considered as special cases.

It is assumed that the reader is familiar with the operation modes of the standard SR converter as described in [2], [5], and [7].

II. PRINCIPLES OF OPERATION

A. Switching Modes

In the idealized (half- or full-bridge) SR power converter, the current waveform consists of a succession of sections of sine waves. In between two consecutive zero crossings of the resonant current there are generally two current segments, the first of which is usually denoted (for historical reasons) as the “diode current” and the second as the “thyristor current.”

These two current segments are distributed between input and output ports in such a way as to satisfy the conservation of charge and power.

The distribution of current segments between input and output ports also serves the purpose of damping the state variables of the resonant circuit. (The word “damping” is used freely here. We will assume the resonant circuit to be damped as power is extracted from it.) For this purpose, the “diode” current segment is fed back to the input port. This specific implementation of damping has to be paid for by extra losses, for the distortion factor \((i_{\text{rms}}/i_{\text{dc}})\) of the input current is higher than is strictly necessary. Damping of the resonant circuit could also be provided by the output voltage only. The difference between this and a “standard” SR converter is shown in Fig. 1.

From the current waveforms in Fig. 1(b) it is obvious that in this “new” converter no power is fed back to the source. A practical implementation and a more abstract version of a power network that generates the waveforms from Fig. 1(b) is depicted in Fig. 2(a) and (b), respectively. The network as shown in Fig. 2(b), where all switches are assumed to be built up from pairs of antiparallel thyristors, facilitates multi-quadrant operation as well. Because of the symmetry of Fig. 2(b) with respect to the input and the output, the ports can arbitrarily be labeled as “input” or “output.” Throughout this paper the port with the smallest voltage magnitude is labeled as “output” (step-down mode), unless otherwise noted. Fig. 3 gives an overview of the switch operation and associated waveforms for four important switching modes in step-down operation. According to the analysis in Section II.B, these switching modes correspond to operation in the four respective quadrants in the \( U_{\text{dc}}-I_{\text{dc}} \) plane.
three quadrants, indicating that four-quadrant operation is also feasible for the case in which the output voltage is greater than the source voltage (step-up mode).

B. Regions of Operation

For all four quadrants the energy balance over one positive half-cycle can be stated as

$$ E_s(S_{sd}Q_{sd} + S_{st}Q_{st}) = U_o(S_{od}Q_{od} + S_{ot}Q_{ot}) $$

where $Q_{sd}$ and $Q_{st}$ represent the magnitude of the charge transferred by the diode and thyristor current segments, respectively. The coefficients $S_{ij}$ denote the direction of current flow in the source ($i = s$) and output ($i = o$) lines of the converter for the diode ($j = d$) and thyristor ($j = t$) current intervals, respectively. Note that $S_{ij}$ is either $-1$, $0$, or $+1$ and that $Q_{sd}$ and $Q_{st}$ are defined as positive quantities in all cases.

From (1) we derive

$$ \frac{Q_t}{Q_d} = \frac{E_sS_{sd} - U_oS_{sd}}{E_sS_{st} - U_oS_{st}} $$

$$ = \frac{S_{sd} - qS_{sd}}{S_{st} - qS_{ot}} $$

where $q$ is defined by $q = U_o/E_s$. 

As $Q_t/Q_d \geq 0$ by definition, it follows that

$$ (S_{sd} - qS_{sd})/(S_{st} - qS_{ot}) \leq 0. $$

From Fig. 3 we can obtain the values for the $S_{ij}$ for the four different quadrants. Filling in the appropriate values of $S_{ij}$ in (3) yields expressions for the allowed ranges of the normalized output voltage $q$, which is displayed in the last column of Table I. The allowable range for $q$ does indeed comply with the corresponding quadrant in all cases. This implies that the proposed operation modes, as reflected by Fig. 3, do not violate the principle of conservation of energy.

C. Steady-State Characteristics

All the converter operation modes mentioned in Section II.B can be made equivalent to a succession in time of linear networks. For steady-state operation it is necessary that state variables (i.e., capacitor voltage and inductor current) be continuous at the boundaries of the successive intervals. Our analysis will be restricted to steady-state operation modes where the value of successive peak capacitor voltages $V_{cp}(k)$ and $V_{cp}(k + 1)$ are in accordance with

$$ V_{cp}(k) = - V_{cp}(k + 1). $$

Therefore we only need to consider two successive current segments, and add (4) to obtain a set of equations defining steady-state operation. We are especially interested here in the relationship between different circuit variables in steady-state operation, for this relationship gives us a tool for evaluating possible operation regions independent of the type of controller used.

The analysis given in the Appendix yields a general expression for the delay angle $\psi$, (Fig. 1) in a form similar to
the expressions found in [2], [5], and [6]. Employing the notation introduced in Section II.A results in

\[ \cos \psi_r = \frac{(-S_{st}E_s + S_{st}U_o + V_{cp})^2 - (S_{st}E_s - S_{st}U_o + V_{cp})^2 - (S_{st}E_s - S_{st}U_o - S_{st}E_s + S_{st}U_o)^2}{2(S_{st}E_s - S_{st}U_o - S_{st}E_s + S_{st}U_o)(S_{st}E_s - S_{st}U_o + V_{cp})} \]  

(5)

Dividing both denominator and numerator by \( E_s \) we obtain

\[ \cos \psi_r = \frac{(-S_{st} + qS_{st} + \lambda)^2 - (S_{st} - S_{st} + \lambda)^2 - (S_{st} - qS_{st} - S_{st} + qS_{st})^2}{2(S_{st} - qS_{st} - S_{st} + qS_{st})(S_{st} - qS_{st} + \lambda)} \]  

(6)

where \( \lambda \) is defined by \( V_{cp}/E_s \).

Expression (6) is a key equation that gives the relationship between \( \lambda \) and \( q \) for all operation modes.

For the reader familiar with the full-bridge SR converter it may be worthwhile to evaluate this expression for that power circuit. For the full-bridge SR converter the \( S_i \) are

\[ S_{sd} = -1, \quad S_{st} = S_{sd} = S_{st} = 1. \]

Thus (6) reduces to the familiar expression

\[ \cos \psi_r = \frac{1 + q - q \lambda}{1 + q - \lambda} \]  

(7)

which is equivalent to

\[ \lambda = \frac{(1 + q)(1 - \cos \psi_r)}{q - \cos \psi_r} \]  

(8)

The same expression may be found in [6, (41)].

We proceed with our analysis by stating

\[ -1 \leq \cos \psi_r \leq 1. \]  

(9)

Substituting (6) in (9) for the four quadrants, while applying the appropriate \( S_i \) according to Table I, generates a region for every quadrant in which steady-state operation is exclusively possible. These regions can be mapped onto a plane, in which the horizontal axis denotes \( q (= U_o/E_s) \), the normalized output voltage; and the vertical axis denotes \( \lambda (= V_{cp}/E_s) \), the normalized peak capacitor voltage. The region where steady-state operation is possible is shown arc by each quadrant in Fig. 4.

It is interesting to note that in quadrants 1 and 2, steady-state operation is feasible down to a lower value of \( \lambda \), i.e., down to a lower peak capacitor voltage than in the "standard" full-bridge SR converter, where \( \lambda \) is limited to being greater than or equal to 2. This implies that the resonant current remains continuous over a greater operating range than in the "standard" SR converter.

### III. Control

The control electronics contains a so-called "V_{ peak }-controller" which controls the delay angle \( \psi_r \) such that the peak capacitor voltage is maintained at a specified value \( V_{cpref} \) (see (4)) even under dynamic conditions. An incorporated \( V_{cppeak} \) predictor generates a real-time prediction of the next peak capacitor voltage based on the actual values of \( i_l(t) \), \( U_o(t) \), \( E_s(t) \), and \( V_c(t) \). Whenever the predictor indicates that turnover to the next current segment would render the specified value of \( V_{cp} \), the turnover is actually initiated. The \( V_{cppeak} \) predictor does not account for losses in the resonant circuit, so that the actual value of the peak capacitor voltage will be slightly below the specified value. Note that the delay angle \( \psi_r \) does not serve the control of the average load current. As shown in Figs. 1 and 3, the resonant pulses are separated by a zero-current dwell time or interpulse time \( t_i \). The average load current is controlled by adjusting the interpulse time. This control method is basically described in [7].

### IV. OPERATION IN THE q = 1 REGION

Operation in the \( q = 1 \) region requires some additional control with respect to the losses that occur in the resonant circuit. The problem will be pointed out with reference to the idealized current waveforms in Fig. 5.

The waveshape in Fig. 5 is seen to be changing continuously with rising \( q \). For the \( q \neq 1 \) cases power is extracted from the resonant circuit in the first current segment, and in the second current segment it is delivered to the resonant circuit. Average damping over one half-cycle is zero, as the energy content of the resonant circuit is assumed to be the same at any current zero. The net energy \( W \) that is transferred to the resonant circuit should be just enough to compensate for losses.

In the first quadrant step-down mode this energy is equal to

\[ W = Q_i E_s - (Q_r + Q_d) U_o. \]  

(10)

In the \( q = 1 \) region no net energy can be transferred to the
resonant circuit (where $Q_a \geq 0$). Due to losses the $V_{\text{peak}}$ controller will then not be able to maintain the peak capacitor voltage at the specified level, causing the oscillation to cease eventually when the peak capacitor voltage drops below $E_s$. See Fig. 4. Two methods for overcoming this problem will be described.

A. Adding Discrete Amounts of Energy

The first method is described in [7] and is based on a virtual short circuit of the output, every now and then. This is done, for instance, by closing switches $SW_{s1}$ and $SW_{s2}$ in Fig. 2(b). During this "cycle-stealing" process a fixed amount of energy is added to the resonant circuit, raising $V_{\text{cp}}$ by $2E_s$. A disadvantage of this method is that the array of current pulses to the output is interrupted every now and then, thus introducing a low-frequency ripple.

B. Adding an Adjustable Amount of Energy

By the second and superior method a continuous adjustable amount of energy is supplied to the resonant circuit such that it guarantees full static and dynamic stability under all feasible conditions. The approach takes advantage of the properties of the $V_{\text{peak}}$ controller, mentioned previously.

An adjustable amount of energy can be added to the resonant circuit by a virtual short circuit of the power-demanding port during part of the thyristor cycle. This signifies that the resonant current waveform will consist of three current segments. The cut-in angle of this third segment is controlled in such a way as to keep the peak capacitor voltage at the predefined level. Although this third current segment is only required near $q = 1$, it does no harm if it is implemented for the whole operation range. Because the duration of this third segment is typically much shorter than the second, the influence on the formulae is slight in all modes.

The proposed resonant waveforms are depicted in Fig. 6, together with typical input and output current waveforms. The implementation of such a control mechanism in a $V_{\text{peak}}$ controlled SR converter is straightforward and requires very little extra hardware.

Note that the well-known SR converters can take advantage of the three-segment current waveform in the $q = 1$ region as well.

V. VERIFICATION

The operation modes of the novel converter topology were evaluated on a converter that was fully equipped with antiparallel SCR’s. The test converter had the following specifications:

- **source voltage**: $E_s = 100 \text{ V}$
- **maximum inverter frequency**: $f_i = 10 \text{ kHz}$
- **maximum peak capacitor voltage**: $V_{\text{cp}} = 300 \text{ V}$
- **output voltage range**: $-150 < U_o < 150 \text{ V}$
- **resonant capacitor**: $C_1 = 660 \text{ nF}$
- **resonant inductor**: $L_1 = 260 \mu\text{H}$
- **input filter capacitor**: $C_i = 50 \mu\text{F}$
- **output filter capacitor**: $C_o = 50 \mu\text{F}$
- **power at full load**: $P_o = 750 \text{ W}$
- **interpulse time**: $t_d > 10 \mu\text{s}$

To enable the SCR’s to turn off properly, the interpulse time $t_d$ should exceed the SCR turn-off time (10 $\mu\text{s}$). When MOSFET’s are used, the minimum $t_d$ reduces to zero, so that the power transfer capability of the network increases considerably.

Although a high efficiency is potentially an important feature of the novel topology, the converter was not laid out to prove this. The test converter was primarily intended to evaluate the operation modes and the control electronics. Nevertheless, a maximum efficiency of 88 percent was obtained.

Fig. 7(a)-(d) shows the source- and load-current waveforms for all four quadrants for $|q| < 1$. The basic two-segment waveshapes are in agreement with the waveforms of Fig. 1. The overshoot in $i_2$ at the end of each pulse is caused by the reverse recovery of the SCR’s. The waveforms of $i_2$ and $i_o$ are generated by the control electronics, which clips the overshoot mentioned. Waveforms for $|q| > 1$ are not shown, because they are essentially equal to the $|q| < 1$ waveforms (see Section II.A).

The significance of three-segment current waveforms follows from Fig. 8. The converter is able to operate in a steady-state mode at $q = 1$, because the third current segment maintains the capacitor peak voltage at the predefined level of 300 V. The first current segment, which is basically a damping segment, is as short as the control electronics allows it to be. The current $i_2$ in the common (ground) line shows a tiny negative first segment. Due to converter losses the second segment is effectively damping. Only the third segment delivers energy to the resonant circuit.

All four quadrant operation modes, both $|q| < 1$ and $|q| > 1$, are brought together in Fig. 9. The converter is fed from a dc source $E_s = 100 \text{ V}$ and generates a 20-Hz output voltage $U_o = 140 \sin (40 \pi t)$ at a capacitive load of 50 $\mu\text{F}$. From the
signs of $U_o$ and $I_o$ it follows in which quadrant the converter operates. Above Fig. 9 a time scale is indicated. From 20 to 25 ms the converter is idle because the output capacitor is loaded to a value which is close enough to the reference voltage. The three-segment current waveform guarantees that at $t = 25$ ms the $q = 1$ barrier is passed without considerable loss of peak capacitor voltage. The continuous change of $U_o$ and $q$ causes a corresponding change in $Q_d$ and $Q_t$ (see (1)), which is reflected in the envelopes of $i_o$ and $i_1$.

The theoretical limitations of the converter in the $U_o$-$I_o$ plane are shown in Fig. 10. The maximum current in the 3rd and 4th quadrant (trajectories $e$ and $f$) are substantially below the 1st and 2nd quadrant currents (trajectories $a$ and $d$). In the 3rd and 4th quadrant operations the thyristor current is either flowing through the source or the load (Fig. 3(c) and (d)), while in the 1st and 2nd quadrants the thyristor current is simultaneously flowing through the source and load (Fig. 3(a) and (b)). The average output current can be calculated from the average resonant current. From the definition of $S_{ij}$ (see Section II.B) it follows that

$$I_o = \frac{S_{ad}Q_d + S_{ot}Q_t}{Q_d + Q_t} \quad I_1.$$

\[ (11) \]
Eliminating the ratio $Q_d/Q_i$ from (11) using (1) leads to

$$I_0 = \frac{E_s(S_{sd} - S_{st}S_{sd})}{E_i (S_{sd} - S_{st}) + U_{o} (S_{st} - S_{od})} \quad (12)$$

where $S_{ij}$ follows from Table I. For instance at trajectory $a$ the ratio $I_0/I_1$ equals 1, while at trajectory $f$ it equals $-E_s/(E_s + U_o)$.

The maximum average resonant current follows from

$$I_0 = 4C_1 V_{cp} f_i. \quad (13)$$

The trajectories $a$ to $f$ are calculated from (12) and (13) where $V_{cp}$ is maintained at 300 V. The calculations are carried out for an interpulse time of $t_d = 10 \mu s$. The measured data is plotted in Fig. 10 as well. At first sight the measured data is in fair agreement with the calculated trajectories. However, as shown in [5] and [6], the converter losses can be represented by a raise in the output voltage of $P_{loss}/I_o$. If we assume that this corresponds to shifting the calculated trajectories over approximately $+15 \text{ V}$ in the $U_o$ direction in the 1st and 4th quadrant and over $-15 \text{ V}$ in the 2nd and 3rd quadrant, than a very good agreement can by noticed.

VI. CONCLUSIONS

The proposed power network and control techniques make it possible to construct a transformerless SR converter with common ground for input and output ports, with the following properties.

1) The converter is capable of both “step up” and “step down” operation.

2) A single-quadrant converter uses only six semiconductor switches for “full-bridge” operation.

3) The converter has an inherent high efficiency due to:
   
   a) the fact that only two semiconductor switches are in the current path;
   
   b) the absence of a power transformer; and
   
   c) the virtual absence of switching losses as a result of the resonant character of the operation.

4) The converter operates as a dc autotransformer without a transformer being present.

5) The converter is inherently short-circuit proof.

APPENDIX

We will analyze the circuit of Fig. II with respect to the waveform depicted in Fig. 11.

For brevity we introduce the following notations:

$$\beta = \omega_1 t$$

$$\omega_1 = 1/\sqrt{L_1 C_1} \quad (14)$$

$$Y_1 = \sqrt{C_1/L_1} \quad (15)$$

$$Z_1 = \sqrt{L_1/C_1}$$

$$U_{sd} = S_{sd} E_s$$

$$U_{st} = S_{st} E_s$$

$$U_{od} = S_{od} U_o$$

$$U_{ot} = S_{ot} U_o$$

$$V_{CA} = V_c(\beta_k)$$

$$V_{CB} = V_c(\beta_k + \psi_{rk})$$

$$V_{CC} = V_c(\beta_k + \psi_{rk} + \psi_{rk})$$

$$i_B = i(\beta_k + \psi_{rk})$$

We recall the circuit equations valid for $\beta_k < \beta < \beta_k + \psi_{rk}$

$$i(\beta) = Y_1 (U_{sd} - U_{od} - V_{CA}) \sin(\beta - \beta_k) \quad (16)$$

$$V_c(\beta) = V_c(\beta_k) + (U_{sd} - U_{od} - V_{CA}) \{1 - \cos(\beta - \beta_k)\} \quad (17)$$

and the circuit equations valid for $\beta_k + \psi_{rk} < \beta < \beta_k + \psi_{rk} + \psi_{rk}$

$$i(\beta) = i(\beta + \psi_{rk}) \cos(\beta - \beta_k - \psi_{rk})$$

$$+ Y_1 (U_{st} - U_{ot} - V_{CB}) \sin(\beta - \beta_k - \psi_{rk}) \quad (18)$$

$$V_c(\beta) = V_{CB} + i(\beta_k + \psi_{rk}) \sin(\beta - \beta_k - \psi_{rk})$$

$$+ (U_{st} - U_{ot} - V_{CB}) \{1 - \cos(\beta - \beta_k - \psi_{rk})\}. \quad (19)$$

6) The converter offers the possibility to generate a single-phase ac voltage with low distortion from a dc source.

7) By adding branches to the power network and applying adequate control techniques converters with any number of input and output lines can be constructed using only one resonant circuit.
The resonant current will be zero at the end of the thyristor which after some manipulating reduces to

\[
\cos \psi_{rk} = \frac{(-V_{ca} - U_{st} + U_{ot})^2 - (U_{sd} - U_{ot} - V_{ca})^2 - (U_{st} - U_{ot} - U_{sd} + U_{ot})^2}{2(U_{st} - U_{ot} - U_{sd} + U_{ot})(U_{sd} - U_{ot} - V_{ca})}.
\]  

(31)

current segment, thus

\[
i(\beta_k + \psi_k + \psi_{rk}) = 0.
\]  

(25)

From (23) and (25) we derive

\[
\tan (\psi_{rk}) = -\frac{Z_i(\beta_k + \psi_{rk})}{U_{st} - U_{ot} - V_{cb}}
\]  

(26)

for physical reasons

\[
0 \leq \psi_r(k) \leq \pi
\]  

(27)

substituting (27) in (26):

\[
\begin{cases}
-V_{ca} - U_{st} + U_{ot} \geq 0 \quad \text{(28)} \\
(-V_{ca} - U_{st} + U_{ot})^2 = Z_i^2 i^2 + (U_{st} - U_{ot} - V_{cb})^2 \quad \text{(29)}
\end{cases}
\]

Using (29), (22) and (21) we obtain

\[
(-V_{ca} - U_{st} + U_{ot})^2 = (U_{sd} - U_{ot} - V_{ca})^2 \sin^2 \psi_{rk}
\]

\[
+ \{U_{st} - U_{ot} - V_{ca} - (U_{sd} - U_{ot} - V_{ca})(1 - \cos \psi_{rk})\}^2.
\]  

(30)

By substitution of (15) to (16) in (31) we turn back to our original notation and (5) is obtained.

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