Localizing trapped charge carriers in NO2 sensors based on organic field-effect transistors
Andringa, A.; Roelofs, W.S.C.; Thelakkat, M.; Kemerink, M.; Leeuw, de, D.M.

Published in:
Applied Physics Letters

DOI:
10.1063/1.4758697

Published: 01/01/2012

Document Version
Publisher's PDF, also known as Version of Record (includes final page, issue and volume numbers)

Please check the document version of this publication:

• A submitted manuscript is the author's version of the article upon submission and before peer-review. There can be important differences between the submitted version and the official published version of record. People interested in the research are advised to contact the author for the final version of the publication, or visit the DOI to the publisher's website.
• The final author version and the galley proof are versions of the publication after peer review.
• The final published version features the final layout of the paper including the volume, issue and page numbers.

Link to publication

Citation for published version (APA):

General rights
Copyright and moral rights for the publications made accessible in the public portal are retained by the authors and/or other copyright owners and it is a condition of accessing publications that users recognise and abide by the legal requirements associated with these rights.

• Users may download and print one copy of any publication from the public portal for the purpose of private study or research.
• You may not further distribute the material or use it for any profit-making activity or commercial gain
• You may freely distribute the URL identifying the publication in the public portal

Take down policy
If you believe that this document breaches copyright please contact us providing details, and we will remove access to the work immediately and investigate your claim.
Localizing trapped charge carriers in NO$_2$ sensors based on organic field-effect transistors

Anne-Marije Andringa, W. S. Christian Roelofs, Michael Sommer, Mukundan Thelakkat, Martijn Kemerink et al.

Citation: Appl. Phys. Lett. 101, 153302 (2012); doi: 10.1063/1.4758697

View online: http://dx.doi.org/10.1063/1.4758697

View Table of Contents: http://apl.aip.org/resource/1/APPLAB/v101/i15

Published by the American Institute of Physics.

Related Articles

Field-effect-based chemical sensing using nanowire-nanoparticle hybrids: The ion-sensitive metal-semiconductor field-effect transistor
Appl. Phys. Lett. 102, 023501 (2013)

Interface states in metal-insulator-semiconductor Pt-GaN diode hydrogen sensors

Gas temperature measurements inside a hot wall chemical vapor synthesis reactor

Organic hydrogen gas sensor with palladium-coated β-phase poly(vinylidene fluoride) thin films

A design for a compact time-of-flight mass spectrometer

Additional information on Appl. Phys. Lett.

Journal Homepage: http://apl.aip.org/

Journal Information: http://apl.aip.org/about/about_the_journal

Top downloads: http://apl.aip.org/features/most_downloaded

Information for Authors: http://apl.aip.org/authors

ADVERTISEMENT
Localizing trapped charge carriers in NO₂ sensors based on organic field-effect transistors

Anne-Marije Andringa, 1,2,a) W. S. Christian Roelofs, 2,3 Michael Sommer, 4,5 Mukundan Thelakkat, 4 Martijn Kemerink, 3 and Dago M. de Leeuw 1,2,b)

1Molecular Electronics, Zernike Institute for Advanced Materials, University of Groningen, Nijenborgh 4, 9747 AG Groningen, The Netherlands
2Philips Research Laboratories, High Tech Campus 4, 5656 AE Eindhoven, The Netherlands
3Department of Applied Physics, Technische Universiteit Eindhoven, P.O. Box 513, 5600 MB Eindhoven, The Netherlands
4Applied Functional Polymers, Universität Bayreuth, 95440 Bayreuth, Germany
5Macromolecular Chemistry, Universität Freiburg, 79104 Freiburg, Germany

(Received 13 August 2012; accepted 28 September 2012; published online 8 October 2012)

Field-effect transistors have emerged as NO₂ sensors. The detection relies on trapping of accumulated electrons, leading to a shift of the threshold voltage. To determine the location of the trapped electrons we have delaminated different semiconductors from the transistors with adhesive tape and measured the surface potential of the revealed gate dielectric with scanning Kelvin probe microscopy. We unambiguously show that the trapped electrons are not located in the semiconductor but at the gate dielectric. The microscopic origin is discussed. Pinpointing the location paves the way to optimize the sensitivity of NO₂ field-effect sensors. © 2012 American Institute of Physics. [http://dx.doi.org/10.1063/1.4758697]

Nitrogen dioxide (NO₂) is a major air pollutant, which is released during the combustion of fossil fuels. This gas plays an important role in the formation of ozone, acid rain, and photochemical smog. Inhalation of NO₂ has been linked to adverse respiratory effects including airway inflammation in healthy people and to increased respiratory symptoms in people with asthma. The huge impact of NO₂ emission on public health and the environment has led to extensive scientific and technological progress in the field of NO₂ sensors. 1,2

Many sensors are commercially available, such as electrochemical, resistive, and optical sensors.

Recently, field-effect transistors (FETs) have attracted attention as an alternative NO₂ sensing technology. A wide variety of semiconductors has been investigated, for example, amorphous organic semiconductors, 3 carbon nanotubes, 4 and metal oxide nanowires. 5 In all cases, current changes upon NO₂ exposure have been demonstrated; i.e., a current decrease for n-type semiconductors and a current increase for p-type semiconductors. The current change is caused by a shift of the threshold voltage. This shift is due to fixed negative interface charges. 6 Hence, electron trapping is the generic mechanism for NO₂ detection in field-effect transistors.

The dynamics of electron trapping in NO₂ sensors have been investigated for the model semiconductor ZnO. 7,8 An important factor for the sensing in a field-effect transistor is the gate bias, which sets the electron density. Without applying a gate bias transistors are stable in NO₂ ambient. With a positive gate bias, however, electrons are accumulated that are getting trapped. At infinite time, all induced carriers have become immobile. Then the threshold voltage, here defined as the onset of current flow, is equal to the applied gate bias. The NO₂ concentration determines the charge trapping dynamics. The characteristic time for charge trapping is found to be inversely proportional to the NO₂ concentration. 7

Despite many investigations on the mechanism of NO₂ detection with field-effect transistors the actual location of the trapped charges has remained unresolved. The electron trapping can be either in the bulk of the semiconductor or at the interface between the semiconductor and the gate dielectric. The exact location cannot easily be determined because the gate dielectric interface is buried under the semiconductor. Here, we used the very simple but effective technique of exfoliating the semiconductor with adhesive tape. The revealed gate dielectric is then accessible for characterization with scanning Kelvin probe microscopy (SKPM). 9,10 This technique was earlier applied to reveal the location of trapped charges due to gate bias stress 11 and to link the threshold voltage shift in a transistor with a SAM-modified gate dielectric to charges trapped by the SAM. 12

To apply the exfoliation technique, we choose organic semiconductors. Using adhesive tape they can be completely removed at once. The transistors were charged by applying a gate bias in an NO₂ ambient. In situ measurements of the surface potential within the transistor channel were performed before and after exfoliation, using SKPM measurements. Comparison of the obtained surface potentials with and without the semiconductor present did pinpoint the location of the trapped electrons at the gate dielectric interface. The location could be confirmed by using a variety of organic semiconductors.

Field-effect transistors were prepared on heavily doped Si wafers acting as common gate. A 200 nm thermally grown SiO₂ layer was used as bottom gate dielectric. Gold source and drain contacts with a thickness of 30 nm were defined by conventional photolithography, resulting in finger transistors with a channel length and width of 10 and 10 000 μm.

---

a) Electronic mail: annemarie.andringa@gmail.com.
b) Electronic mail: dago.de.leeuw@philips.com.
The transistors were then exposed to 1.5 ppm NO₂ and sub-
with high molecular weight polystyrene (Mw 994 000 g/mol, 
plied from a cylinder containing 3 ppm NO₂ in the carrier 
gas N₂ (Praxair). Additional nitrogen was used to further 
ence, a transistor was stressed without NO₂ for 60 s by 
ing that all free charge carriers have been trapped. As a refer-
shift was then only 0.5 V. This small value rules out conven-
tional gate bias stress as a cause for the threshold voltage 
shift on these time scales.

The charged transistors were analyzed with SKPM as 
quickly as possible after measuring the transfer curves, 
allowing for a direct measurement of the surface potential. 
During the SKPM measurement, all electrodes were 
grounded. We note that perylene bisimide is a unipolar 
-n-type semiconductor that does not support holes. Therefore 
the bulk perylene bisimide semiconductor cannot screen neg-
avtive charges in the channel and SKPM can be used to visu-
alisere trapped negative charges. The local surface potentials 
in the channel are presented in Figure 1(b). The pristine tran-
sistor with a 0 V threshold voltage shows a surface potential 
of around 0 V, which indicates that there are no immobile 
charges present. The values of the surface potentials mea-
sured in the channel of the charged transistors are negative 
and in correspondence with the value of threshold voltage. 
The good agreement indicates that the origin of the threshold 
oltage shift is trapped charges. We note that the slight devi-
ation originates from the finite spatial resolution of the 
SKPM system and a decrease of the amplitude of the sur-
face potential with time, especially in light. Starting the 
potential profile measurement after determining the thresh-
old voltage takes about one minute. The nonzero potential 
measured on top of the source and drain contacts is again 
due to the spatial resolution.

SKPM does not distinguish between electrons trapped in 
the bulk perylene bisimide semiconductor or at the gate 
dielectric interface. The experiment to find the exact location 
of the trapped charges is schematically depicted in Figure 2. 
The transistor with the trapped electrons exhibits a positive 
threshold voltage. The trapped charges are either in the semi-
conductor (I) or at the dielectric (II). In both cases, because 
there is no screening by the unipolar bulk n-type semi-
conductor, the trapped charges give rise to a negative surface 
potential with a magnitude equal to the value of the threshold 
oltage shift. A distinction can be made after exfoliation of 
the semiconductor. In case I, the exfoliation will remove the 
semiconductor including the trapped charge carriers. The 
resulting surface potential is then zero. In case II, the trapped 
charges will stay behind at the dielectric, and a negative sur-
face potential remains.

An N1400 ActivInk transistor is exposed to NO₂ and a 
gate bias of 20 V is applied for 60 s. The surface potential, 
measured as quickly as possible after charge trapping, is pre-
sented as the black curve in Figure 3(a). The negative surface 

respectively. A 2 nm Ti layer was used as an adhesion layer 
for the contacts. To reduce gate bias stress and to facilitate the 
exfoliation process, the gate dielectric was passivated with vapor deposited hexamethyldisilazane (HMDS).

As a semiconductor we use a N,N-dialkylsubstituted- 
(1,7&1,6)-dicyanoperylene-3,4:9,10-bis(dicarboximide) de-
ivative (Polyera ActivInk™ N1400), a well-established 
air-stable n-type semiconductor that exhibits charge carrier 
 mobilities of 0.01-0.4 cm²/Vs. The chemical structure is 
given as inset in Figure 1(a). The semiconductor was blended 
with high molecular weight polystyrene (Mₙ 994 000 g/mol, 
Aldrich Chem. Co.). This high molecular weight polymer 
provides mechanical robustness to the film for improved exfoliation while the device performance is not compromis-
ed, as shown in recent studies on solution blending of or-

Thin films were made by spin coating a blend containing 
3.6 mg/ml of ActivInk N1400, filtered with a 5 μm filter, and 
18 mg/ml polystyrene in chloroform. The perylene bisimide 
films were annealed in vacuum at 110°C for 1 h to remove 
residual water and solvents.

Electrical characterization of the blend was performed 
under vacuum using an HP 4155B semiconductor parameter 
analyzer. The extracted mobility was about 0.02 cm²/Vs, and 

The inset shows the chemical structure of ActivInk 
N1400. (b) Potential profiles corresponding to the trans-
fer curves of Figure 1(a) with ActivInk N1400 still present.
potential indicates the presence of trapped charges. To locate the charges, the experiment was repeated and the exfoliation technique was applied. The transistor is exposed to NO$_2$ using the same charge trapping procedure. However, now the semiconductor is delaminated after stress using adhesive tape and tweezers, as shown in Figure 3(b). The exposed gate dielectric is probed with SKPM. The potential profile after exfoliation is shown as the red curve. The surface potentials are similar with and without semiconductor, which demonstrates that the charges are not trapped in the semiconductor but trapped at the gate dielectric interface. The minor differences are due to recovery in ambient light before the SKPM measurement starts, when the semiconductor is still present.

We note that it is well-known that exfoliation of two insulating materials can yield static charges by contact electrification or tribo-charging. However, as discussed previously the potentials measured here are not generated by the peeling process. First the measured potentials are reproducible, and second, the correspondence of the threshold voltage shift indicates the presence of trapped charges. We note that it is well-known that exfoliation of two insulating materials can yield static charges by contact electrification or tribo-charging. However, as discussed previously the potentials measured here are not generated by the peeling process. First the measured potentials are reproducible, and second, the correspondence of the threshold voltage shift indicates the presence of trapped charges.

FIG. 3. Comparison of surface potential before and after delamination. (a) Surface potential profiles of an N1400 ActivInk transistor after applying a 20 V gate bias for 60 s in NO$_2$. The black curve shows the potential profile with the semiconductor still present and the red curve shows the potential profile after delamination. The surface potentials are identical both with and without semiconductor, which demonstrates that the charges are not trapped in the semiconductor but trapped at the gate dielectric interface. (b) The actual exfoliation process, using adhesive tape and tweezers.

To support the assignment of trapped charges to the gate dielectric we repeated the experiments with two other semiconductors, viz., poly(perylene bisimide acrylate) (PPerAcr, M$_n$ 30 900 g/mol, PDI 1.86) and polytriarylamine (PTAA). Both semiconductors can be completely removed by stripping. The chemical structures are presented in the insets of Figure 4. The synthesis and properties of PPerAcr have been described previously. Thin films were spincoated from a 5 mg/ml solution in chloroform and annealed for one hour at 210°C. Field-effect transistors showed unipolar $n$-type characteristics with a mobility of about 4 × 10$^{-3}$ cm$^2$/Vs. The threshold voltage shifted upon application of a gate bias in an NO$_2$ ambient. The kinetics was comparable to that of the low molecular weight perylene bisimide. The surface potentials before and after exfoliation are presented in Figure 4(a). When the semiconductor is still present a large negative surface potential is measured. Because PPerAcr is a unipolar $n$-type semiconductor the trapped charges again cannot be screened. The surface potentials before and after exfoliation are similar confirming that the charges are trapped at the gate dielectric interface.

The experiments were repeated using PTAA, a well-established air-stable unipolar $p$-type semiconductor that exhibits charge carrier mobilities of 10$^{-3}$ to 10$^{-2}$ cm$^2$/Vs. In an NO$_2$ ambient the threshold voltage of a PTAA transistor shifts towards the applied positive gate bias. The sign of the shift indicates the presence of trapped electrons. We note that the barrier for electron injection into PTAA is too large to inject electrons within the time scale of the experiments. The presence of the electrons could be due to surface
condensation of the \( \text{SiO}_2 \) gate dielectric,\(^{24}\) but the origin is not completely clear. Subsequently the surface potentials of the stressed transistor were measured before and after exfoliation. Figure 4(b) shows that the surface potential with the PTAA semiconductor still present is about 0 V throughout the channel. The trapped electrons did not appear in the surface potential as they were screened by mobile holes in the \( p \)-type PTAA semiconductor. However, the trapped electrons were clearly visible as a large negative surface potential after peeling off the PTAA semiconductor. For both PPerAcr and PTAA AFM measurements showed that the semiconductor was completely removed by exfoliation. The magnitude of the surface potential showed a good agreement with the threshold voltage shift, pointing to electron trapping. SKPM measurements after exfoliation revealed that the trapped electrons are located at the gate dielectric.

The microscopic mechanism of the charge trapping remains unknown. It is different from that in commercially available chemiresistors. When the resistor is exposed to \( \text{NO}_2 \), the \( \text{NO}_2 \) adsorbs on the surface of the metal oxide and redox reactions take place.\(^{1}\) The extraction of electrons from the metal oxide results in an increase in the width of the depletion layer and of the corresponding potential barriers at the grain boundaries. Then the resistance increases, or the current decreases. Transistors, however, are stable in \( \text{NO}_2 \). When applying a positive gate bias, electrons accumulated in the channel are getting trapped. At infinite time, all induced charge carriers are immobile, leading to a threshold voltage equal to the applied gate bias. To determine the location of the trapped electrons we have delaminated the semiconductor with adhesive tape and measured the surface potential of the revealed gate dielectric with scanning Kelvin probe microscopy. The exfoliation technique can be utilized because the semiconductor is bound by weak van der Waals forces. Three different organic semiconductors have been used. The exfoliation experiments have unambiguously shown that the trapped electrons are located not in the semiconductor but at the gate dielectric, here \( \text{SiO}_2 \). Pinpointing the location paves the way to optimize the sensitivity of \( \text{NO}_2 \) field-effect sensors.

We gratefully acknowledge technical assistance by H. Verberne and T. C. T. Geuns and fruitful discussions with E. C. P. Smits and S. G. J. Mathijssen. We acknowledge financial support from the Zernike Institute for Advanced Materials, the Netherlands Organization for Scientific Research (NWO, Vidi grant 700.57.425), and from EU project ONE-P (No. 212311).


