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A novel 3D stacking method for Opto-electronic dies on CMOS ICs

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Abstract: A high speed, high density and potentially low cost solution for realizing a compact transceiver module is presented in this paper. It is based on directly bonding an Opto-electronic die on top of CMOS IC chip and creating a photoresist ramp to bridge the big step (around 220 μ m) from Opto-electronic pads to CMOS IC pads. The required electrical connection between them is realized lithographically with a process than can be scaled to full wafer production. A 12-channel transmitter based on the technique was fabricated and test shows good performance up to 12.5 Gb/s/ch.

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1. Introduction

The required interconnect bandwidth in high-performance computing systems is increasing exponentially. Optical interconnects are a promising solution to overcome the fundamental limitation of electrical interconnects. This is mainly due to the lack of electrical charge in photons allowing for data rate independent and low loss transmission in dielectric and glass waveguides [1]. Even using high speed optical links, more than a thousand channels per processor module will be required to fulfill the I/O requirements [2] which can only be supported by using the whole surface of the chip for the communication interface rather than its perimeter [3].

Several projects have explored the use of vertical cavity surface emitting lasers (VCSELs) and photo-detectors (PDs) vertically stacked on the VCSEL drivers and TIA/LA CMOS chips to form high speed, high density and low cost parallel communication modules for data transfer [4–6]. They either use wire bonding for making the required electrical connections

[4] leading to limited RF performance, or a novel Holey CMOS transceiver which had holes etched away into the CMOS chip in a complicated process to allow for the use of flip-chip bonding [5, 6].

In this paper, we demonstrate a novel 3D stacking solution, an artist's impression of which is shown in Fig. 1. The basic idea is to use a pick and place machine to position the Opto-electrical dies on top of the CMOS wafer containing the complementary ICs (TIA chips for a photo-detector array and laser drivers for a VCSEL array) as shown in the Fig. 1(a). In this paper, we will use the novel stacking method to demonstrate a VCSEL array based transmitter although it can be used widely as an efficient way to connect any fix paths of two quite different height surfaces on a wafer scale process. Fig. 1(b) illustrates the specific structure of each unit in Fig. 1(a). The process described in this paper include: placing the VCSEL array die on the CMOS IC, using a thick photoresist (PR) pattern to create a continuous ramp between the pads on the VCSEL driver and VCSEL array and finally an electrical-plating process to form the desired metal traces, which connect top and bottom pads on both ends of the PR ramp. The process is fully CMOS compatible, uses low temperature processes and can be applied on a wafer scale using low cost pick and place technology. The fabricated 3D stacked transmitter is then tested to show that the components are still working after the process and that high speed operation is maintained.

Fig. 1. (a) 3D stacking model demonstration. (b) 3D stacking single module chip artificial show based on VCSEL array and VCSEL CMOS driver.

2. 3D stacking process

The CMOS IC VCSEL driver has its 10 Gb/s transmission lines in the top metal layer. Since the VCSEL array is directly placed on the CMOS IC, a 20 μ m non-conductive bonding layer is necessary to keep the impedance of transmission lines from being affected. In the prior work, we demonstrated a manual method for placing the VCSEL array at the right place on the CMOS chip [7]. The drawback of that method was that the accuracy of the placement and the thicknesses of the bonding layer (insulating epoxy) were difficult to control. Here we introduce a new way of assembly in which thick positive PR plays the role of the bonding layer. Several advantages follow: first, the PR can be spun on a wafer scale; second, the thickness of PR can be controlled simply by choosing the spinning rate and spinning time; third, the unwanted PR can be easily removed after bonding.

After spinning the PR on the chip, the VCSEL array, measuring 200 μ m in thickness, is placed directly onto the VCSEL driver IC. The VCSEL array itself works as the mask for the exposure and development of the PR bonding layer leaving the desired thickness of bonding layer between the chips. The PR bonding layer becomes stable after baking the chip again in a temperature higher than the pyrolyzation point of the PR. The scanning electron microscope (SEM) image of the stacked bonding chip is given in Fig. 2.

Fig. 2. VCSEL array bonding on the CMOS.

After bonding, there is a big height difference between the top of the VCSEL array pads and bottom pads on the CMOS driver (around $220\mu\text{m}$). Lithography on this topography needs a PR layer with very consistent edge covering. We used multilayer PR to obtain enough PR thickness and minimizing edge bead effect at the same time. Using lithography we define an area of undeveloped PR which can be roughly described as an elongated rectangle the length of which is the array length and the width of which matches the distance between the pads on both chips. After lithography and development, the samples were put directly onto a hotplate, elevating the hotplate temperature slowly from room temperature to the soft point temperature of the PR to change the PR pattern's shape. When exposed to soft point temperature surface tension on the developed rectangular PR shape causes the sharp sidewalls to sag leading to smooth transitions critical for the plating process. Since the subsequent steps (sputtering, lithography for defining plating step, electrical plating, etc) involved thermal processing steps, we increased the temperature of the post-bake above the normal soft-point temperature to reach the pyrolyzation point of the PR. This ensured that the PR pattern stayed stable in the following steps. A SEM picture (see Fig. 3) shows the PR pattern which forms a smooth slope between the VCSEL array and VCSEL driver. The picture was taken after sputtering a seed layer on the chip to eliminate the charge effect on image quality.

Fig. 3. After reflow and seed layer.

After sputtering the seed layer, a lithography step is used to define the plating area. The chip now looks like in the Fig. 4(a). The PR pattern smoothly covers the topology of the chip

from the top VCSEL array pads to the bottom driver pads, which is verified by the zoom in pictures in the Fig. 4(b) and Fig. 4(c). In this step the length and the width of the plating area were defined by the lithographic mask.

Fig. 4. SEM image of the lithography between VCSELS and CMOS driver IC (a). The lithographically defined metallization positions near the VCSEL array (b) or near VCSEL driver pads (c) respectively.

The electrical plating process selectively grows gold paths on the exposed seed layer and the amount of cycles controls the thickness of the gold paths. Combining this process with the lithographic definition of metal trace's length and width, full control over the metal traces geometry is achieved. These gold paths can be designed as Co-Planar Waveguides (CPW) to improve the impedance matching between the driver circuit and the VCSELS. In this demonstration, we used simple straight bars with relatively thick gold layer (around $4\mu\text{m}$) to reduce the resistance and inductance. Figure 5 shows the metal traces after plating.

Fig. 5. SEM image of the plating metal traces (a). The plating quality near the VCSEL array (b) or near VCSEL driver pads (c) respectively.

After removing the PR and the seed layer, the plated metal traces form a continuous connection between the VCSEL array pads and the driver pads, as shown in Fig. 6(a). In Fig. 6(b) and Fig. 6(c), we show the quality and coverage of the pads on both top and bottom surfaces of the integrated transmitter chip. The alignment on the driver pads is perfect. The alignment of the metal traces to the pads on the VCSEL array is slightly off ($\sim 15\mu\text{m}$), which

is due to the VCSEL array placement process. On the other hand, this demonstrates the tolerance of the 3D stacking method to placement errors, which are in the order of magnitude of low cost pick and place machines.

Fig. 6. SEM image of the electrical path between VCSELs and CMOS driver IC (a). The plating quality near the VCSEL array (b) or near VCSEL driver pads (c) respectively.

3. Test results

We used probe needles to test resistance and isolation of the plated metal traces on the finished stacked device. The resistance of a single metal path from the driver pad to the VCSEL pad is smaller than 1 Ohm. The isolation between metal paths is over 10^5 Ohm. Ground-Signal-Ground (GSG) RF probe is used to test the DC performance of VCSEL array when driven through the plated metal traces from driver pads. The test results of the forward current-forward voltage-output light power (I-V-P) performance are shown in Fig. 7, which also includes the original VCSEL performance as reference.

Fig. 7. I-V-P testing results.

We can see the I-V and I-P curves of 3D stacked VCSEL chip have a similar trend as the original VCSEL chip. The threshold of the 3D stacked chip shows a higher current threshold (~ 3.3 mA) than the original VCSEL (~ 1.3 mA). This is not caused by the VCSEL itself but rather is due to the driver pads being connected in parallel to the VCSEL and CMOS driver output circuit. When we apply bias through the driver output pads, a part of the current will flow through the electrostatic discharge (ESD) protection circuit of the CMOS IC. This will not be the case when the 3D stacked chip is powered directly through the driver chip as shown below. The pure VCSEL performance after process can be measured by breaking the

metal paths between the driver pads and VCSEL pads on purpose. Doing this, identical I-V and I-P curves were obtained.

Figure 8 shows the test results of S_{11} reflection coefficient of the new 3D stacking solution and wire bonding solution. The wire bonding performance was captured on the chip, where the same type of VCSEL array is bonded at the same place on a CMOS IC driver, realizing the electrical connection between VCSEL array and CMOS driver by standard wedge bonding machine. The diameter of gold bonding wire is $25\mu\text{m}$. We can see, that at low frequencies, both the wire bonded chip and the new 3D stacked chip have reflections lower than -9dB , which is almost as low as directly testing VCSEL chip itself (around -11dB). However the S_{11} of the wire bonded chip continues to increase above 12GHz , while the 3D stacking solution does not. The 3D stacking approach with its lower power reflection above 12GHz shows therefore great potential for next generation VCSEL based interconnects which are projected to work at 20Gb/s and beyond.

Fig. 8. S_{11} testing results.

In order to test the performance of the 3D stacked VCSEL array transmitter, the required low speed serial communication pads as well as DC power supply and ground pads were wire bonded to a PCB. The high speed digital signal for driving the CMOS driver was generated by a 10Gb/s pattern generator using a PRBS of $2^{31}-1$ pattern length and applied using an RF probe to the input pads of the driver IC (IPtronics IPVD12X12). When embedded in a system wire bonds and RF probing can be eliminated by attaching the 3D stacked chip to the board using flip chip technology. The typical eye pattern for single working channel is measured (seen Fig. 9(a)), which shows the clear open eye diagram at 10Gb/s . An open-eye is also achieved at a speed of 12.5Gb/s , seen Fig. 9(b).

Fig. 9. (a) Eye diagram at 10Gb/s . (b) Eye diagram at 12.5Gb/s .

Since the driver IC channels are disabled in the absence of modulated input signals, only partial loading of the 3D stacked chip was tested. From these testing no temperature related performance degradation of VCSEL transmitter was observed. Finite element simulation of the stacked chip operating at full load, conducted by the authors, suggests that the stacked VCSEL array will operate at 10°C above the temperature of the driver which with proper heat sink can be kept below 45°C .

4. Conclusions

A new 3D stacking approach was proposed and demonstrated in this paper. Taking a transmitter chip as an example, the method was used to stack a 200 μ m thick VCSEL array die on the commercial VCSEL CMOS driver IC. The PR ramp supported the metal traces, connecting the pads of the driver IC with those of the VCSEL chip. The measured results show the metal traces have very low resistance and high isolation (between them). Open eye patterns are achieved both at 10 Gb/s and 12.5 Gb/s. In addition, this method paves the path for impedance matched co-planar waveguides interconnection, which will be essential in the future high speed VCSEL based multi-lane based modules (above 20 Gb/s). Furthermore, the highest temperature used in our method is lower than 200 °C, which is lower than normal wire bonding and flip-chip bonding temperatures. This new approach can also be applied for stacking other Opto-electronic dies on the other substrate, such as photodiode arrays on the counterpart CMOS ICs.

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