A tunable transconductor for analog amplification and filtering based on double-gate organic TFTs

Citation for published version (APA):

DOI:
10.1109/ESSCIRC.2011.6044995

Document status and date:
Published: 01/01/2011

Document Version:
Publisher’s PDF, also known as Version of Record (includes final page, issue and volume numbers)

Please check the document version of this publication:
• A submitted manuscript is the version of the article upon submission and before peer-review. There can be important differences between the submitted version and the official published version of record. People interested in the research are advised to contact the author for the final version of the publication, or visit the DOI to the publisher’s website.
• The final author version and the galley proof are versions of the publication after peer review.
• The final published version features the final layout of the paper including the volume, issue and page numbers.

Link to publication

General rights
Copyright and moral rights for the publications made accessible in the public portal are retained by the authors and/or other copyright owners and it is a condition of accessing publications that users recognise and abide by the legal requirements associated with these rights.

• Users may download and print one copy of any publication from the public portal for the purpose of private study or research.
• You may not further distribute the material or use it for any profit-making activity or commercial gain
• You may freely distribute the URL identifying the publication in the public portal.

If the publication is distributed under the terms of Article 25fa of the Dutch Copyright Act, indicated by the “Taverne” license above, please follow below link for the End User Agreement:
www.tue.nl/taverne

Take down policy
If you believe that this document breaches copyright please contact us at:
openaccess@tue.nl
providing details and we will investigate your claim.
A Tunable Transconductor for Analog Amplification and Filtering based on Double-gate Organic TFTs

D. Raiteri, F. Torricelli, E. Cantatore, A.H.M. van Roermund
Eindhoven University of Technology, Department of Electrical Engineering, MSM
Eindhoven, The Netherlands - Email: d.raiteri@tue.nl

Abstract—This paper presents a transconductor designed using a physical model of double-gate p-type organic thin film transistors (OTFTs). A control voltage can be used to vary the output resistance and the transconductance over one order of magnitude. The voltage gain does not depend on process parameters and therefore is insensitive to shelf and operational degradation. This circuit can be used as a tunable resistor, in voltage amplifiers or in $G_mC$ filters.

I. INTRODUCTION

The interest in electronics manufactured with organic semiconductors (i.e. “organic electronics”) has been constantly growing in the last twenty years. This technology has made a lot of progress both from the performance and the reliability point of view, enabling the design of increasingly more complex organic circuits. Digital circuits, like RFID transponders [1] and microprocessors [2] have been demonstrated. Recently the first comparators, digital-to-analog [3], [4] and analog-to-digital converters [5], [6] have been shown, but more effort must be spent on analog circuit design. Indeed different kinds of organic sensors have already been reported [7] and the lack of a proper frontend and analog signal conditioning is the last hurdle for the realization of fully-integrated smart sensors with organic technologies.

In this paper is presented the design of a linear transconductor suitable for the implementation of voltage amplifiers and $G_mC$ active filters. A novel physical model is used to describe the organic thin-film transistor (OTFT) behavior.

II. DUAL GATE ORGANIC TFTS AND THEIR MODEL

The organic transistors used in this paper are p-type pentacene TFTs with bottom gate structure fabricated using a commercial technology [8] and a new physical model of the OTFT was adopted for this design.

The current conduction in organic TFTs is typically modelled using the concept of variable range hopping (VRH) [9]. According to this theory, in organic semiconductors free carriers jump between localized energy states, therefore the density of states (DOS) defines the electrical properties of the material. In this technology the DOS is well approximated as the sum of two exponential functions [10], [11]: one is valid for the deep states (low energy) and one for the tail states (high energy). In the rest of the paper subscripts “d” and “t” will refer respectively to these two kinds of states.

The channel current $I_c$ can be found combining the deep and tail currents [10], given by

$$I_{d,t} = \beta_{d,t}(V_G - V_S - V_T)^{\gamma_{d,t}} - \beta_{d,t}(V_G - V_D - V_T)^{\gamma_{d,t}},$$

where the prefactor $\beta$ in (1) depends on both geometric and physical parameters of the transistor and the exponent $\gamma$, always larger than two, takes into account the superlinear variation of the mobility with the concentration of charge carriers (and thus $V_G$). The total transistor current can finally be calculated as

$$I_{DS} = I_c \cdot I_s,$$

where the factor $I_s$ takes account of the channel length modulation and reads:

$$I_s = 1 + \left(\frac{V_DS}{V_{Early}}\right)^{1/\gamma_t}.$$  

$I_s$ models the channel modulation due to the space charge limited (SCL) transport in the depletion region [13]. The value of $V_{Early}$ depends on the transistor length, and has been suitably characterized from measurements. In order to keep the continuity of the model the factor $I_s$ multiplies also the linear current, but its effect in the linear region is negligible due to the low $V_{DS}$.

Given the “shunt combination” of currents in (2), only the smallest among deep and tail current is relevant for the total channel current: hence for hand calculations the smallest among the currents (1) can be considered alone.

The OTFTs used in this work have a second gate controlling the back side of the channel. This “top” gate has the property to influence the transistor threshold, inducing a capacitive coupling of the top gate with the channel [8]. It is worth noticing that in our p-type transistors $V_T$ is positive for zero top gate bias, hence the devices are conductive already for $V_{GS} = 0V$.

In this equation $V_{TG}$ is the voltage applied to the top gate, while the flat band voltage $V_{FB}$ is an intrinsic property of the bottom gate stack, and $k$ is a constant depending on the coupling of the top gate with the channel [8]. It is worth noticing that in our p-type transistors $V_T$ is positive for zero top gate bias, hence the devices are conductive already for $V_{GS} = 0V$.

Figure 1 shows the measured and the modelled transfer characteristics of a transistor obtained varying the top gate bias (here it is evident the threshold shifting effect of $V_{TG}$). Figure 2 plots transfer and output characteristic of a transistor, measured and modelled for $V_{TG} = 0$.
III. DESIGN OF THE TRANSCONDUCTOR

The design of a transconductor begins with the choice of the actual transconductive element. The technology used, like almost every other organic one, does not provide linear resistors, hence the choice is limited between the linear and saturation regions of the OTFT. In this case linearity was preferred over transconductance, and thus the output resistance of the transistor $M_2$ (see schematic in Fig. 3) was used to create the transconductance. The transistor $M_2$ acts as source follower and applies the input voltage on $M_2$. The voltage drop on $M_2$ sets the current that the current mirror ($M_3$ and $M_4$) transfer to the output branch. $M_5$ simply cascodes the output. In case of an ideal source follower and current mirror the transconductance of the circuit would be:

$$G_m = 1/v_{02}$$

Unfortunately the actual transconductance always happens to be smaller, especially due to few peculiarities of current mirrors in unipolar organic technologies.

A. Current Mirror

Transistors $M_3$ and $M_4$ mirror the current from the input branch to the output one. Although really simple, this basic current mirror gains additional interest due to the different physics of the technology underneath. Our transistors have positive threshold voltage, hence the sink device $M_3$ is always operating in the linear region and $M_4$ works in saturation only for high source-drain voltages. In our circuit $M_5$ limits the voltage drop on $M_1$, which, therefore, is always biased in the ohmic region too. Because of their bias point, it is not possible to obtain together the same transfer function for both the bias and the small-signal currents.

Indeed, being $M_3$ and $M_4$ in ohmic region, their current is strongly dependent on $V_{DS}$, and this voltage changes in a different way for the two devices. If we apply (1) to the current mirror, it can be shown that the small signal current gain $T = g_{m,44}/g_{m,33}$ is always smaller than one. The transconductances $g_{m,d4}$ and $g_{m,d3}$ can be written respectively as:

$$g_{m,d4} = \beta_d g_{d4} \left( (V_{GS} - V_{FB})^{\gamma d-1} - (V_{GD} - V_{FB})^{\gamma d-1} \right)$$

$$g_{m,d3} = \beta_d g_{d3} (V_{GS} - V_{FB})^{\gamma d-1},$$

and $T$ can be calculated to be:

$$T = 1 - \frac{(V_G - V_D - V_{FB})^{\gamma d-1}}{(V_G - V_S - V_{FB})^{\gamma d-1}},$$

where $V_G$ and $V_S$ are the DC gate and source voltage of both $M_3$ and $M_4$, while $V_D$ is the DC drain voltage of $M_4$. $T$ is less than 1 even when $V_D = V_G$ and the bias currents are identical. This is possible because a small variation of $V_G S_3$ corresponds to a change in $V_{DS3}$ and they both contribute to the variation of $I_{SD3}$. In the case of $M_4$, $V_{DS4}$ does not need to change with $V_{GS4}$, thus the derivative of $I_{SD4}$ is in general different from the one of $I_{SD3}$.

B. Transductive Device and Source Follower

The dimensions of $M_2$ play the most important role in the final transconductance, but an unsuitable choice of $M_3$ and $M_4$ can also negatively affect the performance of the final circuit. This happens when the variations of the voltage on $M_4$ and of the control voltage of $M_1$ are not negligible. Too small devices $M_1$ and $M_3$ will cause $V_{GS1}$ and $V_{GS3}$ to be large, decreasing the linearity and drastically reducing the input range. On the other hand, too wide $M_1$ would result in a waste of area, while a wide $M_1$ would cause a decrease of the input range. Indeed, for low inputs, the source of $M_1$ would saturate to ground due to the positive threshold voltage. Hence the linear part of the characteristic would not start for $V_1 = 0V$, but for $V_1 > V_{GS1}(I_{MAX})$. According to these considerations the final design adopts the same dimensions for all the devices of the input branch.

A slightly higher transconductance of the source follower is advantageous in the transconductor, therefore the top gate of $M_1$ is also driven by the input voltage. It is easily derived combining (1) and (5) that in this configuration the transconductance of the input device increases by a factor $(1 + k)$.

As explained in the subsection IIIIA, the devices $M_3$ and $M_4$ operate in their linear region. For this reason the output resistance is really low and the output branch needs to be cascaded. This task is carried out by $M_5$. It is worth noticing that the presence of $M_5$ does not increase the output resistance up to around $g_{m,v_{02}}$, because the source degeneration is weak and the resulting gain of the local negative feedback is low. For this reason the output resistance of the transconductor is, at first order, equal to the output resistance of $M_5$. This consideration
let us immediately infer the small signal voltage gain of the circuit (when the output is loaded with a current source - a condition that will be referred to as “unloaded”). Both the transconductance and the output resistance are determined by the $r_0$ of the two OTFTs $M_2$ and $M_3$, hence the unloaded voltage gain reads:

$$G = \frac{G_m}{r_0}.$$  

(9)

C. Output Resistance and Gain

In order to increase the voltage gain, it is possible to change the dimensions of $M_3$ to decrease the channel length modulation. Table I summarizes the results of different simulations where the $W$ and $L$ of $M_3$ have been scaled up by the same factor S. The values of $V_{Eavly}$ for different channel lengths have been measured. As expected the output resistance $R_{out}$ rises and so does the gain $G$. This scaling however does not produce a proportional increase in the gain, in fact the output resistance of $M_3$ affects the bias point of $M_4$ and causes a drop of $T$ and consequently of $G_m$.

<table>
<thead>
<tr>
<th>S</th>
<th>W [$\mu$m]</th>
<th>L [$\mu$m]</th>
<th>$G_m$ [nA/V]</th>
<th>$R_{out}$ [MΩ]</th>
<th>$G$</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1k</td>
<td>5</td>
<td>4.55</td>
<td>228</td>
<td>1.03</td>
</tr>
<tr>
<td>2</td>
<td>2k</td>
<td>10</td>
<td>4.51</td>
<td>491</td>
<td>2.21</td>
</tr>
<tr>
<td>4</td>
<td>4k</td>
<td>20</td>
<td>3.8</td>
<td>927</td>
<td>3.52</td>
</tr>
<tr>
<td>8</td>
<td>8k</td>
<td>40</td>
<td>2.9</td>
<td>1800</td>
<td>5.22</td>
</tr>
</tbody>
</table>

TABLE I

**EFFECT OF THE CASCADE CHANNEL LENGTH ON THE GAIN**

Fig. 3. Schematic for the proposed transconductor.

Fig. 4. Output current as a function of the input voltage for different values of $V_{bias} = 0V, 5V, 10V, 15V$ $(V_{out} = 5V)$. The continuous line represents the measured data, the stippled line the simulated ones.

Fig. 5. Measured output resistance for different values of $V_{bias} = 0V, 5V, 10V, 15V$ $(V_{out} = 5V)$.

Fig. 6. Measured transconductance as a function of the input voltage for different values of $V_{bias} = 0V, 5V, 10V, 15V$ $(V_{out} = 5V)$.

The transconductor was realized in the PolymerVision technology and both the transconductance and the output resistance of the transistor have been evaluated. The circuit was operated at $V_{DD} = 20V$ and different measurements have been taken for different values of the control voltage $V_{bias}$ with a step for the independent variable of $100mV$.

The output resistance is shown in Fig. 5 as a function of the output voltage. This plot was derived from the output current measured applying a constant voltage $V_{in} = 5V$ and sweeping $V_{out}$ from ground to $V_{DD}$. The measured and simulated output currents are shown in the inset. While increasing the control voltage $V_{bias}$, the output current drops and the resistance rises. The maximum output current goes from $4.098\mu A$ for $V_{bias} = 0V$ to $337.3nA$ for $V_{bias} = 20V$.

The transconductance was derived from the output current (Fig. 4) obtained sweeping the input voltage from ground to $V_{DD}$. For this measure the output was biased with a voltage source at $V_{out} = 5V$. The resulting transconductance as a function of the input voltage $V_{in}$ is shown in Fig. 6. The current and the transconductance decrease with $V_{bias}$. Varying the control voltage from ground to $V_{DD}$, $G_m$ goes from $18.67\mu A/V$ to $2.16nA/V$. From Fig. 6 the influence of $V_{bias}$ on the linearity of the circuit can also be evaluated. The higher
the control voltage, the larger is the linear input range or, with the same input range, a higher linearity is achieved.

The sets of data in Fig. 4, 5 and 6 (summarized in Table II for $V_{in} = 5V$ and $V_{out} = 5V$) also confirm what stated the section III C. The unloaded gain of the circuit is indeed almost independent on the bias voltage (and on $V_T$), while it depends on the difference between the output resistance of the devices $M_2$ and $M_3$. The two devices have here same $W/L$ ratio and channel length, hence the gain is about one. The actual gain value is slightly higher than 1 because the output resistance of the mirror, i.e. of $M_4$, increases the output resistance of the transconductor compared to the $R_{out}$ of $M_6$. This effect more than compensates the reduction in transconductance $G_{rn}$ due to the actual transfer factor $T$ and to the source follower.

Connecting together input and output nodes, a tunable resistor connected to $V_{DD}$ is obtained. The measured current of such configuration is shown in Fig. 7 for different values of the control voltage $V_{bias}$.

The last figure (Fig. 8) shows the simulated Bode magnitude plot of the transconductor in a $G_{m}C$ filter configuration (see the schematic in the inset). The capacitance of the filter has a value of $C = 100pF$ and the load $M_6$ is $0V_{DD}$ connected to embody a current source. The loss of gain due to the finite output resistance of the mirror, i.e. of $M_4$, increases the output resistance of the transconductor compared to the $R_{out}$ of $M_6$. This effect more than compensates the reduction in transconductance $G_{rn}$ due to the actual transfer factor $T$ and to the source follower.

Connecting together input and output nodes, a tunable resistor connected to $V_{DD}$ is obtained. The measured current of such configuration is shown in Fig. 7 for different values of the control voltage $V_{bias}$.

V. CONCLUSION

Adopting a physical model of OTFTs a transconductor suitable for analog signal conditioning was designed in a unipolar double gate technology. Simulations approximate well the measurement and demonstrate what analytically derived. The unloaded voltage gain mainly depends on a channel length ratio and is weakly sensitive to most process parameters, e.g. the threshold voltage, and hence to their time variation due to ageing.

ACKNOWLEDGMENT

The authors would like to acknowledge the support of Kris Mynie (IMEC) for making the masks and of Polymer Vision for the fabrication of the circuits. This research is supported by the Dutch Technology Foundation STW, which is the applied science division of NWO, and the Technology Programme of the Ministry of Economic Affairs.

REFERENCES