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A new concept for spatially divided Deep Reactive Ion Etching with ALD-based passivation

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Abstract. Conventional Deep Reactive Ion Etching (DRIE) is a plasma etch process with alternating half-cycles of 1) Si-etching with SF_6 to form gaseous SiF_x etch products, and 2) passivation with C_4F_8 that polymerizes as a protecting fluorocarbon deposit on the sidewalls and bottom of the etched features. In this work we report on a novel alternative and disruptive technology concept of Spatially-divided Deep Reactive Ion Etching, S-DRIE, where the process is converted from the time-divided into the *spatially divided* regime. The spatial division can be accomplished by inert gas bearing ‘curtains’ of heights down to $\sim 20\ \mu\text{m}$. These curtains confine the reactive gases to individual (often linear) injection slots constructed in a gas injector head. By horizontally moving the substrate back and forth under the head one can realize the alternate exposures to the overall cycle.

A second improvement in the spatially divided approach is the replacement of the CVD-based C_4F_8 passivation steps by ALD-based oxide (e.g. SiO_2) deposition cycles. The method can have industrial potential in cost-effective creation of advanced 3D interconnects (TSVs), MEMS manufacturing and advanced patterning, e.g., in nanoscale transistor line edge roughness using Atomic Layer Etching.

Introduction

3D through-silicon vias (TSVs) date back to two patents in the 1960s [1, 2], *cf.* Fig. 1. Yet, it is only now with the continuous on-chip scaling reaching the point where Moore’s Law (essentially an economic law) approaches its limits that TSV technology receives increasing interest for 3D integration [3]. Other drivers next to cost reduction are the reduced form factor and the increased performance of TSV-connected stacked-die devices, such as reduced RC delay and low power consumption. TSV technology is also accelerating the rapidly growing market of microelectromechanical systems (MEMS) by enabling the interconnection of multifunctional chips stacked in a heterogeneously 3D-integrated System-in-Package (*i.e.* the so-called ‘*More than Moore*’ domain). Today, the industrial technology of choice for etching both TSV and MEMS structures in silicon is Deep Reactive Ion Etching (DRIE).

Figure 1. TSV structures proposed in Shockley’s patent [1].

Spatially divided Deep Reactive Ion Etching: a new concept

The conventional technology of choice for silicon DRIE etching is the room temperature Bosch process [4, 5] illustrated in Fig. 2a. This process consists of two alternating half-cycles: 1) etching with SF_6 plasma, and 2) passivation of the sidewalls and bottom of the etched features with a protecting $-(\text{C}_2\text{F}_4)_n$ - fluorocarbon, PTFE-like) polymer liner deposited from C_4F_8 plasma.

Figure 2. a) Conventional Bosch etch process scheme with temporal switching of consecutive etch and passivation half-cycles. The horizontal bar in grey represents a pre-patterned hard mask; (b) alternative spatial process modes with C_4F_8 passivation; (c) alternative with spatial ALD SiO_2 passivation of a wafer which moves horizontally back and forth under spatially divided reaction zones. Blue arrows pointing upwards indicate exhaust lines. Notice the difference in height of the gas bearing compartments (down to $\sim 20 \mu\text{m}$) and the plasma compartments (order $\sim \text{mm}$); not to scale.

The first half-cycle is an ion-assisted isotropic etch step with SF_6 plasma. It would proceed - if non-interrupted - mainly by the non-directional F-containing radicals to form volatile SiF_x products that are pumped off. In order to minimize the lateral etching component the etch steps are quickly interrupted by C_4F_8 passivation steps. During each etch step a bias voltage is applied to the substrate holder. This causes a directional physical ion bombardment from the plasma onto the substrate which sputters the polymer off the feature's bottom part, thus leaving the sidewall passivation intact, and enabling the anisotropic etching.

The etch and passivation cycle times are each typically 1-10 s with $0.1\text{--}1 \mu\text{m}$ etched per cycle. The process enables plasma etching of deep vertical microstructures (aspect ratios $\text{AR} \geq 20:1$) in silicon with etch rates of typically $3\text{--}5 \mu\text{m}/\text{min}$, and selectivities up to $\sim 200:1$ against a hard oxide mask (usually SiO_2) [6].

An accelerated etch alternative is to convert the above process from its temporal (i.e. *time-separated*) into the *spatially separated* regime [7]. The spatial separation can be accomplished by inert gas (e.g. N_2) bearing 'curtains' of heights down to $\sim 20 \mu\text{m}$, or even smaller (Fig. 2b). These curtains confine the reactive gases to individual (often linear) injection zones constructed in a gas injector head. By horizontally moving the substrate back and forth under the multiple injector head one can create the alternate exposures needed to complete the overall cycle. The optimum pressure in each injection slot is obtained by balancing the various gas flows which are injected into and exhausted from the slots, and by a proper design of the distance between the various slots and the gas bearing gap height (a smaller gap causes a larger pressure field gradient between the various channels).

The passivation step in spatial DRIE: ALD-based, low-pressure or atmospheric

The selected mask material generally affects etch rate, undercutting, and surface quality of etched features [8]. Oxidic ALD-deposited hard masks like Al_2O_3 are reported to have lower pinhole density and thus superior etch selectivity than conventionally deposited etch hard masks [9, 10]. Thus a further improvement in the spatial approach can be expected from the replacement of the CVD-based C_4F_8 passivation steps by ALD-

based deposition cycles of SiO_2 , or other oxides (e.g. Al_2O_3). Unlike the C_4F_8 case the ALD-based passivation layer is self-limiting and chemisorptive of nature, and less complex in its layer thickness control. This will lead to improved control of the anisotropy and sidewall smoothness in the total DRIE process.

The idea of using temporal ALD passivation in DRIE of high aspect ratio nanosize features was conceived recently [11], yet without any experimental data given. Experimental evidence was reported by Dingemans *et al.* [12]. They published a time-efficient plasma-assisted process for low-temperature (50–400 °C) temporal ALD of SiO_2 using $\text{H}_2\text{Si}[\text{N}(\text{C}_2\text{H}_5)_2]_2$ precursor known as SAM.24, and O_2 -plasma. Precursor dosing times as short as ~50 ms were sufficient to obtain a high conformality ($95 \pm 5\%$) over high aspect ratio (30:1) trenches, as illustrated in Fig. 3a. This indicates that the recombination of O-radicals in such trenches plays no dominant role as was also discussed recently by Knoops *et al.* [13].

Figure 3. SEM images of deep silicon trenches lined with ALD oxide layers: a) a plasma ALD SiO_2 layer deposited at low-pressure in trenches with aspect ratio ~30 during 830 cycles on top of an ALD Al_2O_3 /thermal SiO_2 layer stack inside. Note, that the wavy appearance of the full trench is due a sample cleaving artefact; (after ref. [12] © Electrochemical Society 2012); b) an ALD Al_2O_3 layer deposited at 1 atm. in 138:1 aspect ratio trenches during 600 cycles in a rotary ALD reactor (trenched wafers kindly provided by Fraunhofer CNT/Namlab, Dresden). Note: in an actual DRIE application the passivation would require only a few ALD cycles (i.e. monolayers of SiO_2 or Al_2O_3).

We found that a non-plasma *atmospheric* spatial ALD alternative for oxidic passivation is also possible. Figure 3b shows such an Al_2O_3 layer deposited from trimethyl aluminum and water vapor during 600 repeated cycles of 13.5 ms each in the rotary atmospheric ALD reactor described earlier [14]. The layer has good step conformality ($\geq 80\%$) in trenches with ultrahigh aspect ratios exceeding 130:1. Atmospheric ALD of Al_2O_3 has already successfully been commercialized for the solar cell industry in equipment that deposits films almost two orders of magnitude faster than in conventional (temporal) ALD [15]. This opens up the way to the development of ultrafast atmospheric passivation in DRIE, which would not only simplify and accelerate etching, but also reduce costs (sub-second passivation cycles with, for example, Al_2O_3 depositing at 1.2 nm/s).

Spatial DRIE Reactor Design

The basics of a full spatial DRIE process scheme are illustrated in Fig. 2c. Figure 4 gives an impression of the basics in spatial reactor gas inlet design: a wafer is moving under a (plasma) injector head with inlets for etch gas (SF_6/O_2), bearing gas (N_2) and passivation gas (conventional C_4F_8 or ALD oxide). The pressures p_e , p_p and p_{pu} assumed for the etch, passivation and purge zones, respectively, and the corresponding flow rates Φ_e and Φ_p , lengths L_e and L_p and heights H_e , H_p and H_g of the injection zones are listed in Fig. 4. H is a convenient design parameter to obtain the desired pressures. The pressure drop over each channel is proportional to the cube of its compartment height ($\Delta p \sim H^3$), and linear in L and Φ . Depending on the pressures needed for the spatial DRIE process one can calculate the different dimensions of the bearings. A typical example for low-pressure DRIE is shown in Figure 4, indicating these dimensions to be in the mm to sub-mm range. Note, that the pressure for passivation, p_p , is taken to be one order of magnitude higher than the pressure p_e for etching.

Assumptions

Pressures:

- ▶ $p_e = 13 \text{ Pa}$ (0.1 Torr)
- ▶ $p_p = 133 \text{ Pa}$ (1 Torr)
- ▶ $p_{pu} = 12 \text{ Pa}$
- ▶ $\Delta p_e = p_e - p_{pu} = 1 \text{ Pa}$
- ▶ $\Delta p_p = p_p - p_{pu} = 121 \text{ Pa}$

Flow rates:

- ▶ $\Phi_e = 120 \text{ sccm}$
- ▶ $\Phi_p = 260 \text{ sccm}$

Dimensions:

- ▶ $L_e = 5 \text{ mm}$
- ▶ $L_p = 5 \text{ mm}$

Requirements:

Dimensions:

- ▶ $H_e = 4 \text{ mm}$
- ▶ $H_p = 700 \mu\text{m}$

Figure 4. Schematic of the multichannel gas injector head in spatial DRIE. The injector contains the etch gas inlet, the passivation gas inlet(s) and an outer guard gas inlet to screen off the ambient atmosphere. All inlets can be separated from each other by purge outlets (drawn) and by bearing gas inlets (not drawn here, but see Fig. 2c). Each gas is injected through an inlet with or without microplasma source.

Thus the energy of the fluorine ions from the etching plasma will be higher than that for any ions attracted from the passivation plasma (more collisional losses for F-ions in case of C_4F_8 passivation or oxygen ions in case of oxide ALD passivation). Therefore, in an entirely spatial process with continuous voltage biasing of the full substrate, the ion bombardment of the passivation layer will be sustained during the etch half-cycle.

Timescale Analysis for Convection, Diffusion, Deposition and Mass Supply

In order to further optimize the spatial SF_6/O_2 etch and SiO_2 deposition process parameters preliminary gas transport simulations were performed to analyze all relevant timescales involved. The simulation program used is a general purpose CFD model CVD-X developed to predict and optimize deposition processes in the semiconductor industry [16]. In this program specific models for the description of rarefied gas transport inside trenches have been incorporated. Using these models, transient multi-scale simulations have been performed of flow, precursor transport and deposition reactions in ALD-type reactors filled with high aspect ratio etched wafers.

A short synopsis of the most relevant formulas involved is given in Table 1. For more details on the simulation program one is referred to ref. 16. The simulations were done for the passivation of a wide range of lateral feature scales. The three main categories of features studied are a) microsystem cavities with $50 \mu\text{m}$ openings and aspect ratio 5:1, b) $1 \mu\text{m}$ wide 3D-vias (aspect ratio 10:1, areal density $100/\text{mm}^2$) and c) sub-micron ($0.15 \mu\text{m}$) trenches (aspect ratio 10:1, areal density $10^4/\text{mm}^2$); see Table 2.

Figure 5 shows some of the main simulations results. For a typical conventional DRIE reactor with ~30 liters volume and process parameter (flow rates, pressure, temperature) settings of ref. 12 the relevant process time is dominated by the flushing time scale, which is of the order of seconds (6.12 sec for 90 % volume flushed; 12.25 sec for 99 % volume flushed). The calculated optimum saturation time (transition point from the Langmuir-dominated regime to the supply-dominated regime) at 50°C is around 20-50 ms, as shown in Figure 5a. This corresponds very well with the experimentally determined Si-precursor dosing times for saturation [12].

The results in miniaturized reaction zones of 2.5 mm height and 5 mm length (in both directions), representative for our spatial reactor dimensions, indicate an optimal pressure range from ~0.5 Torr for flat structures (Fig. 5a) to ~5 torr for TSVs (Fig. 5b) and microsystems (Fig. 5c), at $\sim 100^\circ\text{C}$, and 5 - 200 ms timescales depending on the feature's aspect ratio; see Figs. 5b-d.

It is evident that for lower temperatures and higher aspect ratio features the timescales increase (more Langmuir-dominated). Yet, the corresponding timescales for depositing a few passivation monolayers remain typically in the sub-second regime, even at room temperature, i.e. the targeted process temperature for DRIE in the spatial regime.

Considering the mass supply needed to etch bulk silicon (specific density of $5 \cdot 10^{22} \text{ atoms}/\text{cm}^3$) it will be obvious that the Si-etching half-cycle requires prolonged time intervals. This requirement is the main driving force for the development of high-density plasmas in Si-etching.

Table 1. Formulas used for the timescale analysis of convection, diffusion, deposition and mass supply in the different 3D feature cases, listed in Table 2. (a = aspect ratio; A = area). More details in ref. [16].

Eq. 1. Convection, flushing reactor volume	$\tau_{\text{supply, gas}} = \frac{P_{\text{tot}} \cdot M_{\text{precursor}} \cdot V_{\text{reactor}}}{R \cdot \Phi_{\text{tot}}}$
Eq. 2. Reactor diffusion	$\tau_{\text{diff, reactor}} = \frac{H_{\text{reactor}}^2}{D}$
Eq. 3. Trench diffusion	$\tau_{\text{diff, trench}} = \frac{L_{\text{trench}}^2}{D_{\text{Kn}}} \quad D_{\text{Kn}} = \frac{4D_{\text{trench}}}{3} \cdot C_0$
Eq. 4. Langmuir deposition flat	$\tau_{\text{Langmuir, flat}} = \frac{n_{\text{tot}} \cdot R \cdot T}{c_{\text{gs}} \cdot f_s \cdot C_0 \cdot P_{\text{precursor}}} \quad C_0 = \sqrt{\frac{R \cdot T}{2\pi \cdot M_{\text{precursor}}}}$
Eq. 5. Langmuir deposition trenches	$\tau_{\text{Langmuir, trench}} = \tau_{\text{Langmuir, flat}} \cdot \left(\frac{3}{2}a^2 + \frac{19}{4}a + 1 \right)$
Eq. 6. Required mass saturating flat	$\tau_{\text{supply, flat}} = \frac{A_{\text{flat}} \cdot d_{\text{layer}} \cdot \rho_{\text{solid}}}{c_{\text{gs}} \cdot (M_{\text{solid}} / M_{\text{precursor}}) \cdot \Phi_{\text{precursor}}}$
Eq. 7. Required mass saturating trenches	$\tau_{\text{supply, trench}} = \frac{A_{\text{trench}} \cdot d_{\text{layer}} \cdot \rho_{\text{solid}}}{c_{\text{gs}} \cdot (M_{\text{solid}} / M_{\text{precursor}}) \cdot \Phi_{\text{precursor}}}$

Table 2. Dimensions and densities of three characteristic 3D-features used in the timescale analysis of convection, diffusion, deposition and mass supply in spatial DRIE: microsystem cavities with 50 μm openings and aspect ratio 5:1; 1 μm wide 3D-vias (aspect ratio 10:1, areal density 100/ mm^2) and sub-micron (0.15 μm , DRAM-like) trenches (aspect ratio 10:1, areal density 10⁴/ mm^2). Flat wafers are used as a reference.

Feature characteristic	Flat wafer	μ -systems & Sensors/actuators	TSVs	DRAM
Type	-	MEMS cavities	TSV	trench (pore)
Diameter/width (μm)	0	50	1	0.15
Depth (μm)	0	250	10	1.5
Aspect ratio	-	5	10	10
Density (number/ mm^2)	0	10	100	10 ⁴
Exposed area (%)	0	2	0.008	0.02
Area multiplier	1.0	1.39	1.003	1.007

Microplasma sources

The dimensions of the DRIE reactor design described above, call for the use of miniaturized plasma sources or arrays. In view of the accelerated etch rate requirements a logical further step is to make the etch cycle proceed at higher pressure, ideally at atmospheric pressure, or at least sub-atmospheric, *e.g.* 100 mTorr. At higher pressures one can expect higher electron densities (n_e), and correspondingly higher ion and radical formation [17]. Power densities achieved in microdischarges (kW.cm^{-3} to MW.cm^{-3}) are orders of magnitude larger than those in conventional large-scale systems (W.cm^{-3}) [18].

Today, high-density plasma sources are now being designed and explored by the use of microplasma sources or arrays. Generally, this research aims at achieving a $\sim$ hundred-fold increase in electron density [19], significantly beyond the traditional densities of 10^{12} cm^{-3} , thus enabling high-speed etching at correspondingly higher pressures. The challenge is to avoid increased ion scattering, so that the energy and directionality of the ion bombardment is maintained to combine increased etch rates with good anisotropy control in 3D Si etching. Figure 6 shows the potential gain in plasma density (n_e) upon miniaturization of ultrahigh-frequency plasma sources in combination with the use photo-stimulation by UV light sources.

The new concept of ALD passivation for RIE in an all-spatial regime can also be combined with microplasma sources replacing the traditional plasma sources.

Figure 5. Estimated timescales for a) flat substrates and for various categories of 3D features with different densities (cf. Table 2): b) 0.15-1 μm 3D trenches and vias with aspect ratio 10:1, c) microsystems with 50 μm trenches with aspect ratio 5:1, and d) overview at 50 $^{\circ}\text{C}$.

Figure 6. Characteristics of microplasmas in a plane of the spatial size d and the plasma density n_e . From ref. [19]; © IEE Japan, 2006.

As a first step we have designed a Dielectric Barrier Discharge microplasma source with a rectangular (0.5 mm wide x 5 mm long) opening for the reactant gas, which is now being tested and optimized for its etching behavior at close distances from an RF-biased substrate (≤ 2 cm). The etching is done in combination with passivation by C_4F_8 CVD and by ALD-based oxide (Al_2O_3). Preliminary results obtained are not yet optimized: the maximum Si-etch rate achieved so far was 4 $\mu\text{m}/\text{min}$ at only 35 W plasma source power, 10 V substrate bias, 1.2 mbar, 50 sccm SF_6 and 2 cm distance between the microplasma source and the Si-sample. We are confident that further optimization (higher powers and concentrations, shorter distances of ≤ 0.5 cm, SiO_2 ALD passivation, and light stimulation) will give the necessary improvement.

Concluding remarks and outlook

We have described a novel alternative and disruptive concept of Deep Reactive Ion Etching, which converts the conventional time-divided process into the *spatially-divided* regime. The spatial separation is realized by inert gas bearing ‘curtains’ of heights above the wafers down to ~ 20 μm . These curtains confine the reactant gases to individual (e.g. linear) injection slots constructed in a gas injector head. By horizontally moving the substrate back and forth under the head one can expose the wafer to the alternate gases in the overall cycle without the intermittent reactor volume refreshment time delay that occurs upon every cycle.

Spatially-divided Deep Reactive Ion Etching has the potential of yielding unprecedented etch rates in 3D Si etching and becoming a future high-speed alternative for the conventional Bosch process in cost-effective creation of advanced 3D interconnects (TSVs), MEMS manufacturing and other applications.

An additional advantage of the spatial DRIE regime is the significant reduction of passivation that settles on (and flakes from) the reactor walls since in this regime no etch or passivation products deposit. Moreover, fluorine-free, thus environmentally friendlier passivation chemicals can be used. When, in addition, the etch process is applied with ALD-based SiO₂ passivation rather than with CVD-based C₄F₈-based half-cycles, the anisotropy control can be simplified, and yield *e.g.* reduced scallops and mask undercut.

Finally, we note that the concept of spatial etching can also be applied in other demanding application fields such as (plasma enhanced) ALE, *i.e.* Atomic Layer Etching for nanoscale MOSFET devices requiring etching with atomic layer resolution [20,21] and supreme sidewall passivation to suppress line edge roughness. This technology, based on cycles similarly composed of etch/purge/passivation/purge is not commercially viable yet, but can certainly be optimized in the spatially divided regime.

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