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A temperature and disturbance insensitive calibration method for high speed Digital to Analog Converters

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Abstract—The accuracy of a Digital to Analog Converter (DAC) is crucial for its operation. Due to production tolerances [1], the DAC static accuracy is limited, increasing the Integral Non-Linearity (INL). Traditionally, various calibration techniques are used to improve the INL [2].

In a Current Steering (CS) DAC, the output signal is generated by switchable current sources, the current cells, see Fig. 1. Typically, calibration techniques incorporate an additional current source (Calibration DAC, CALDAC) in each current cell, which adds a correction current to the main current source thereby cancelling the error of the main current source. However, the response of the CALDAC to voltage disturbances and temperature variations differs from the response of the main current source.

In the proposed calibration method, the new current cell contains the same unit transistors for both the main current source and the CALDAC, guaranteeing matched response for all current cells. The CALDAC contains an excess of current source unit transistors. Hence, some of these transistors in the CALDAC must be enabled and others must be disabled. By carefully selecting the enabled transistors, the mismatch of the enabled CalDAC transistors cancel the mismatch of the main current source of the current cell.

Therefore, all calibrated current cells feature matched temperature coefficients and disturbance response. For an exemplary 6+6bits segmented current steering DAC, the expected 99% yield INL improves with almost 3 bits while using only 30% additional unit transistors.

Index Terms—DAC, Linearity, Calibration, Disturbance response, Temperature response

I. INTRODUCTION

The static DAC linearity, e.g. INL (Integral Non Linearity), is mainly limited by the finite matching of the DAC current source transistors. The mismatch between identically sized and biased transistors is given in (1) [1].

\[
\frac{\sigma I_\bar{I}}{I} = \frac{A_3^2 + A^4R^2}{(V_{GS} - V_T)^2} \cdot \frac{1}{2WL}
\]  

Using large devices \((W \cdot L)\) reduces the random mismatch, but increases occupied area and hence increases the systematic mismatch and degrades high-frequency performance. The dynamic linearity, e.g. SFDR (Spurious Free Dynamic Range), is usually limited by the achieved static linearity, and further reduced at high speeds by the parasitic capacitances and resistances of the current source transistors. Therefore, to achieve high linearity at high speed, both small and accurate current source transistors are necessary.

To improve the DAC static linearity and to reduce the size of the DAC current source transistors, calibration of the mismatch errors of the DAC current sources can be used. An example of calibration in a Current Steering DAC (CSDAC) is shown in Fig. 1 [2]. For an analysis of different correction methods, see [3].

Two types of calibration strategies can be distinguished: foreground and background calibration. Background calibration is continuously running while the DAC is actively used [4]. It suffers from increased power consumption during operation and the output signal may be polluted by spurious emissions of the calibration activities. Foreground calibration is only active when the DAC is idle, e.g. at startup, and hence avoids the aforementioned disadvantages. However, discrepancies in the environment between calibration and use, e.g. temperature or supply voltage, can reduce the advantages of the calibration. In addition, the advantages of the existing calibration methods also reduce at high speeds [4].

The proposed foreground calibration method uses identical unit transistors in both the current source and the CalDAC to guarantee matched responses to disturbances and temperature variations. The current cell is calibrated by combining unit transistors with opposite mismatch within one current cell such that their combined mismatch is minimized.

The next section explains the temperature and disturbance sensitivity of the conventional calibration. In section III, a new
II. TEMPERATURE AND DISTURBANCE DEPENDENCE

An exemplary schematic of a CSDAC using CalDAC calibration is shown in Fig. 1, which is used in [5] and [6]. In the current cell, named Calibrated Unit Element (CUE), transistor \( M_1 \) is the main current source with output current \( I_{\text{main}} \). Due to process spreading and systematic mismatches, the value of \( I_{\text{main}} \) deviates from the nominal designed value \( T_{\text{main}} \), i.e., for the \( n \)-th current source:

\[
I_{\text{main},n} = T_{\text{main}} + I_{\text{error},n} \tag{1}
\]

The CalDAC generates a correction current \( I_{\text{cor},n} \) such that the output of each CUE \( I_{\text{cue},n} \) equals the value of \( T_{\text{cue}} \):

\[
I_{\text{cue},n} = I_{\text{main}} + I_{\text{error},n} + I_{\text{cor},n} = T_{\text{cue}}. \tag{2}
\]

The range of the CalDAC output current must be chosen such that all expected mismatch values of the main current source can be corrected. The range of the expected mismatch values can be calculated with the well-known MOST matching formula of (1).

A. Temperature response

The bias voltage of the CMOS DAC main current sources is usually generated by a reference current and a diode connected transistor, which is illustrated in Fig. 4. The relationship between transistor current and gate-source voltage is:

\[
I_D = \frac{\mu C_{\text{ox}} W}{2L} (V_{\text{GS}} - V_T)^2. \tag{3}
\]

In the biasing configuration of Fig. 4, the drain current \( I_D \) is constant and the mobility \( \mu \) in (4) is dependent on temperature, hence \( V_{\text{GS}} - V_T \) is dependent on temperature.

The mismatch between the output current of the identically biased transistors \( M_{1,x} \) is given by (1). For high performance DACs, the main current source transistor is usually much larger than the feature size of modern CMOS processes. Thus, the current mismatch is dominated by the threshold voltage mismatch:

\[
\left( \frac{\sigma_I}{I} \right)^2 = \frac{4A_T^2}{(V_{\text{GS}} - V_T)^2} \cdot \frac{1}{2WL}. \tag{4}
\]

This assumption is confirmed by measurements of an existing DAC implementation [8].

It is shown that the mismatch is dependent on \( V_{\text{GS}} - V_T \), and that \( V_{\text{GS}} - V_T \) is dependent on temperature, hence the matching of identically biased transistors is dependent on temperature. At high temperatures, the mobility of the carriers (\( \mu \)) decreases. Therefore, at high temperatures, \( V_{\text{GS}} - V_T \) increases to compensate for the decreasing \( \mu \). Together with the matching equation of (5), it is clear that when the temperature increases, i.e., \( V_{\text{GS}} - V_T \) increases, the relative threshold mismatch decreases.

Mismatch measurements of the existing DAC at normal and high temperature confirm this analysis. Fig. 5 shows the standard deviation of the output current of the 15 unary current cells. The mismatch clearly exhibits a square root dependence on the drain current, which is in conformance with (5) in
combination with the drain current relationship of a MOS transistor in saturation, as shown by (4).

In the discussed conventional CUE, the mismatch of a main current source is compensated by the nominal value of the CalDAC output current, i.e. \( I_{\text{cue},n} = I_{\text{main}} + I_{\text{error},n} \). Hence, both \( I_{\text{main}} \) and \( I_{\text{error},n} \) are set by temperature independent references, while \( I_{\text{error},n} \) is temperature dependent. Therefore, the temperature coefficient of \( I_{\text{cue},n} \) depends on the ratio between \( I_{\text{cue},n} \) and \( I_{\text{error},n} \). Fig. 6 shows the buildup of the output current of two exemplary CUEs. The CUEs are calibrated at \( T = 25^\circ\text{C} \), but for \( T \neq 25^\circ\text{C} \), the CalDAC calibration is not valid. In the analysis above, it is assumed that the CalDAC transistors which generate \( I_{\text{cor},n} \) do not have mismatch and hence no temperature dependence.

In reality, mismatch is present, and hence the CalDAC output current \( I_{\text{cor},n} \) is dependent on temperature. However, the biasing voltage \( V_{b_{\text{cal}}} \) of the CalDAC is higher than the bias voltage of the DAC main current sources \( M_1 \). Hence, the mismatch of the CalDAC transistors is less than the main current source mismatch. Moreover, because of different biasing voltage, temperature dependence of the CalDAC is totally different than the temperature dependence of the main current source. This introduces additional cell-dependent temperature response.

To quantify the temperature dependence, a simple transistor level schematic based on [6] is realized and simulated. Two calibrated CUEs with threshold voltage mismatch between each other are simulated over a temperature range of \(-50^\circ\text{C} \) to \(125^\circ\text{C} \). The temperature dependence of the CUEs output current difference, i.e. \( \text{error}_{\text{low}} - \text{error}_{\text{high}} \), can be as large as 8 CalDAC LSBs, which is 1.3% of the CUE output current.

Thus, for foreground calibration, the INL degrades and also the SFDR worsens when temperature changes. This phenomenon is confirmed by INL and SFDR measurements of an existing DAC [8].

**B. Disturbance response**

Next to the discussion about the temperature dependence of the calibration, the CUEs also exhibit a calibration dependent disturbance response. It can easily be argued that two CUEs with different ratios between main current and CalDAC current have different responses to a disturbance on the gate node of the CalDAC current sources. This also holds for disturbances on other nodes of the CUEs. For an exemplary DAC implemented in a CMOS 65nm process, the disturbance sensitivity is simulated using the circuit of Fig. 7. The simulation circuit consists of two current cells with different correction currents and a disturbance at the common bias voltage node \( V_{\text{b_{cal}}} \). The disturbance response is defined as the difference in the output current response of the two current cells: \( \frac{I_{\text{cor,1}} - I_{\text{cor,2}}}{I_{\text{cor,1}} + I_{\text{cor,2}}} \). The result of an AC-simulation of the disturbance response of two CUEs with different correction current is shown by the top waveform of Fig. 8.

The cell dependent response difference of more than 50% (6dB) will certainly introduce input code dependent behavior, which results in spurious emissions, significantly reducing the SFDR.

**III. PROPOSED NEW CALIBRATION METHOD**

To match the response of the correction hardware to temperature and on-chip disturbances, and hence extend the

![Fig. 5. For an existing DAC current cell array, increasing the bias current and hence the output current improves the output current standard deviation. More importantly, the output current matching improves for higher temperature.](image)

![Fig. 6. Output current temperature dependence of two CUEs](image)

![Fig. 7. Circuit for simulating the disturbance sensitivity of a CalDAC implementation](image)

![Fig. 8. Difference in response of two current cells with different calibrated mismatch for both the conventional CalDAC and the new proposed CalDAC](image)
advantages of the foreground calibration, a new calibration method is proposed.

In the proposed CUE, only identical unit transistors are used in every CUE. These unit transistors are divided in two groups, \( M - K \) unit transistors are in the fixed group and \( K + X \) unit transistors are in the configurable group. The \( M - K \) unit transistors in the fixed group are always enabled. \( K \) unit transistors in the configurable group are enabled and \( X \) units are disabled. The \( M - K \) units of the fixed group and \( K \) units of the configurable group together generate the same nominal output current as the \( M \) unit transistors in the main current source of the conventional CalDAC configuration. Which \( K \) of the \( K + X \) units in the configurable group enabled, is chosen such that the mismatch of the configurable group transistors compensate the mismatch of the fixed group and together generate the desired output current.

A novel principle is the use of identical unit transistors for both the fixed group and the configurable group, sharing a common bias voltage, providing a matched response for every CUE in the DAC. Another novel concept is to compensate the mismatch of the fixed group of transistors in the current cell with the mismatch of the configurable group transistors, generating a temperature stable and disturbance insensitive calibration.

A. Hardware

A schematic overview of the new CalDAC implementation is shown in Fig. 9. The \( M - K \) main current source transistors provide the fixed current \( I_{\text{main}} \), \( K \) units in the group of \( P = K + X \) unit transistors in the CalDAC are switched on to generate the correction current \( I_{\text{cor}} \). The value of \( X \) defines the added amount of redundant current sources with respect to the \( M \)-transistor intrinsic current cell. The value of \( P \) is an indication of the calibration freedom but also of the added layout complexity, since every transistor in the CalDAC is controlled separately. Fig. 10 shows an example of how the currents in the CUE are combined.

Two different calibration methods are used for the unary current cells and the binary current cells, which are described separately. The flowchart of the complete calibration algorithm is shown in Fig. 11.

1) Unary current cells: The principle of the calibrating algorithm of one CUE is to select which transistors of the CalDAC should be switched on such that \( I_{\text{cue}} \) is properly corrected. Fig. 12 gives an example, where \( M = 8 \), \( K = 3 \) and \( X = 3 \). The top figure shows the output amplitude of the unit transistors (which are named \( a-k \)), and gives the first step. Transistors \( a \) to \( e \) are in the fixed group and hence are always enabled. Transistors \( f \) to \( k \) are in the configurable group. The first step in the algorithm is to sort the transistors in the CalDAC according to their output amplitude and then switch on \( K \) of the highest amplitude transistors. In the example, transistors \( f \) to \( h \) have the highest output current of the six CalDAC transistors and hence are enabled. Transistors \( i \) to \( k \) have the lowest output current and hence are disabled.
The main hardware component necessary to implement the binary current cells is the CalDAC. The algorithm is insensitive to the ADC offset errors with equal relative importance.

For the binary calibration, the simple comparator check consists of the sum of all binary current cells and one LSB current source area with approximately 30%.

There is a trade-off between the additional hardware and hardware complexity in the choice for \( K \) and \( X \). The achieved improvement between the intrinsic INL and the calibrated INL depends on \( K \) and \( X \). Monte Carlo simulations of 1200 DACs per one configuration point are executed to investigate the effects of using different values for \( K \) and \( X \) on the 99% yield INL.

First, these simulations show that with a fixed number of CalDAC transistors \( (P) \), the highest improvement of INL is achieved when \( K = X \), since then the number of possible combinations is maximized. For different values of \( K \), \( X \) and unit transistor matching, the 99% yield INL values, with respect to 12 bits accuracy, are shown in Fig. 13. It is clear that using more transistors in the CalDAC results in more possibilities for the algorithm and hence higher improvement when applying the calibration method. It is also observed that the improvement between the intrinsic INL and the calibrated INL is constant when the values of \( K \) and \( X \) are fixed.

When for the exemplary 6+6 bits DAC, 12 bit linearity is required and 99% yield for the INL specification, the combination of 3% unit transistor matching and a CalDAC with \( K = X = 20 \) results in an improvement of static linearity from 9.4 bits to 12.2 bits, while only increasing the current source area with approximately 30%.
B. Temperature response

To investigate the temperature coefficient of the proposed calibration method, the same transistor level simulation of section II is performed. After calibration, the temperature dependence of the difference between the two currents is less than 0.001% of the total output current over the complete temperature range, which is 1000 times lower than the conventional CalDAC calibration. Thus, the proposed calibration principle results in a temperature stable calibration.

C. Disturbance response

The same number of transistors is switched on in every CUE. Therefore, every CUE has approximately the same response to disturbances, independent of the correction current, which guarantees that the advantages of the calibration are also present at high speeds. For simulating the disturbance sensitivity, a disturbance voltage is added to the gate node voltage of the CalDAC transistors ($V_{b1}$ in Fig. 9), which in this CalDAC is the same as the gate node of the main current source transistors. The difference in output response of the two exemplary CUEs is shown as the bottom waveform in Fig. 8. Over the complete frequency band, the difference in response between the two CUEs is less than -70dB. Since the response difference is magnitudes lower than the conventional CalDAC, it is expected that the spurious emissions due to on-chip disturbances are significantly reduced when using the novel CalDAC implementation.

V. CONCLUSION

The proposed novel calibration method overcomes the problems with the cell-dependent temperature coefficients of the Calibrated Unit Elements. Also the cell-dependent response to disturbances is reduced. Due to the reduction of these two cell-dependent responses, the spectral purity of the DAC output signal should be improved. The new calibration algorithm provides opportunities to improve the post calibration INL of a DAC. For an exemplary 6+6bits segmented current steering DAC, the expected 99% yield INL improves with almost 3 bits when using only 30% additional current cell area. The required additional hardware for the measurement loop is negligible.

The proposed new calibration method will obviate the need for background calibration, while also providing calibration advantages to high DAC speeds.

REFERENCES