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Multicore for 4G: 3GPP versus ETSI

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Mobile internet: cost in US$/GB

Mobile internet is fueled by a steady decrease in cost per GB: $0.1x /5 years, ...
Cellular downlink [Mbit/sec]

3.3 Gb/s peak DL rate (LTE-A Rel 10)

DL bit rate

10x / 5 year

1990  2000  2010  2020

GSM  GPRS  UMTS  LTE  HSPA+

3GPP = 3rd Generation Partnership Project
technical specifications: GSM, EDGE, 3G, LTE, ...

... and by a matching steady increase in (peak) downlink data rate of 10x / 5 years, ...
CMOS feature size [nm]

... enabled by a steady decrease in (CMOS) feature size of “only” 0.5x / 5 years, ...

ITRS = International Technology Roadmap for Semiconductors
≈ industry consensus
versus

![Graph showing the decrease in node size from 1970 to 2020. The graph compares Intel node data with ITRS 2010 predictions, showing a trend towards smaller node sizes over time.]
Can ITRS keep up with 3GPP?

- constrained by:
  - battery capacity [Wh] (only 20%/5 years)
  - a thermal limit of 3W for handsets

node [Intel]
ITRS 2010
0.5x/5y

GSM
GPRS
UMTS
LTE-A
HSPA+
LTE
nm

Can ITRS keep up with 3GPP?
Plan: “GMAC[16b]/200mJ” (= GMAC/s/200mW)

Focus on “Multiply–ACumulate” (MAC) part of baseband processing
Assume power budget of 200 mW for “MAC part”
Quantify:
• available GMAC/200mJ [16b] for “ITRS year”
• required MAC/b (16b–MAC/received bit) for “3GPP year”
⇒ required GMAC/s for high-end data rate for “3GPP year”

Robert H. Dennard [1974]:
\[ L \propto \alpha, \quad V \propto \alpha \] (“constant field”)  
\[ C \propto \alpha, \quad I \propto \alpha \] (constant I/\mu)  
⇒ delay = \( CV/I \propto \alpha \)
⇒ energy = \( CV^2 \propto \alpha^3 \)

With Dennard scaling: /5 year
\[ \text{CMOS} \quad \alpha \quad 0.5 \]
⇒ Energy \( \alpha^3 \) \quad 0.125
⇒ GMAC/J \( \alpha^{-3} \) \quad 8×
3GPP bit rate \quad 10×

... the outlook seems promising!
Dennard scaling? Does “V \propto L”? No! Feature size/voltage: we have lost an order of magnitude! ... and the gap is widening
GMAC[16b]/200mJoule

However, Dennard scaling lasted only 1 decade: 1991 – 2002
Baseband (simplified): MAC/bit

- “MAC part”: mostly complex numbers, $2 \times 16$: FIRs, IIRs, FFTs, correlators, $M \times V, M \times M, M^{-1}$, data selection, ...
- WCDMA: a rake receiver also uses “$1 \times 16$” complex MAC (additions)
- total: $100 \leftrightarrow 300$ MAC/bit (simple $\leftrightarrow$ advanced algorithms)
- trend: towards more advanced algorithms, to mitigate interference
3GPP versus ITRS: an increasing GMAC gap

- 2010 – 2020: modem power up 13x (more with heavier algorithms!)
Closing the gap 1: increase power budget

- Power of MAC part will increase 13× in the current decade:
- Unlikely for smart phones, but
- Some increase likely for tablets

Larger surface area of tablets:
- More room for batteries
- Larger area to emit heat
- More room for antennas
Closing the gap 2: peak rate for bursts only

- keep average bit rate @ constant power of 200mW
- allow peak rate for bursts only (throttling the DL stream)
- period << thermal time constant handset
- period < user response time (content dependent)

- This results in a decreasing duty cycle of the baseband processing.
- Bonus: fewer DSP resources needed.
- This requires a standardized protocol with the base stations.
Closing the gap 3: optimize algorithms

Equivalent algorithms may require fewer MACs/bit, e.g.

- Fast FIR
- frequency-domain filtering
- ...

... but unlikely to provide 13×

Simpler algorithms for high bit rates: *(scalable algorithms, adaptation):*

- high bitrates only feasible when channel is “clean”;
- .. allowing for simpler algorithms that require fewer MAC/bit.

That is, high MAC/bit algorithms only when channel is challenging.
Closing the gap 4: more parallelism at low $V_{dd}$

1. scale $V_{dd}$ with $\sqrt{\text{load increase}}$ to keep dynamic power constant
2. calculate $f_{\text{clock}}$ slow down
3. compensate lower $f_{\text{clock}}$ by increase in parallelism
4. calculate area & watch in horror!

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Closing the gap 5: optimize HW architecture

Conflict:

- multi-standard, multi-channel push: HW → SW
- to close the power gap push: SW → HW

- Efficiency of DSPs [GMAC/J] is improving relative to HW SIMD, SIMD width, complex number support, special instructions, ... ... historically a few % per year, likely to continue.
- share of load on DSP to decrease over time?
- DSP flexibility often overkill; more tailored flexibility needed
- (how to quantify flexibility, versatility ...?)
#accumulators, area

- **power, without discussed measures**

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versus : conclusion

In the decade 2010–2020:

• the cellular peak downlink data rates will increase 100x
  (the associated baseband workload may grow even more)

• whereas CMOS feature size will decrease by only 4x
  and, as a result, MAC/200mJ will increase by only 8x

To close this 13x gap between available and required GMAC/200mJ, we need to:

1. allow for a somewhat higher power budget for modems in tablets,
2. restrict peak rates to a controlled duty cycle,
3. optimize baseband algorithms & adapt them to channel conditions,
4. operate at a (slightly) lower Vdd by using more parallelism (?),
5. optimize the hardware: by (less?) usage of more efficient vector DSPs.
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THANK YOU