InP membrane on silicon integration technology

Smit, M.K.

Published in:
Photonics Conference (IPC), 2013 IEEE

DOI:
10.1109/IPCon.2013.6656456

Published: 01/01/2013

Document Version
Publisher’s PDF, also known as Version of Record (includes final page, issue and volume numbers)

Please check the document version of this publication:

• A submitted manuscript is the author’s version of the article upon submission and before peer-review. There can be important differences between the submitted version and the official published version of record. People interested in the research are advised to contact the author for the final version of the publication, or visit the DOI to the publisher's website.
• The final author version and the galley proof are versions of the publication after peer review.
• The final published version features the final layout of the paper including the volume, issue and page numbers.

Link to publication

Citation for published version (APA):

General rights
Copyright and moral rights for the publications made accessible in the public portal are retained by the authors and/or other copyright owners and it is a condition of accessing publications that users recognise and abide by the legal requirements associated with these rights.

• Users may download and print one copy of any publication from the public portal for the purpose of private study or research.
• You may not further distribute the material or use it for any profit-making activity or commercial gain
• You may freely distribute the URL identifying the publication in the public portal?

Take down policy
If you believe that this document breaches copyright please contact us providing details, and we will remove access to the work immediately and investigate your claim.
InP Membrane On Silicon integration technology

Meint. K. Smit, TU Eindhoven - COBRA Research Institute
P.O.Box 513, 5600 MB Eindhoven, The Netherlands, m.k.smit@tue.nl

Abstract: Integration of light sources in silicon photonics is usually done with an active InP-based layer stack on a silicon-based photonic circuit-layer. InP Membrane On Silicon (IMOS) technology integrates all functionality in a single InP-based layer.

Integration of light sources and amplifiers is still a major problem for silicon photonics. Even though there is important progress, processes with good quality lasers are not yet available, and for most applications silicon photonics can only offer half solutions: the lasers have to be integrated in a hybrid way. This is a serious impediment for scaling to larger circuit complexity, as available in advanced InP-based integration processes.

Several approaches are followed for providing silicon with lasers and optical amplifiers. A fascinating approach is the silicon-based Ge-laser using a quasi-direct bandgap layer. It is created with a combination of strain and high n-doping, which bring the Fermi-level in the indirect band close to that of the direct band. MIT succeeded in demonstrating laser operation [1], but the efficiency is in the 10^{-3} range and a major improvement is required to bring it close to the efficiency of InP lasers. Most other players use III-V materials for providing the silicon platform with optical gain. The III-V stack can be integrated in two different ways: by wafer (or die) bonding, or by hetero-epitaxial growth.

UCL has recently reported an InAs/GaAs Quantum Dot (QD) laser fabricated with hetero-epitaxial growth on a silicon substrate [2]. Due to the low gain of QD-material and the low index contrast with the silicon substrate fabrication of compact components is difficult. Therefore, it appears unlikely that hetero-epitaxial growth is a viable option for integration of large scale photonics ICs.

Using wafer or die bonding the photonic circuit can be produced in a thin high-index membrane with a high vertical contrast (usually Si or SiGe, but InP is also possible). An important advantage of the high vertical contrast is that passive components like couplers, demultiplexers, and filters become much smaller than in low-index contrast waveguide systems, like conventional InP technology. At present three different approaches are followed. They are schematically depicted in Figure 1.

UCSB [3] follows an approach in which the active III-V wafer stack is bonded on top of the silicon waveguide layer in order to provide the silicon waveguide mode with gain, as depicted in Figure 1(a). In order to achieve a high gain the confinement of the waveguide mode in the gain layer has to be high, but this will cause a large discontinuity at the junction between the passive and the III-V-loaded silicon waveguide. This problem is solved by using tapers for adiabatic coupling between the active and the passive waveguide sections. These introduce additional length, however. Reported total lengths are in the order of 150 µm per coupler, which contributes significantly to the total circuit size.
IMEC, COBRA-TU/e and LETI were the first to report a full optical link on a silicon wafer [4]. The link consisted of a laser fabricated by IMEC and a detector fabricated by COBRA, which were connected via a waveguide fabricated in a silicon membrane by LETI. The laser and the detector were fabricated in a III-V layer stack covered with a polished SiO$_2$ layer, which was bonded on top of the silicon waveguide layer as depicted in Figure 2(b). The light was coupled from the III-V waveguide through the SiO$_2$-layer to the silicon waveguide with a tapered coupler. IMEC has since replaced the molecular bonding using SiO$_2$ by adhesive bonding using a BCB polymeric layer which is more tolerant to non-flatness of the bonding surfaces. Using this approach it has recently demonstrated a 4-channel WDM laser that produces more than 4 mW output power in the silicon waveguide [5]. Taper lengths in this approach are comparable to the approach of UCSB, in the order of 150 µm.

COBRA-TU/e, in cooperation with IMEC, is working on an alternative approach in which the couplers between the III-V and the silicon waveguide layer are avoided by integrating the passive circuitry also in the III-V layer stack and thus avoiding the need for an additional silicon waveguide layer. It is depicted in Figure 2(c). We have called this approach **IMOS: InP Membrane On Silicon**. By avoiding the fairly long couplers IMOS circuits will be more compact than circuits employing a silicon layer. Even more important: because light does not have to be coupled through the BCB bonding layer, IMOS allows the use of a thick BCB layer between the photonic and the electronic layer. This offers sufficient thermal isolation to operate InP lasers on top of hot CMOS when double-sided cooling is applied.

IMOS uses InP and Si for the task for which they are best suited: InP for photonics and silicon for electronics.

![Figure 1: Three different ways to integrate Photonic ICs on silicon or CMOS wafers with InP-based lasers and optical amplifiers.](image)

**Legend**
- Silicon
- silicon dioxide or BCB
- active InGaAsP/InP
- passive InP

**References**


