A Self-calibrating current-steering 12-bit DAC based on new 1-bit self-test scheme

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A SELF-CALIBRATING CURRENT-STEERING 12-BIT DAC BASED ON NEW 1-BIT SELF-TEST SCHEME

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Abstract - This paper presents a self-test self-correction scheme for segmented current steering (CS) DACs. Prior art is critically analyzed. The new scheme improves the DAC linearity by improving the accuracy of the thermometer current sources. The algorithm, which controls the scheme, is described in details. A 12-bit CS DAC, with 6-6 segmentation, is implemented using the new scheme and algorithm. The DAC core is designed with 10-bit intrinsic linearity and this is improved to 12-bit level via self-calibration. High-level simulation results and the CMOS layout of the DAC are presented. Further enhancements of the scheme are suggested.

Keywords - digital-to-analog converters, self-calibration, current-steering circuits.

I. INTRODUCTION

The rapid development of silicon technology, the reduction of the power supply voltages, and the ever increasing demands for resolution and linearity make self-calibration capabilities of digital-to-analog converters (DACs) an eventual necessity. Their implementation demands reliable but simple self-tests and self-correction algorithms.

To keep a competitive edge, companies often manufacture chips with the latest available technology that is still neither well characterized nor stable. Moreover, the reduced voltage head-room does not allow high overdrive voltages, which further deteriorates the intrinsic circuit characteristics. Such drawbacks have a particularly negative impact on DACs, where element-matching is a key requirement. On the other hand, the growth in digital electronics and the market driven mixed-signal needs require DAC systems having ever higher effective resolution and ever improving linearity. That is why DAC self-calibration techniques have become a focal point of research in the recent past. The self-calibration capabilities allow automatic compensation of production tolerances, react on changes of chip physical parameters which lead to the design of smaller, more efficient, and better converters.

This article gives an overview of the major calibration techniques for DACs, presents a new self-calibration scheme, and suggests further steps of research in this area. Section II discusses prior art in the field. Section III presents a new self-calibration algorithm. Section IV describes its implementation in a design example. Section V suggests a variation of the presented self-calibration scheme. Finally, conclusions are drawn in section VI.

II. OVERVIEW OF SELF-CALIBRATION

The vast majority of current calibration techniques for DACs employ self-test to measure the value under calibration. A notable alternative is presented in [1], where the reference current is forced on the signal current sources via current copiers. No significant further development of this technique followed in the literature, because of its two major problems: the capacitor leakage current and the charge feed-through from the switch, [2]. Nowadays, self-tests capabilities are a built-in part of the self-calibration schemes. The process of self-calibration in CS DACs can be considered as a combination of two parts: data acquisition (self-test) and value self-correction. Background calibration is when these two processes are run continually. Start-up calibration is when these processes are executed only once at chip power-up and the results are memorized.

A. Background calibration.

A notable work in the field of background calibration is presented in [3]. The concept of a floating current source is introduced: instead of terminating the current cell to ground, it is terminated to a resistor, which in fact conducts the signal current. The voltage drop over this resistor is used by a measuring device (e.g. ΣΔ ADC [3]). The concept uses two matched resistors: one for calibration and another for the normal DA conversion. These ideas are further developed in [4], where the measuring device is sim-

plified to a current comparator, which via an analog loop implements the self-test and the self-correction steps for the current calibration process. However, due to the voltage drop on the current measuring resistors and its supporting circuitry, these works [3], [4], would become problematic if designed for low power supply CMOS processes. Furthermore, a common problem for the continual background calibration techniques is the potential interference of the calibration activities (clocks, switchings, etc.) with the output of the DAC. This might have a bi-directional negative impact, in the sense that the activity of the calibration may interfere with the output current, and similarly the activity of the DA conversion may affect the calibration. For example, there can be deterioration of the output signal due to calibration spurs, shown in [4], and similarly there can be deterioration of the calibration accuracy due to switching voltage variations in the current cell. A solution is proposed in [5] to reduce the calibration spurs in the output DAC frequency spectrum, in which the clock rate is randomized for the background-running calibration, effectively spreading its power over a larger frequency range. Secondly, a solution is proposed by extra capacitive loading of the internal nodes [4], to help smooth out the switching glitches, but this slows down the current cell response.

B. Start-up calibration.

The other major class of DAC calibration techniques is start-up calibration. These execute the self-test and the self-correction operations only once, with chip power-up. Then, the results are memorized and further used during the DA conversion. The power-up calibration techniques for CS DACs can be divided into two sub-classes: correction of the output current; and correction of the individual current sources.

B.1. Correction of the output current.

A recent work applying the technique of correction of the output current is reported in [6]. A single calibrating DAC (CALDAC) operates in parallel with the main DAC. Their currents are summed up at the output of the chip, so that the CALDAC currents compensate the static errors of the main DAC, for every input digital word. A 16-bit ADC is used to measure the static errors of the main DAC. The data is used in a loop for the generation of the CALDAC correction digital words. Thus, the self-test is a combination between a highly-linear ADC and digital processing. It is applied once with chip power-up and the results are stored. The main problem of this technique comes from the fact that two different DACs operate in parallel. That is to say, the main DAC and the CALDAC operate with different currents and hence their responses are different. Therefore, synchronization problems limit its dynamic performance at higher sampling frequencies, [6].

B.2. Self-correction of the individual current sources.

A calibration technique that inherently reduces the negative impact on the DAC dynamic performance is the adjustment of the DAC individual current sources. The converter reported in [7] is an example of such a technique. It is also one of the top state-of-the-art designs found in the literature, in terms of static linearity (INL<0.7LSB, DNL<0.3LSB for 16bits of resolution) and dynamic performance (75dB up to 200MHz signal frequency at 400MS/s). The calibration targets the currents generated by the thermometer current sources. Their adjustment is done by mini-CALDACs attached to each thermometer current source. Such a technique prevents major dynamic problems due to calibration, because the correction firstly is embedded in the current sources; and secondly is static, i.e. not carried out during the normal signal DA conversion. The self-test is supported by an off-chip 6-bit successive approximation ADC, which in combination with the calibration engine adjusts the thermometer current sources to 18-bit level. This design is discussed in more details here, since it serves as a useful background to the self-test self-calibration CS DAC scheme proposed later. Figure 1 shows the architecture of the current generation of [7].

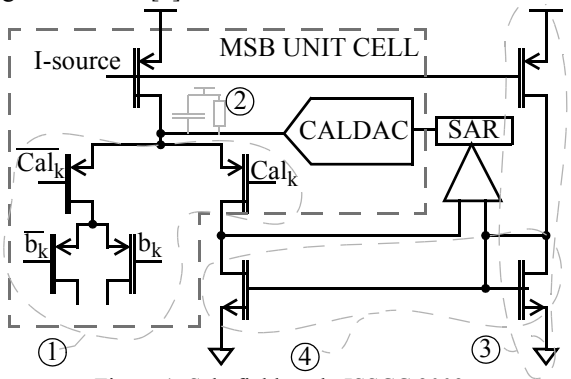

Figure 1: Schofield et al., ISSCC 2003.

The start-up self-test measures the major source of static current errors, coming from the random and the systematic mismatch of the transistor-based segmented current sources. It cannot account for the slow varying errors that appear during the normal operation of a DA conversion, e.g. temperature-dependent offsets. It cannot account either for the signal dependent errors and the errors associated with the loads of the current sources. However, the negative side effects of self-test, as explained in the

previous sub-sections, have a much reduced effect on the dynamic performance of the system core.

The thermometer (MSB) current source is realized with a PMOS transistor operating in parallel with a CALDAC, see Figure 1. Their combined currents are either switched via $\overline{Cal}_k$ for normal DA conversion or alternatively switched via Cal_k for calibration. A self-test capability measures the difference between this current and a master current via the 6-bit off-chip SAR ADC and the NMOS transistors. The acquired information in the digital domain is fed as a correction word to the CALDAC.

This scheme does not correct for the mismatches in the current source loads - the PMOSTs controlled by $\overline{Cal}_k$, Cal_k, $\bar{b}_k$, and b_k, noted as ① in Figure 1. The mismatch offsets in these transistors are transformed to a current mismatch due to the body effect of the current source transistor. Furthermore, there is a different CALDAC word for every calibrated current source and hence a different number of parallel calibrating current source transistors get turned on. Consequently, the thermometer current sources have different output impedances (noted as ②). That is why to minimize both of these negative effects, the combined parallel output impedances of the current source transistor and the CALDAC should be high enough. Furthermore, there is an inherent post-calibration mismatch between the binary (non-segmented) and the thermometer (segmented) parts. All the thermometer current sources are calibrated to a common master (noted as ③). Its mismatch with regard to the binary part, is added to the calibrated thermometer current sources. This would appear as a DNL error on the transition between the non-segmented and the segmented parts. Finally, the way the self-test is based on information acquired in the voltage domain (noted as ④), which includes the extra capacitive loading of the voltage comparator, limits the speed and hence is only appropriate for start-up calibration.

Nevertheless, this calibration idea proves to be effective not only in achieving an excellent static linearity but also in maintaining a state-of-the-art dynamic performance for the DA conversion.

III. PROPOSED SELF-TEST DAC SCHEME

A DAC self-test, self-correction scheme is proposed here, Figure 2, which builds on the ideas presented in [7]. Improvements are mainly implemented in three directions: (1) the self-test engine is realized on-chip and it is simplified to a current comparator (1-bit ADC) (relaxed analog part for extended DSP); (2) the self-calibration mini-DACs are designed bi-directional (area save); (3) the current source and the

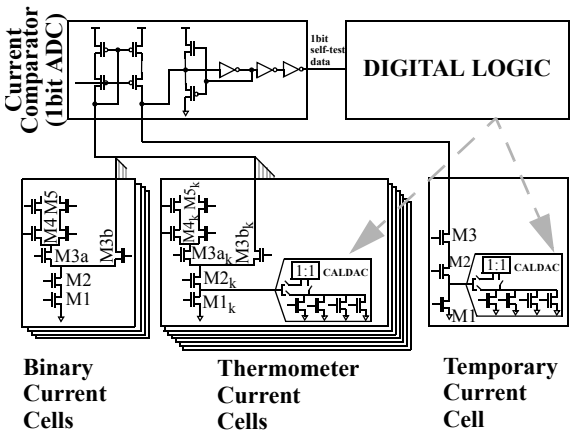

Figure 2: Proposed self-test, self-calibration DAC scheme.

CALDAC are shielded by an extra cascode (reduced non-calibrated errors).

The current sources are implemented with NMOSTs (as opposed to the PMOSTs of [7]), to save area, reduce capacitance, and gain voltage head-room. The latter allows to cascode one more NMOST, $M2_k$, on top of the current source NMOST and the CALDAC. The self-test capability considers *M1, M2, and the CALDAC*, as one single current source. Hence, the errors of *M2* are also inherently corrected and the effect of load mismatch of *M3, M4,* and *M5* is reduced. Furthermore, a single bit ADC (a current comparator, [8]), is used as a measuring device. The comparator, the current source being calibrated, and the digital logic effectively realize an on-chip algorithmic ADC. The current comparison is done in the current domain, which allows higher calibration speeds. Therefore, the presented scheme is enhanced with a continual background capability, which is described later in this article. Furthermore, the mini-CALDACs are bi-directional. A programmable current mirror sets the direction of the calibrating current, which effectively increases the resolution of the CALDAC by 1-bit, without doubling its area! Finally, the binary current sources plus one extra LSB are used as a reference current to calibrate the thermometer current sources. This is why the reference current is called the binary reference in the following text. A simplified block diagram of the self-calibration scheme is shown in Figure 3.

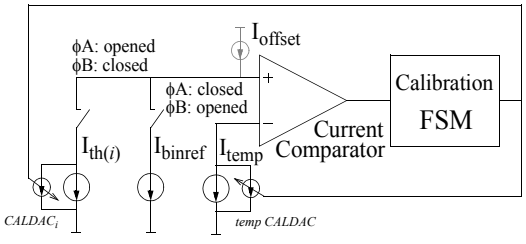

Figure 3: High-level scheme of the proposed calibration algorithm.

All thermometer current sources $I_{th(i)}$ are calibrated to the binary reference I_{binref}. To compensate for the unavoidable input offset of the current comparator I_{offset}, an extra temporary current source I_{temp} is used. The calibration is based on two phases: ϕA and ϕB. During ϕA, I_{temp} is fine-tuned to I_{binref}, so that I_{offset} is inherently also recorded. Therefore, the I_{temp} at the end of ϕA is:

$$\phi A: \quad I_{temp} \approx I_{binref} + I_{offset} \; . \tag{1}$$

The result is stored in the CALDAC of I_{temp}. During ϕB, instead of I_{binref}, the $\boldsymbol{i}^{\text{th}}$ thermometer current source $I_{th(i)}$, is connected to the input of the comparator. The $I_{th(i)}$ is fine-tuned to I_{temp}. Due to the exchanged positions of the currents being calibrated at the comparator's inputs, the recorded I_{offset} in ϕB is the negative counterpart to the one recorded in ϕA. Therefore, $I_{th(i)}$ at the end of ϕB is:

$$\phi B: \quad I_{th(i)} \approx I_{temp} - I_{offset}. \tag{2}$$

Substituting (1) in (2), I_{offset} is cancelled and $I_{th(i)}$ is calibrated to I_{binref}, free of offset.

$$I_{th(i)} \approx I_{binref} + I_{offset} - I_{offset} \approx I_{binref}. \tag{3}$$

The result is stored in the $\boldsymbol{i}^{\text{th}}$ CALDAC and the operation is repeated for the next thermometer current source.

The entire algorithm controlling the self-correction scheme is organized as a FSM with 8-states. It is shown in Figure 4.

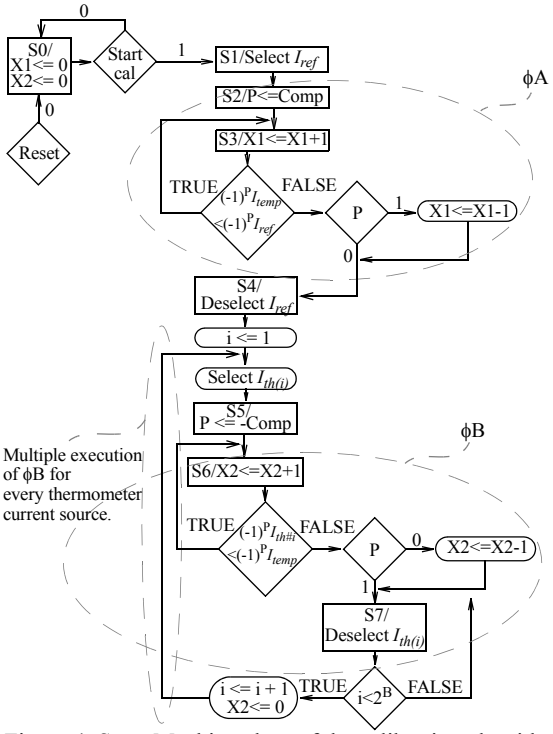

Figure 4: State-Machine chart of the calibration algorithm.

X1 is the register that contains the digital calibrating word for the CALDAC of I_{temp}. X2 is the register that contains the digital calibrating word for the CALDAC of $I_{th(i)}$, during its calibration. I denotes the $i^{\text{-th}}$ thermometer current source. P is the polarity of calibration. If P=1, then calibrating current is subtracted from the coarse thermometer current source; if P=0, then calibrating current is added. B is the level of segmentation.

To minimize the post-calibration spread of currents, the algorithm controls the quantization error I_q with which the currents are calibrated. Thus, I_q is the difference between the fine-tuned current and the reference used, assuming an ideal comparator. In ϕA, I_{temp} is fine-tuned to I_{binref} within a positive I_q, i.e. the post fine-tuned I_{temp} is always greater than I_{binref}, regardless of its pre fine-tuned value. In such a way, the post fine-tuned I_{temp} can be approximated as a stochastical value, with an uniform distribution, a mean value of $\overline{I_{temp}} = I_{binref} + \frac{1}{2} I_{LSBCALDAC}$, and width of $I_{LSBCALDAC}$. On the other hand, in ϕB, the thermometer current sources, $I_{th(i)}$ are fine-tuned to I_{temp} within a negative I_q, i.e. the post fine-tuned $I_{th(i)}$ are always smaller than I_{temp}, regardless of their pre fine-tuned value. In such a way, the post fine-tuned $I_{th(i)}$ can be approximated as a stochastical value, with a uniform distribution, a mean value $\overline{I_{th(i)}} = \overline{I_{temp}} - \frac{1}{2} I_{LSBCALDAC}$, and width of $I_{LSBCALDAC}$.

The stochastical distribution of the post-calibrated values of $I_{th(i)}$ is a product of the uniform probability functions of I_{temp} and $I_{th(i)}$. The resulting probability function for $I_{th(i)}$ can be approximated with a triangular shape, see Figure 5, the spread of which is $\pm I_{LSBCALDAC}$ and the mean value of which is $\overline{I_{th(i)}} = I_{binref}$.

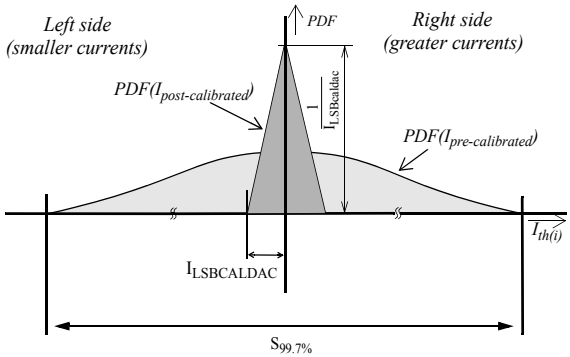

Figure 5: Pre-Calibration and Post-Calibration PDFs.

IV. 12-BIT SELF-CALIBRATED DAC IMPLEMENTATION

The proposed self-calibration scheme is realized in a 12-bit current-steering DAC. To save area, the intrinsic accuracy of the DAC core is designed to 10-bit level with $INL < 2LSB$. This implies approximately 16-times smaller current sources ([9], [10]) can be used. Via calibration of the thermometer current sources, this linearity is improved to 12-bit level. The post-calibration accuracy of the thermometer current sources depends on the LSB step of their CALDAC, $I_{LSBcaldac}$. Their standard deviation, for a PDF as given in Figure 5, can be calculated to be:

$$\sigma_{t_{PC}} = \frac{I_{LSBcaldac}}{\sqrt{6}}, \qquad (4)$$

with PC stands for post calibration, t - thermometer, $\sigma_{t_{PC}}$ is the post-calibrated standard deviation of a thermometer current source. For statistical reference, see [11]. The required post-calibrated relative accuracy of the thermometer current source, given any intrinsic accuracy and targeted linearity (in terms of INL), can be derived to be:

$$\left(\frac{\sigma_t}{I_t}\right) = \sqrt{\frac{INL_{max}^2 - 3^2 2^B \left(\frac{\sigma_u}{I_u}\right)_b^2}{3^2(2^{N-1} - 2^B)2^B}}, \qquad (5)$$

This formula is derived from the generic expression for the INL, found in [10], as a function of the relative matching of the unit-elements. The unit-elements are divided in two groups: those used by the binary current sources (not calibrated) and those used by the thermometer current sources (calibrated). The second group is expressed in (5).

The main specifications for implementation of the presented calibration scheme are summarized in Table 1.

Parameter	Description	Value
N	Resolution	12bit
B	Segmentation	6-6
I_{LSB}	1 LSB current of the DAC core.	5μA
$\left(\frac{\sigma_u}{I_u}\right)_b$	Relative unit-element intrinsic matching (before calibration). Relative unit-element intrinsic matching for the binary current sources, which are not calibrated (after calibration).	1.48%
I_{LSBcal}	1 LSB current of the CALDACs.	257nA

Table 1: Important parameters of the designed converter.

High-level, MATLAB based, statistical simulations of the static linearity of the DAC are shown in Figure 6. The simulations are run for 100 cases. Before calibration, Figure 6 a), the DAC linearity is at a 10-bit level and its INL stays within the 2LSB limits. After calibration, Figure 6 b), the linearity of the DAC is improved to 12-bit level and its INL does not exceed the 0.5LSB limits.

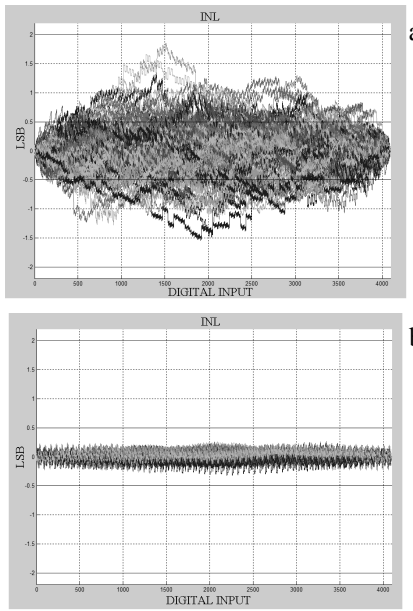

Figure 6: INL for 100 DAC samples: a) pre-calibration (intrinsic); b) post-calibration INL.

The layout of the 12-bit self-calibrated DAC is shown in Figure 7. The chip is realized in a standard 0.25μm CMOS process. The dimensions of the chip core are $1.2mm \times 1.2mm$. The array of current sources (NMOST *M1*) is indicated with ①. The array of CALDACs is twice bigger and is marked with ②. The array of the cascoded transistors (NMOSTs *M2,*

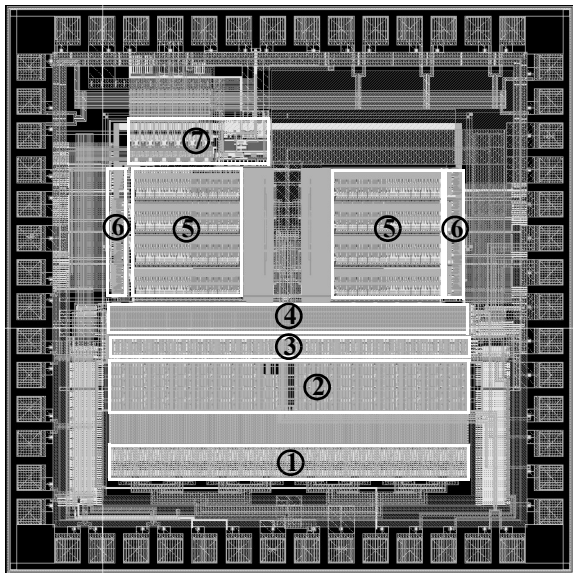

Figure 7: Layout of the 12-bit self-calibrated DAC.

M3a, and *M3b*) are indicated with ③. The digital logic and the current comparator are stacked above this, marked with ④. The data flip-flops and the current switches (NMOSTs *M4* and *M5*) are positioned symmetrically to the output, indicated with ⑤. The binary-to-thermometer decoder is also laid out symmetrically to the output, marked with ⑥. The data and clock buffers are shown with ⑦.

V. FURTHER ENHANCEMENTS

The above proposed self-calibrating scheme belongs to the group of the start-up calibrations. That is why it cannot account for slow varying errors, which might appear during the normal DA conversion. In addition, the results of the calibration have to be stored in CMOS memory elements, which may occupy more than the half of the silicon area of the array of CALDACs. Therefore, the variation of the presented scheme that employs background calibration might be of interest for some applications. It is shown in Figure 8.

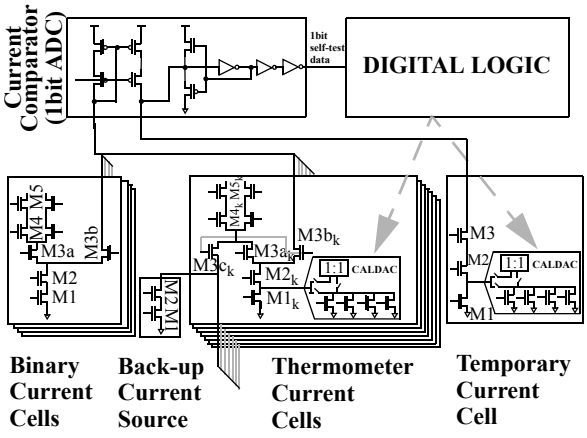

Figure 8: Background calibration variation of the proposed self-test/self-calibration DAC scheme.

A single back-up current source is added to the scheme. Another NMOST, $M3c_k$, is added to the common-source point of the current switches in the thermometer current cell. It is controlled by the signal controlling $M3b_k$, so that when the thermometer cell is selected for calibration, the back-up current source provides current for the current switches, $M4_k$. In such a way, ϕA of the calibration algorithm can be executed once with chip start-up and ϕB can be run continually in background. Therefore, the memory elements of the thermometer CALDACs can be designed as simple capacitors, the discharge of which is relaxed, as they are used in the digital domain.

VI. CONCLUSION

The proposed self-test self-correction scheme is a self-contained, monolithic solution, designed for start-up calibration. It targets the thermometer current sources of a segmented CS DAC. Its self-test algorithm is based on a single bit ADC (a current comparator). The scheme is implemented in order to create a 12-bit DAC using a 10-bit core. It occupies about an order of magnitude less area than a 12-bit intrinsic DAC because of the relaxed matching requirements of the coarse current source transistors. Furthermore, the components used for calibration do not require high accuracy. All major first-order problems are compensated at an algorithmic level. A variation of the self-calibration scheme is proposed that continually corrects the thermometer current sources and may significantly reduce the silicon area of the calibration part of the chips.

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