A 96 % efficient high-frequency DC-DC converter using E-mode GaN DHFETs on Si


Published in:
IEEE Electron Device Letters

DOI:
10.1109/LED.2011.2162393

Published: 01/01/2011

Document Version
Publisher’s PDF, also known as Version of Record (includes final page, issue and volume numbers)

Please check the document version of this publication:
• A submitted manuscript is the author’s version of the article upon submission and before peer-review. There can be important differences between the submitted version and the official published version of record. People interested in the research are advised to contact the author for the final version of the publication, or visit the DOI to the publisher’s website.
• The final author version and the galley proof are versions of the publication after peer review.
• The final published version features the final layout of the paper including the volume, issue and page numbers.

Link to publication

Citation for published version (APA):

General rights
Copyright and moral rights for the publications made accessible in the public portal are retained by the authors and/or other copyright owners and it is a condition of accessing publications that users recognise and abide by the legal requirements associated with these rights.

• Users may download and print one copy of any publication from the public portal for the purpose of private study or research.
• You may not further distribute the material or use it for any profit-making activity or commercial gain
• You may freely distribute the URL identifying the publication in the public portal

Take down policy
If you believe that this document breaches copyright please contact us providing details, and we will remove access to the work immediately and investigate your claim.
A 96% Efficient High-Frequency DC–DC Converter Using E-Mode GaN DHFETs on Si
Jo Das, Member, IEEE, Jordi Everts, Member, IEEE, Jeroen Van Den Keybus, Marleen Van Hove, Domenica Visalli, Puneet Srivastava, Student Member, IEEE, Denis Marcon, Student Member, IEEE, Kai Cheng, Maarten Leys, Stefaan Decoutere, Johan Driesen, and Gustaaf Borghs

Abstract—III-Nitride materials are very promising to be used in next-generation high-frequency power switching applications. In this letter, we demonstrate the performance of normally off AlGaN/GaN/AlGaN double-heterostructure FETs (DHFETs) using a boost-converter circuit. The figures of merit of our large (57.6-mm gate width) GaN transistor are presented: $R_{ON} \cdot Q_G$ of 2.5 $\Omega \cdot nC$ is obtained at $V_{DS} = 140$ V. The switching performance of the GaN DHFET is studied in a dedicated high-frequency boost converter: both the switching times and power losses are characterized. We show converter efficiency values up to 96.1% at 500 kHz and 93.9% at 850 kHz at output power of 100 W.

Index Terms—Converters, efficiency, GaN, high voltage, power field-effect transistors (FETs), SPICE.

I. INTRODUCTION

F

OR power switching applications, there is a trend to increase the switching frequency in order to reduce the size of the converter design. In this perspective, GaN-based materials have attracted a lot of attention because of their outstanding properties such as high power density and high breakdown voltage [1], [2]. Moreover, it has been shown that these heterostructures can be grown on large-diameter Si substrates [3], which is of course a major cost advantage.

For switching applications, enhancement-mode (E-mode) devices are usually preferred. Different concepts have been proposed in the literature [4]–[6] to convert the GaN device from the conventional depletion mode (D-mode) to E-mode.

We have recently shown that E-mode operation can be obtained by selective removal of the in situ grown passivation layer under the gate [7]. We will show the potential of this approach for high-frequency power conversion applications. In the literature, some demonstrations of GaN-based devices in converter circuits have been already shown. An efficiency value of 97.8% for D-mode devices on SiC has been demonstrated [2]. For E-mode devices, recently, efficiency values of 96% at 200 kHz have been presented [8].

In this letter, we discuss the results of a boost converter with a compact design for a frequency range between 300 kHz and 1 MHz. High efficiency values at high switching frequencies are demonstrated, proving the high potential of the GaN technology.

II. DEVICE FABRICATION AND CHARACTERIZATION

The GaN devices are fabricated starting from a $\text{Si}_3\text{N}_4/\text{Al}_{0.45}\text{Ga}_{0.55}\text{N/GaN/Al}_{0.18}\text{Ga}_{0.82}\text{N}$ metal–organic vapor-deposition-grown heterostructure on a 100-mm Si(111) substrate ($\rho > 5000 \, \Omega \cdot \text{cm}$) [9]. The III-nitride heterostructure is capped with a 50-nm in situ-grown $\text{Si}_3\text{N}_4$ layer in order to passivate the surface and prevent strain relaxation of the $\text{Al}_{0.45}\text{Ga}_{0.55}\text{N}$ layer [10]. To process the layers into devices, the following steps are executed: device isolation, ohmic contact formation, gate fabrication, $\text{Si}_3\text{N}_4$ passivation, and deposition of an interconnection layer.

The III-nitride heterostructure is designed in such a way that E-mode devices are obtained: by scaling down the $\text{Al}_{0.45}\text{Ga}_{0.55}\text{N}$ top-layer thickness below 5 nm, and by selectively removing the in situ $\text{Si}_3\text{N}_4$ layer under the gate, positive threshold voltages can be obtained [7]. In this letter, we have used a 4-nm-thick $\text{Al}_{0.45}\text{Ga}_{0.55}\text{N}$ top barrier layer. The GaN channel layer and $\text{Al}_{0.18}\text{Ga}_{0.82}\text{N}$ buffer layer thickness are 150 nm and 1 $\mu$m, respectively.

On-wafer transfer characteristic measurements are done on small devices, with total gate width $W_G = 200 \, \mu$m and gate length $L_G = 1.5 \, \mu$m. From these measurements, threshold voltage $V_T = 0.15$ V, on-resistance $R_{ON} = 12 \, \Omega \cdot \text{mm}$, and maximum saturation current $I_{DS} = 0.4 \, \text{A/mm}$ are extracted. The off-state breakdown voltage (measured at gate voltage $V_{GS} = 0$ V) depends on gate–drain gap $L_{GD}$ and the buffer thickness [11]. For $L_{GD} = 8 \, \mu$m, we obtained $V_{BD}$ as high as 550 V, where $V_{BD}$ is defined as the drain voltage at which the leakage current $I_{DS}$ increases to 1 mA/mm. Note that, although the average $V_{BD}$ measured on small test devices is 550 V, we will limit the operating voltage of the final GaN switching device in the converter setup to 200 V in order to avoid any possible device degradation during operation.
III. BOOST CONVERTER: DESIGN AND REALIZATION

To show the potential of the GaN double-heterostructure FET (DHFET) devices for high-frequency power switching applications, a high-frequency hard-switching boost converter is constructed, as this is often used, e.g., for power factor correction. Starting from the dc and $C-V$ characterization of the devices, a SPICE model for the GaN DHFETs was made prior to the converter design. We have already shown before that the model is scalable to large gate-width GaN devices [12]. For this letter, GaN DHFETs with total gate width $W_G = 57.6$ mm are used. To integrate these GaN DHFETs into the boost converter circuit, the dies are packaged onto an AlN carrier acting as a heat spreader. Mounting is done using a 25-μm-thick AuSn preform layer in order to obtain an excellent heat transfer between the GaN die and the carrier. Furthermore, AlN is mounted in a next step on an additional Cu heat sink.

The schematic of the circuit is shown in Fig. 1. A SiC diode (Cree C3D04060, 600 V, 4 A) is used because of its very low recovery current. The converter has a custom-made gate driver circuit [13], which can deliver drive signals up to 6 MHz. The voltage range of the gate driver is adjustable, making it possible to deliver negative voltages. This way, both D-mode (normally on) and E-mode (normally off) devices can be used in the setup. Finally, special attention was paid to the compactness of the converter. Therefore, an ultracompact planar inductor ($L = 33.9$ μH) was developed in-house, with a volume of only 19.2 cm$^3$. However, a disadvantage of the small inductance is the bigger hysteresis loss per cycle.

IV. CONVERTER RESULTS

Using the boost converter setup, the dynamic on-resistance $R_{ON-DYN}$ and gate charge values $Q_G$ of the GaN transistor are measured [13]. $R_{ON-DYN}$ is calculated as $V_{DS}/I_{DS}$ during the on-state of the transistor in the boost converter. $R_{ON-DYN}$ = 0.23 Ω and only shows a minor increase with increasing off-state drain voltage $V_{DS, OFF}$, proving the absence of surface or bulk electron trapping in the device. $Q_G$ is determined by integrating the gate drive current during the turn-on switching of the transistor. From these measurements, a total gate charge value of 11 nC is obtained at $V_{DS, OFF} = 140$ V, resulting in $R_{ON} \ast Q_G$ as low as 2.5 Ω nC for the E-mode GaN DHFET. This value is comparable with commercial Si-based 200-V-rated MOS transistors but significantly higher compared with commercial devices from EPC [14]. The $Q_G$ value of our GaN devices, which is still relatively high due to the very thin top AlGaN layer, could still be improved by scaling down the gate length to submicrometer dimensions.

Fig. 2 shows the switching behavior of the E-mode GaN DHFET. We can see that the measured rise and fall time values are in close agreement with the SPICE simulations. Note that the gate was switched between 2 and −8 V, whereas the output voltage of the converter was at 140 V. The two reasons for the negative gate voltage are to obtain a faster turnoff of the device and to avoid unintended switching imposed by disturbances. For the turn-on, the maximum gate voltage is limited to 2 V to avoid an excessive current in the Schottky gate diode. As a result, the fall time $t_{FALL}$ = 20 ns of the drain voltage is much higher than the rise time $t_{RISE}$ = 5 ns. To reduce the fall time, the maximum allowable gate voltage should be increased beyond 2 V. Therefore, it would be an advantage to replace the Schottky gate by a MOS gate so that a larger positive gate swing can be obtained.

In a next step, the boost converter efficiency was measured as a function of the switching frequency and output power (see Fig. 3). Duty cycle $D$ was kept constant at 50%. The highest efficiency values were obtained at $P_{OUT} = 100$ W; at 500 and 850 kHz, efficiency values as high as 96.1% and 93.9%, respectively, are obtained. Note that the efficiency (at constant $P_{OUT}$) slightly depends on $V_{OUT}$ (and, thus, also on $I_{OUT}$). This is mainly because the conduction losses are higher at higher output currents. To the best of our knowledge, this is the highest efficiency reported for E-mode GaN DHFETs on Si substrates at these high switching frequencies. It clearly shows the high potential of GaN-on-Si devices for high-frequency power switching applications compared with commercial Si-based MOSFET devices [15], [16].

To have a better understanding of the efficiency limitations in the converter, we analyzed the power losses in the converter.
inductor and interconnection losses), which are around 2 W at measurement.

We can also estimate the parasitic losses (e.g., in the figure. By a comparison of the SPICE simulation and 3% of the total losses, and therefore, they are not included in the figure. Using SPICE simulations. Fig. 4(a) shows the losses of the SiC diode and the GaN DHFET as a function of the switching frequency. It is clear that, at high switching frequencies, the GaN DHFET losses are dominated by the switch-on losses because of the relatively high fall time of the drain-to-source voltage. Note that the losses of the gate driver are less than 3% of the total losses, and therefore, they are not included in the figure. By a comparison of the SPICE simulation and measurements, we can also estimate the parasitic losses (e.g., inductor and interconnection losses), which are around 2 W at

Using SPICE simulations. Fig. 4(a) shows the losses of the SiC diode and the GaN DHFET as a function of the switching frequency. It is clear that, at high switching frequencies, the GaN DHFET losses are dominated by the switch-on losses because of the relatively high fall time of the drain-to-source voltage. Note that the losses of the gate driver are less than 3% of the total losses, and therefore, they are not included in the figure. By a comparison of the SPICE simulation and measurements, we can also estimate the parasitic losses (e.g., inductor and interconnection losses), which are around 2 W at $P_{\text{OUT}} = 100$ W and $V_{\text{OUT}} = 140$ V are constant.

Simulating $P_{\text{GAN-ON}}$ and $P_{\text{SiC-Diode}}$ at different $P_{\text{OUT}}$ as a function of $D$, $V_{\text{OUT}} = 140$ V and $f = 500$ kHz are kept constant.

Using SPICE simulations. Fig. 4(a) shows the losses of the SiC diode and the GaN DHFET as a function of the switching frequency. It is clear that, at high switching frequencies, the GaN DHFET losses are dominated by the switch-on losses because of the relatively high fall time of the drain-to-source voltage. Note that the losses of the gate driver are less than 3% of the total losses, and therefore, they are not included in the figure. By a comparison of the SPICE simulation and measurements, we can also estimate the parasitic losses (e.g., inductor and interconnection losses), which are around 2 W at $P_{\text{OUT}} = 100$ W and $f = 500$ kHz. Fig. 4(b) shows the diode and DHFET losses for different duty cycles and different $P_{\text{OUT}}$.

From this figure, it is clear that the DHFET losses are dominant at higher duty cycles because of the higher DHFET conduction losses at these conditions.

V. Conclusion

A 100-W compact boost converter has been designed for a frequency range up to 1 MHz using a GaN-on-Si E-mode device and a SiC diode. Low switching times ($t_{\text{rise}} = 5$ ns and $t_{\text{fall}} = 20$ ns) and $R_{\text{on}} \times Q_{\text{g}} = 2.5 \, \text{Ω} \, \text{nC}$ at $V_{\text{DS}} = 140$ V are demonstrated. Moreover, high conversion efficiency values of 96.1% and 93.9% are obtained at switching frequencies of 500 and 850 kHz, respectively, showing the high performance of the E-mode GaN-on-Si DHFETs.

Acknowledgment

The authors would like to thank B. Sijm for wafer growth; E. Vandenplas, J. Viaene, and K. Geens for wafer processing; and X. Kang for measurement assistance.

References


