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Mode transition timing and energy overhead analysis in noise-aware MTCMOS circuits

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\textbf{A B S T R A C T}

Multi-threshold CMOS (MTCMOS) is commonly utilized for suppressing leakage currents in idle integrated circuits. The deactivation/reactivation energy consumption however degrades the effectiveness of the MTCMOS technique for providing significant savings in total energy consumption in CMOS integrated circuits. The sources of mode transition energy consumption in noise-aware MTCMOS circuits are investigated in this paper. The mode transition energy overheads of various recently published low-noise ground-gated MTCMOS circuits are characterized. With a digital triple-phase sleep signal slew rate modulated MTCMOS circuit, the overall mode transition energy consumption is reduced by up to 45.31\% as compared to the other MTCMOS circuits that are evaluated in this paper in a UMC 80 nm CMOS technology. Furthermore, digital triple-phase sleep signal slew rate modulation shortens the mode transition overhead by up to 65.26\% as compared with the other MTCMOS noise suppression techniques that are evaluated in this paper.

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1. Introduction

With CMOS technology scaling, leakage currents have become important sources of power consumption in nanoscale integrated circuits [1–16]. Power/ground gating with a multi-threshold CMOS (MTCMOS) technology is the most widely used leakage power suppression technique in idle integrated circuits [1–12,15,16]. In an MTCMOS circuit, high threshold voltage (high-$V_{th}$) sleep transistors (header and/or footer) are used to cut off the power supply and/or the ground connections to an idle low threshold voltage (low-$V_{th}$) circuit block. A ground-gated MTCMOS circuit is shown in Fig. 1. An MTCMOS circuit consumes significant energy during transitions from ACTIVE mode to SLEEP mode and from SLEEP mode to ACTIVE mode. Lower energy consumption during mode transitions is critically important to achieve higher energy efficiency in MTCMOS circuits.

With the increasing number of autonomous power/ground gating domains that are employed for more effective suppression of leakage currents in each new CMOS technology generation, reactivation noise (power and ground bouncing noise) that is produced by awakening MTCMOS circuit blocks has become an important reliability concern in modern integrated circuits [4–6]. Novel MTCMOS circuits with lower deactivation/reactivation energy consumption and suppressed noise are therefore highly desirable.

A variety of MTCMOS circuit techniques that employ sleep signal slew rate modulation for reactivation noise suppression are proposed in recently published papers [6–8]. The energy and timing overheads that are associated with these noise-aware MTCMOS circuit techniques are however overlooked in these publications. In this paper, mode transition energy consumption in noise-aware MTCMOS circuits is evaluated in detail. The breakeven idle intervals and mode transition timing overheads for achieving net energy savings are identified with different low-noise MTCMOS circuits. With a digital triple-phase sleep signal slew rate modulation technique, the total mode transition energy consumption, breakeven idle interval, and overall mode transition timing overhead are reduced by up to 45.31\%, 60\%, and 65.26\%, respectively, as compared to the other noise-aware MTCMOS circuits that are evaluated in this paper.

This paper is organized as follows. The sources of deactivation/reactivation energy consumption in MTCMOS circuits are investigated in Section 2. Different noise-aware MTCMOS circuit techniques are described in Section 3. The mode transition energy consumption, breakeven idle intervals, and mode transition timing overheads of noise-aware MTCMOS circuits are evaluated under an equal-noise constraint in Section 4. The paper is summarized in Section 5.
2. Deactivation/reactivation energy consumption in MTCMOS circuits

MTCMOS is effective in suppressing the leakage currents that are produced by an idle circuit. However, additional energy is consumed by an MTCMOS circuit during transitions from ACTIVE mode to SLEEP mode (deactivation process) and from SLEEP mode to ACTIVE mode (reactivation process) [6,7,9–13]. Lower mode transition energy consumption enables an MTCMOS circuit to transition to low-leakage SLEEP mode more frequently, thereby allowing more significant savings in total energy consumption [9–13]. MTCMOS circuit techniques with lower mode transition energy consumption and suppressed SLEEP mode leakage currents are therefore highly desirable. The sources of energy consumption during mode transitions in an MTCMOS circuit are identified in this section.

The voltage waveforms of the sleep signals (Sleep_Global and Sleep_Local) and the virtual ground line of a ground-gated MTCMOS circuit are shown in Fig. 2. The global sleep signal (Sleep_Global) transitions low to initiate a deactivation event. The leakage currents that are produced by the MTCMOS circuit are suppressed in the SLEEP mode. Additional dynamic switching energy is however consumed by the MTCMOS circuit to transition to the SLEEP mode. While turning off the sleep transistor, dynamic switching energy (ED_Sleep_Generator) is consumed (from T1 to T2) by the sleep signal generator. Additional switching energy (ED_VGND + ED_Internal_Nodes) is consumed (from T2 to T3) as the virtual ground line and the internal nodes of low-Vth circuit block are charged towards VDD in the SLEEP mode. The leakage energy (ED_Leakage) that is consumed by the sleep signal generator and the MTCMOS circuit during the deactivation delay (T1 to T2) also contributes to the deactivation energy consumption. The overall deactivation energy consumption overhead (EDeactivation) is

\[
E_{Deactivation} = E_{D_{Sleep\,Generator}} + E_{D_{Internal\,Nodes}} + E_{D_{VGND}} + E_{D_{Leakage}}.
\]

At the end of SLEEP mode, Sleep_Global transitions high to initiate a reactivation event. Energy (ER_Sleep_Generator) is consumed (from T4 to T5) by the sleep signal generator while turning on the sleep transistor during a reactivation event. The internal nodes of low-Vth circuit block transition to correct logic states stage by stage depending on the input vectors that are applied to the MTCMOS circuit. Energy (ER_Switching + ER_Short_Circuit) is consumed (from T5 to T6) due to the switching and short circuit currents that are produced by the low-Vth circuit block during a reactivation event [4–7]. The leakage energy (ED_Leakage) consumed by the sleep signal generator and the MTCMOS circuit during the reactivation delay (T4 to T5) also contributes to the reactivation energy consumption. The overall reactivation energy consumption overhead (EReactivation) is

\[
E_{Reactivation} = E_{R_{Sleep\,Generator}} + E_{R_{Switching}} + E_{R_{Short\,Circuit}} + E_{R_{Leakage}}.
\]

The breakeven point of energy consumption is achieved when the leakage energy savings in idle mode is equal to the total mode transition energy consumption due to the deactivation and reactivation events as given in the following equation:

\[
P_{Active\,Leakage}(T4 - T2) + \int_{T2}^{T4} P_{Leakage}(t) dt = E_{Deactivation} + E_{Reactivation}.
\]

\[
P_{Active\,Leakage} = \text{the leakage power consumed by the sleep signal generator and the MTCMOS circuit when the low-leakage SLEEP mode is exercised (sleep transistor is cut off).}
\]

The breakeven point energy consumption is assumed to be achieved after the virtual ground line is charged to the steady-state voltage Vstable in the SLEEP mode. Under this scenario, the virtual ground line is discharged from Vstable to ~0 V during a reactivation event. Depending on the actual MTCMOS circuit, however, the breakeven point of energy consumption can be achieved before the virtual ground line is charged to Vstable in the SLEEP mode, as shown in Fig. 3. Under this scenario, the virtual ground line can be discharged either from Vstable or from a voltage level lower than Vstable towards ~0 V during a reactivation event, as shown in Fig. 3.
transitions from 0 V to an intermediate voltage level \( V_X \) (0 V < \( V_X < V_{DD} \)) during the first step of a reactivation event. The sleep signal is maintained at \( V_X \) until the virtual ground line is discharged to a sufficiently low voltage level. The sleep signal is subsequently raised from \( V_X \) to \( V_{DD} \) during the second step of reactivation. The reactivation noise is suppressed due to the weaker conductivity of the sleep transistor and the lower voltage swing on the virtual ground line during the first and the second, respectively, wake up steps [8].

A sleep signal modulator for stepwise \( V_{gs} \) MTCMOS circuit is proposed in [8]. The output signal of the stepwise \( V_{gs} \) sleep signal modulator, Sleep_Local (that is connected to the gate terminal of the sleep transistor) with the stepwise \( V_{gs} \) MTCMOS circuit. Furthermore, significant short circuit currents are produced by the stepwise \( V_{gs} \) sleep signal generator during mode transitions [7]. The stepwise \( V_{gs} \) MTCMOS circuit therefore suffers from high energy consumption during mode transitions.

### 3.3. Triple-phase sleep signal slew rate modulation

A triple-phase sleep signal slew rate modulation (TPS) technique is presented in [6] to suppress the reactivation noise while accelerating the reactivation process in MTCMOS circuits. The concept of triple-phase sleep signal slew rate modulation is shown in Fig. 5. The sleep signal rises fast from 0 V to the threshold voltage of sleep transistor to reduce the reactivation delay without producing significant noise during Phase_1 [6,7]. The sleep signal is subsequently decelerated to suppress the noise waveform in Phase_2 where the peak reactivation noise is produced. After the virtual ground line voltage is reduced to a very low level close to 0 V, the rise of sleep signal is accelerated again to shorten the remaining duration of reactivation process in Phase_3.

A fully digital triple-phase sleep signal slew rate modulator is proposed in [6] to produce the triple-phase sleep signal that is shown in Fig. 5. With the triple-phase sleep signal modulator [6,7], the rising speed of sleep signal is adjusted by monitoring the
4. Evaluation of low-noise MTCMOS circuits

A ground-gated 32-bit Brent-Kung adder is designed with the UMC 80 nm multi threshold voltage CMOS technology (high-\(I_{th_{\text{NMOS}}}=+370 \text{ mV}, \text{low-}I_{th_{\text{NMOS}}}=+155 \text{ mV}, \text{high-}I_{th_{\text{PMOS}}}=\text{–}310 \text{ mV}, \text{low-}I_{th_{\text{PMOS}}}=\text{–}105 \text{ mV}, \text{and } V_{DD}=1 \text{ V}) [17] to evaluate the mode transition phenomenon with different sleep signal slew rate modulation techniques in this section. The sleep transistor is sized 5 \(\mu\text{m}\) to achieve similar (within 5%) delay along the critical signal propagation path (in ACTIVE mode) of MTCMOS circuit as compared to the standard purely low-\(I_{th}\) circuit. The mode transition noise is characterized with the parasitic impedance (composed of two-stage inverters), stepwise sleep signal modulator (TPS-Digital). The sleep signal waveforms are tuned to suppress the peak ground bouncing noise to a significantly suppressed as compared to the stepwise \(V_{gs}\) sleep signal modulator [6,7]. Both the breakeven idle interval and the overall mode transition timing overhead of an MTCMOS circuit are thereby shortened with the digital triple-phase sleep signal modulator as compared to the single-phase and stepwise \(V_{gs}\) sleep signal modulators.

### Table 1

<table>
<thead>
<tr>
<th>Mode transition related design metrics of different sleep signal slew rate modulated MTCMOS circuits</th>
<th>90 °C</th>
<th>25 °C</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Circuit Technique</strong></td>
<td><strong>Single-Phase</strong></td>
<td><strong>Stepwise (V_{gs})</strong></td>
</tr>
<tr>
<td><strong>Peak Ground Noise (mV)</strong></td>
<td>2.090</td>
<td>2.337</td>
</tr>
<tr>
<td>(T_{R_{\text{MAX}}}) (ns)</td>
<td>44.12</td>
<td>12.15</td>
</tr>
<tr>
<td>(T_{R_{\text{MAX}}}) (ns)</td>
<td>42.20</td>
<td>12.12</td>
</tr>
<tr>
<td>(T_{\text{D}}) (ns)</td>
<td>1.25</td>
<td>11.0</td>
</tr>
<tr>
<td>(E_{\text{PEK}}) (pJ)</td>
<td>1.972</td>
<td>1.02</td>
</tr>
<tr>
<td>(E_{\text{PEK}}) (pJ)</td>
<td>1.628</td>
<td>0.720</td>
</tr>
<tr>
<td>(E_{\text{PEK}}) (pJ)</td>
<td>0.034</td>
<td>0.530</td>
</tr>
<tr>
<td>Steady-State SLEEP Power (nW)</td>
<td>70.0</td>
<td>87.2</td>
</tr>
<tr>
<td>Breakeven Idle Interval (number of clock cycles)</td>
<td>50</td>
<td>38</td>
</tr>
<tr>
<td>(T_{\text{Overhead}}) (number of clock cycles)</td>
<td>95</td>
<td>63</td>
</tr>
</tbody>
</table>

With suppressed deactivation and reactivation energy consumption, the TPS-Digital MTCMOS circuit achieves the lowest overall mode transition energy consumption (reactivation energy...
consumption + deactivation energy consumption) as shown in Fig. 6. The TPS-Digital MTCMOS circuit suppresses the overall mode transition energy consumption by 45.31% (35.28%) and 29.27% (11.95%) as compared to the single-phase and stepwise $V_{gs}$ MTCMOS circuits, respectively, at 90°C (25°C). TPS-Digital MTCMOS circuit thereby provides the highest energy efficiency during mode transitions in an MTCMOS circuit.

The single-phase MTCMOS circuit consumes the lowest steady-state SLEEP mode leakage power due to the simplest and smallest sleep signal modulator among the MTCMOS circuits that are evaluated in this paper. The single-phase MTCMOS circuit reduces the steady-state SLEEP mode leakage power consumption by up to 14.77% and 10.09% as compared to the stepwise $V_{gs}$ and TPS-Digital MTCMOS circuits, respectively, as listed in Table I.

The duration of idle mode of an MTCMOS circuit has to be longer than the overall mode transition timing overhead ($T_{overhead}$: sum of deactivation delay, reactivation delay, and break-even idle interval) for providing net energy savings in the SLEEP mode, thereby justifying the transition to low-leakage SLEEP mode. The breakeven idle interval and overall mode transition timing overhead associated with different MTCMOS circuits are evaluated next. The operating frequency of adders is assumed to be 1 GHz.

Assuming an extreme case where the number of idle clock cycles from the end of deactivation to the beginning of reactivation ($T_{22} \approx T_{D} \approx 0$), the overall energy consumption of an MTCMOS circuit with a cut-off sleep transistor is the sum of reactivation and deactivation energy consumptions (with the virtual ground line voltage maintained close to 0 V). Alternatively, in more practical scenarios where the duration of SLEEP mode is nonzero ($T_{D} \approx 0$), the cumulative energy consumption of an MTCMOS circuit with a cut-off sleep transistor increases with the number of idle clock cycles due to the leakage power consumed by the low-$V_{th}$ adder and the dynamic power consumed as the virtual ground line and the internal nodes of the low-$V_{th}$ adder are charged towards $V_{DD}$. The energy consumed by an idle MTCMOS circuit where the low-leakage sleep mode is not exercised (sleep transistor is maintained on) increases faster with increased number of idle clock cycles as compared to an MTCMOS circuit where the low-leakage sleep mode is exercised (sleep transistor is cut off) as shown in Fig. 7. All the MTCMOS circuits that are evaluated in this paper achieve the breakeven point of energy consumption before the virtual ground line is charged to the steady-state voltage in SLEEP mode. For the single-phase MTCMOS circuit, at least 50 idle clock cycles are required for the accumulated leakage energy savings to exceed the mode transition energy overhead at 90°C, as shown in Fig. 7(a). Alternatively, only 20 idle clock cycles are required to achieve net savings in energy consumption with the TPS-Digital MTCMOS circuit at 90°C.

The effectiveness of ground gating for leakage power savings is degraded at lower temperature [4,5]. The breakeven idle intervals with all three MTCMOS circuits are therefore elongated at 25°C, as shown in Fig. 7(b).

TPS-Digital MTCMOS circuit achieves the shortest breakeven idle interval due to the lowest mode transition energy consumption among the MTCMOS circuits that are evaluated in this paper, as shown in Fig. 8. Alternatively, the stepwise $V_{gs}$ and single-phase MTCMOS circuits require the longest breakeven idle interval at 25°C and 90°C, respectively. The TPS-Digital MTCMOS circuit shortens the breakeven idle interval by 60% (47.37%) and 47.37% (35.48%) as compared to the single-phase and stepwise $V_{gs}$ MTCMOS circuits, respectively, at 90°C (25°C).

The TPS-Digital sleep signal modulator monitors the virtual ground line voltage during a reactivation event, thereby...
dynamically adjusting the rising speed of sleep signal. When a reactivation event is initiated immediately after the breakeven point of energy consumption is achieved, the virtual ground line voltage of the TPS-Digital MTCMOS circuit is lower than the steady-state SLEEP mode voltage. The TPS-Digital sleep signal modulator thereby transitions to Phase_3 (where the sleep signal is accelerated) earlier as compared to the scenario where the virtual ground line is discharged from ~V_{DS} during a reactivation event. Alternatively, the single-phase and stepwise V_{GS} sleep signal modulators cannot track the voltage of virtual ground line. The TPS-Digital MTCMOS circuit therefore provides the shortest reactivation delay ($R_{BE}$: the reactivation delay that is measured by assuming a reactivation event is initiated immediately after the breakeven point of energy consumption is achieved as shown in Fig. 3(b)) among the MTCMOS circuits that are evaluated in this paper, as shown in Table 1. The TPS-Digital MTCMOS circuit reduces $R_{BE}$ by up to 76.69% and 40.43% as compared to the single-phase and stepwise $V_{GS}$ MTCMOS circuits, respectively. Furthermore, the TPS-Digital MTCMOS circuit consumes the lowest reactivation energy ($E_{RBE}$: the energy that is consumed by an MTCMOS circuit and the sleep signal modulator during $R_{BE}$). $E_{RBE}$ is reduced by up to 67.2% and 36.46% with the TPS-Digital MTCMOS circuit as compared to the single-phase and stepwise $V_{GS}$ MTCMOS circuits, respectively.

The TPS-Digital MTCMOS circuit achieves the shortest overall mode transition timing overhead. Alternatively, the single-phase and stepwise $V_{GS}$ circuits suffer from the longest overall mode transition timing overhead at 90°C and 25°C, respectively. The TPS-Digital MTCMOS circuit shortens the overall mode transition timing overhead by 65.26% (50.5%) and 47.62% (48.98%) as compared with the single-phase and stepwise $V_{GS}$ MTCMOS circuits, respectively, at 90°C (25°C) as shown in Fig. 9. TPS-Digital MTCMOS circuit allows more frequent transitions to the low-leakage SLEEP mode due to the reduced overall mode transition timing and energy overheads. Digital triple-phase sleep signal slew rate modulation thereby provides more significant savings in overall energy consumption as compared to the other MTCMOS circuits that are evaluated in this paper.

5. Conclusions

The sources of mode transition energy consumption with noise-aware MTCMOS circuits are identified in this paper. The deactivation/reactivation energy consumptions of various recently published low-noise MTCMOS circuit techniques are evaluated. The breakeven idle intervals and mode transition timing overheads with different MTCMOS circuits are investigated. A digital triple-phase sleep signal slew rate modulated MTCMOS circuit suppresses the overall mode transition energy consumption by up to 45.31% as compared to the other noise-aware MTCMOS circuits that are evaluated in this paper in a UMC 80 nm CMOS technology. Furthermore, the digital triple-phase MTCMOS circuit reduces the breakeven idle interval and the overall mode transition timing overhead by up to 60% and 65.26%, respectively, as compared with the other low-noise MTCMOS circuits that are evaluated in this paper. Digital triple-phase sleep signal slew rate modulation is therefore recommended as the most energy efficient technique for achieving fast mode transitions with negligible reactivation noise in MTCMOS circuits.

References


