Mode transition timing and energy overhead analysis in noise-aware MTCMOS circuits

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Mode transition timing and energy overhead analysis in noise-aware MTCMOS circuits

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ABSTRACT

Multi-threshold CMOS (MTCMOS) is commonly utilized for suppressing leakage currents in idle integrated circuits. The deactivation/reactivation energy consumption however degrades the effectiveness of the MTCMOS technique for providing significant savings in total energy consumption in CMOS integrated circuits. The sources of mode transition energy consumption in noise-aware MTCMOS circuits are investigated in this paper. The mode transition energy overheads of various recently published low-noise ground-gated MTCMOS circuits are characterized. With a digital triple-phase sleep signal slew rate modulated MTCMOS circuit, the overall mode transition energy consumption is reduced by up to 45.31% as compared to the other MTCMOS circuits that are evaluated in this paper in a UMC 80 nm CMOS technology. Furthermore, digital triple-phase sleep signal slew rate modulation shortens the mode transition timing overhead by up to 65.26% as compared with the other MTCMOS noise suppression techniques that are evaluated in this paper.

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1. Introduction

With CMOS technology scaling, leakage currents have become important sources of power consumption in nanoscale integrated circuits [1–16]. Power/ground gating with a multi-threshold CMOS (MTCMOS) technology is the most widely used leakage power suppression technique in idle integrated circuits [1–12,15,16]. In an MTCMOS circuit, high threshold voltage (high-$|V_{th}|$) sleep transistors (header and/or footer) are used to cut off the power supply and/or the ground connections to an idle low threshold voltage (low-$|V_{th}|$) circuit block. A ground-gated MTCMOS circuit is shown in Fig. 1. An MTCMOS circuit consumes significant energy during transitions from ACTIVE mode to SLEEP mode and from SLEEP mode to ACTIVE mode. Lower energy consumption during mode transitions is critically important to achieve higher energy efficiency in MTCMOS circuits.

With the increasing number of autonomous power/ground gating domains that are employed for more effective suppression of leakage currents in each new CMOS technology generation, reactivation noise (power and ground bouncing noise) that is produced by awakening MTCMOS circuit blocks has become an important reliability concern in modern integrated circuits [4–8].

Novel MTCMOS circuits with lower deactivation/reactivation energy consumption and suppressed noise are therefore highly desirable.

A variety of MTCMOS circuit techniques that employ sleep signal slew rate modulation for reactivation noise suppression are proposed in recently published papers [6–8]. The energy and timing overheads that are associated with these noise-aware MTCMOS circuit techniques are however overlooked in these publications. In this paper, mode transition energy consumption in noise-aware MTCMOS circuits is evaluated in detail. The breakeven idle intervals and mode transition timing overheads for achieving net energy savings are identified with different low-noise MTCMOS circuits. With a digital triple-phase sleep signal slew rate modulation technique, the total mode transition energy consumption, breakeven idle interval, and overall mode transition timing overhead are reduced by up to 45.31%, 60%, and 65.26%, respectively, as compared to the other noise-aware MTCMOS circuits that are evaluated in this paper.

This paper is organized as follows. The sources of deactivation/reactivation energy consumption in MTCMOS circuits are investigated in Section 2. Different noise-aware MTCMOS circuit techniques are described in Section 3. The mode transition energy consumption, breakeven idle intervals, and mode transition timing overheads of noise-aware MTCMOS circuits are evaluated under an equal-noise constraint in Section 4. The paper is summarized in Section 5.

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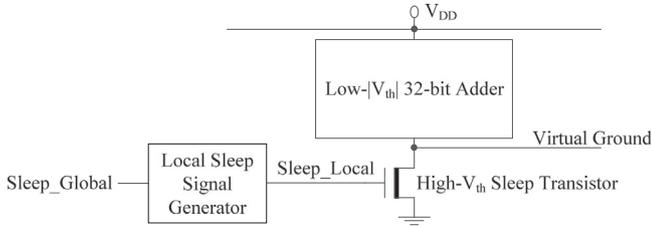E-mail addresses: H.Jiao@tue.nl (H. Jiao), eekursun@ust.hk (V. Kursun).

Fig. 1. A ground-gated 32-bit Brent-Kung adder. "Sleep_Global" is the input signal coming from the on-chip power management unit. "Sleep_Local" is the sleep signal that is applied to the local ground-gated MTCMOS circuit block. Local sleep signal generator can be a simple buffer or a more sophisticated circuit for reshaping the sleep signal, depending on the MTCMOS implementation.
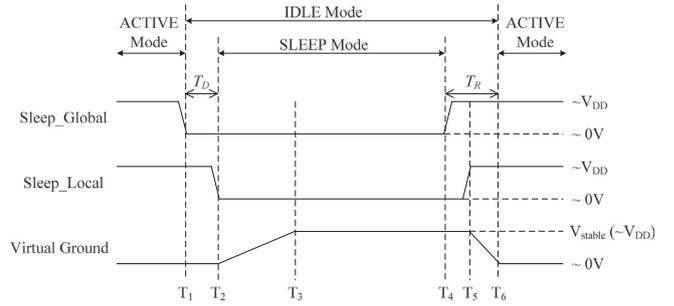

Fig. 2. The voltage waveforms of the sleep signals and virtual ground line in a ground-gated MTCMOS circuit during different modes of operation. T_D: deactivation delay. T_R: reactivation delay. The breakeven point of energy consumption is achieved after the virtual ground line is charged to the steady-state voltage V_{stable} in the SLEEP mode.

2. Deactivation/reactivation energy consumption in MTCMOS circuits

MTCMOS is effective in suppressing the leakage currents that are produced by an idle circuit. However, additional energy is consumed by an MTCMOS circuit during transitions from ACTIVE mode to SLEEP mode (deactivation process) and from SLEEP mode to ACTIVE mode (reactivation process) [6,7,9–13]. Lower mode transition energy consumption enables an MTCMOS circuit to transition to low-leakage SLEEP mode more frequently, thereby allowing more significant savings in total energy consumption [9–13]. MTCMOS circuit techniques with lower mode transition energy consumption and suppressed SLEEP mode leakage currents are therefore highly desirable. The sources of energy consumption during mode transitions in an MTCMOS circuit are identified in this section.

The voltage waveforms of the sleep signals (Sleep_Global and Sleep_Local) and the virtual ground line of a ground-gated MTCMOS circuit are shown in Fig. 2. The global sleep signal (Sleep_Global) transitions low to initiate a deactivation event. The leakage currents that are produced by the MTCMOS circuit are suppressed in the SLEEP mode. Additional dynamic switching energy is however consumed by the MTCMOS circuit to transition to the SLEEP mode. While turning off the sleep transistor, dynamic switching energy ($E_{D\_Sleep\_Generator}$) is consumed (from T_1 to T_2) by the sleep signal generator. Additional switching energy ($E_{D\_VGND} + E_{D\_Internal\_Nodes}$) is consumed (from T_2 to T_3) as the virtual ground line and the internal nodes of low-$|V_{th}|$ circuit block are charged towards V_{DD} in the SLEEP mode. The leakage energy ($E_{D\_Leakage}$) that is consumed by the sleep signal generator and the MTCMOS circuit during the deactivation delay (T_1 to T_2) also contributes to the deactivation energy consumption. The overall deactivation energy consumption overhead ($E_{Deactivation}$) is.

$$E_{Deactivation} = E_{D\_Sleep\_Generator} + E_{D\_Internal\_Nodes} + E_{D\_VGND} + E_{D\_Leakage}.$$

(1)

At the end of SLEEP mode, Sleep_Global transitions high to initiate a reactivation event. Energy ($E_{R\_Sleep\_Generator}$) is consumed (from T_4 to T_5) by the sleep signal generator while turning on the sleep transistor during a reactivation event. The internal nodes of low-$|V_{th}|$ circuit block transition to correct logic states stage by stage depending on the input vectors that are applied to the MTCMOS circuit. Energy ($E_{R\_Switching} + E_{R\_Short\_Circuit}$) is consumed (from T_5 to T_6) due to the switching and short circuit currents that are produced by the low-$|V_{th}|$ circuit block during a reactivation event [4–7]. The leakage energy ($E_{R\_Leakage}$) consumed by the sleep signal generator and the MTCMOS circuit during the reactivation delay (T_4 to T_6) also contributes to the reactivation energy consumption. The overall reactivation energy consumption

overhead ($E_{Reactivation}$) is

$$E_{Reactivation} = E_{R\_Sleep\_Generator} + E_{R\_Switching} + E_{R\_Short\_Circuit} + E_{R\_Leakage}.$$

(2)

The breakeven point of energy consumption is achieved when the leakage energy savings in idle mode is equal to the total mode transition energy consumption due to the deactivation and reactivation events as given in the following equation:

$$P_{Active\_Leakage} * (T_4 - T_2) - \int_{T_2}^{T_4} P_{Leakage}(t)dt = E_{Deactivation} + E_{Reactivation}.$$

(3)

$P_{Active\_Leakage}$ is the leakage power consumed by the sleep signal generator and the MTCMOS circuit when the low-leakage SLEEP mode is not exercised (sleep transistor is maintained on). $P_{Leakage}$ is the leakage power consumed by the sleep signal generator and the MTCMOS circuit when the low-leakage SLEEP mode is exercised (sleep transistor is cut off). The minimum duration of SLEEP mode (T_2 to T_4 in Fig. 2) for which an MTCMOS circuit provides net savings in total energy consumption is the breakeven idle interval [13]. The mode transition timing overhead ($T_{Overhead}$) of an MTCMOS circuit is

$$T_{Overhead} = T_D + Breakeven\_Idle\_Interval + T_R,$$

(4)

where T_D ($T_2 - T_1$) and T_R ($T_6 - T_4$) are the deactivation delay and reactivation delay, respectively.

Provided that the duration of SLEEP mode is shorter than the breakeven idle interval, the energy consumed during mode transitions is higher than the leakage energy savings that is provided by the SLEEP mode. Gating the low-$|V_{th}|$ circuit block is ineffective since the overall energy consumption is increased as compared to a conventional low-$|V_{th}|$ circuit without any ground gating. The SLEEP mode of an MTCMOS circuit should be exercised only if the duration of idle mode is longer than the mode transition timing overhead.

The breakeven point of energy consumption is assumed to be achieved after the virtual ground line is charged to the steady-state voltage V_{stable} in the SLEEP mode in Fig. 2. Under this scenario, the virtual ground line is discharged from V_{stable} to ~ 0 V during a reactivation event. Depending on the actual MTCMOS circuit, however, the breakeven point of energy consumption can be achieved before the virtual ground line is charged to V_{stable} in the SLEEP mode, as shown in Fig. 3. Under this scenario, the virtual ground line can be discharged either from V_{stable} or from a voltage level lower than V_{stable} towards ~ 0 V during a reactivation event, as shown in Fig. 3.
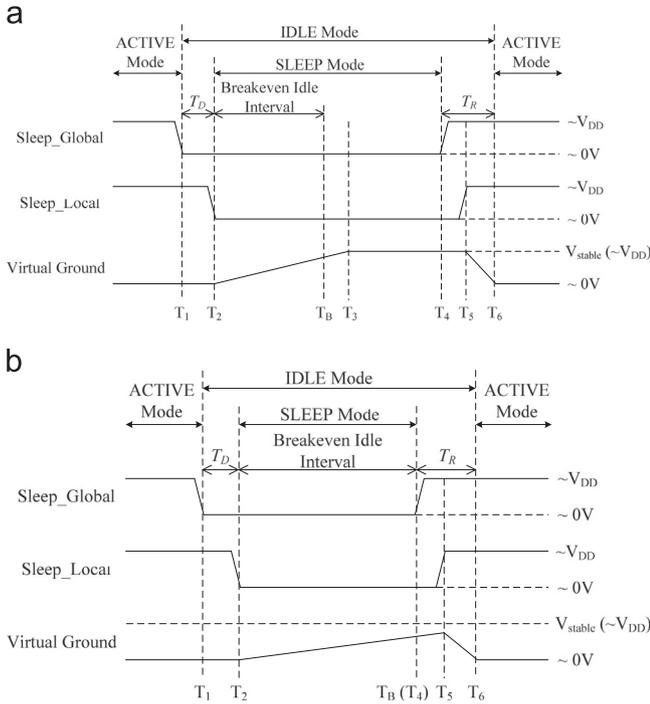
Fig. 3. The voltage waveforms of the sleep signals and virtual ground line in a ground-gated MTCMOS circuit during different modes of operation. T_D: deactivation delay. T_R: reactivation delay. The breakeven point (T_B) of energy consumption is achieved before the virtual ground line is charged to the steady-state voltage V_{stable} in the SLEEP mode. (a) A reactivation event is initiated after the virtual ground line is charged to the steady-state voltage V_{stable} in the SLEEP mode. (b) A reactivation event is initiated immediately after the breakeven point of energy consumption is achieved.

3. Mode transition in noise-aware MTCMOS circuits

When an idle MTCMOS circuit is awaken, high instantaneous currents flow through the sleep transistors. Significant reactivation noise is produced on the power and ground distribution networks [4–8]. Sleep signal slew rate modulation is effective in suppressing the reactivation noise in an MTCMOS circuit [6–7]. Mode transition energy consumption and timing overhead of recently published noise-aware MTCMOS circuits that employ sleep signal slew rate modulation are briefly discussed in this section.

3.1. Single-phase sleep signal slew rate modulation

The instantaneous currents that cause reactivation noise are primarily composed of switching and short circuit currents that are produced by the low-$|V_{th}|$ circuit block in an MTCMOS circuit [4–7]. By sufficiently increasing the rise delay of a single-phase sleep signal, the rate of change of instantaneous currents is reduced [6,7]. The reactivation noise is thereby suppressed in an MTCMOS circuit.

Single-phase sleep signal slew rate modulation however significantly increases the reactivation delay and energy consumption of MTCMOS circuits. Both the breakeven idle interval and overall mode transition timing overhead are prohibitively long when the single-phase sleep signal slew rate modulation technique is applied to an MTCMOS circuit.

3.2. Stepwise V_{gs} MTCMOS

A stepwise V_{gs} MTCMOS circuit technique to suppress mode transition noise is presented in [6]. Stepwise V_{gs} MTCMOS employs a two-step wake up scheme as shown in Fig. 4. The sleep signal
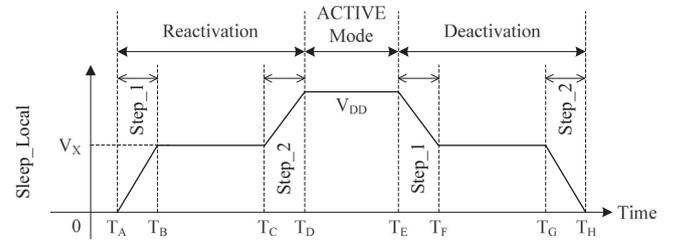

Fig. 4. The timing diagram of the local sleep signal (that is connected to the gate terminal of the sleep transistor) with the stepwise V_{gs} MTCMOS circuit.
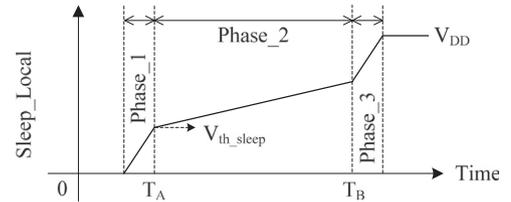

Fig. 5. The timing diagram of the local sleep signal (that is connected to the gate terminal of the sleep transistor) with the triple-phase sleep signal slew rate modulated MTCMOS circuit.

transitions from 0 V to an intermediate voltage level V_X ($0\,V < V_X < V_{DD}$) during the first step of a reactivation event. The sleep signal is maintained at V_X until the virtual ground line is discharged to a sufficiently low voltage level. The sleep signal is subsequently raised from V_X to V_{DD} during the second step of reactivation. The reactivation noise is suppressed due to the weaker conductivity of the sleep transistor and the lower voltage swing on the virtual ground line during the first and the second, respectively, wake up steps [8].

A sleep signal modulator for stepwise V_{gs} MTCMOS circuit is proposed in [8]. The output signal of the stepwise V_{gs} sleep signal modulator, Sleep_Local (that is connected to the gate terminal of the sleep transistor as shown in Fig. 1), is discharged from V_{DD} to an intermediate voltage level (between V_{DD} and 0 V) before being fully discharged to 0 V during a deactivation event, as shown in Fig. 4. The stepwise V_{gs} MTCMOS circuit therefore suffers from a long deactivation delay. Significant weak inversion currents are produced by the low-$|V_{th}|$ circuit block during the long deactivation process of a stepwise V_{gs} MTCMOS circuit. Furthermore, significant short circuit currents are produced by the stepwise V_{gs} sleep signal generator during mode transitions [7]. The stepwise V_{gs} MTCMOS circuit therefore suffers from high energy consumption during mode transitions.

3.3. Triple-phase sleep signal slew rate modulation

A triple-phase sleep signal slew rate modulation (TPS) technique is presented in [6] to suppress the reactivation noise while accelerating the reactivation process in MTCMOS circuits. The concept of triple-phase sleep signal slew rate modulation is shown in Fig. 5. The sleep signal rises fast from 0 V to the threshold voltage of sleep transistor to reduce the reactivation delay without producing significant noise during Phase_1 [6,7]. The sleep signal is subsequently decelerated to suppress the noise waveform in Phase_2 where the peak reactivation noise is produced. After the virtual ground line voltage is reduced to a very low level close to 0 V, the rise of sleep signal is accelerated again to shorten the remaining duration of reactivation process in Phase_3.

A fully digital triple-phase sleep signal slew rate modulator is proposed in [6] to produce the triple-phase sleep signal that is shown in Fig. 5. With the triple-phase sleep signal modulator [6,7], the rising speed of sleep signal is adjusted by monitoring the

voltage level of Sleep_Local and virtual ground line. The transitions between the three phases of reactivation occur automatically. This digital sleep signal modulator is effective for reducing the reactivation delay and energy consumption as compared to the single-phase sleep signal slew rate modulator [6,7]. Furthermore, the deactivation delay and energy consumption with the digital triple-phase sleep signal modulator are significantly suppressed as compared to the stepwise V_{gs} sleep signal modulator [6,7]. Both the breakeven idle interval and the overall mode transition timing overhead of an MTCMOS circuit are thereby shortened with the digital triple-phase sleep signal modulator as compared to the single-phase and stepwise V_{gs} sleep signal modulators.

4. Evaluation of low-noise MTCMOS circuits

A ground-gated 32-bit Brent-Kung adder is designed with the UMC 80 nm multi threshold voltage CMOS technology (high-$V_{th\_NMOS} = +370$ mV, low-$V_{th\_NMOS} = +155$ mV, high-$V_{th\_PMOS} = -310$ mV, low-$V_{th\_PMOS} = -105$ mV, and $V_{DD} = 1$ V) [17] to evaluate the mode transition phenomenon with different sleep signal slew rate modulation techniques in this section. The sleep transistor is sized 5 μm to achieve similar (within 5%) delay along the critical signal propagation path (in ACTIVE mode) of MTCMOS circuit as compared to the standard purely low-$|V_{th}|$ circuit. The mode transition noise is characterized with the parasitic impedance model of 40-pin Dual In-line Package (DIP-40) [4–8]. The parasitic resistance, inductance, and capacitance of the 40-pin Dual In-line Package are 217 mΩ, 8.18 nH, and 5.32 pF, respectively [4–8]. Post-layout HSPICE simulation is performed with different MTCMOS circuits.

The on-chip hottest temperature is assumed to be 90 °C (a typical number in modern multi-core high performance microprocessors [14–15]) for both short idle periods and active mode of operation. Three different sleep signal modulators are designed to produce the real sleep signals for the ground-gated MTCMOS circuit under an equal-noise constraint at 90 °C [7]: single-phase sleep signal modulator (composed of two-stage inverters), stepwise V_{gs} sleep signal modulator, and the fully digital triple-phase sleep signal modulator (TPS-Digital). The sleep signal waveforms are tuned to suppress the peak ground bouncing noise to a negligible level that is less than 2 mV with different MTCMOS circuit techniques at 90 °C [7]. Low on-die temperatures down to the room temperature (25 °C) assuming active cooling during long idle periods are also considered in this study. The three sleep signal slew rate modulated MTCMOS circuits are characterized at both 25 °C and 90 °C in this section.

Various mode transition related design metrics of different sleep signal slew rate modulated MTCMOS circuits are shown in Table 1. The TPS-Digital and single-phase MTCMOS circuits both adapt well to the fluctuations of die temperature and maintain the effectiveness in suppressing the reactivation noise even at 25 °C (the lowest temperature that is considered in this study) as listed in Table I. The parasitic capacitors attached to the internal nodes of low-$|V_{th}|$ circuit block and the virtual ground line are however not discharged to sufficiently low voltage levels at the end of the relaxation period (T_C as shown in Fig. 4) at low die temperatures with the stepwise V_{gs} MTCMOS circuit. When the second wake up step is initiated, therefore, significant amount of noise is produced by the stepwise V_{gs} MTCMOS circuit at 25 °C as listed in Table I.

The stepwise V_{gs} and TPS-Digital MTCMOS circuits are effective in reducing the reactivation delay (T_R) as compared to the single-phase MTCMOS circuit. When the virtual ground line of the ground-gated MTCMOS circuits is discharged from the steady-state SLEEP mode voltage to ~ 0 V during a reactivation event (the reactivation scenario that is shown in Figs. 2 and 3(a)), the stepwise V_{gs} and TPS-Digital MTCMOS circuits reduce the maximum reactivation delay (T_{R_MAX}) by 72.46% (64.68%) and 67.25% (64.54%), respectively, as compared to the single-phase MTCMOS circuit at 90 °C (25 °C).

The stepwise V_{gs} and TPS-Digital MTCMOS circuits are also effective in suppressing the reactivation energy consumption (E_R) as shown in Fig. 6. Significant accumulated weak inversion currents are produced by the low-$|V_{th}|$ 32-bit adder due to the longer reactivation process in the single-phase MTCMOS circuit at 90 °C, thereby increasing the maximum reactivation energy consumption (E_{R_MAX}) by 93.14% and 91.46% as compared to the stepwise V_{gs} and TPS-Digital MTCMOS circuits, respectively, assuming that the virtual ground line of the ground-gated MTCMOS circuits is discharged from the steady-state SLEEP mode voltage to ~ 0 V during a reactivation event (the reactivation scenario that is shown in Figs. 2 and 3(a)). The TPS-Digital and stepwise V_{gs} MTCMOS circuits reduce the maximum reactivation energy consumption by 15.7% and 14.9%, respectively, as compared to the single-phase MTCMOS circuit at 25 °C.

The stepwise V_{gs} MTCMOS circuit suffers from a long deactivation delay as discussed in Section 3.2. The deactivation delay (T_D, the time interval from Sleep_Global falls to 10 mV until Sleep_Local falls to 10 mV) is reduced by up to 89.91% and 87.27% with the single-phase and TPS-Digital MTCMOS circuits, respectively, as compared to the stepwise V_{gs} MTCMOS circuit. Due to the long deactivation delay, the stepwise V_{gs} MTCMOS circuit also increases the deactivation energy consumption (E_D, the total energy consumed by a sleep signal generator and MTCMOS circuit together during the deactivation delay) by up to 15.59x and 7.91x as compared to the single-phase and TPS-Digital MTCMOS circuits, respectively, as shown in Fig. 6.

With suppressed deactivation and reactivation energy consumption, the TPS-Digital MTCMOS circuit achieves the lowest overall mode transition energy consumption (reactivation energy

Table 1
Mode transition related design metrics of sleep signal slew rate modulation techniques.

| Temperature	90 °C			25 °C		
Circuit Technique	Single-Phase	Stepwise V_{gs}	TPS-Digital	Single-Phase	Stepwise V_{gs}	TPS-Digital
Peak Ground Noise (mV)	2.090	2.337	1.999	3.145	15.43	2.966
T_{R_MAX} (ns)	44.12	12.15	14.45	36.83	13.06	13.01
T_{R_BE} (ns)	42.20	12.12	10.26	33.27	13.02	7.756
T_D (ns)	1.25	11.8	1.69	1.041	10.32	1.314
E_{R_MAX} (pJ)	1.972	1.021	1.030	0.987	0.859	0.832
E_{R_BE} (pJ)	1.628	0.720	0.534	0.441	0.373	0.237
E_D (pJ)	0.034	0.530	0.067	0.016	0.1999	0.042
Steady-State SLEEP Power (nW)	70.0	87.2	87.1	60.6	71.1	67.4
Breakeven Idle Interval (number of clock cycles)	50	38	20	62	76	40
$T_{Overhead}$ (number of clock cycles)	95	63	33	98	101	50
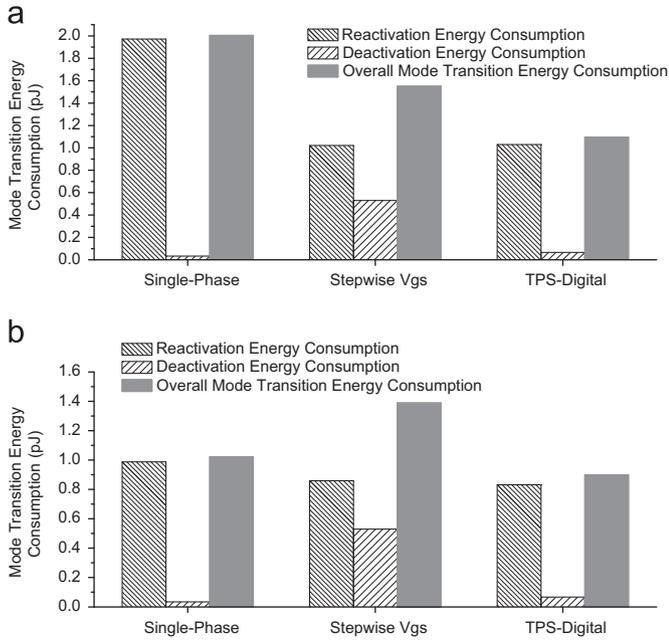
Fig. 6. The reactivation, deactivation, and overall mode transition energy consumption with various sleep signal slew rate modulated MTCMOS circuits. (a) T=90 °C. (b) T=25 °C.

consumption+deactivation energy consumption) as shown in Fig. 6. The TPS-Digital MTCMOS circuit suppresses the overall mode transition energy consumption by 45.31% (35.28%) and 29.27% (11.95%) as compared to the single-phase and stepwise V_{gs} MTCMOS circuits, respectively, at 90 °C (25 °C). TPS-Digital MTCMOS circuit thereby provides the highest energy efficiency during mode transitions in an MTCMOS circuit.

The single-phase MTCMOS circuit consumes the lowest steady-state SLEEP mode leakage power due to the simplest and smallest sleep signal modulator among the MTCMOS circuits that are evaluated in this paper. The single-phase MTCMOS circuit reduces the steady-state SLEEP mode leakage power consumption by up to 14.77% and 10.09% as compared to the stepwise V_{gs} and TPS-Digital MTCMOS circuits, respectively, as listed in Table I.

The duration of idle mode of an MTCMOS circuit has to be longer than the overall mode transition timing overhead ($T_{Overhead}$: sum of deactivation delay, reactivation delay, and breakeven idle interval) for providing net energy savings in the SLEEP mode, thereby justifying the transition to low-leakage SLEEP mode. The breakeven idle interval and overall mode transition timing overhead associated with different MTCMOS circuits are evaluated next. The operating frequency of adders is assumed to be 1 GHz.

Assuming an extreme case where the number of idle clock cycles from the end of deactivation to the beginning of reactivation (T_2 to T_4, see Figs. 2 and 3) is 0, the overall energy consumption of an MTCMOS circuit with a cut-off sleep transistor is the sum of reactivation and deactivation energy consumptions (with the virtual ground line voltage maintained close to 0 V). Alternatively, in more practical scenarios where the duration of SLEEP mode is nonzero ($T_4 - T_2 \neq 0$), the cumulative energy consumption of an MTCMOS circuit with a cut-off sleep transistor increases with the number of idle clock cycles due to the leakage power consumed by the low-$|V_{th}|$ adder and the dynamic power consumed as the virtual ground line and the internal nodes of the low-$|V_{th}|$ adder are charged towards V_{DD}. The energy consumed by an idle MTCMOS circuit where the low-leakage sleep mode is not exercised (sleep transistor is maintained on) increases faster with increased number of idle clock cycles as compared to an MTCMOS circuit where the low-leakage sleep mode is exercised (sleep transistor is cut off) as shown in Fig. 7. All the MTCMOS circuits
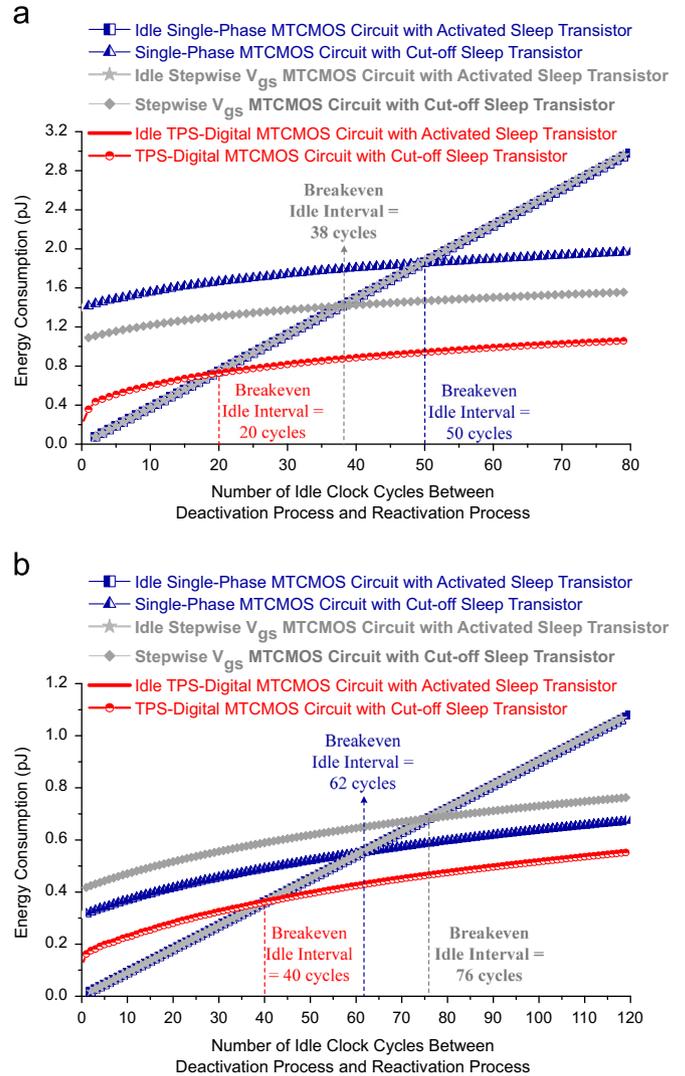

Fig. 7. The energy consumption of different sleep signal slew rate modulated MTCMOS circuits. The breakeven idle intervals of the MTCMOS circuits are shown in the figure. (a) T=90 °C. (b) T=25 °C.

that are evaluated in this paper achieve the breakeven point of energy consumption before the virtual ground line is charged to the steady-state voltage in SLEEP mode. For the single-phase MTCMOS circuit, at least 50 idle clock cycles are required for the accumulated leakage energy savings to exceed the mode transition energy overhead at 90 °C, as shown in Fig. 7(a). Alternatively, only 20 idle clock cycles are required to achieve net savings in energy consumption with the TPS-Digital MTCMOS circuit at 90 °C.

The effectiveness of ground gating for leakage power savings is degraded at lower temperature [4,5]. The breakeven idle intervals with all three MTCMOS circuits are therefore elongated at 25 °C, as shown in Fig. 7(b).

TPS-Digital MTCMOS circuit achieves the shortest breakeven idle interval due to the lowest mode transition energy consumption among the MTCMOS circuits that are evaluated in this paper, as shown in Fig. 8. Alternatively, the stepwise V_{gs} and single-phase MTCMOS circuits require the longest breakeven idle interval at 25 °C and 90 °C, respectively. The TPS-Digital MTCMOS circuit shortens the breakeven idle interval by 60% (47.37%) and 47.37% (35.48%) as compared to the single-phase and stepwise V_{gs} MTCMOS circuits, respectively, at 90 °C (at 25 °C).

The TPS-Digital sleep signal modulator monitors the virtual ground line voltage during a reactivation event, thereby
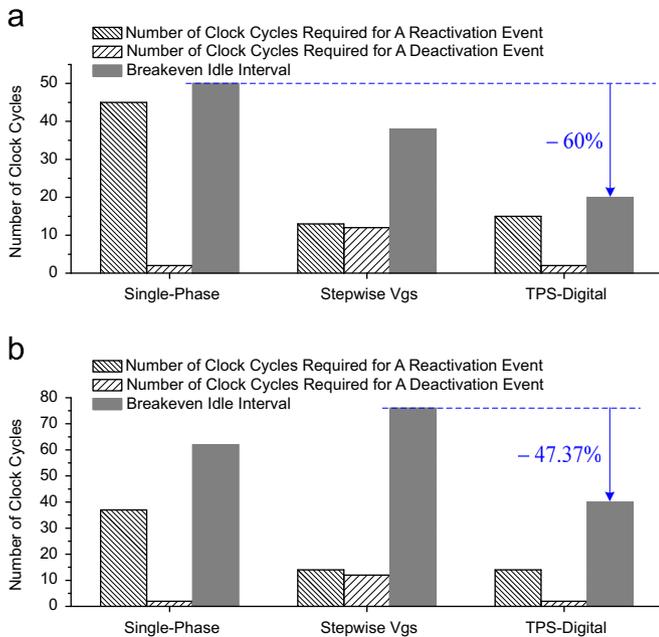
Fig. 8. The breakeven idle intervals with various sleep signal slew rate modulated MTCMOS circuits. The numbers of clock cycles that are required for reactivation and deactivation events with the MTCMOS circuits are also shown in the figure. (a) $T=90\,°C$. (b) $T=25\,°C$.
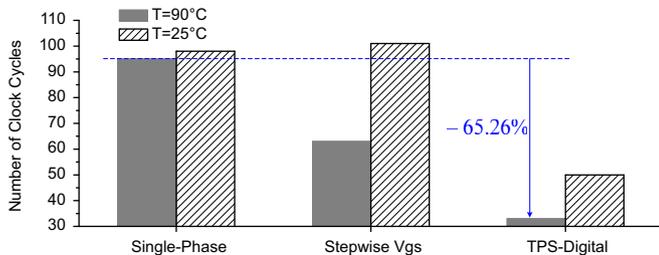

Fig. 9. The overall mode transition timing overhead with various sleep signal slew rate modulated MTCMOS circuits.

dynamically adjusting the rising speed of sleep signal. When a reactivation event is initiated immediately after the breakeven point of energy consumption is achieved, the virtual ground line voltage of the TPS-Digital MTCMOS circuit is lower than the steady-state SLEEP mode voltage. The TPS-Digital sleep signal modulator thereby transitions to Phase_3 (where the sleep signal is accelerated) earlier as compared to the scenario where the virtual ground line is discharged from $\sim V_{DD}$ during a reactivation event. Alternatively, the single-phase and stepwise V_{gs} sleep signal modulators cannot track the voltage of virtual ground line. The TPS-Digital MTCMOS circuit therefore provides the shortest reactivation delay (T_{R_BE}: the reactivation delay that is measured by assuming a reactivation event is initiated immediately after the breakeven point of energy consumption is achieved as shown in Fig. 3(b)) among the MTCMOS circuits that are evaluated in this paper, as shown in Table I. The TPS-Digital MTCMOS circuit reduces T_{R_BE} by up to 76.69% and 40.43% as compared to the single-phase and stepwise V_{gs} MTCMOS circuits, respectively. Furthermore, the TPS-Digital MTCMOS circuit consumes the lowest reactivation energy (E_{R_BE}: the energy that is consumed by an MTCMOS circuit and the sleep signal modulator during T_{R_BE}). E_{R_BE} is reduced by up to 67.2% and 36.46% with the TPS-Digital MTCMOS circuit as compared to the single-phase and stepwise V_{gs} MTCMOS circuits, respectively.

The TPS-Digital MTCMOS circuit achieves the shortest overall mode transition timing overhead. Alternatively, the single-phase

MTCMOS and stepwise V_{gs} circuits suffer from the longest overall mode transition timing overhead at 90 °C and 25 °C, respectively. The TPS-Digital MTCMOS circuit shortens the overall mode transition timing overhead by 65.26% (50.5%) and 47.62% (48.98%) as compared with the single-phase and stepwise V_{gs} MTCMOS circuits, respectively, at 90 °C (25 °C) as shown in Fig. 9. TPS-Digital MTCMOS circuit allows more frequent transitions to the low-leakage SLEEP mode due to the reduced overall mode transition timing and energy overheads. Digital triple-phase sleep signal slew rate modulation thereby provides more significant savings in overall energy consumption as compared to the other MTCMOS circuits that are evaluated in this paper.

5. Conclusions

The sources of mode transition energy consumption with noise-aware MTCMOS circuits are identified in this paper. The deactivation/reactivation energy consumptions of various recently published low-noise MTCMOS circuit techniques are evaluated. The breakeven idle intervals and mode transition timing overheads with different MTCMOS circuits are investigated. A digital triple-phase sleep signal slew rate modulated MTCMOS circuit suppresses the overall mode transition energy consumption by up to 45.31% as compared to the other noise-aware MTCMOS circuits that are evaluated in this paper in a UMC 80 nm CMOS technology. Furthermore, the digital triple-phase MTCMOS circuit reduces the breakeven idle interval and the overall mode transition timing overhead by up to 60% and 65.26%, respectively, as compared with the other low-noise MTCMOS circuits that are evaluated in this paper. Digital triple-phase sleep signal slew rate modulation is therefore recommended as the most energy efficient technique for achieving fast mode transitions with negligible reactivation noise in MTCMOS circuits.

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