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A Discrete-Time Amplifier Based On Thin-Film Trans-Capacitors for Sensor Systems on Foil

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Abstract

Organic materials can be used to fabricate sensors for physical and chemical quantities, and also to make electronics. The integration of these two elements holds the promise to enable novel smart-sensors on foil. In this paper, we deal with the design of the first stage of a signal conditioning chain on foil: the amplifier. The poor electrical performance of organic TFTs hampers the design of complex circuits, and negatively affects the characteristics of continuous-time amplifiers. In order to improve small-signal gain and speed, a mixed discrete-time and continuous-time approach is presented in this paper for the sensor frontend. A new device, the Thin-Film Trans-Capacitor, is presented and used to build the discrete-time amplifier, while the continuous time amplifier exploits a simple traditional architecture to improve yield. Simulations of the circuit proposed show that the total gain of the sensor frontend increases of about one decade without any detrimental effect on the speed. CAD (Computer-Aided Design) simulations confirm the results of the simple mathematical model we present.

Keywords: organic electronics; sensor frontend; switching capacitor; trans-capacitor; sample and hold

1. Introduction

Thin-Film Transistor (TFT) technologies, based on organic and metal-oxide semiconductors, are emerging as suitable solution for sensor systems on foil. This kind of technology allows the realization of large-area electronics that can be manufactured on cheap plastic foils due to the low temperatures needed for the production process [1], [2]. Thanks to these features, besides mechanical flexibility [3] and high throughput [4], ultra-low cost could be achieved in mass production, enabling disposable integrated circuits. For instance, RFID (Radio-Frequency IDentification) augmented with an organic sensor could be integrated on packages at single item level to monitor the freshness of food or the storage conditions of pharmaceuticals.

The functionality of a smart sensor (Fig. 1) is obtained thanks to the integration of analog, digital and mixed signal circuits on the same plastic foil. Typically the main analog building blocks consist of an organic sensor [5] and a sensor frontend for first analog amplification and signal processing [6]. Afterwards, the analog signal is converted into a digital word [7], [8], [9], [10] and transmitted to a base station by means of an RFID [11], [12] for further processing.

This paper deals with the design of a frontend for organic sensors that allows higher gain than a single-stage topology without any detrimental effect on its speed. The final frontend exploits two Thin-Film Trans-Capacitors (TFTC) [13] in front of a continuous-time amplifier, thus implementing

at the same time a sample-and-hold (S&H) function, low noise amplification, and common mode rejection.

In Section 2, we present the design and the characterization of a continuous-time fully differential amplifier. In Section 3 and 4, we introduce the technology used to design the Thin-Film Trans-Capacitor and its design. The discrete-time fully-differential amplifier is analyzed in Section 5, and the simulated data of the combination of the two amplifiers are show in Section 6. In Section 7, some conclusions are drawn. Sections 3 to 6 expand considerably the material presented in [13].

2. A continuous-time single-stage fully-differential amplifier

Limitations imposed by the technology (as single-type TFTs, poor gain, large threshold voltage, large process parameter variations and mismatch) considerably restrict the design choices when building a voltage amplifier on foil. In our case, the technology is p-type only, thus the input pair can only be p-type (M2 and M4 in Fig. 2).

The tail current source should also be a p-type TFT and work in saturation, but unfortunately the tail source cannot be the output transistor of a current mirror (as explained in [6]). However, this function can be easily embodied by a p-type TFT used in a Zero-Vgs configuration (M3 in Fig. 2): this provides high output resistance and thus a relatively supply-independent bias current I_{tail}.

Neither passive loads nor self biasing solutions (e.g. current mirrors) are possible, due to the lack of resistors and complementary devices. Therefore the output loads can only be implemented with diode-connected or Zero-Vgs TFTs (M1 and M5 in Fig. 2a and Fig. 2b respectively).

2.1. Design and simulation

The diode load solution provides small impedance at the output node, which potentially increases the bandwidth, but also limits the gain to about 2 and keeps the output common mode very close to ground. This last effect makes very difficult the use of additional level shifters, and thus prevents the possibility to DC-couple several gain stages. Using a Zero-Vgs load the time response worsens, but higher gain can be achieved (up to 40dB with some design effort) and the output common mode voltage can be designed to be closer to half the supply. For these reasons, Zero-Vgs loads have been preferred in this work.

In both topologies of Fig. 2, the gain of the circuit is very sensitive to input common-mode variations, thus cascading multiple amplification stages is very cumbersome or even impossible. Figure 3 shows the output common-mode (Fig. 3a) and the gain (Fig. 3b) as a function of the input common-mode simulated for the Zero-Vgs differential amplifier of Fig. 2b. As shown in Fig. 3a, when the input common-mode $V_{CM,IN}$ is low, both the drain of M3 and the outputs are around $V_{DD}/2$, as expected. When the input common-mode $V_{CM,IN}$ becomes larger than half the supply, $V_{D,3}$ follows the inputs and the output common-mode drops, together with the bias current.

From Fig. 3b, the consequences on the gain can be observed. For a low input common-mode, the input transistors work in linear region ($|V_{DS}| \approx 0V$ and $|V_{GS} - V_T| >> 0$) and the output resistance of the amplifier drops. On the other hand, when $V_{CM,IN}$ is too high, the bias current drops drastically,

the load transistors M1 and M5 exit the saturation region and provide a low output resistance. In both cases, a detrimental effect on the gain is observed.

Varying the dimension of the input devices causes a different overdrive voltage on the input TFTs (Fig. 3b), and hence it shifts the gain plateau to the right for larger widths. Increasing the width of the input devices also increases the gain due to the larger transconductance g_m. Unfortunately the difference between input and output common-mode increases too, making the design of level shifters for multi-stage DC-coupled amplifiers more complicate. Since lowering the width of the input devices also lowers the differential gain (which is already small), the final differential amplifier was designed with input device as wide as the load ones.

2.2. Layout and measurements

Figure 4 shows the layout and the photograph of the realized circuit. Both the input TFTs and the output loads have been dimensioned with the same W/L ratio and with the same channel length. Therefore, also the number of sub-channels in the interdigitated TFTs was chosen the same.

Moreover, the tail source should provide exactly the same current provided by the two load transistors. In order to avoid systematic errors that could worsen the performance of the circuit in addition to process variations, the tail transistor was implemented using two devices in parallel, identical to the loads.

In the final layout, also two output buffers were included. These are required to perform transient measurements without affecting the circuit with external capacitive or resistive parasitics due to the measurement setup.

The tapeout includes several instances of this continuous-time amplifier, and in Fig. 5 the differential output and gain measured on 14 of them are shown.

For these measurements, the positive input was swept from ground to V_{DD} = 20V, while the negative input was kept constant at 12 V. In this way, the differential output was measured and the maximum random offset could be estimated to be about 0.8 V. From these measurements also the maximum differential gain could be evaluated. Indeed, when the positive input reaches 12 V, the input common-mode is also 12 V and, according to the simulations, the maximum gain is achieved. However, the measured gain was much smaller than the simulated one, probably due to the degradation of the semiconductor mobility, and consequently to the reduced input transconductance, after a few weeks of shelf-life. Also its variability is not negligible, showing that, even after a careful design process, variations and aging strongly impact the performance of this analog circuit made with organic transistors.

3. Dual-gate organic TFT technology

Both the continuous- and the discrete-time amplifiers described here were designed with the same three metal layers TFT technology [2] that we used in previous works [6], [14] (Fig. 6). The bottom-gate bottom-contact transistors are made on a 25 µm thick plastic foil (PEN), temporarily glued on a rigid carrier for the ease of processing. An 80 nm thick gold film is used for each of the

three conductive layers. The p-type organic semiconductor pentacene is deposited from solution and is about 200 nm thick. The insulator layers are made with a solution-processed polymer (PVP). The bottom layer, between the gate and the channel of the transistor, is about 380 nm thick, while the top insulator, between semiconductor and top-gate, has a thickness of about 1400 nm.

This double-gate organic TFT technology was originally developed for display applications where it is paramount to achieve large aperture ratios. For this reason, a third metal layer was added to the stack in order to cover the driving transistor of each pixel. This third metal layer can be used in a transistor (Fig. 6) as a top-gate, and the effect of a bias of the top-gate can be modeled by a shift of the threshold voltage. Indeed, the equation of the channel current is:

$$I_{ch} = \beta(V_G - V_S - V_T)^\gamma - \beta(V_G - V_D - V_T)^\gamma, \quad (1)$$

where the threshold voltage V_T can be expressed as:

$$V_T = V_{FB} - \eta(V_{TG} - V_S). \quad (2)$$

In these equations, β contains the geometrical parameter (W, L, C_{ox}) of the device and the mobility (μ) of the semiconductor. The power γ is not equal to 2 as in standard silicon MOS transistor, but it is slightly larger, due to the dependence of the mobility on the gate voltage. The flat band voltage V_{FB} is a parameter defined by the intrinsic characteristics of the semiconductor-insulator-metal stack, while η weights the influence of the top-gate voltage on the channel of the transistor. Its value depends on the thickness of the two insulator layers and, for our technology, η = 0.25.

4. Thin-Film Trans-Capacitor

With this three-metal-layers technology, we designed a Thin-Film Trans-Capacitor (TFTC). That is a parametric capacitor (PC) useful to perform discrete-time signal amplification. The capacitance value C of a capacitor realized in a TFT technology can be expressed as a function of its geometric parameters using the well-known parallel-plates formula:

$$C = \varepsilon_0 \varepsilon_r \frac{WL}{h} \quad (3)$$

where ε_0 and ε_r are the electric and the dielectric constant respectively, W and L are the width and the length of the two facing plates, and h is their distance. In a double-gate technology, normal capacitors can be realized between gate and source layers, between gate and top-gate layers, and between the source and top-gate layers. The value of *h* for each layer pair differs due to the different thickness of insulator between the plates.

Combining in a single device the three types of capacitor, a novel parametric capacitor can be designed. Its cross-section is shown in Fig. 7. In this device the dimensions of top-gate and gate plates are defined by the geometry of the metal armatures; the middle plate, on the other hand, has a parametric width. In our application, a synchronous signal will be applied to the device in order to accumulate or to deplete the semiconductor. These two states correspond to different dimensions to the central plate, hence the three capacitors can be switched from their minimum

to their maximum capacitance value and vice versa. This variation will be used afterwards to amplify the sampled signal.

For our purpose, we use the top-gate voltage to control the accumulation state in the semiconductor underneath. If the overdrive voltage applied to the top gate is larger than zero, a layer is created in which majority charge carriers are accumulated at the interface between semiconductor and top insulator. Thus we can find two different regions, in the V_G-V_{TG} plane (Fig. 8): on the right hand side of the straight line

$$V_{TG} = -\frac{V_G}{\eta} + \frac{V_{FB}}{\eta} \tag{4}$$

an accumulation layer is created in the semiconductor, while on the left hand side the semiconductor is depleted.

The new device can be modeled (Fig. 9a) using three variable capacitors: a top-gate to source (C_{TGS}), a top-gate to gate (C_{TGG}) and a source to gate (C_{SG}) capacitor.

Based on the size of the plates involved, it is possible to define for each capacitor the value of its capacitance when the semiconductor works in accumulation and when in depletion. When the semiconductor is depleted we find:

$$\begin{aligned} C_{TGS} &= FW\, L_G\, \eta\, C_{ox} \\ C_{TGG} &= 0 \\ C_{SG} &= (W_G L_G - FW)\, L_G \frac{\eta}{\eta + 1} C_{ox} \end{aligned} \tag{5}$$

On the other hand, when the accumulation layer is created, we find:

$$\begin{aligned} C_{TGS} &= W_G\, L_G\, \eta\, C_{ox} \\ C_{TGG} &= 0 \\ C_{SG} &= W_G\, L_G\, C_{ox} \end{aligned} \tag{6}$$

In the previous equations, W_G is the width of gate (G), top-gate (TG) and semiconductor (OSC) layers, FW is the width of the source metal strip (Fig. 7) and L_G is the length of the device (in the plane perpendicular to the picture of Fig. 7). The PC design of Fig. 7 does not take into account the variations due to the lithographic process and to mask misalignments. However, these problems can be easily overcome adapting the design of the device to the specific use. For instance, in our case, we use the top-gate to control the charge accumulation in the semiconductor (and thus the width of the central plate). Therefore, to improve robustness against misalignments, a pyramidal layout can be used, designing $W_G = W_{OSC} + E_{OSC}$ and $W_{OSC} = W_{TG} + E_{TG}$, where W_X is the width of the layer X (G, TG or OSC) and E is the minimum enclosure imposed by the design rules. Following this approach, the plate width W_G in Equation (5) and (6) has to be replaced by W_{TG}, but the ratio between the capacitance values in the two different conditions remains the same, and the discussion that follows remains valid.

Each pair of bias voltages V_G-V_{TG} determines the capacitance value of the capacitors in the schematic of Fig. 9a. These values are shown in a three dimensional space in Fig. 10 (W_G = 50 µm, L_G = 50 µm, FW = 5 µm, C_{ox} = 9.5e^{-17} F/µm^2), on the left hand side. We can observe that far enough from the roll-off the value of the capacitance is almost independent of the voltage applied to the plates. The right hand side of the same figure shows the value of each capacitor as a function of only one voltage, while the others are biased at 0 V. The more gradual transition as a function of V_{TG} reflects the weaker coupling due to the higher distance of the top-gate from the semiconductor.

5. A discrete-time single-stage fully-differential amplifier

The performance of the continuous-time amplifier discussed in Section 2 suffers from various limitations: low gain, small input range, low speed, low linearity, large mismatch, to mention the most important. Some of these drawbacks can be partially solved with a considerable increase in the circuit complexity [15], and a consequent decrease in reliability. Unfortunately the poor performance of large-area technology TFTs makes also the design of discrete-time circuits difficult. In our technology, high-quality switches cannot be embodied by the normally-on transistor without large voltages to switch them off (low off-resistance) and the on-resistance is typically large (causing voltage drops and slow response). Moreover, the well-known circuit techniques to cancel charge injection, reduce offsets, and counteract leakage exploit negative feedback, which is almost impossible to realize as discussed before. For these reasons, a new device was designed to minimize the number of switches required for the sampling, to amplify the signal and to enable faster response.

In order to perform fast analog amplification, we explore in this article a discrete-time parametric amplifier, based on the concept described here below. The amplifier works in two phases (Fig. 11). During the first phase the input signal is connected to a parametric capacitor (PC) and the output voltage $v_{out,\phi1}$ follows the input v_{in}.

At the beginning of the second phase, the switch opens and the charge accumulated on the capacitance $C_{\phi1}$ is fixed:

$$Q = C_{\varphi1} \cdot v_{in,\varphi1} \tag{7}$$

where the value $v_{in,\phi1}$ is the last input voltage before the switch is opened. In the second phase the capacitance value of the parametric capacitor is changed (varying the top-gate bias, as will be described in detail in section 5.2). The charge accumulated in the capacitor in the second phase can then be expressed as:

$$Q = C_{\varphi2} \cdot v_{out,\varphi2}. \tag{8}$$

Imposing charge conservation the gain of the circuit results:

$$G = \frac{v_{out,\varphi2}}{v_{out,\varphi1}} = \frac{C_{\varphi1}}{C_{\varphi2}}. \tag{9}$$

Compared to switched-capacitor discrete-time solutions, the parametric amplifier requires fewer devices (no OpAmps are needed) and needs no charge transfer in the gain phase, which brings an inherent benefit with respect to robustness and speed.

5.1. Design

Based on the considerations in Section 4 and 5, the TFTC can be used as a parametric capacitor to design a discrete-time parametric amplifier. The circuit does not involve active elements and thus does not introduce additional noise, apart from the thermal noise due to the switches involved in the sampling of the analog signal. Moreover, the gain is insensitive to the absolute value of the parametric capacitance, which can be designed to address other requirements like speed ($\tau = C_{PC}R_{switch}$) or noise level (kT/C_{PC}).

The charge accumulated in the first phase does not need to be transferred to a different capacitor, thus it does not require additional settling time for transport. On the other hand, some time is required to commute the semiconductor state. However, the semiconductor works in accumulation and not in inversion, hence the charge carriers do not need to be borrowed by the contacts as in standard silicon technologies, but just need to be collected at the semiconductor-dielectric interface. For this reason, it is possible to create gain without detrimental effects on speed.

Another important point has to be considered: the switching activity of the top-gate metal layer of the new device, needed to change the capacitance value, causes important charge injections on the other plates. The use of two parametric capacitors in a differential amplifier configuration is thus needed to cancel out the spikes due to the charge injection, as the disturbance appears then as a common mode for the differential amplifier that follows them. In the embodiment of Fig. 12, the continuous-time differential amplifier presented in Section 2 is used to process the differential signal at the output of the parametric capacitor amplifier, reject the common mode, and drive the following stages of the signal conditioning chain, or to provide a suitably large input directly to an analog to digital converter.

In the differential parametric capacitor amplifier DPCA (Fig. 12), during the first phase the switches S1 connect the differential input $V_{diff\_in} = V_{in+} - V_{in-}$ to the two PCs. For one of them V_{in+} is connected to the gate and V_{in-} to the source, while for the second PC the gate is connected to V_{in-} and the source to V_{in+}. After the capacitors are charged, the switches S1 are disconnected and the value of the capacitance can be changed varying the control voltage applied to the top-gate. The differential voltage $V_C = V_{C+} - V_{C-}$ is immune from the injection due to the switching control voltage and can be further amplified by the following continuous-time differential amplifier.

Before evaluating the gain provided by the differential PC amplifier, it is important to discuss the missing switch between the differential input and the source terminal of the PCs. Indeed this configuration allows, in the second phase, a direct path from the time variant input to the amplified sampled output. However, the small-signal input applied to the source plate affects the gate plate voltage divided by a capacitive partition (between C_{SG} and C_{TGG}, see Fig. 9a) and it is not

amplified by the PC; for this reason, its contribution to the differential output should be negligible with respect to the sampled value. If it is not the case, an additional switch exploiting the same function of S1 can be also included, though the new switch would require a different synchronization from S1 and the control signal. In fact, if we opened the switches together, all devices would be floating and all potentials would shift with an equal amount of the control voltage, leaving the state of the semiconductor unchanged. For this reason, the second switch would require a delayed trigger providing enough skew to allow the semiconductor to commute its state.

5.2. Analysis

Considering the low quality of the TFTs on foil as switch, the reliability issues of complex circuits, and the small accuracy of data converters, we considered the influence of the direct path of the input to the output a second order effect and opted for a solution without additional switch. Based on this choice, we can evaluate the gain of the differential PC amplifier evaluating the output voltage V_C in the second phase applying charge conservation at the output node of the variable capacitors, i.e. the gate plate. Naming V_{low} and V_{high} the two possible levels of the control voltage applied to the top-gate plate, and referring to Fig. 9a and to Fig. 12 for the capacitance names and for the voltages in the discrete-time amplifier, we can first evaluate the behavior of the voltage on the node V_{C+} between the two phases. The charge on the gate plate of the device connected to the positive terminal of the continuous-time amplifier in the two different phases can be expressed as:

$$Q_1 = (V_{in+} - V_{low})C_{TGG,\varphi1} + (V_{in+} - V_{in-})C_{SG,\varphi1}, \tag{10}$$

$$Q_2 = (V_{C+} - V_{high})C_{TGG,\varphi2} + (V_{C+} - V_{in-})C_{SG,\varphi2}. \tag{11}$$

Imposing the charge conservation, i.e. $Q_1 = Q_2$, V_{C+} can be expressed as:

$$V_{C+} = V_{in+}\left(\frac{C_{TGG,\varphi1}+C_{SG,\varphi1}}{C_{TGG,\varphi2}+C_{SG,\varphi2}}\right) - V_{in-}\left(\frac{C_{SG,\varphi1}-C_{SG,\varphi2}}{C_{TGG,\varphi2}+C_{SG,\varphi2}}\right) + \frac{V_{high}C_{TGG,\varphi2}-V_{low}C_{TGG,\varphi1}}{C_{TGG,\varphi2}+C_{SG,\varphi2}}. \tag{12}$$

The first two terms on the right hand side of this expression represent the effect of the differential input, while the last one gives the common-mode contribution due to the switching activity at the top-gate plate.

At the negative input of the continuous time amplifier, the same process takes place, but the inputs are inverted. Therefore:

$$V_{C-} = V_{in-}\left(\frac{C_{TGG,\varphi1}+C_{SG,\varphi1}}{C_{TGG,\varphi2}+C_{SG,\varphi2}}\right) - V_{in+}\left(\frac{C_{SG,\varphi1}-C_{SG,\varphi2}}{C_{TGG,\varphi2}+C_{SG,\varphi2}}\right) + \frac{V_{high}C_{TGG,\varphi2}-V_{low}C_{TGG,\varphi1}}{C_{TGG,\varphi2}+C_{SG,\varphi2}}. \tag{13}$$

The amplified differential signal $V_C = V_{C+} - V_{C-}$ as a function of the differential input V_{in} is thus independent of the common mode due to the switching activity and can be written as:

$$V_C = V_{in}\left(\frac{C_{TGG,\varphi1}+C_{SG,\varphi1}}{C_{TGG,\varphi2}+C_{SG,\varphi2}} + \frac{C_{SG,\varphi1}-C_{SG,\varphi2}}{C_{TGG,\varphi2}+C_{SG,\varphi2}}\right). \tag{14}$$

The differential gain of the differential parametric capacitor amplifier G_{DPCA} can thus be calculated as:

$$G_{DPCA} = \frac{C_{TGG,\varphi1}+2C_{SG,\varphi1}-C_{SG,\varphi2}}{C_{TGG,\varphi2}+C_{SG,\varphi2}}. \quad (15)$$

The subscript '1' indicates the value of the capacitance in the sampling phase, which takes place with accumulated semiconductor (Equation (6)), and the subscript '2' indicates the value of the capacitance in the second phase, when the semiconductor is depleted (Equation (5)). Since the value of the capacitance in both phases is largely independent of the voltage signal applied to the capacitors (Figure 10), the gain is signal independent providing intrinsic linearity.

The expression of the discrete-time gain G_{DPCA} can be rewritten, using Equation (5) and (6), as a function of the geometry of the device:

$$G_{DPCA} = \frac{2\frac{W_G}{FW}}{\frac{W_G}{FW}+\frac{1}{\eta}} \frac{\eta+1}{\eta}. \quad (16)$$

This equation analytically shows that the gain is independent of the absolute value of the capacitance; indeed, the length of the device L_G is cancelled out in the ratio between numerator and denominator. In our technology, the coupling of the top-gate is $\eta = 0.25$, which leads, if $W_G >> FW$, to a maximum theoretical gain equal to

$$G_{DPCA,max} = 2\,\frac{\eta+1}{\eta} = 10. \quad (17)$$

6. A sensor frontend combining discrete- and continuous-time amplification

The complete sensor frontend includes the discrete-time amplifier and the continuous-time amplifier (Fig. 12). The considerations in Section 2 on continuous-time amplification are not affected by the use of TFTs with top-gate. However, some interesting observations can be made for double-gate technologies. Connecting together gate and top-gate of the input transistors (see M2 and M4 of Fig. 2 and Fig. 6b) increases the input transconductance by a factor 1+η (in line with Equation (1) and (2)), while, concerning the devices used in a Zero-Vgs configuration (M1, M3 and M5), the top-gates should be connected to their own source terminal, in order to prevent detrimental effects on the output resistance due to the threshold voltage variation.

The top-gate voltage could also be used for more sophisticated purposes (see, e.g. [15]). For instance, the tail top-gate could be used within a common-mode feedback network to control the output common-mode, and the load top-gates could be used to zero the offset of the amplifier due to mismatch between M2 and M4, and between M1 and M5.

The gain of the DPCA increases proportionally the gain of the continuous-time differential amplifier (Fig. 13) without any detrimental effect on its speed. Indeed, the bandwidth of the parametric capacitor is much higher than any normal continuous-time differential amplifier topology known in this technology. The increased gain and preserved speed are confirmed in Fig. 13, where two simulated transients are shown. The continuous line corresponds to the system

exploiting the differential parametric capacitor amplifier together with the continuous-time differential amplifier, while the dashed line is obtained using a just normal capacitor instead of the parametric capacitor. The differential input was set to 10 mV and the simulated gain of the continuous-time differential amplifier $G_{DiffAmpl}$ is about 11, in agreement with the data measured on its real implementation. The shape of the step response is the same in both cases, but the amplitude of the output signal is almost ten times larger using the differential parametric capacitor amplifier, as one would expect from Equation (17).

In simulation, none of these results could be achieved using conventional circuit methods like cascading two continuous-time differential amplifiers. When cascading amplifiers, indeed, the gain is strongly reduced by the mismatch between the output common mode of the first stage and the input common mode of the second one. The use of a level shifter would reduce this problem, but would introduce a gain loss itself. Also the time response of a cascade of amplifiers worsens due to the presence of two low-frequency singularities instead of one.

The last important benefit of the proposed solution is the wider input common mode range. Indeed the DPCA allows almost any input common mode within the supply and its output common mode depends almost exclusively on the voltage step applied to the top-gate. In this way the continuous-time differential amplifier can always be used at its ideal bias.

7. Conclusion

Organic electronics manufactured with only p-type semiconductor suffer from many drawbacks due to the low mobility and to the low intrinsic gain of organic TFTs. These technology limitations affect heavily the performance of analog circuits, especially hampering the use of negative feedback configurations and resulting in low gain (typically < 30) and poor gain accuracy. In sensor frontend applications, a S&H circuit is often used together with a low noise amplifier in order to relax the speed constraints on the analog to digital converter. In this paper, we proposed a new device implementing a Thin-Film Trans-Capacitor (TFTC) that can be used to sample and amplify the signal coming from the sensor before a conventional continuous-time fully-differential amplifier. The parametric amplification takes place with no additional low-frequency singularities, and therefore improves the gain of the frontend (of a factor ~10 for the technology we used) while preserving its speed. Moreover the gain is independent of the absolute value of the input capacitance that can therefore be sized to fulfil speed or noise specifications. Also, the parametric amplification is intrinsically linear. Even if experimental data on matching and ageing are not available yet, both these effects should have a limited effect on the results presented in this work, in fact the thickness of the insulator is better controlled than other TFT parameters (e.g. threshold voltage, mobility) and is not affected by time and bias stress.

List of figure

List of references

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[14] D. Raiteri, F. Torricelli, P. van Lieshout, A.H.M. van Roermund, E. Cantatore, A synchronous rail-to-rail latched comparator based on double-gate organic thin-film-transistors, Proceedings of IEEE ESSCIRC 2012, pp.141,144, 17-21 Sept. 2012.

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Figure 1

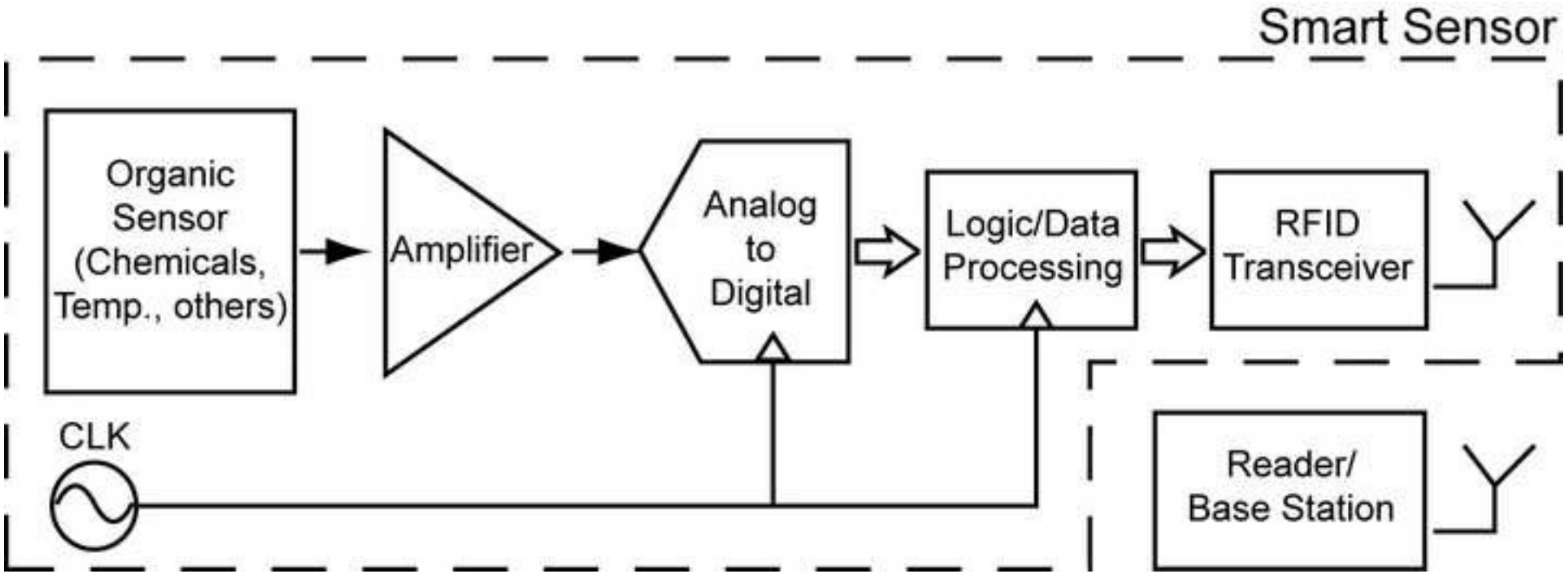

Smart Sensor
Organic Sensor (Chemicals, Temp., others)
Amplifier
Analog to Digital
Logic/Data Processing
RFID Transceiver
CLK
Reader/ Base Station

Figure 2

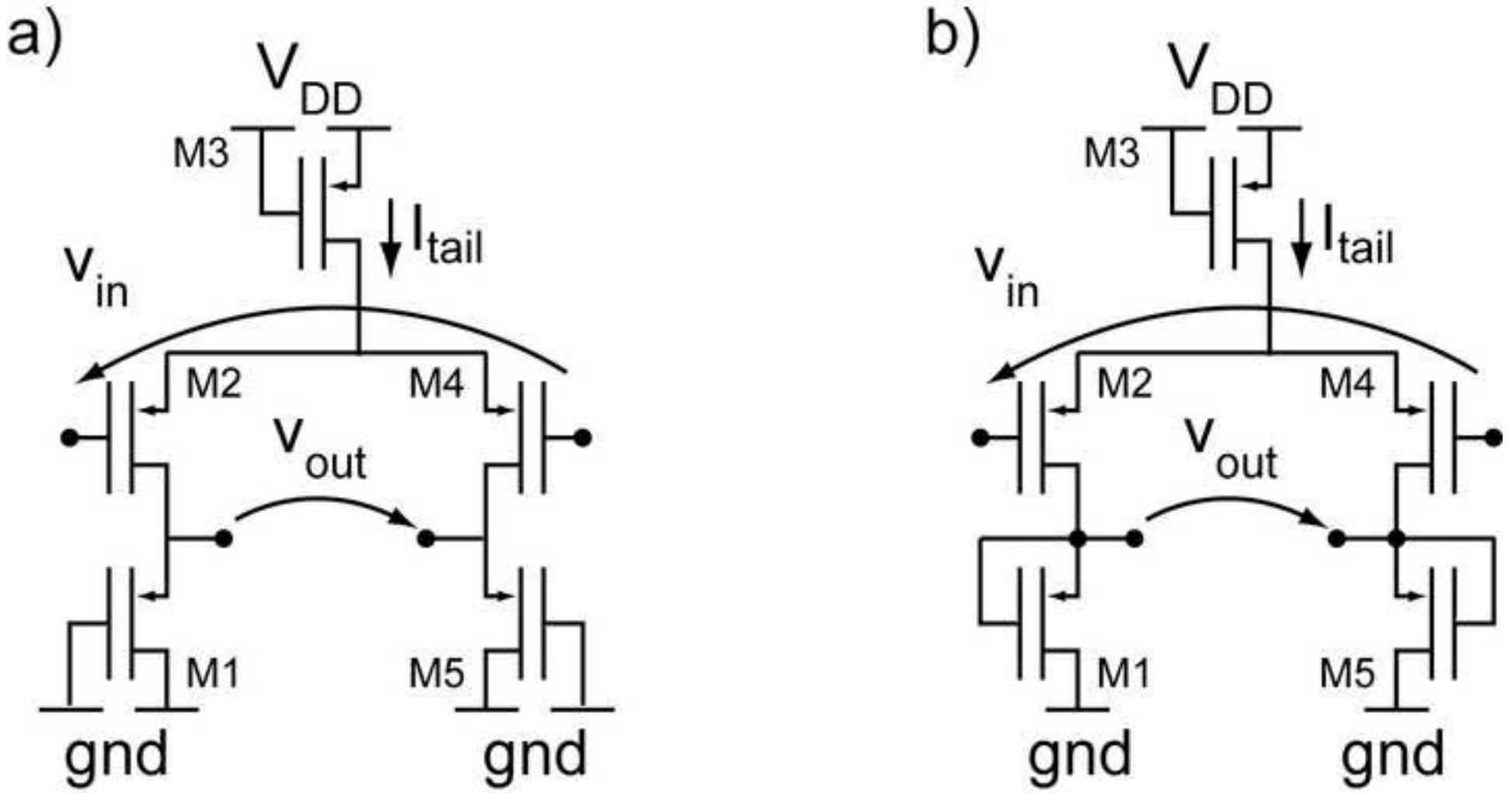

a)
V DD
M3
I tail
v in
M2
M4
v out
M1
M5
gnd
gnd
b)
V DD
M3
I tail
v in
M2
M4
v out
M1
M5
gnd
gnd

Figure 3

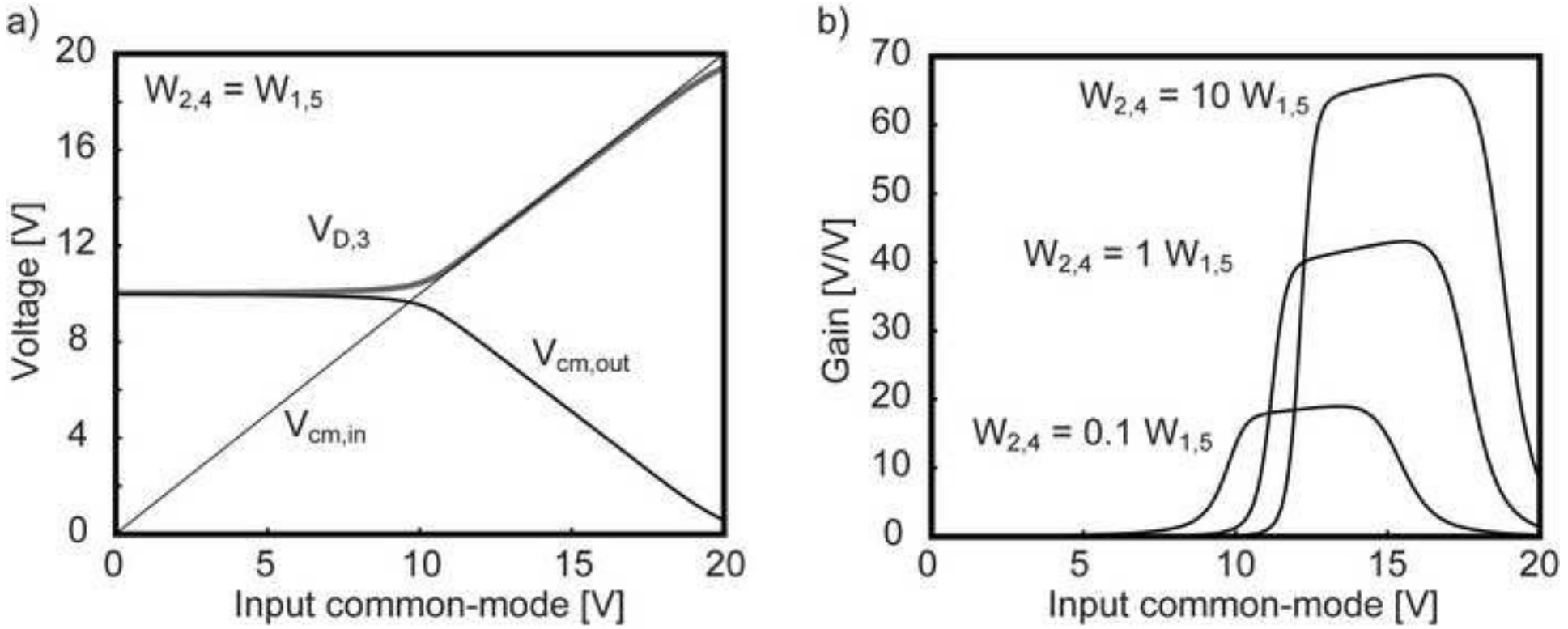
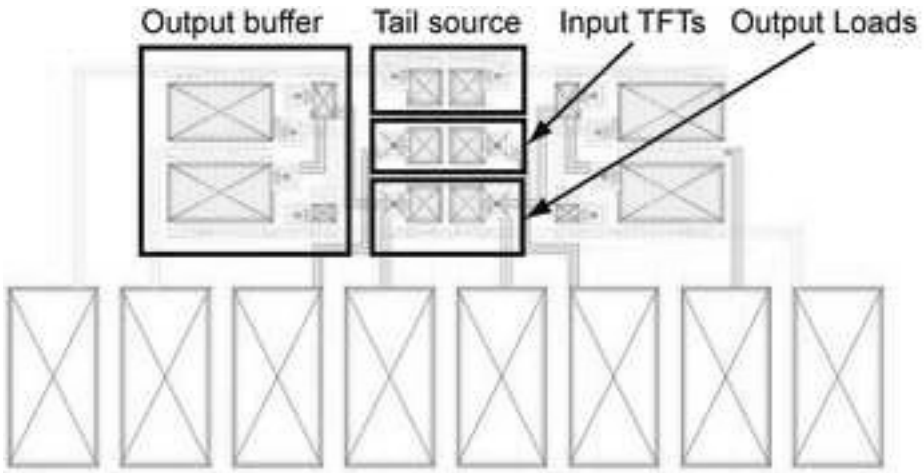

a)
$W_{2,4} = W_{1,5}$
$V_{D,3}$
$V_{cm,out}$
$V_{cm,in}$
Voltage [V]
Input common-mode [V]
0
4
8
12
16
20
0
5
10
15
20
b)
$W_{2,4} = 10\ W_{1,5}$
$W_{2,4} = 1\ W_{1,5}$
$W_{2,4} = 0.1\ W_{1,5}$
Gain [V/V]
Input common-mode [V]
0
10
20
30
40
50
60
70
0
5
10
15
20

Figure 4



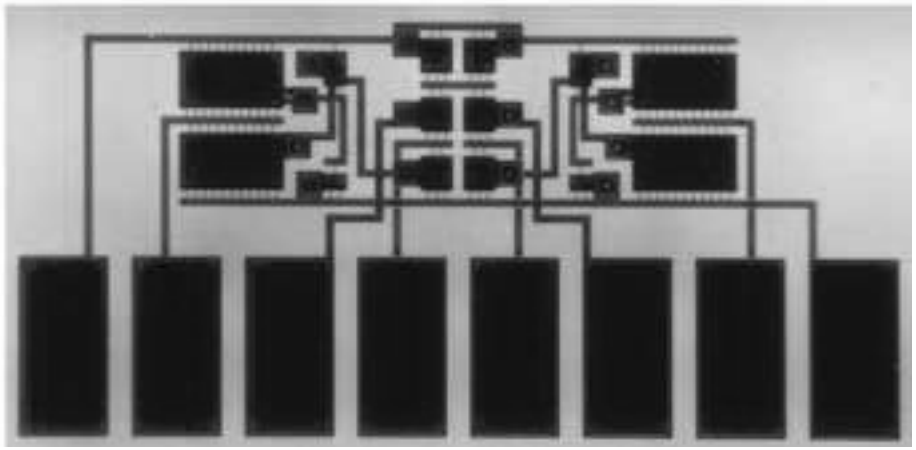


Figure 5

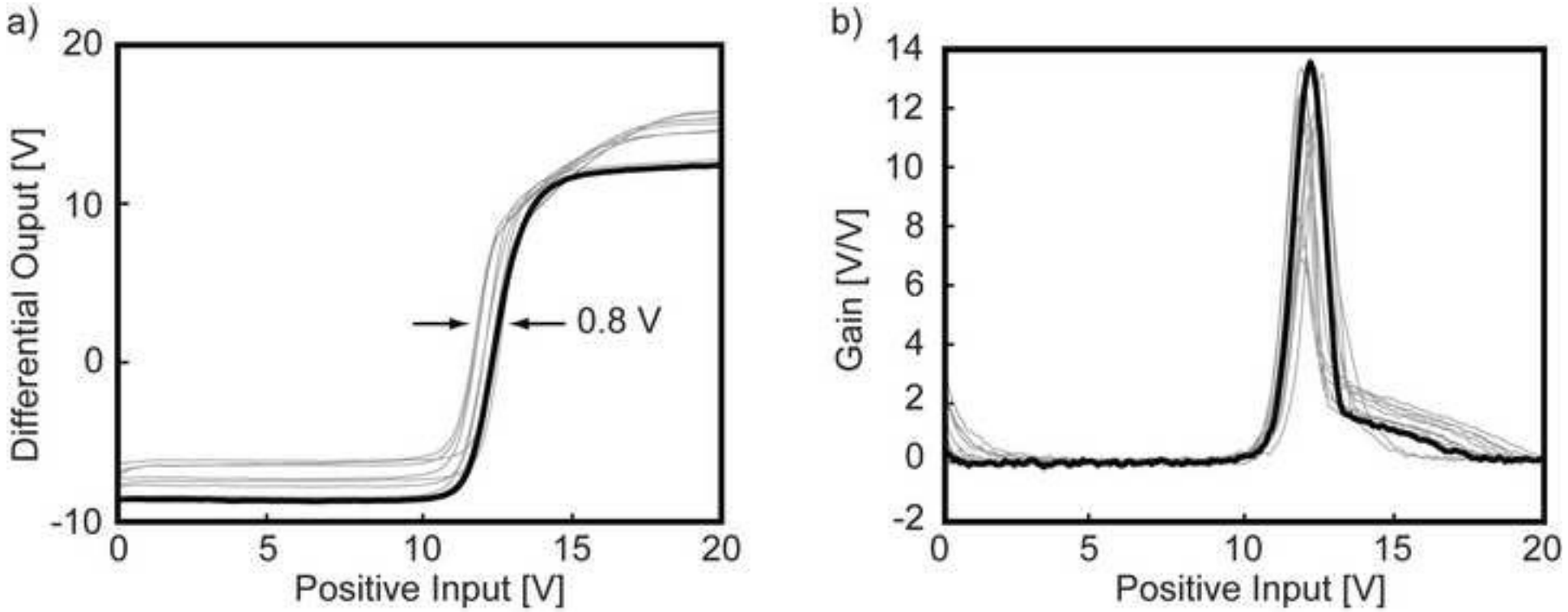

a)
Differential Ouput [V]
20
10
0
-10
0
5
10
15
20
Positive Input [V]
0.8 V
b)
Gain [V/V]
14
12
10
8
6
4
2
0
-2
0
5
10
15
20
Positive Input [V]

Figure 6

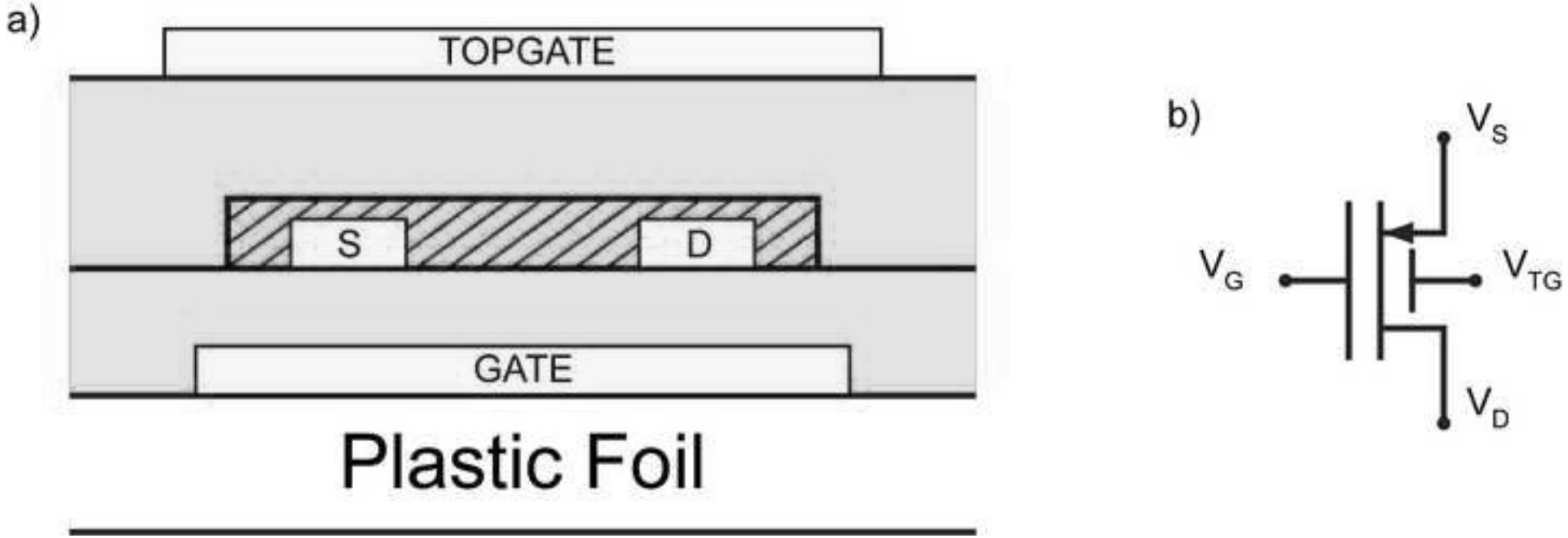


Figure 7

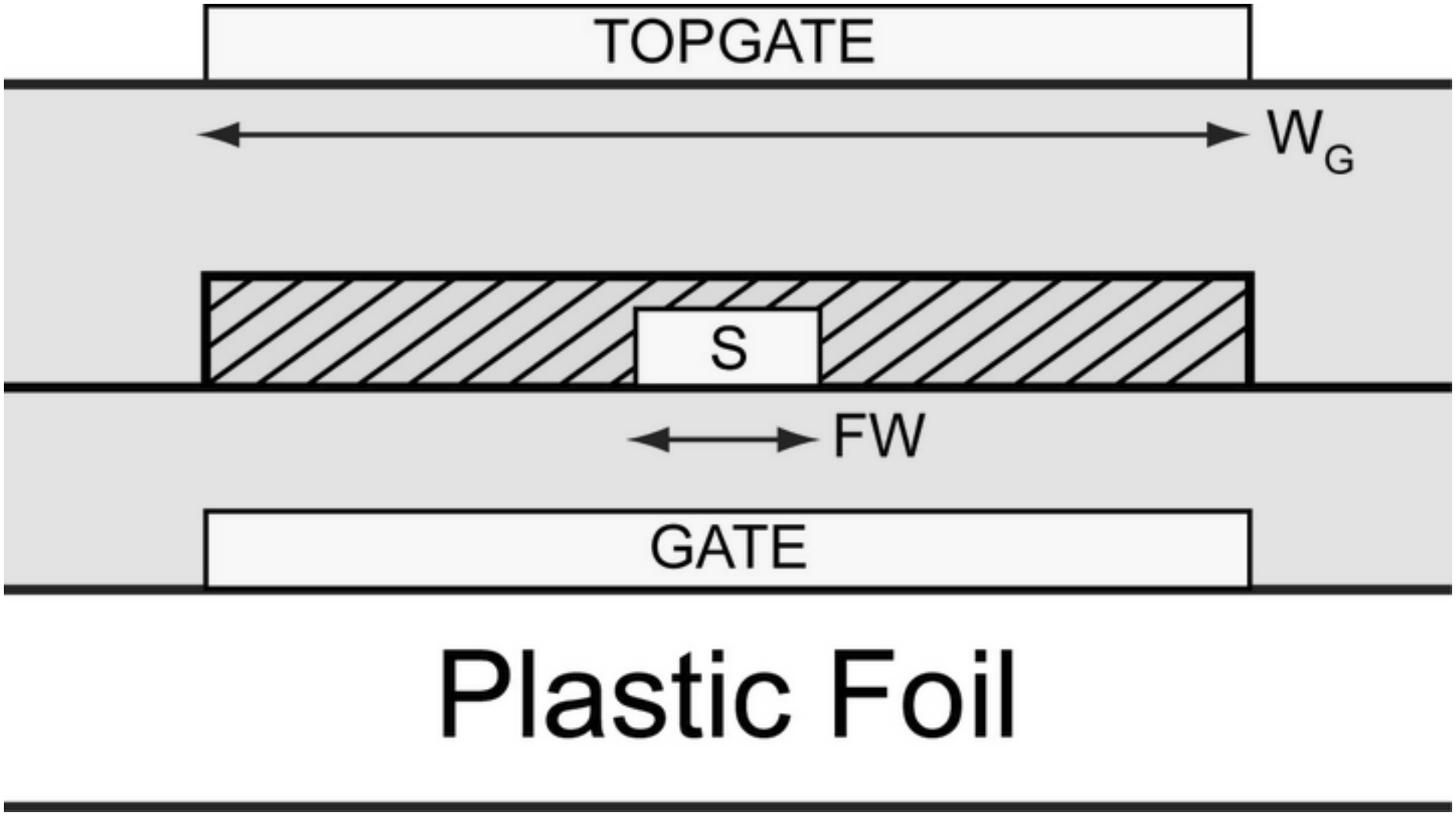


Figure 8

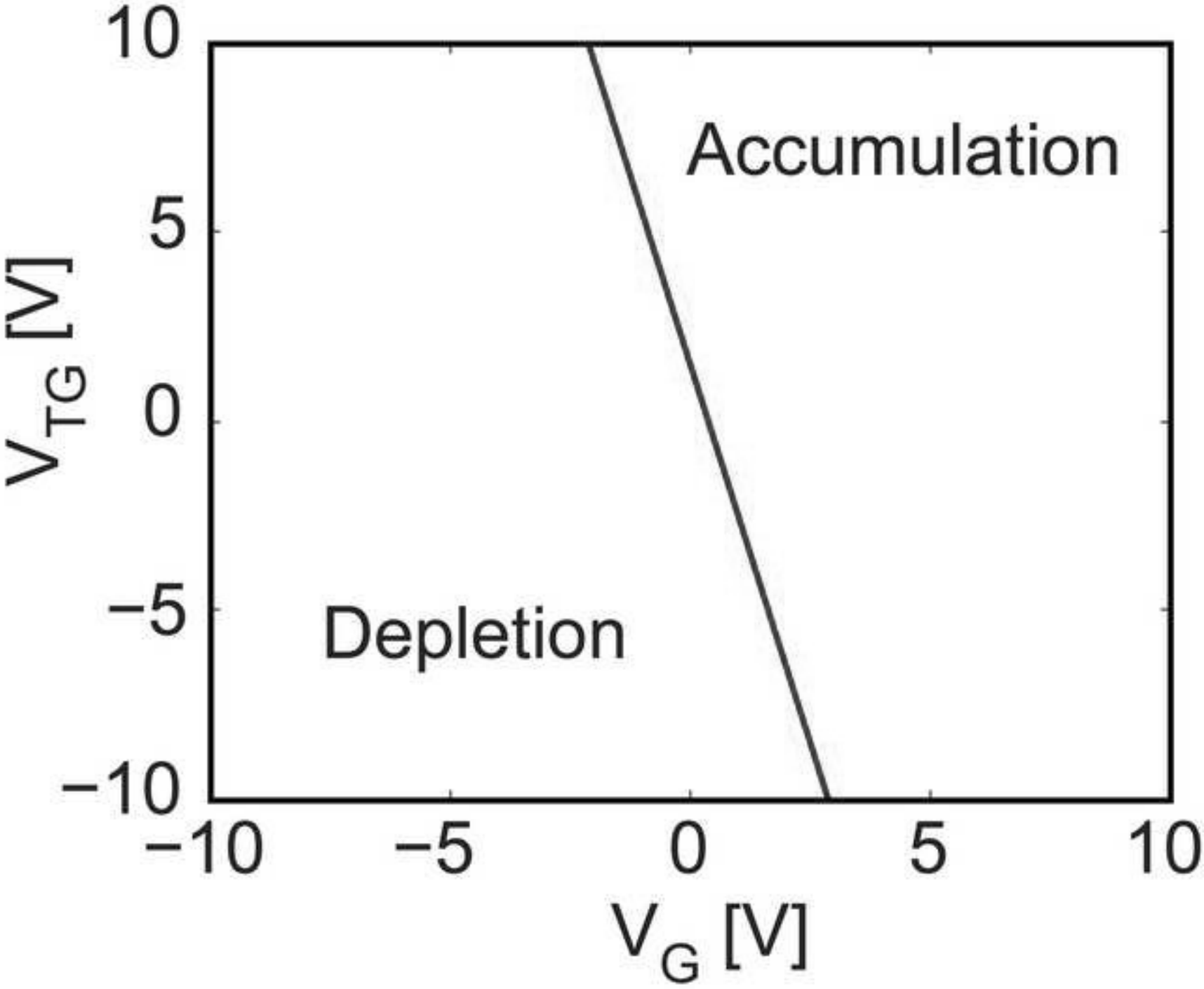


Figure 9

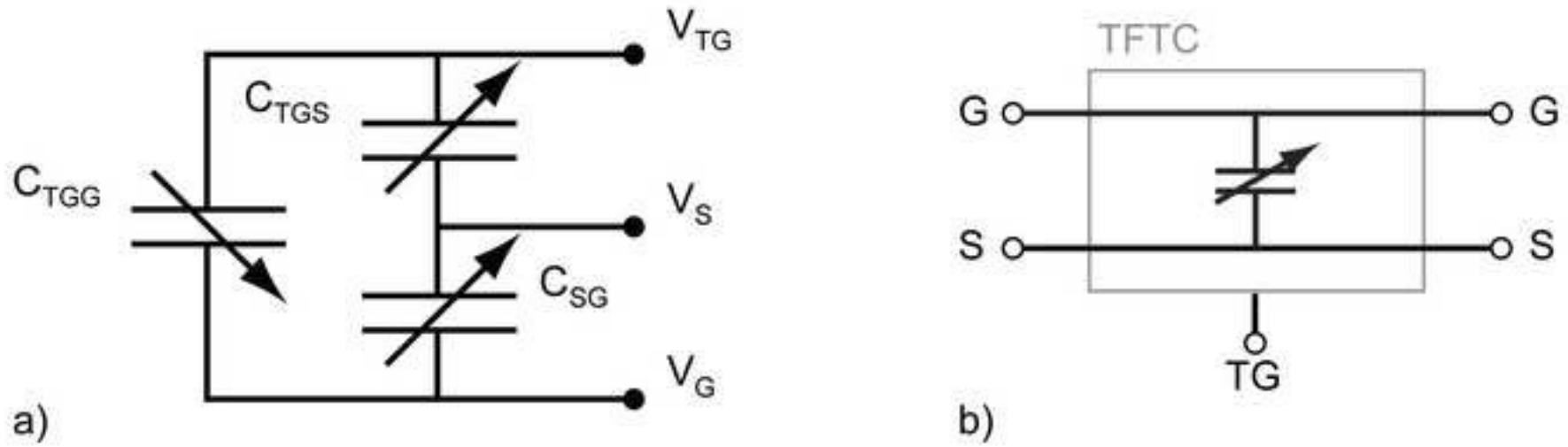


Figure 10

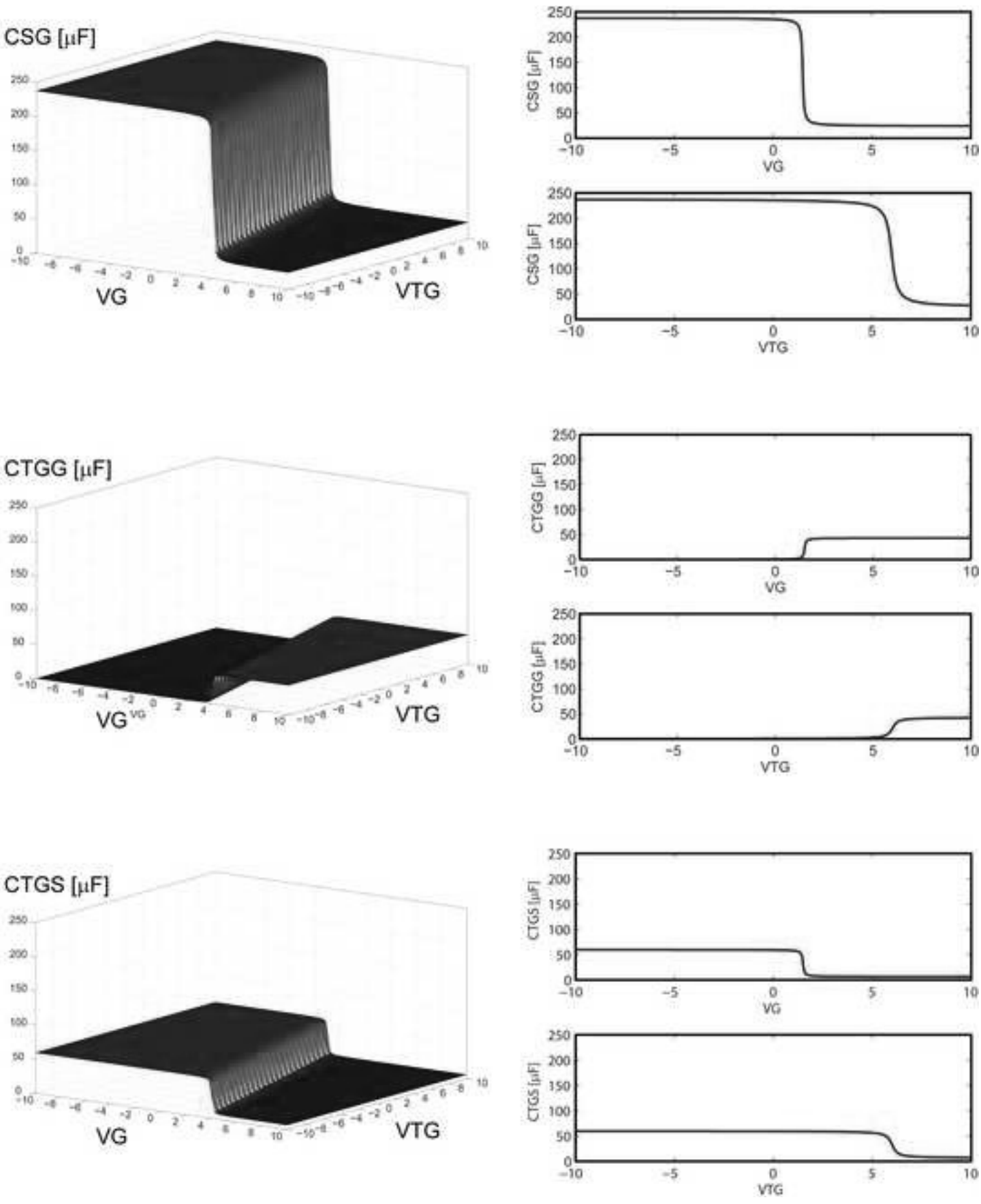

CSG [μF]
VG
VTG
CSG [μF]
VG
CSG [μF]
VTG
CTGG [μF]
VG
VTG
CTGG [μF]
VG
CTGG [μF]
VTG
CTGS [μF]
VG
VTG
CTGS [μF]
VG
CTGS [μF]
VTG

Figure 11

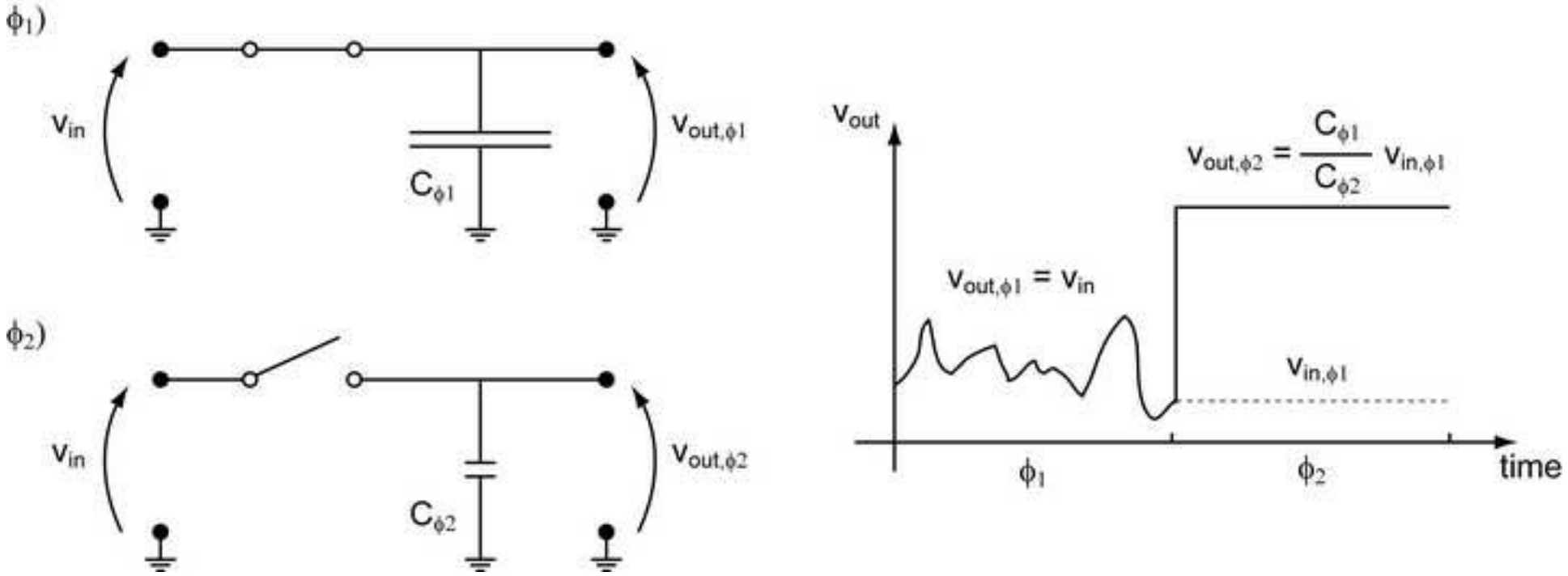

ϕ1)
Vin
Vout,ϕ1
Cϕ1
ϕ2)
Vin
Vout,ϕ2
Cϕ2
Vout
Vout,ϕ2 = Cϕ1/Cϕ2 Vin,ϕ1
Vout,ϕ1 = Vin
Vin,ϕ1
ϕ1
ϕ2
time

Figure 12

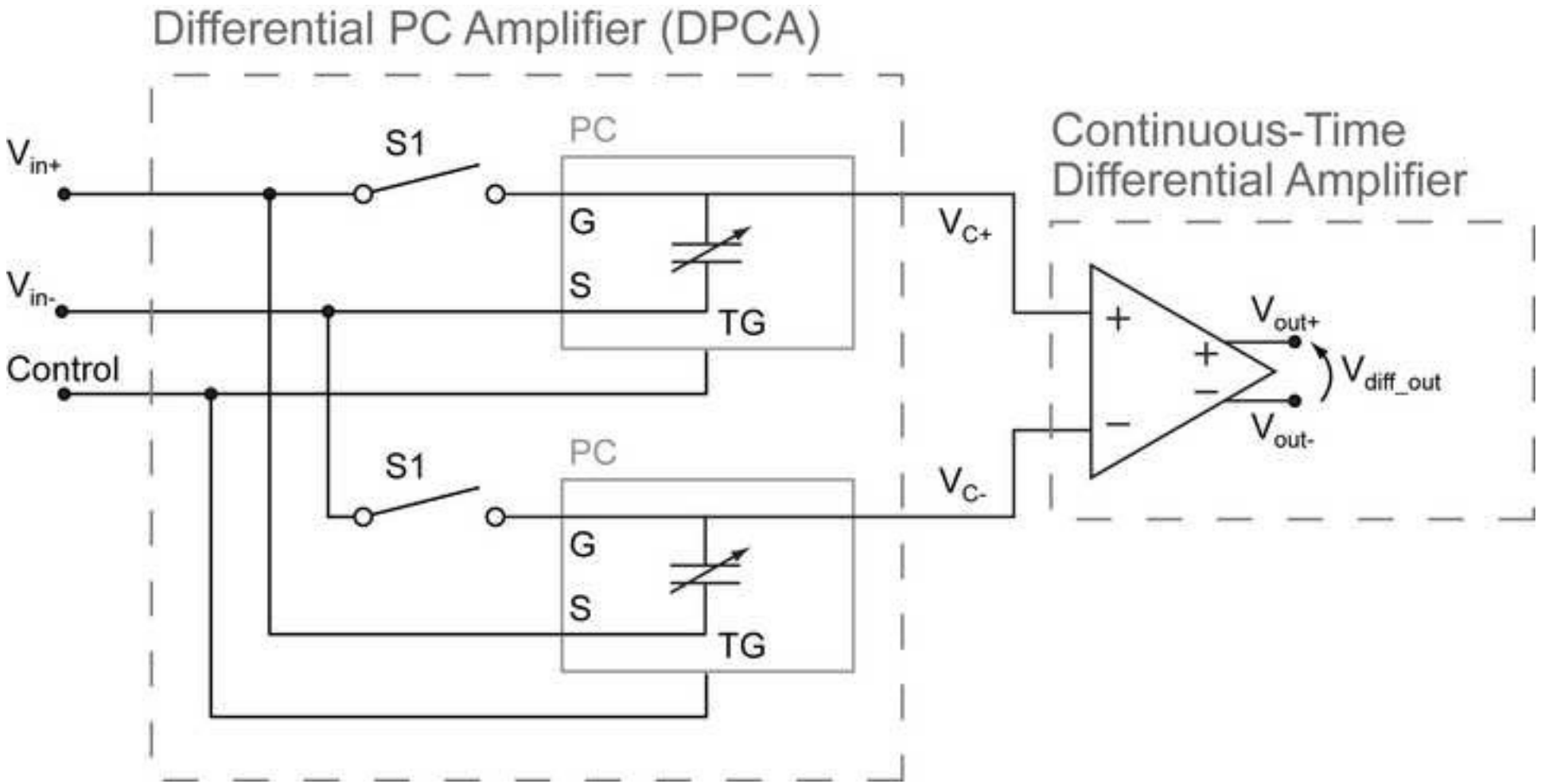
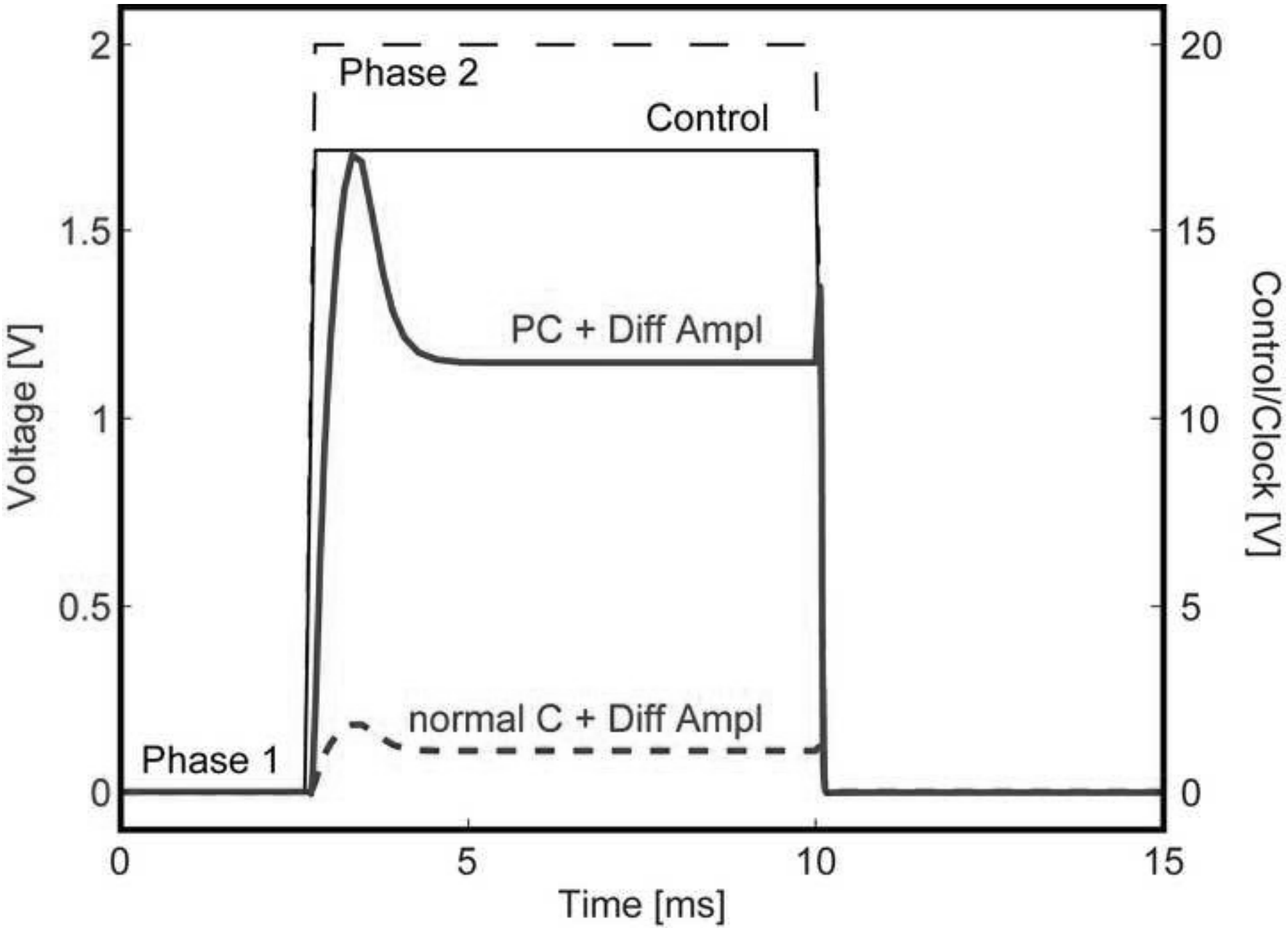

Differential PC Amplifier (DPCA)
PC
S1
G
S
TG
PC
S1
G
S
TG
Control
V_{in+}
V_{in-}
V_{C+}
V_{C-}
Continuous-Time
Differential Amplifier
V_{out+}
V_{out-}
V_{diff_out}

Figure 13


Phase 2
Control
PC + Diff Ampl
normal C + Diff Ampl
Phase 1
Voltage [V]
Control/Clock [V]
Time [ms]
0
0.5
1
1.5
2
0
5
10
15
20