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Charge transport and light emission in organic field-effect transistors

PROEFSCHRIFT

ter verkrijging van de graad van doctor aan de Technische Universiteit Eindhoven, op gezag van de rector magnificus prof.dr.ir. C.J. van Duijn, voor een commissie aangewezen door het College voor Promoties, in het openbaar te verdedigen op woensdag 12 november 2014 om 16:00 uur

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Chapter 1

Introduction

1.1 Rise of the field-effect transistor

A transistor is a micro-electronic device used to manipulate a current between two contacts with an external bias voltage on a third contact. One class of transistors is the so-called field-effect transistor (FET). They consist of a metal (the 'gate') and a semiconductor (the 'active layer') to which the drain and source electrodes are connected laterally to inject and collect carriers. An insulator separates these two layers. Biasing the gate causes charge in the semiconductor, to form a conductive 'channel'. This charge increases the conductance of the semiconductor layer. It can thus be said that the gate is programming the resistance of the channel in the semiconductor, hence the name trans-resistor, or 'transistor' for short.[1]

The idea of the field-effect transistor was first suggested by Linienfield in 1926.[2] In 1948, the first point-contact transistor was realized at Bell laboratories, for which the Nobel prize in physics was awarded in 1956.[3] Four years later, in 1960, the first field-effect transistor was fabricated in the same laboratories.[4] For this transistor the metal-oxide-semiconductor design was used. The majority of today's transistors, and also the transistors used in this thesis, are based on this concept. An important breakthrough for the success of transistors was the invention of the integrated circuit at Texas Instruments around 1960, for which the Nobel prize in physics was awarded in 2000.[5] The integrated circuit allows packing many transistors on a small surface area. Since then an enormous progress has been made in scaling down the lateral dimensions of the transistor. Hereby the transistor density has been increased, reaching over 1 billion transistors that can nowadays be found in a commercial computer chip. Transistors are now applied in all electronic appliances such as televisions, mobile phones, and even washing machines. In fact the transistor became vital for society in less than 50 years. Without the field-effect transistor, today's life would look completely different.

1.2 Organic field-effect transistors

Silicon technology has been the dominant force in integrated device manufacturing and will retain this position in the foreseeable future. Every application that can be miniaturized can be fulfilled with standard silicon components. However the use of single crystalline silicon is cost prohibitive for applications that cannot be miniaturized. That holds for large area electronics where numerous discrete devices have to be integrated on low-cost substrates as glass or plastic. Large area production is envisaged to be via on foil via e.g. roll-to-roll processing, therefore this application area is also called system-on-foil.

Currently amorphous silicon is used for large area production, but different semiconducting materials are being investigated. One class of materials are organic

semiconductors, such as polymers. Polymers are well known for their insulating properties. However, in 1977 organic semiconducting polymers were found in which the electrical conductivity could be increased by more than 7 orders of magnitude via chemical doping , which was rewarded with the Nobel prize in chemistry in 2000.[6] The progress realized in stability and processability of conjugated polymers has triggered research on their use as the active element in microelectronic devices. The main advantages of the application of semiconducting polymers are their easy processing, e.g. spin coating, inkjet or silk-screen printing, and their mechanical flexibility. Their physical and materials properties can be tuned by organic chemistry. Many polymers are soluble, allowing processing from solution which is ideal for processing in large areas and high volumes. Moreover, the processing temperatures of these organic semiconductors are generally low, allowing fabricating the semiconductors on flexible and light-weight substrates.

The performance of solution processed organic field-effect transistors (OFETs) has steadily increased during the last few years. The transistors meet mobility and stability requirements to be applied in simple integrated circuits.[7-8] Recently, solution processed polymers have been developed with a mobility of over 10 cm^2/Vs,[9] which is an order of magnitude higher than that of amorphous silicon.[10]

1.2.1 Applications of organic transistors

Transistors are traditionally used as an electrical switch in logic circuits. A promising application of the organic transistor is the radio-frequent identification (RFID) tag, which is used to read out information wirelessly.[11-12] The required speed of the transistors in 13.56 MHz RFID-tags can be reached with organic semiconductors, while the advantages of organics can be exploited when fabricating flexible tags at low cost in high volumes. Another promising application for organic transistors is the use in biological enviroments.[13-14] Not all materials are suitable for biological purposes, but organic semiconductors offer a variety of materials that seem to be appropriate. Polymers are investigated for drug delivery and organic transistors have already been used to readout neuronal activity.[14-17]

The key property of the field-effect transistor is the ability to accurately control the charge density in the organic semiconductor by the gate. This property makes it a valuable test-bed for fundamental research investigating charge transport in organic semiconductors. Charge density control may also be exploited for applications as for instance sensors. Gas sensors have been based on transistors, where sensitivities down to the ppb level were reached by accurately tuning the charge density.[18-20]

Conjugated polymers are typically wide bandgap semiconductors with an optically allowed absorption and emission in the visible region. This property makes the organic materials suitable for light-emitting and photovoltaic applications. Light emission is regularly obtained in an organic light-emitting diode (OLED), in which an organic semiconductor is sandwiched between two electrodes. By applying a bias over the diode, holes are injected by one electrode and electrons are injected by the other. The charge carriers meet in the semiconductor and recombine to form excitons. These excitons subsequently decay by the emission of light. OLEDs are already commercially available in for instance mobile telephones, television screens and lamps. Recently even curved displays based on organic light-emitting diodes (OLEDs) have been introduced into the market, starting to exploit the benefits of organic materials. The brightness obtained in OLEDs is, however, restricted due to a limited efficiency at high current densities.[21] The transistor offers control over the charge density in the semiconductor. By simultaneously injecting holes and electrons in a transistor, high light intensities can be obtained in a so-called 'light-emitting field-effect transistor' (LEFET).[22] To improve the transistor performance, knowledge of the transistor operation mechanism is required, both on the macroscopic- and on the microscopic scale.[23] Below first the general working mechanism of field-effect transistors is explained. Subsequently, charge transport models in organic materials on a microscopic scale are discussed. Finally the role of contacts is discussed and the LEFET is further introduced.

1.2.2 Operation mechanism of OFETs

The lay-out of a field-effect transistor is schematically presented in Figure 1.1a. Charges are injected at the source contact and are collected by the drain contact. By applying a bias to the third electrode, the gate, charges are accumulated at the semiconductor-gate dielectric interface, yielding a conducting channel. A typical transfer characteristic is shown in Figure 1.1b, where the source-drain current is presented as a function of gate bias. By modifying the gate bias, the conductivity of the channel is changed and the transistor can be switched in to a highly conducting on-state and a low conducting off-state. The OFET switches from the off- to the on-state at the threshold (gate) voltage, V_{th}.

When a transistor is able to transport just one type of charge carrier the transistor is called unipolar. The transistor is *n*-type when the carriers are negative (electrons) or *p*-type when the carriers are positive (holes). A transistor that conducts both electrons and holes is ambipolar. A typical transfer characteristic of an ambipolar OFET is shown in Figure 1.1e. The transistor is in the on-state, at negative as well as at positive gate biases. Holes are accumulated at large negative gate biases and electrons are accumulated at

large positive gate biases. At intermediate biases, when the gate bias is in between the source and the drain bias, both electrons and holes are accumulated, as schematically depicted in Figure 1.1b. In this ambipolar regime a low number of charges is accumulated and therefore the current is low. Copolymers with diketopyrrolopyrrole (DPP) units have recently emerged as attractive materials with good ambipolar properties and will therefore be used in this thesis.[41]

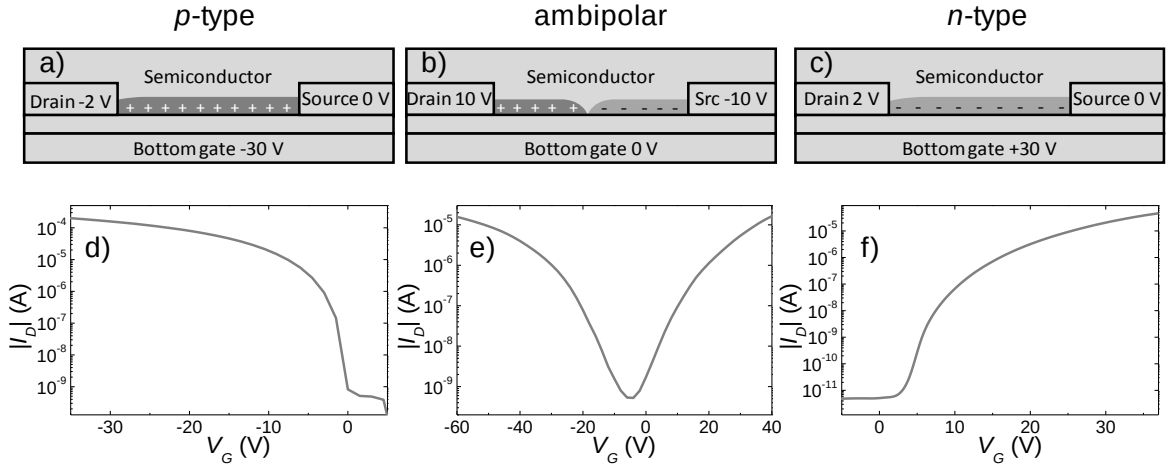

Figure 1.1: a)-c) Schematic illustration of an organic field-effect transistor. d)-e) Transfer characteristics. a),d) An unipolar *p*-type transistor, b),e) an ambipolar transistor, and c),f) an unipolar *n*-type transistor.

When the drain bias, V_D, is small compared to the effective gate bias, V_G - V_{th}, the transistor functions in the linear regime ($|V_D| << |V_G - V_{th}|$). The source-drain current increases linearly with drain bias. In this regime the charge density in the accumulation layer may be approximated as being constant throughout the channel. The source-drain current in the linear regime I_D can then be described by:

$$I_D = \mu V_D (V_G - V_{th}) C_G W / L \tag{1.1}$$

with W and L the width and length of the transistor, C_G the gate capacitance, and μ the charge carrier mobility. The mobility in organic semiconductors generally depends on the charge carrier density, which varies by the gate bias. The dependence of the mobility on the gate bias varies from device to device, which makes that the threshold voltage is generally ill defined. Therefore, the mobility is usually extracted by taking the first derivative of the source-drain current to the gate bias:

$$\mu_{lin} = \left| \frac{L}{W C_G V_D} \frac{\partial I_D}{\partial V_G} \right| \tag{1.2}$$

1.3 Charge transport models

In crystalline inorganic semiconductors charge transport is typically described by band transport. Organic semiconductors however are disordered and therefore the electrical transport has to be described differently. The transport in organic field-effect transistors

has been described by various models, which have recently been reviewed extensively.[24-26] In these models charges are localized as a result of energetic disorder. The charge transport is dominated by thermally assisted hopping of carriers between localized states. The transport process is schematically depicted in Figure 1.2.

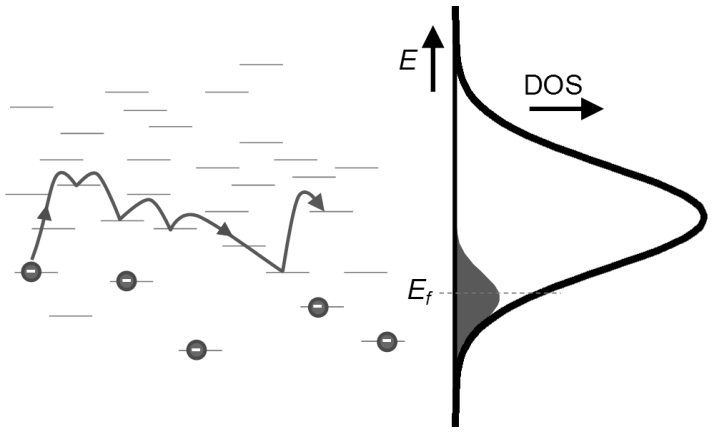

Figure 1.2: Schematic of charges hopping through a disordered energy landscape in the LUMO, where states are distributed Gaussian in energy, *E*. States are filled up to the Fermi level E_F.

Crucial for the charge transport is the distribution of the localized states in energy and space. This distribution is described by the density of states (DOS). Generally a certain shape of the density, typically an exponent or Gaussian, is assumed and its width and height are fitted to describe the measurements.[25, 27-28] The two most commonly used transport models are the variable range hopping (VRH) model and the mobility edge (ME) or multiple trapping and release (MTR) model. In the VRH-model the conductivity is essentially described by a network of hopping sites, where the hopping rate of each hop is determined by the distance and the energy distance of the hop.[28-29] Effectively, the charge transport of the entire network is assumed to be determined by the most difficult hops in the network. In the ME-model band transport is assumed to occur above a certain 'mobility edge'-energy.[30] In these models the mobility is assumed constant in the band and zero in states below the mobility edge. Charge carriers need to be excited above the edge to participate in the charge transport. Effectively, the device conductivity is set by the fraction of carriers that is thermally excited in the conduction band.

The ability to control the charge density in the semiconductor makes the OFET an useful test-bed to experimentally study charge transport. By varying the gate bias information about the conductivity is gained as a function of the doping level of the semiconductor. To test charge transport models, typically the transistor source-drain current is measured as function of temperature, drain bias, and gate bias. Both the VRH-model and the ME-model are generally able to describe the macroscopic electrical properties of an OFET, while the underlying physical principles in these models are fundamentally different. Additional information is needed to distinguish between the

various models. To this end the dataset can be extended with information about the Seebeck coefficient or the potential distribution in the transistor channel.[31-32] Alternatively the shape of the DOS can be measured, as will be shown in Chapter 2.

1.4 Contact resistance

A crucial step in charge transport in OFETs is the injection of charges from the source into the organic semiconductor. For injection, charges need to overcome an energy barrier. This energy barrier depends on the energy level alignment at the semiconductor-metal interface. The relevant energy levels of organic semiconductors are the highest occupied molecular orbital (HOMO) and the lowest unoccupied molecular orbital (LUMO). A schematic energy diagram of these energy levels is presented in Figure 1.3a. The HOMO and the LUMO are separated in energy by the bandgap energy. For hole conduction, holes need to be injected from the Fermi level E_F of the metal contact into the HOMO and for electron conduction electrons need to be injected from the Fermi level into the LUMO. When the energy difference between the Fermi level and the HOMO (LUMO) level is larger than a few times the thermal energy, k_{BT}, there will be an energy injection barrier for holes (electrons).

The injection energy barrier is usually modeled as a contact resistance, R_C. This resistance is in series with the channel resistance, $R_{channel}$, as depicted in Figure 1.3b. Ideally, the resistances for injection and extraction of charges are low compared to the resistance of the transistor channel. Then the behavior of the transistor is fully determined by the transistor channel as described in Equation (1.1). Lots of research on OFETs has focused on reducing the contact resistance, which has recently been reviewed.[33]

In Chapter 5 contact resistance turns out to be essential for describing LEFETs. Moreover, when neglecting contact resistance in extracting the carrier mobility in OFETs, strongly deviating numbers may be found as described in Chapter 4. This shows that the presence of injection barriers can be crucial for the device behavior.

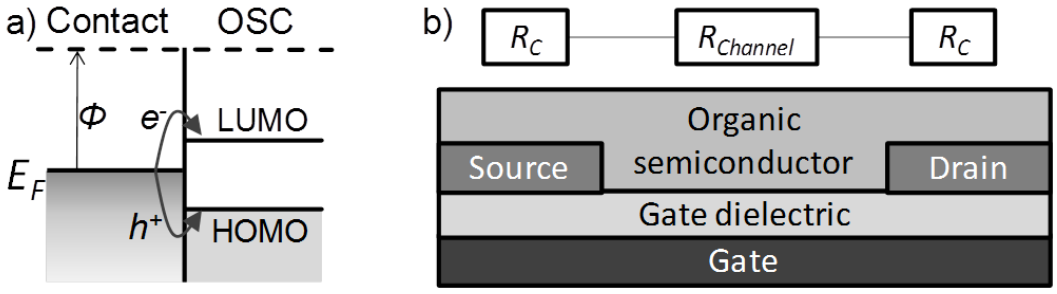

Figure 1.3: a) Energy diagram of the interface between a metal contact and the organic semiconductor (OSC). The dashed line represents the vacuum level. b) Schematic of an OFET with equivalent circuit where the R_c's represent the resistance associated with the injection and extraction of charges at the contact-semiconductor interfaces.

1.5 Light-emitting organic field-effect transistor

Light-emitting organic field-effect transistors (LEFETs) are being investigated as a potential source for bright light emission.[22, 34-35] For light emission holes and electrons need to recombine, hence both have to be present in the semiconductor. In the ambipolar regime both charges are accumulated simultaneously, where the gate is biased in between the source and drain voltage. The charge carriers meet in the channel of the transistor, where electrons and holes recombine to form excitons and decay by the emission of light. The light output depends on the recombination rate which is proportional to the product of accumulated electron and hole density, on the singlet-triplet formation ratio, and on the photoluminescence efficiency of the semiconductor. Furthermore, excitons may be lost due to quenching of excitons by polarons, quenching by the electrodes or by exciton-exciton annihilation. These losses suppress light emission.

The advantage of a field-effect transistor for light emission is the control of the recombination zone. By biasing the gate in between the source and the drain voltage, the recombination zone can be set in the middle of the channel, as shown in Figure 1.1b.[36-38] Recombination then occurs away from the metal contacts and contact quenching is thereby avoided. Indeed, high external quantum efficiencies have been reported in transistors.[22] Remarkably however, there are many examples in literature where electroluminescence is observed when the transistor is operated in one of the unipolar regimes (Figure 1.1a or 2.1c).[39-40] This is unexpected, the light emission should be completely suppressed in the unipolar regime, because then only one type of charge carrier is accumulated. This 'unipolar light emission' will be discussed and explained in Chapter 5.

Recently developed polymers show high mobilities for both electrons and holes.[41] The current densities in transistors can be high enough to reach the threshold for electrically pumped lasing. However, these current densities can only be realized in the unipolar regime of the transistor, where the gate bias is larger than the drain bias. Unfortunately light emission is then impeded, because only one type of charge carrier is accumulated. On the other hand, the highest recombination efficiency is obtained when the transistor is biased in the ambipolar regime where the current is inherently low. The challenge in organic LEFETs is to find a way to utilize the high current densities found in the unipolar regime and combine this with the high EL efficiencies found in the ambipolar regime.[34] In order to meet this challenge, in Chapter 6 a transistor with two gates is investigated for enhanced light emission.

1.6 Scope of this thesis

The aim of the research described in this thesis is to improve the description of charge transport of organic transistors and improve light emission from the transistors. For that crucial physical aspects of the transistor are studied. First the microscopic charge transport properties of OFETs are discussed in Chapters 2 and 3. Then the effect of contact resistance on transistors is investigated in Chapters 4 and 5. Subsequently in Chapters 5 and 6 the OFET will be applied for light emission and in Chapter 7 for logic circuitry. In more detail:

In **Chapter 2** the organic semiconductor in an OFET is studied microscopically. The density of states is extracted using 'Scanning Kelvin probe microscopy' (SKPM). The applicability range of the measurement technique is pushed to its fundamental limit by measuring a semiconductor of only a single monolayer thick. The description of the charge transport is improved by using the measured density of states. This shows that detailed knowledge of the density of states is a prerequisite to consistently describe the transfer characteristics of organic field-effect transistors.

In **Chapter 3**, scanning tunnelling microscopy (STM) is performed on an OFET. So far STM has not been accessible for in-situ characterization of organic semiconductors due to their low intrinsic conductivity. The hole accumulation layer created at sufficiently negative gate bias can however act as back contact, allowing a tunnelling current. Intrinsic organic semiconductors can therefore be in-situ characterized with high spatial and energetic resolution in functional devices.

In **Chapter 4** a novel technique is developed to measure the mobility in a transistors independent of the contact resistance. A mobility extraction method is applied that does not require the injection or uptake of charges, making it insensitive to contact resistances. The method uses two additional finger-shaped gates that capacitively generate and probe an AC current in the OFET channel. Particularly for ambipolar materials the true mobilities are found to be substantially larger than determined by conventional (DC) schemes.

In **Chapter 5** light emission from ambipolar organic field-effect transistors (OFETs) is described when they are operated in the unipolar regime. In this regime light emission is expected to be completely suppressed, because only one type of charge carrier is accumulated. Using SKPM it was found that light emission from OFETs predominantly originates from the unipolar regime when the charge transport is injection limited. The counterintuitive unipolar light emission is quantitatively explained by injection of minority carriers into tail states of the semiconductor at the contact-semiconductor interface.

In **Chapter 6** the addition of an extra gate to a light-emitting field-effect transistor is studied to evaluate the suitability of this geometry for electrically pumped lasers. In the dual-gate transistor one gate can accumulate electrons and the other holes. The high field-effect mobility yields high current densities in the separate channels. When the electron and hole currents can be forced to recombine the recombination current could easily exceed the lasing threshold. However it was found that independent hole and electron accumulation is mutually exclusive with vertical recombination and light emission.

In **Chapter 7** ambipolar transistors are combined into an integrated circuit. A fast ring oscillator was created using simple processing steps and using a diketopyrrolopyrrole type polymer as a semiconductor. The maximum oscillation frequency was determined to be a record high 42 kHz.

Finally in **Chapter 8** an outlook will be presented. This outlook is focused on the future of light-emitting OFETs for lasing. This outlook is focused on a pulsed driving scheme applied to the dual-gate field-effect transistor. Computer simulations show that a singlet exciton density may be obtained that exceeds the lasing threshold. Moreover, quenching mechanisms introduced by electrically pumping are minimized in the device concept.

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Chapter 2

Describing charge transport in OFETs using a measured density of states

Abstract

The width and shape of the density of states (DOS) are key parameters to describe the charge transport of organic semiconductors. Here we extract the DOS using scanning Kelvin probe microscopy on a self-assembled monolayer field-effect transistor (SAMFET). The semiconductor is only a single monolayer which has allowed extraction of the DOS over a wide energy range, pushing the methodology to its fundamental limit. The measured DOS consists of an exponential distribution of deep states with on top additional localized states. The charge transport has been calculated in a generic variable range hopping model that allows any DOS as input. We show that with the experimentally extracted DOS an excellent agreement between measured and calculated transfer curves is obtained. This shows that detailed knowledge of the density of states is a prerequisite to consistently describe the transfer characteristics of organic field-effect transistors.

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2.1 Introduction

Organic semiconductors are applied in organic photovoltaic cells, organic light-emitting diodes, and organic field effect transistors (OFETs). The charge transport in organic semiconductors can be described by taking into account the disordered microstructure.[1-2] Crucial in the reported models is the characteristic width and shape of the density of states (DOS).[3] Presently, a certain shape, typically a single exponential or Gaussian, is assumed and its width and height are fitted to describe the transfer curve of field-effect transistors.[4-6] Several techniques have been used to extract the DOS independently from the electrical IV-characteristics.[7-13] A complication arises when the technique used affects the DOS itself, such as electrochemical oxidation and reduction.[14] Preferably a method is used that determines the DOS without changing the state of the semiconductor and without making physical contact. Here we use scanning Kelvin probe microscopy (SKPM) on functional field-effect transistors as introduced by Tal *et al*.[11] By probing the local surface potential in the channel as a function of the applied gate bias the DOS of the organic semiconductor can be extracted. It has been shown that the use of a thick semiconductor film limits the energy range over which the DOS can be accurately determined.[7] Hence, we here use a monolayer of semiconducting molecules self-assembled in a field-effect transistor (SAMFET).[15]

To model the electrical transport in a transistor usually a shape of the DOS is assumed. By fitting the IV-characteristics, key parameters of the DOS as characteristic temperature or width are obtained. A direct validation of these parameters does not exist. Here we calculate the charge transport using a generic variable range hopping model that allows any DOS as input. With the experimentally extracted DOS as input an excellent agreement between modeled and measured transfer curves is obtained; with a single exponential DOS an unsatisfactory description is obtained. This shows that a priori knowledge of the DOS is a prerequisite to accurately predict the charge transport in organic semiconductors.

2.2 SKPM method

The operation mechanism of SKPM is elucidated in Figure 2.1. In black the situation is depicted where the gate is at the flat band voltage and the self-assembled monolayer (SAM) is grounded. No electrostatic field is present between the gate and the SAM and, therefore, no charges are accumulated. With SKPM a bias V_{skpm} is applied to the tip such that the electrostatic field between tip and surface is nullified. In orange the situation is depicted where a negative gate bias is applied to accumulate holes. The added charges fill the highest occupied molecular orbital (HOMO) of the semiconductor. Consequently the HOMO-level E_{HOMO} shifts with respect to the Fermi level E_F that is fixed by the

grounded source and drain electrodes. The change of the HOMO level with respect to the Fermi level is measured with SKPM as $\Delta E_{HOMO} = q\Delta V_{skpm}$, with q the elementary charge.

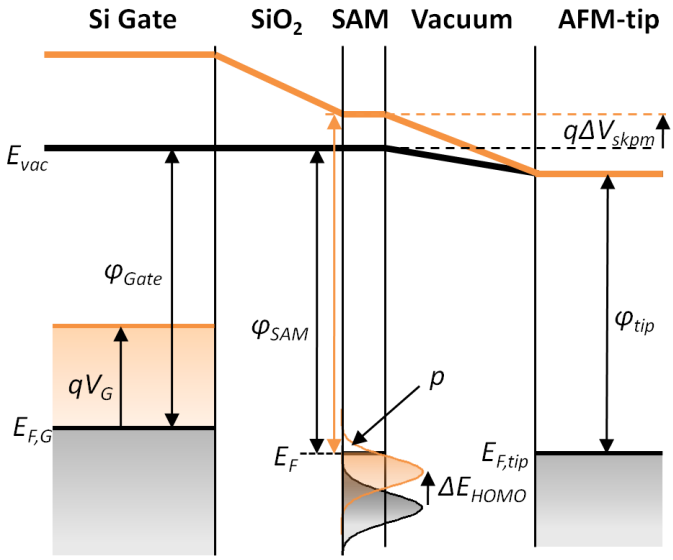

Figure 2.1: Energy band diagram of the Kelvin probe experiment. In black is the situation depicted when no gate bias is applied and orange when a negative gate bias V_G is applied.

The DOS is extracted from the measured surface potentials as function of gate bias, V_G. By decreasing the gate bias with ΔV_G, a number of holes Δp is accumulated in the semiconductor:

$$\Delta p = C\left(\Delta V_G - \Delta V_{skpm}\right)/qd_{org}\,, \tag{2.1}$$

with C the areal capacitance of the gate dielectric and d_{org} the thickness of the semiconductor. At the same time the shift of the HOMO level ΔE_{HOMO} is measured by SKPM. With this information the DOS of the HOMO at the Fermi level is extracted as:

$$g(E_f) = \frac{\Delta p}{\Delta E_{HOMO}} = \left[\left(\frac{dV_{skpm}}{dV_G}\right)^{-1} - 1\right]\frac{C}{d_{org}q^2}\,. \tag{2.2}$$

This equation only holds at the temperature T = 0 K and when the potential distribution in the semiconductor is homogeneous. These two assumptions are considered in more detail below.

First we investigate the implications of the assumption of T = 0 K. At finite temperatures a distribution of states around E_F will be filled. As a result the shift of the HOMO level will not only depend on the DOS at E_F, but also on the DOS around E_F. This leads to a broadening of the measured DOS. For the specific case of an exponential DOS and $T < T_0$ the hole concentration can be written as:

$$p = N_{\exp}\exp\left(\frac{E_F}{k_B T_0}\right)\frac{\pi T}{T_0\sin\left(\pi T/T_0\right)}\,, \tag{2.3}$$

in which T_0 is the characteristic temperature of the exponential DOS, N_{exp} is the total number of exponential states and k_B is Boltzmann's constant. By taking the derivative of Equation (2.3) with respect to E_F and combining with Equation (2.1), a similar equation as Equation (2.2) is obtained, but with the right hand side multiplied by a correction factor:

$$g(E_f) = \left[\left(\frac{dV_{skpm}}{dV_G} \right)^{-1} - 1 \right] \frac{C}{d_{org} q^2} \frac{T_0 \sin(\pi T / T_0)}{\pi T}. \tag{2.4}$$

The correction factor is close to unity as long as $T << T_0$. For temperatures around T_0, Equation (2.4) no longer holds. Numerical calculations have shown that at high temperature ($T \geq T_0$) it is impossible with SKPM to accurately measure the DOS; the DOS will then be broadened to at least $k_B T$.

To circumvent calculating the numerical derivative in Equation (2.4), Equations (2.1) and (2.3) can be combined directly yielding:

$$g(E_f) = \frac{C}{d_{org} q} \left(V_G - V_{skpm} - V_0 \right) \frac{\sin(\pi T / T_0)}{\pi k_B T}, \tag{2.5}$$

where V_0 is the difference between V_G and V_{skpm} when the transistor is put in the off-state; all charges are depleted and $V_0 = V_G(p = 0) - V_{skpm}$. The shape of the DOS can then directly be obtained.

If charges are non-uniformly distributed over the thickness of the semiconductor the second assumption breaks down. In conventional thin films with a thickness of more than several tens of nm, the assumption does not hold for any given gate bias.[16] Celebi *et al*. have measured the DOS for different thicknesses of the semiconductor. They indeed report an increase of the measurable range of the DOS with decreasing layer thickness.[7] Here we use a semiconducting monolayer. The film is only one molecule thick, which pushes the methodology to its fundamental limit.

2.3 Experimental

The SAMFETs were prepared as described in reference [17]. Transistor test substrates were used that consists of heavily doped silicon wafers acting as common gate electrode, with thermally grown SiO_2 as gate dielectric and lithographically pre-patterned Au source and drain electrodes. A monolayer of a functionalized quinquethiophene molecule is self-assembled from solution onto the SiO_2 gate dielectric. The chemical structure is shown as inset in Figure 2.2b. The resulting SAMFET was annealed in vacuum at 120 °C for 1 h before measuring. We used a channel width of 10 mm, channel length of 5 µm and a gate capacitance C = 17 nF/cm^2. Non-contact atomic force microscopy (AFM) and SKPM measurements were performed with an Omicron VT-SPM connected to a Nanonis controller in ultra-high vacuum (10^{-9} mbar). Pt-Ir coated AFM-tips (PPP-EFM, Nanosensors, f_{res} ~70 kHz) were used. For SKPM a 1 V AC-tip voltage was applied during

scanning. Before measuring the surface potential as function of the gate voltage, a surface area of 6 x 3 μm^2 was checked for a full coverage with the SAM. In-situ transfer characteristics were measured to check the mobility and the position of the threshold voltage of the SAMFET. During gate sweeps a low ramp speed of the gate bias (~5 mV/s) was used in the SKPM measurements in the sub-threshold regime, in order to assure steady state and to assure that the measured surface potentials are the same for both scanning directions. Temperature dependent transfer characteristics of the SAMFETs were measured in the linear regime (drain bias V_D = -2 V) in a high-vacuum (10^{-6} mbar) probe station with a Keithley 4200.

2.4 Measured DOS

Figure 2.2a shows the measured surface potential and the corresponding transfer curve of the SAMFET. The transistor is depleted at gate biases higher than the threshold voltage V_{th}. The SAM does not screen the gate, and SKPM then measures the gate voltage. When V_G is below V_{th} the transistor is on and the accumulated charges start to screen the gate bias. The change in V_{skpm} is then a result of the shift of the HOMO level with respect to the Fermi level and can be used to calculate the DOS as explained above. However, at gate voltages below -15 V the measured surface potential becomes independent of the applied gate voltage (Figure 2.2a). Such invariance of the surface potential has been observed before for thicker layers, where the assumption of an independent vertical potential distribution in the semiconductor breaks down at relatively low gate fields. Here, for the SAM, the assumption breaks down at a much higher gate field and, consequently, a larger range of the DOS is probed.

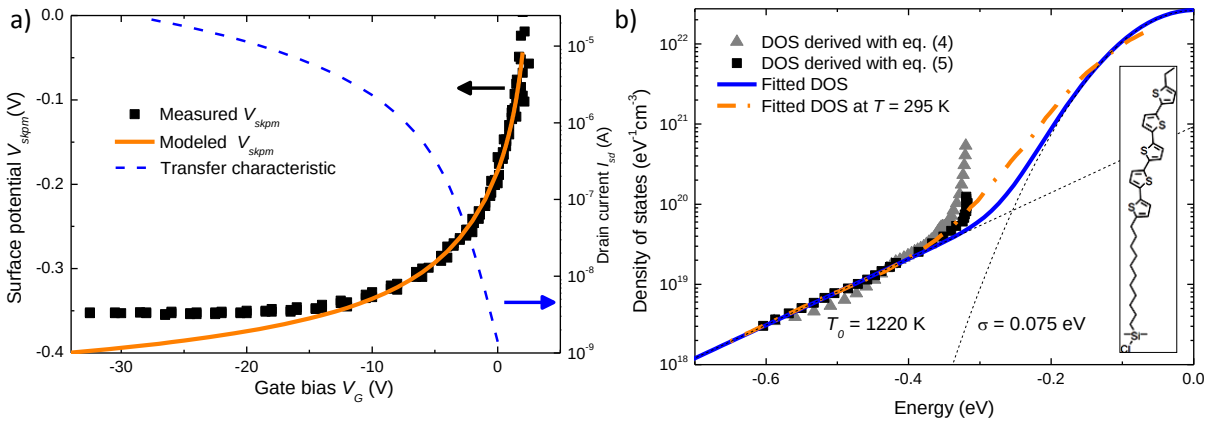

Figure 2.2: a) Symbols: measured surface potential as function of the applied gate bias. Solid line: calculated V_{skpm} at 295 K based on the extracted DOS (solid line in b). Dashed line (right axis): transfer curve at 295 K. b) DOS vs. energy. Symbols: measured values. Solid line: fitted DOS. Dash-dotted line: calculated shape of the DOS when it is measured at 295 K. The thin dashed lines are drawn to clarify the Gaussian and the exponential part of the DOS. Inset: structure of the SAM-molecule.

The DOS as calculated from both Equations (2.4) and (2.5) is shown in Figure 2.2b. The deep lying states (energies below – 0.4 eV) that are measured in the sub-threshold regime can be described by an exponential function with a width T_0 of 1220 K. Comparable high T_0 values are found in other direct DOS measurements on organic transistors.[7-13] However, the values are much higher than those found from direct fitting of the entire transfer characteristics with mobility models based a single exponential DOS. Typically a temperature of about 500 K is reported.[4, 18-19] A reason for the discrepancy is a steeper DOS at higher energies. The exponential shape of the DOS found in transistors is in contradiction with the Gaussian-shaped DOS that is mostly observed in diode-like devices.[2] The exponential tail is probably a result of disorder at the semiconductor-dielectric interface which is probed here, whereas in diodes the bulk semiconductor is measured.

Figure 2.2b shows that energies higher than about -0.4 eV the measured DOS indeed starts to increase and the characteristic temperature decreases. We note that the extracted points at the upper highest energies are unreliable. There the assumption of an independent potential distribution in the semiconductor breaks down. However, within the experimental accuracy the DOS increases significantly with energy.

To describe the measured DOS we add on top of the exponential DOS additional localized states. To limit the total number of states we describe this part not with an exponential function but with a Gaussian one. The DOS as extracted from the measurements, the solid blue line in Figure 2.2b, can now be presented as:

$$g(E) = \frac{N_{\exp}}{k_B T_0} \exp\left(\frac{E}{k_B T_0}\right) + \frac{N_{Gauss}}{\sigma_{Gauss}\sqrt{2\pi}} \exp\left(-\frac{E^2}{2\sigma_{Gauss}^2}\right), \qquad (2.6)$$

with N_{Gauss} the number of Gaussian states, σ_{Gauss} = 0.075 eV the width of the Gaussian DOS, T_0 = 1220 K and N_{exp} = $1.0 \cdot 10^{20}$ cm^{-3}. The total number of states $N_{Gauss} + N_{exp}$ = $5 \cdot 10^{21}$ cm^{-3} is fixed by the molecule density of the SAM. The DOS is measured at finite temperatures and the measured DOS will consequently include thermal broadening. The measurements should therefore be compared to the extracted DOS including the thermal broadening. The thermally broadened extracted DOS is shown with the dash-dotted orange line in Figure 2.2b. We note that the width of the Gaussian DOS cannot accurately be extracted from the measurement. However, we show below that the functional dependence and the choice of the parameters of the additional part of the DOS are not critical. Important is that extracted DOS can accurately be described, especially the part where the DOS deviates from an exponential dependence.

2.5 Describing charge transport

The charge transport in organic semiconductors is dominated by thermally assisted hopping of charge carriers between localized states. The magnitude of the current depends on the shape of the DOS. To model the charge transport we use a hopping transport model that allows an arbitrary density of states as input. To this end we follow the Mott/Martens-type approach, which assumes that only hops from the Fermi level to a typical transport level E^* contribute to the conductivity. The transport level is the characteristic energy to which a carrier has to hop in order to contribute to the conduction. The Mott/Martens approach was previously shown to provide a good description for VRH-hopping systems.[1, 20] In brief, the number of states, *B,* that can be reached in a single hop depends on the DOS, the maximum hopping distance *R* and the maximum energy difference of a hop ΔE, and is given by

$$B = \pi R^2 d_{org} \int_{E_F}^{E_F+\Delta E} g(E - E_{HOMO}) dE \,. \tag{2.7}$$

The onset of macroscopic conduction is reached when a percolating path is formed. This occurs when each site is connected to a critical number of bonds B_c. Percolation theory has shown that for a two dimensional hopping medium such as the present SAMFET B_c = 4.5.[21]

In order to calculate the integral in Equation (2.7), the position of the Fermi level with respect to the HOMO level has to be known. The Fermi level depends on the charge density accumulated in the channel. This density, $p(V_g)$, is electrostatically induced by the gate bias and follows from Equation (2.1) as: $p(V_G) = \left(V_G - V_{skpm} - V_0\right) C / q d_{org}$. In calculating the charge density the spatial variation of the potential as a result of the applied drain bias is taken into account as described previously.[18] The position of the Fermi level with respect to the HOMO level can now be obtained by numerically solving:

$$p(V_G) = \int f\left(E - E_F\right) g\left(E - E_{HOMO}\right) dE \,, \tag{2.8}$$

where the integral runs over all energies and where *f* is the Fermi-Dirac distribution function.

The probability *P* for a charge carrier to hop over a spatial distance *R* with energetic distance ΔE (ΔE>0) is given by the Miller-Abrahams expression $P\left(R, \Delta E\right) = \exp\left(-2\alpha R - \Delta E / k_B T\right)$ where α^{-1} is a measure for the localization length.[22] The values of *R* and ΔE are varied to optimize the probability $P(R,\Delta E)$, under the constraint that each site is connected to the critical number of bonds $B = B_C$. The values obtained for *R* and ΔE are the typical hopping distance *R** and the typical activation energy *ΔE**. The calculated activation energy and hopping distance are a function of gate bias and temperature. Finally, the conductivity σ is assumed to be proportional to this optimized

value of P: $\sigma(p,T)=\sigma_0 P(R^*,\Delta E^*)$, where σ_0 is a conductivity prefactor. The hopping model can be used to calculate the electrical transport in a field-effect transistor. The input parameters are the shape and magnitude of the DOS, *g(E)*, and the localization length α^{-1}.

The transfer curves of the SAMFET, source drain current as a function of gate bias, are measured for temperatures between 83 K and 295 K and presented in Figure 3a. We first fitted the measured current using a single exponential DOS. The best fit is obtained for a characteristic temperature of 750 K and is presented by the dash-dotted lines. A good agreement is obtained in accumulation at high gate bias. In the sub-threshold region, up to gate biases of -10 V, the calculated current significantly deviates from the measured current. This discrepancy is expected because SKPM measurements clearly show that in this bias range the characteristic temperature of the DOS is 1220 K, instead of 750 K. A good description of the transfer curves over the entire gate bias range is obtained using the extracted DOS. The calculated currents are presented in Figure 3a by the fully drawn curves. The input parameters were a localization length of 0.48 nm, a characteristic temperature of the exponential part of the DOS as 1220 K and a width of the Gaussian part of the DOS of 0.075 eV. The excellent agreement for low gate biases follows directly from the measured exponential density of states. At higher bias an excellent agreement is obtained due to the increase of the extracted DOS at higher energies. The calculated currents are insensitive to the width of the Gaussian DOS. Comparable currents were obtained using σ = 0.09 eV and σ = 0.06 eV. The origin of this insensitivity as well as the origin of the non-constant activation energy is discussed below.

The drain current as a function of temperature is presented in Figure 2.3b for gate biases between -5 V and -35 V. The current does not follow a simple Arrhenius behavior. The activation energy as calculated above is temperature dependent, it increases with decreasing temperature. The current is first calculated using the single exponential DOS with characteristic temperature of 750 K, similar as in Figure 2.3a. The calculated currents are presented by the dash dotted lines. A reasonable agreement is obtained. A much better agreement however is obtained when the current is calculated using the extracted DOS, presented by the solid lines.

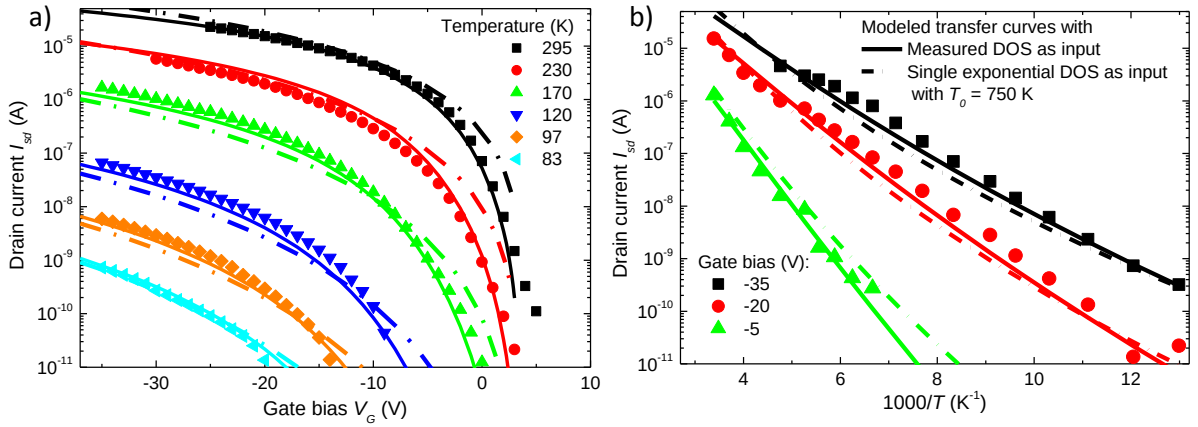

Figure 2.3: The source-drain current vs. applied gate bias (a) and vs. temperature (b). Symbols: measured data. The data is fitted with the numerical VRH-model described in the text using the measured DOS as input (solid lines, α^{-1} = 0.41 nm), and using a single exponential DOS as input (dash-dotted lines, T_0 = 750 K, α^{-1} = 0.58 nm).

The current and activation energy follow from the position of the Fermi level in the DOS and the transport level E^*. The Fermi level is calculated from the extracted DOS by Equation (2.8) and presented by the fully drawn line in Figure 2.4a. The three lines correspond to temperatures between 77 K and 295 K. The top x-axis represents the gate bias, and the bottom x-axis the corresponding induced charge density. The transport level E^* is given by the Fermi energy plus the typical activation energy ΔE^*, derived above. The transport level is presented for temperatures between 77 K and 295 K in Figure 2.4a as the dash-dotted lines. The activation energy decreases with increasing charge density.

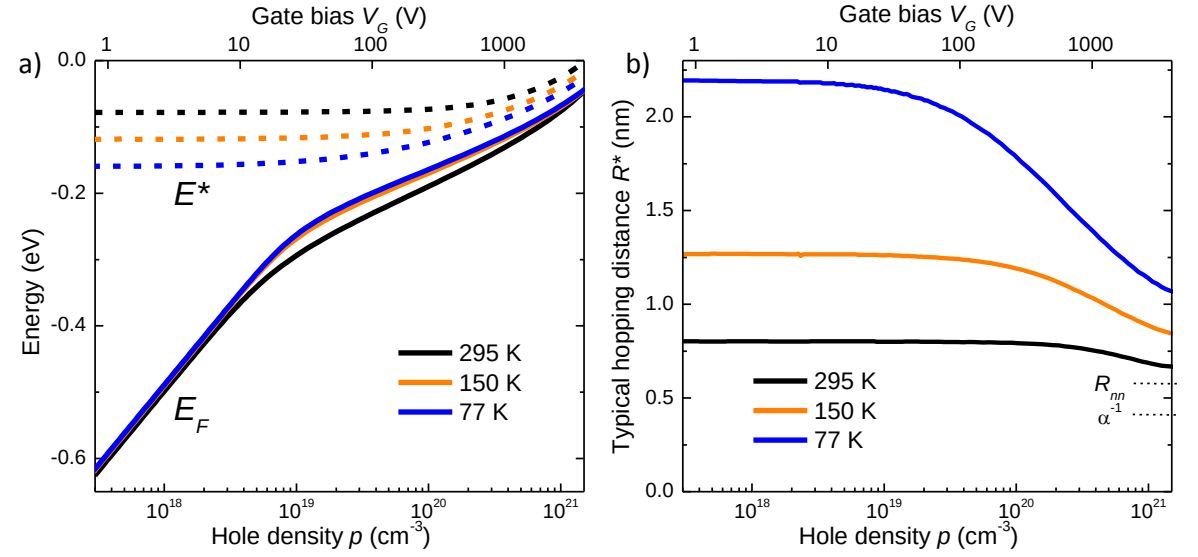

Figure 2.4: a) Calculated position of the Fermi level E_F (solid lines) and the typical transport energy E^* (dashed lines) as function of the charge density p (bottom axis) and of the corresponding gate bias (top axis). b) Calculated values for the typical hopping distance R^*.

At low gate biases the Fermi level is located in the exponential part of the DOS. Therefore in the semi-logarithmic representation a straight line is obtained. At higher

bias the Fermi level is located in the Gaussian part of the extracted DOS. Slight variations in the width of the DOS therefore have a minor influence on the Fermi energy and hence of the quality of the fitted transfer curves. For this reason the DOS at those energies can be equally well be described by an exponential function. This shows that the functional dependence for the shape of the DOS is not critical for the fit of the transfer curves. The transport level is always located in the Gaussian part of the DOS.

To test the internal consistency of our variable range hopping model we have also calculated the typical hopping distance, R^*. The distances are presented as a function of induced charge density and temperature as the dashed curves in Figure 2.4b. Firstly, since the charge transport sites are assumed to be localized, the hopping distance should be larger than the localization length which is indeed the case. Secondly, we find for all conditions that the hopping distance is larger than the nearest neighbor distance R_{nn}, calculated from the areal density of thiophene units as 0.58 nm, which is a prerequisite for true variable range hopping. The calculations show that the system approaches nearest neighbor hopping at very high temperature and charge density.

2.6 Conclusion

The density of states is measured using SKPM, which can be extracted when the potential distribution perpendicular to the channel is homogeneous. The thicker the semiconductor is, the smaller the part of the DOS that can reliably be probed. Here we use a self-assembled monolayer field-effect transistor (SAMFET). The semiconductor is a single monolayer, which is comparable to the thickness of the accumulation layer which has allowed us to extract the DOS over a large energy range. The DOS extracted at low energies consists of an exponential distribution of deep states with a characteristic temperature of 1220 K. The measurements show that at higher energies the DOS increases. The additional localized states are represented by a Gaussian function. To model the charge transport in the SAMFET we use a hopping transport model that allows any arbitrary density of states. With a single exponential DOS the transfer curves cannot adequately be described. However with the experimentally extracted DOS as input a near perfect agreement is obtained. This shows that detailed knowledge of the density of states is a prerequisite to consistently describe the transfer characteristics of organic field-effect transistors.

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Chapter 3

Scanning tunnelling microscopy on OFETs based on intrinsic pentacene

Abstract

The full potential of scanning tunneling microscopy (STM) and spectroscopy (STS) for in-situ characterization of organic semiconductors has so far not been accessible. Here we demonstrate that the underlying problem, the low intrinsic conductivity, can be overcome by working in a field-effect geometry. We present high resolution surface topographies obtained by STM on pentacene organic field-effect transistors (OFET). By virtue of the OFET geometry, the hole accumulation layer that is present at sufficiently negative gate bias acts as back contact, collecting the tunneling current. The presence of a true tunneling gap is established, as is the need for the presence of an accumulation layer. The tunneling current vs. tip bias showed rectifying behavior, which is rationalized in terms of the tip acting as a second gate on the unipolar semiconductor. An explanatory band diagram is presented. The measurements shown indicate that intrinsic organic semiconductors can be in-situ characterized with high spatial and energetic resolution in functional devices.

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3.1 Introduction

Scanning tunneling microscopy (STM) has proven to be a powerful technique to characterize semiconductors with a resolution down to that of a single molecule, defect or impurity level.[1-5] STM not only provides the surface topography, but also information can be obtained about the local density of states by measuring the tunneling current as a function of bias as in scanning tunneling spectroscopy (STS). The additional information on the energy levels makes STS the indicated technique to study organic semiconductors.[6-10] They are typically disordered and the charge transport is due to hopping between the inherently localized states.[11-13] STM and STS are preferably performed in-situ, *i.e.* in the actual device itself, allowing to directly relate the microscopic findings to the macroscopic material properties. In-situ measurements have the additional advantage that the measurements can be followed during device operation to examine for instance the device reliability or the potential distribution in the device.[14-16] Charge transport in organic semiconductors is often investigated in organic field-effect transistors (OFET), where the charge mobility is extracted as a function of the carrier density as was shown in Chapter 2.[17] STM and STS could deliver important microscopic information, such as the density of states, to unravel the semiconductor charge transport mechanism. In-situ STM measurements on organic semiconductors in transistors, however, have not been reported. The reason is that the bulk resistance of the intrinsic semiconductor is too high. Consequently, there is no tunneling gap and the tip crashes on the surface of the semiconductor.[16, 18-19]

The tip-sample current in an STM measurement is used as feedback signal to control the tip scan height. Ideally the resistance of the sample, R_s, is much lower than the tunnel resistance, R_{tun}. The applied tip bias, V_{tip}, then drops only over the tunneling gap. When the sample resistance cannot be disregarded, the feedback system will decrease the tip height to reach the set tip current, I_{set}, but if the set current cannot be obtained the tip crashes. In other words STM requires fulfilling the following condition:

$$V_{tip} / I_{set} = R_s + R_{tun} >> R_s . \qquad (3.1)$$

An in-situ STM measurement in an OFET is schematically depicted in Figure 3.1. The conduction of charge carriers involves three steps: (1) tunneling from the tip to the semiconductor, (2) transportation of the charges to the accumulation layer at the gate dielectric, and (3) conduction via the accumulation layer of the transistor to the source or drain contacts. The sample resistance, R_s is the series resistance of paths 2 and 3. The resistivity of path 2 can be minimized by decreasing the thickness of the organic layer. When the gate is biased above the threshold voltage no charges are accumulated in the channel. For an intrinsic semiconductor the channel resistance, path 3, then is prohibitively large. Equation (3.1) is not fulfilled, a tunnel gap cannot be formed and the

tip crashes. Here however, we demonstrate in-situ STM topography and spectroscopy measurements in a functional OFET. By adjusting the gate bias an accumulation layer is formed. The channel resistance decreases and the requirement Equation (3.1) is fulfilled. A tunnel junction is formed and the current can be measured as a function of applied tip bias. We show that the rectifying current voltage characteristics obtained are a direct consequence of the tip acting as dual gate on a unipolar semiconductor. An explanatory band diagram is presented.

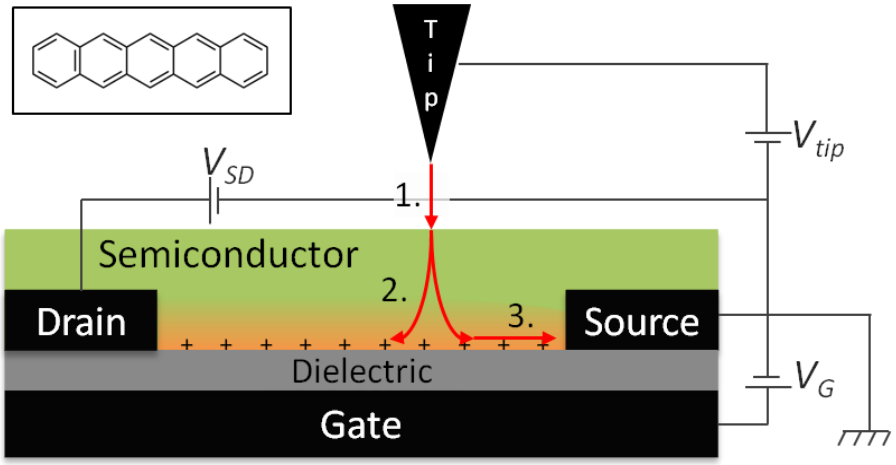

Figure 3.1: Schematic of an in-situ STM measurement on a field-effect transistor, with the applied biases indicated. The tip current has to cross the tunnel gap (1), reach the accumulation layer (2) and finally reach the contacts via the accumulation layer (3). Inset: chemical structure of pentacene.

3.2 Experimental

Pentacene-based OFETs were prepared on a highly-doped Si substrate, acting as bottom gate. A 200 nm thick thermally grown SiO_2 layer on top acts as a gate dielectric. Bottom source and drain Au/Ti (100 nm/5 nm) contacts were defined by standard I-line photolithography. The channel length, *L*, and width *W*, amounted to 5 µm and 1000 µm respectively. Prior to pentacene deposition, the dielectric surface was treated with hexamethyldisilazane (HMDS) to reduce bias stress.[20] Pentacene was evaporated at 150 °C in high vacuum (10^{-7} mbar) at 0.4 Å/s. The resulting pentacene layer has an average thickness of 25 nm and fully covered the substrate. The full coverage is needed to avoid tip crashes on the non-conducting SiO_2. STM measurements were performed with an Omicron SPM driven by a Nanonis controller in UHV (10^{-9} mbar), using a mechanically cut Pt/Ir-wire as tip. The STM measurement to study the tip crash (Figure 3.3) was performed in ambient conditions using a Veeco Multimode with Nanoscope IIIA controller in STM mode. Electrical characterization of the transistors was done in-situ using a Keithley 2636 low-current source-measure unit.

3.3 Scanning tunneling microscopy

A typical transfer curve, where the source-drain current is plotted as a function of gate bias is shown in Figure 3.2a. Forward and backward scans are superimposed; there is no hysteresis. The threshold voltage V_{th}, taken as the onset of current flow, is around 0 V. The transistor shows unipolar *p*-type behavior, where the current is enhanced at negative gate biases due to hole accumulation. At positive gate biases the current is low since no electrons are accumulated. The extracted field-effect hole mobility is 0.3 cm^2/Vs.

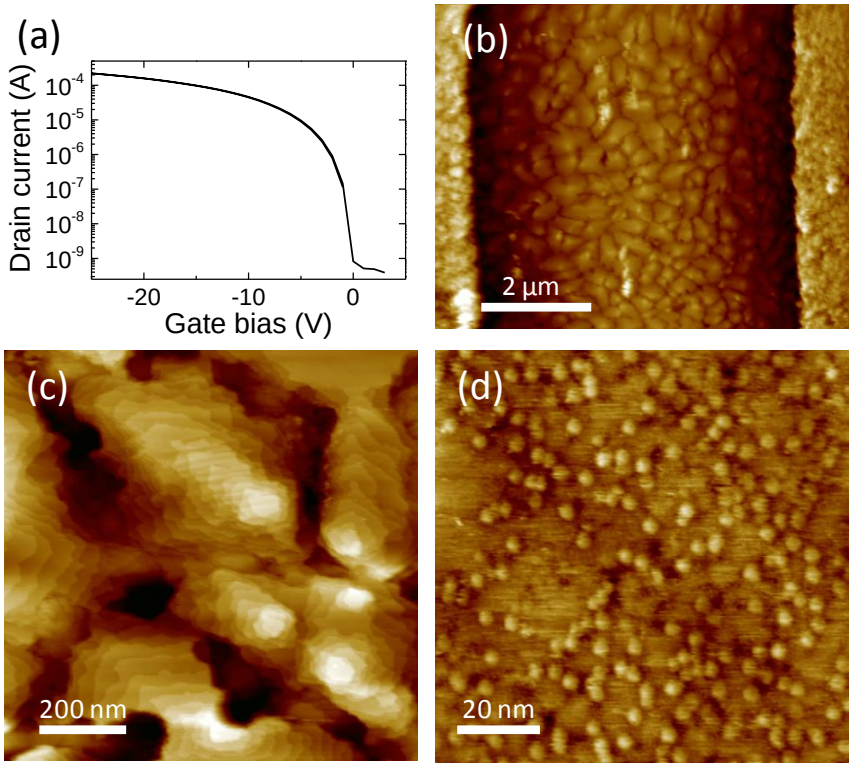

Figure 3.2: a) Transfer characteristic of a pentacene OFET with a drain bias of -2 V. The forward and backward sweeps are on top of each other, there is no hysteresis. b-d) STM height images with increasing spatial resolution. The tip bias is -1 V and the tunneling current is set at 10 pA. b) Scan with source and drain electrodes of the transistor at the left and right side (full height scale FS = 135 nm), c) scan in the transistor channel (FS = 35 nm), and d) scan on a pentacene terrace (FS = 1.5 nm).

STM images were obtained under bias conditions as shown in Figure 3.1. The source and drain contacts were grounded, $V_{S,D}$ = 0 V, and a gate bias of V_G = -10 V was applied to assure the presence of an accumulation layer. The bias on the STM tip was set at -1 V. STM images of the pentacene transistor with increasing spatial resolution are shown in Figure 3.2b-d, respectively. In the large-scale image of Figure 3.2b the source and drain electrodes are visible as the brighter parts on the left and right hand side. Stable images are obtained both on top of the electrodes and in the transistor channel. The morphology of the pentacene on top of the contacts and in the channel is clearly different. Grains formed on top of the electrode are smaller than the ones formed in the

channel. We note that the morphology being a function of the type of surface underlines the need to perform in-situ measurements. Figure 3.2c shows a zoom-in on the transistor channel. Terraces are clearly visible, which are typical for evaporated pentacene.[21-22] The step height of 1.7 ± 0.2 nm corresponds to the c-axis lattice constant of a pentacene. [21-22]

A further zoom-in of the top of a pentacene terrace is presented in Figure 3.2d. Remarkable circular features with a height of 0.5 ± 0.1 nm are observed on the terraces. Both the height and the monodisperse size distribution strongly suggest that these features are related to pentacene molecules lying flat on the surface. A broader shape variation is expected when the features are caused by contamination. The absence of any visible elongation and the fact that the lateral feature size is larger than that of a single molecule can, in view of the overall good resolution, not easily be uniquely attributed to convolution with the STM tip. Likely, changes in the electronic structure surrounding the surface species determine their apparent shape. Importantly, the close to molecular resolution and the fact that the surface could be scanned multiple times without noticeable changes shows that true tunneling to the pentacene film is achieved in the OFET. We note that Gross *et al.* have imaged a pentacene molecule with sub-molecular resolution.[23] However, in order to achieve that high resolution they required a well-defined tip terminated with a CO molecule and an atomically flat metal substrate.

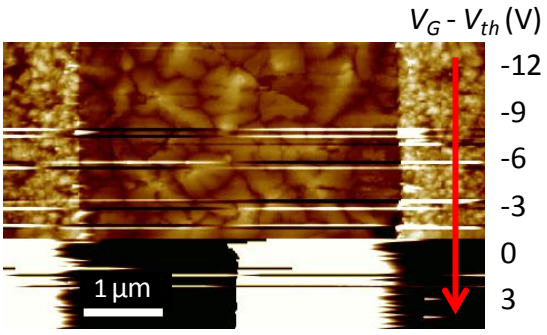

Figure 3.3: STM image obtained by continuously scanning the tip with V_{tip} = -200 mV, $V_{S,D}$ = 0 V and I_{set} = 1 pA while slowly changing the gate bias from accumulation at -15 V to depletion at +6 V. The arrow indicates the scan direction. The tip crashes just before the threshold voltage is reached.

In order to demonstrate the crucial presence of an accumulation layer, we slowly increased the gate bias from accumulation at -15 V to depletion at + 6 V while continuously scanning the tip. The STM images are presented in Figure 3.3. As can be seen from the transfer curve in Figure 3.2a, the channel resistance increases with increasing gate bias. The tip crashes just before the treshold voltage, V_{th}, of the transistor is reached. The channel resistance is then so large that the STM requirement of Equation (3.1) is not any longer fullfilled. The imposibility to scan without the accumulation layer present shows that the charges are conducted via this layer. Charge transport via other

possible pathways, for example via the bulk due to possible unintended doping, is therefore ruled out.

3.4 Scanning tunneling spectroscopy

STM not only provides the surface topography as shown in Figure 3.2, but by measuring the tunneling current as a function of tip bias information can be obtained about the local density of states as well. The states probed in the scanning tunneling mode (STS) depend on the tip bias. When the Fermi level of tip, $E_{F,t}$, is larger than the Fermi level of the pentacene top surface with negative tip biases, electrons from the tip can tunnel to empty states of the pentacene. When the Fermi level of the tip is lower than that of the top pentacene layer with positive tip biases, electrons from the filled pentacene states can tunnel to the tip.

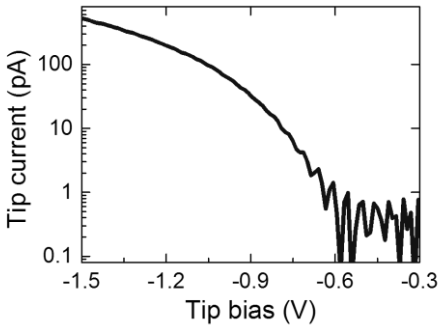

Figure 3.4: Scanning tunneling spectroscopy in the transistor channel at a gate bias of -10 V. The tip bias was swept from -1.5 V to +1.5 V, at constant tip height. Tunneling current was observed for negative tip biases only.

A first measurement is presented in Figure 3.4. The tip bias was swept from -1.5 V to +1.5 V with the feedback loop disabled, *i.e.* the current was recorded at constant tip height. Interestingly, only current was observed at negative tip biases and not at positive tip biases. This rectifying behavior is a direct consequence of the unipolarity of the pentacene transistor. The tip will effectively act as a local second gate, since it is a metal contact separated from the pentacene semiconductor by a vacuum gap.[24] At negative tip biases, the electric field created by the tip attracts holes to the pentacene top surface, effectively accumulating locally extra holes. At positive tip biases, the electric field created by the tip cannot attract electrons to the pentacene top surface because the transistor is unipolar. Instead, holes shall be pushed away, even locally depleting the accumulation layer at the bottom gate SiO_2 dielectric interface.

Band diagrams for the situation of negative and positive tip biases are presented in Figures 3.5a and 3.5b respectively. The gate is biased negatively such that holes are accumulated in the channel and the resistance of path 3 in Figure 3.1 is low. At a negative tip bias, holes are accumulated at the pentacene top surface near the tip due to the local gate effect. The holes will screen the electric field of the tip and therefore this

electric field is mainly restricted to the vacuum gap.[25] Electrons from the tip tunnel to the empty states in the highest occupied molecular orbital (HOMO) level at the pentacene top surface. In contrast, at positive tip bias, no electrons are attracted to the pentacene top surface due to the unipolarity of the transistor. The applied electric field is now distributed between the tip and the accumulation layer. As a result, only a small fraction of the tip bias falls over the tunneling gap, since the semiconductor thickness (~25 nm) is much larger than the tunnel gap (< 1 nm). The effective electric field falling over the vacuum gap is too low to get the tip Fermi level below the HOMO level of the semiconductor. Consequently no electrons can tunnel from the filled HOMO to the tip.

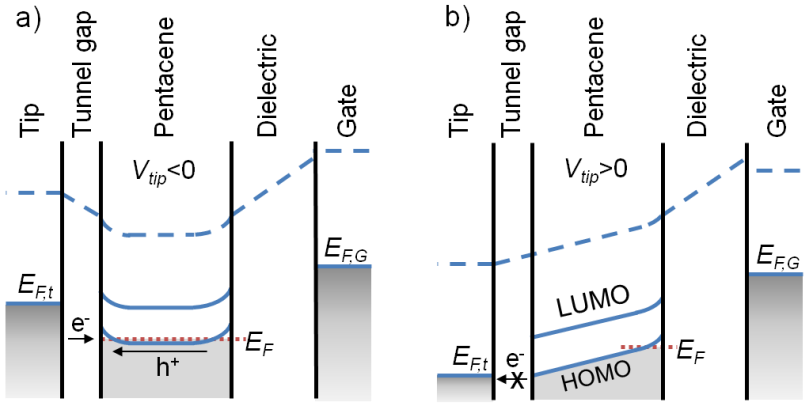

Figure 3.5: Band diagram of the STS measurement experiment for a) a negative tip bias and b) a positive tip bias. In both cases the bottom gate bias is biased negative, in accumulation, and the semiconductor is grounded, fixing the accumulation layer Fermi level, E_F.

We note that in metals the density of states can be extracted from the derivative of the tunnel current. However, this technique assumes a constant Fermi level. Here the Fermi level is not constant due to the local gate effect of the tip. The position of the semiconductor Fermi level changes with respect to the semiconductor HOMO level, when holes are accumulated by the tip. Consequently the density of states of the semiconductor in an OFET cannot directly be extracted from the tunnel current.

3.5 Conclusion

In-situ STM and STS measurements are performed on a functional OFET. As a semiconductor a 25 nm thick pentacene film was used. When the transistor is biased in depletion, the channel resistance is large and as a consequence the tip crashes. When the transistor is biased in accumulation, stable and high resolution STM images could be obtained. The tunneling current measured as a function of tip bias showed a rectifying behavior due the tip acting as a second gate on a unipolar semiconductor. An explanatory band diagram is presented. The STM and STS measurements presented indicate that intrinsic organic semiconductors can be characterized with high spatial and energetic resolution in-situ in functional devices.

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Chapter 4

Contactless charge mobility measurement in organic field-effect transistors

Abstract

With the increasing performance of organic semiconductors, contact resistances become an almost fundamental problem, obstructing the accurate measurement of charge carrier mobilities. Here, a generally applicable method is presented to determine the true charge carrier mobility in an organic field-effect transistor (OFET). The method uses two additional finger-shaped gates that capacitively generate and probe an alternating current in the OFET channel. The time lag between drive and probe can directly be related to the mobility, as is shown experimentally and numerically. As the scheme does not require the injection or uptake of charges it is fundamentally insensitive to contact resistances. Particularly for ambipolar materials the true mobilities are found to be substantially larger than determined by conventional (direct current) schemes.

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4.1 Introduction

The performance of organic field-effect transistors (OFET) increases remarkably, and an increasing number of organic semiconductors is being reported with a charge carrier mobility over that of a-Si, ~1 cm^2/Vs.[1-2] Especially *n*-type and ambipolar polymers recently made strong progression.[3-8] However, as the channel resistance decreases due to the increase of organic semiconductor mobilities, contact resistances often become the bottleneck for the total device performance.[1, 9-10] Many strategies have been reported to decrease the contact resistance for either holes or electrons,[1, 10-11] using self-assembled monolayers,[12-13] doping,[14-15] interlayers,[16-17] or by changing the device lay-out.[9, 18] Contact resistance is an even more fundamental problem in ambipolar transistors, where both electrons and holes need to be injected, as will be discussed in Chapter 5.[5] The electron and hole injection barriers at any contact always sum up to the semiconductor band gap. Hence the injection barrier cannot be negligible for both holes and electrons simultaneously, leading to a contact resistance for at least one of the two charges. By using different contact materials for source and drain this problem can partially be solved, but for ease of fabrication it is preferred to have a single electrode material that is able to inject both types of charge carriers.[19]

For research purposes one is often only interested in the transport properties of the semiconductor. The charge carrier mobility is then typically obtained by measuring the current in an OFET.[20] When the transistor suffers from contact resistance, a lower current and concomitantly a lower mobility is found. Correction for contact resistance is possible by estimating its value.[21-25] The most popular way to do so is by the transfer line method in which the resistance of OFETs as function of the channel length is measured. The extrapolated resistance at zero channel length is a measure for (twice) the contact resistance. This method however requires good device reproducibility.[26-27]

In view of the above there is a clear need for a tool to determine the charge carrier mobility that is insensitive to contact resistance. Here we present such a technique. The basic idea is that an alternating current (AC) is capacitively generated and probed in an OFET channel. To this end two additional finger gates are placed near the accumulation layer. Conventional source and drain contacts are still required to fill the accumulation layer, but do not need to absorb or inject any current and are therefore decoupled from the mobility measurement.

4.2 Materials and methods

4.2.1 Device fabrication

Devices were fabricated on cleaned glass substrates. The finger gates were created by evaporating 40 nm thick Au electrodes through a shadow mask substrate, preceded by a

2 nm Cr adhesion layer. Subsequently a 870 nm thick Cytop dielectric was applied by spin coating, followed by annealing for 30 min. at 150 °C. On top of that, 40 nm Au source and drain electrodes were evaporated through a shadow mask. The active layer, poly[2,5-bis(2-hexyldecyl)-2,3,5,6-tetrahydro-3,6-dioxopyrrolo[3,4-c]pyrrole-1,4-diyl-alt-[2,2'-(1,4-phenylene)bisthiophene]-5,5'-diyl] (PDPPTPT), was applied by spin coating from a chloroform solution and annealed for 30 min. at 200 °C.[28-29] Prior to spin coating, the Cytop dielectric required a treatment with a mild nitrogen plasma to enhance the semiconductor wetting. The gold work function was modified by either applying the semiconductor immediately after the plasma treatment, or first rinsing the gold electrodes with isopropanol. A second Cytop layer was spin coated on top of the stack and annealed at 150 °C. for 30 min. forming the gate dielectric. The thickness of the dielectric was 1.10 µm and 0.85 µm for the device with the solvent-rinsed contacts and non-rinsed contacts, resulting in a gate capacitance of C_G = 1.85 nC/cm^2 and C_G = 2.4 nC/cm^2, respectively. To finish the device, a 40 nm Au gate electrode was evaporated through a shadow mask. OFETs were measured in a high vacuum (10^{-5} mbar) probe station. Transfer characteristics were measured with a Keithley 4200 source-measure unit. Impedance spectroscopy was performed using a Solartron 1260A impedance analyzer in combination with a Keithley 2636 to apply the DC gate bias. The resulting lay-out of the device is shown in Figure 4.1a.

4.2.2 AC characterization method

The device consists of a regular bottom-contact top-gate OFET, with the addition of a pair of finger gates positioned below the transistor channel. A dielectric separates the fingers from the transistor channel to warrant that their influence on the charges in the channel is entirely capacitive. The channel formed between the short distance between a pair of source and drain electrodes is used for simultaneous conventional direct-current (DC)-OFET characterization, whereas the long distance channel is used for AC characterization.

As shown in Figure 4.1b an AC-bias is applied to one of the finger electrodes. The bias alternatingly pushes charges away from, or pulls charges towards the channel region above the finger gate, generating charge waves in the transistor channel. These charge waves are probed capacitively by the second finger gate. The time lag between the drive and probe signals can be related to the charge carrier mobility in the channel above the finger gates. In particular, performing impedance spectroscopy on the fingers, a characteristic frequency, f_c, can be observed. Its value corresponds to the reciprocal transit time of charges moving between the fingers. We define the characteristic frequency of the finger-gate system as the frequency where the conductance divided by

the frequency, *f*, peaks. The physical meaning of this quantity is the charge current per oscillation period flowing between the finger gate electrodes.

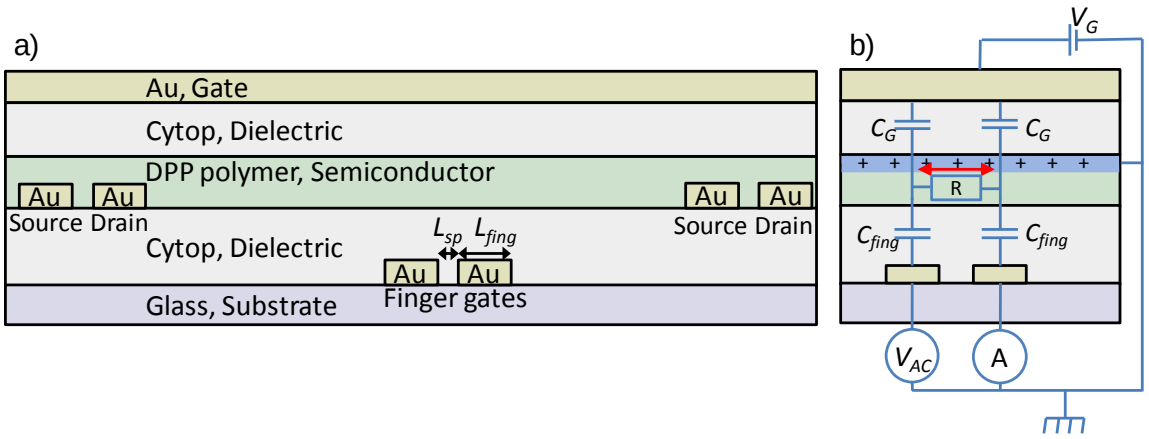

Figure 4.1: a) Cross section of the device lay-out. b) Schematic operation principle of the finger gate structure. The accumulation layer is grounded via the source and drain.

It is important that the modulating finger gates are sufficiently far away from the source and drain contacts, such that the charge density modulations have damped out at the contacts. Then the contacts do not absorb or inject any charges and do not play a role in the AC measurement. With this condition fulfilled, this method differs fundamentally from conventional impedance measurements in which the source and drain do need to absorb and inject charge.[30-34] The characterization is performed at relatively low frequencies, since charges have to travel a long distance to reach the other electrodes, making this technique fundamentally different from e.g. microwave conductivity.

4.3 Derivation of characteristic frequency

In order to determine the relation between characteristic frequency and mobility, the system will first be analyzed analytically for which it is simplified to the four capacitor circuit as drawn in Figure 4.1b. The capacitance between the finger gates is negligible compared to the capacitance of the finger gates to the channel. Furthermore, the charge flow away from the finger gate into the rest of the transistor channel is neglected. On basis of a simple dimension analysis the RC-time τ_{RC} of the system may be expected to scale as:

$$\tau_{RC} \propto RWL_{fing}(C_{fing} + C_G), \tag{4.1}$$

with R the resistance of the accumulation channel, C_G the gate capacitance per unit area, C_{fing} the finger gate capacitance per unit area, W the finger width, and L_{fing} the length of a finger gate electrode. The resistance R is inversely proportional to the amount of accumulated charges and their mobility μ:

$$R = \frac{L}{\left(V_G - V_{th}\right) C_G \mu W}, \tag{4.2}$$

with V_G the gate bias and V_{th} the threshold voltage. The distance L is the length that charges travel from one finger gate to the other finger gate, which is expected to be proportional to the finger gate spacing L_{sp} plus a fraction x of the finger width L_{fing}: $L = L_{sp} + xL_{fing}$. The fraction x depends on the device geometry and shall be found numerically below. The characteristic frequency is expected to scale with the estimated RC-time as $f_c \propto 1/\tau_{RC}$. Combining this with Equations (4.1)-(4.2) yields:

$$f_c \propto \frac{\left(V_G - V_{th}\right)\mu}{L_{fing} L} \frac{C_G}{(C_G + C_{fing})}. \tag{4.3}$$

To find the exact value of the characteristic frequency we analyzed the entire system numerically. Impedance spectroscopy on the finger gates is simulated on a 1D grid by forward time integration. The finger-gate system is considered to be a resistor-capacitor (RC)-network. The transistor channel is split in N separate RC-elements as shown in Figure 4.2a. The fingers are placed at distinct grid cells i with a finger capacitance $C_{fing,i}$. The finger capacitance is set to zero at positions where no finger is located. A time-varying finger gate bias $V_{fing,i}(t)$ is set to one of the fingers, the other finger is grounded and the time dependent current flowing to this finger gate is tracked. A constant mobility μ is assumed, although experimentally the mobility is charge density dependent. This assumption does not change the outcome as long as the variation in charge density is small compared to the average charge density in the channel. For simplicity, the threshold value is assumed to be zero; V_{th} = 0 V. Initially the potential is assumed to be constant in every grid cell, which is set by the source and the drain bias, $V_D = V_S$ = 0 V. The potential and charge density in each grid cell p_i are related via the capacitance as:

$$p_i = C_G\left(V_G + V_i\right) + C_{fing,i}\left(V_{fing,i} + V_i\right), \tag{4.4}$$

where V_G is the gate bias, C_G the gate capacitance and V_i the potential in the channel at grid cell i. Using the continuity equation the (change in) charge carrier density in each grid cell is calculated after each time step Δt:

$$q\frac{\Delta p_i}{\Delta t} = \frac{\Delta j_i}{\Delta x}, \tag{4.5}$$

with q the elementary charge, Δx the distance between subsequent grid cells, and j the current. The current follows from Ohm's law:

$$j_{i,i+1} = q p_i \mu \frac{(V_{i+1} - V_i)}{\Delta x}. \tag{4.6}$$

Finally, after each time step new channel potentials are calculated using Equation (4.4). The densities at the source and drain contacts are kept constant in time, which represents Ohmic injection. We note however that the results do not change by

increasing the distance between the contacts and the finger structure, indicating that the choice of the contacts does not influence the outcome of the simulations. The AC experiment is performed after giving the accumulation layer enough time to be filled by the contacts and the system has found its equilibrium. From the numerical simulations the following relation was found:

$$f_c = \frac{(V_G - V_{th})\mu}{2L_{fing}L} \frac{C_G}{(C_G + C_{fing})}. \tag{4.7}$$

The dependence of x on the device geometry (L_{sp}/L_{fing}) is shown in Figure 4.2b. For a high signal to noise ratio, the finger length is preferably larger than the finger spacing. In this region, when $L_{sp}<L_{fing}$, the fraction x was numerically found to be equal to 0.38. With all parameters in Equation (4.7) known, the characteristic frequency of the system allows one to determine the charge mobility. The parameterization of x makes the method generally applicable for any geometry that fulfills the criterion that the finger gates are far away from the source and drain contacts.

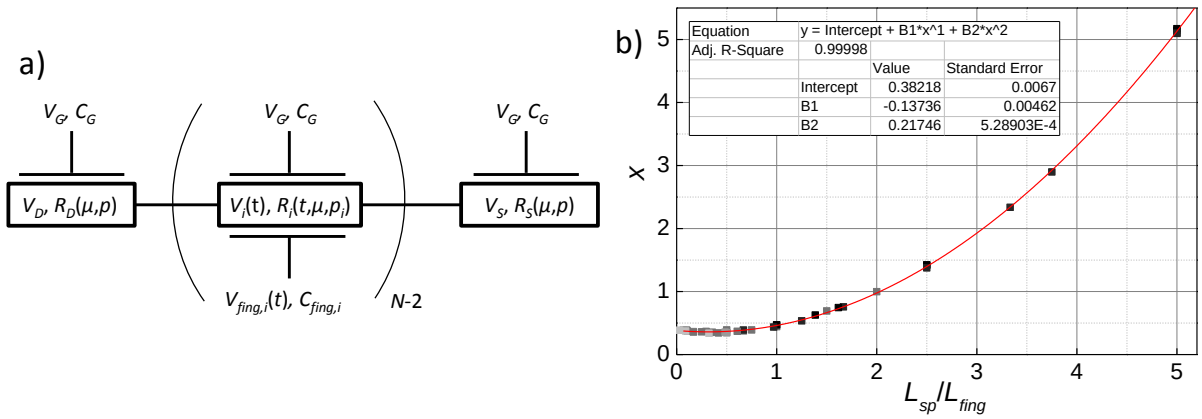

Figure 4.2: a) Schematic drawing of the simulation of the finger gate system. b) The fraction x in $L = L_{sp} + xL_{fing}$ as function of the ratio of the width of the inter-finger gap finger, L_{sp}, over the width of the fingers, L_{fing}. For small values of L_{sp}/L_{fing}, x = 0.38. Within numerical accuracy the points can be parameterized by a second order polynomial as shown by the red line; the legend provides the coefficients. The different colors refer to different lengths of the finger gates L_{sp} ranging from 20 µm (gray) to 300 µm (black).

4.4 Results mobility extraction

4.4.1 Transistor characteristics

Before turning to the AC mobility measurement, we shall first illustrate the urgency to avoid injection barriers by conventionally measuring the mobility in transistors with source and drain contacts having different work functions, but based on the same DPP-polymer (PDPPTPT). Different work functions were established by using plasma cleaned gold and solvent cleaned gold. Rinsing gold contacts by a solvent is known to slightly decrease their work function.[35] In Figure 4.3a the output curves of the two transistors are shown for negative gate biases, i.e. hole accumulation. The drain current of the

transistor with the low work-function contacts (φ_2) shows a clear s-shape indicative for a hole injection barrier.[36] This is not observed in the transistor with the higher work-function contacts (φ_1). Transfer curves of the OFETs are presented in Figure 4.3b, where the gate bias is multiplied by the actual gate capacitance for fair comparison between transistors with different dielectric thicknesses. The transistor with the high work-function contacts (φ_1) shows unipolar hole transport.

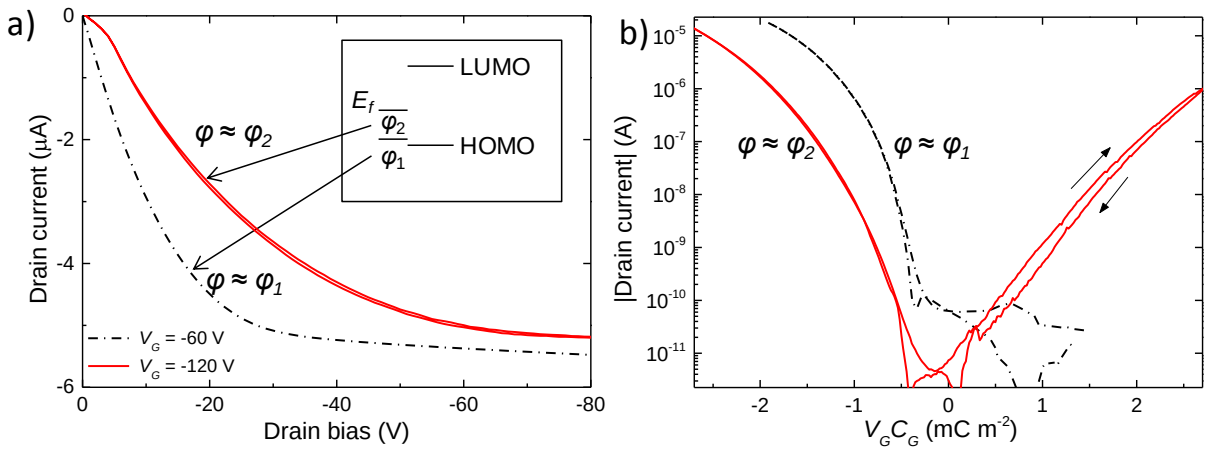

Figure 4.3: a) Output curve of an OFET with gold contacts and an OFET with gold contacts rinsed with isopropanol. Solvent rinsing slightly decreases the gold work function, resulting in a less deep work function (φ_2) than for plasma cleaned gold (φ_1). LFET = 30 µm, WFET = 1 mm. Inset: Schematic energy diagram of the metal-semiconductor interface for three different work-functions φ, illustrating the position of the Fermi level with respect to the HOMO and LUMO level. b) Transfer characteristics of the two transistors at a drain bias of -40 V.

On basis of the inset to Figure 4.3a the negligible electron injection can be rationalized. The linear hole mobility extracted from the transfer curve amounts to 0.28±0.02 cm^2/Vs. The mobility is higher than obtained earlier for PDPPTPT,[28] because of a different gate dielectric and an improved synthesis of the polymer.[29] The transistor with the low work-function contacts (φ_2) shows ambipolar charge transport, but the hole currents at negative gate biases are smaller than those observed in the transistor with the high work-function contacts. Extracted hole and electron mobilities in this case amount to 0.25±0.02 and 0.04±0.02 cm^2/Vs. The uncertainty in the electron mobility is relatively large due to gate leakage currents. As explained above, the price paid for lowering the electron injection barrier and enabling ambipolar operation is the formation of a hole injection barrier. At negative gate bias this lowers the transistor current and consequently a lower (apparent) hole mobility is found for this device. Furthermore, a higher gate bias is needed to reach this mobility, leading to an apparent shift in threshold voltage.

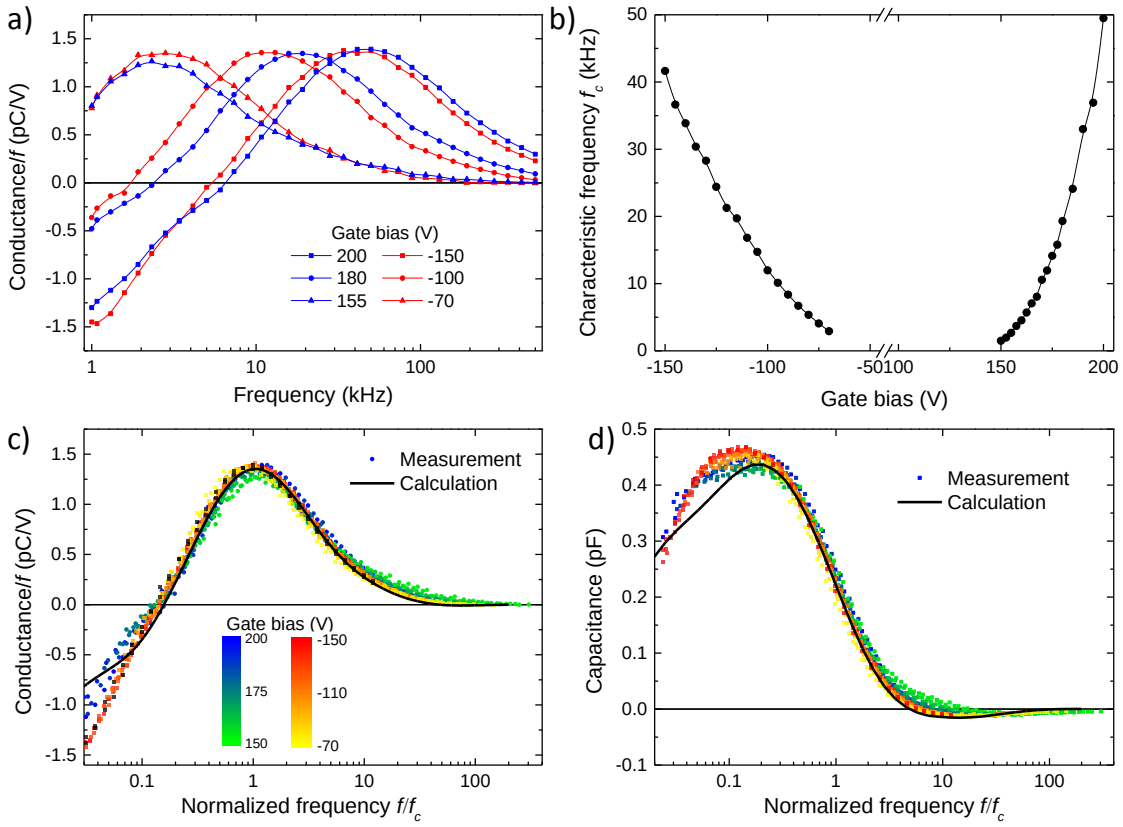

Figure 4.4: Impedance spectroscopy results. a) Conductance-over-*f* for various gate biases. b) Characteristic frequency, defined as the maximum of conductance-over-*f*, as function of gate bias. c,d) Measured and calculated conductance-over-*f* c) and capacitance d) as function of the normalized frequency. The color bars indicate the applied gate bias. L_{fing} = 160 µm and L_{sp} = 50 µm.

4.4.2 Contactless mobility measurement

We shall now turn to the contactless mobility measurement. Impedance spectroscopy was performed on a finger-gate structure on the same substrate on which also the ambipolar OFETs of Figure 4.3 were measured. The source and drain contacts far away from the modulated region were grounded to fix the chemical potential in the channel. Gate biases varying from -150 to -65 V and from 200 to 150 V were applied to create hole or electron accumulation channels, respectively. Note that accumulation layers can be filled completely despite the presence of charge injection barriers. In steady state no current is flowing in the transistor channel and therefore no charges are injected or extracted at the contacts. The finger-gate system was biased by a 3 V AC-bias applied to a finger and sweeping its frequency from 1 kHz to 500 kHz, while monitoring the current at the grounded second finger gate. The resulting conductance-over-*f* data are shown in Figure 4.4a. An impedance signal could be measured both for negative gate biases where holes are accumulated as well as for positive gate biases where electrons are accumulated. The conductance-over-*f* shows a clear maximum at the characteristic frequency of the finger-gate system. A shift of the conductance spectrum to higher frequencies is observed as the absolute gate bias increases, in accordance with Equation

(4.7). The characteristic frequency, here taken as the position of the maximum, as function of gate bias is plotted in Figure 4.4b. In Figures 4.4c and 4.4d the impedance results are compared with the numerical simulations. To show that a meaningful characteristic frequency can be defined also from experiments all data in Figure 4.4a are collapsed on single curves in Figures 4.4c and 4.4d by normalizing the frequency by the characteristic frequency. The drawn lines represent the simulation results and the dots represent the measured data. An excellent qualitative and quantitative agreement is found with the numerical simulation for all measured gate biases.

The mobility can now straightforwardly be extracted from the position of the characteristic frequency. The charge carrier mobility in transistors is usually determined from the transfer characteristics by measuring the change in drain current dI_D upon a small change in the gate bias dV_G using:

$$\mu_{lin} = \frac{dI_D}{dV_G} \frac{L_{FET}}{W_{FET} C_G V_D}, \tag{4.8}$$

with V_D the drain bias, L_{FET} the length and W_{FET} the width of the transistor channel. This method avoids errors due to uncertainties in the threshold voltage. For a fair comparison, the mobility from the impedance data has to be extracted similarly. The mobility will therefore be extracted by calculating the change in characteristic frequency df_c upon a small change in the gate bias by differentiating Equation (4.7):

$$\mu_{imp} = \frac{df_c}{dV_G} \frac{2L_{fing} L \left(C_G + C_{fing} \right)}{C_G}. \tag{4.9}$$

The mobilities extracted from the measured impedance spectra are plotted in Figure 4.5 together with the linear mobilities extracted from the transfer curves of Figure 4.3a. Maximum mobilities extracted by impedance spectroscopy on the finger gates amount to 0.46 and 1.08 cm^2/Vs for holes and electrons, respectively. Both methods show an increase in mobility with increasing charge density. For the region where they overlap the hole mobilities extracted by impedance spectroscopy are similar to the values found in conventional DC-characterization of the transistor without hole injection barriers. However, the transistor with a hole injection barrier shows only comparable mobilities at significantly higher gate biases. A gate field is known to assist charge injection and therefore contact resistance plays a smaller role at high gate biases.[36]

Since electrons suffer from a larger injection barrier, the effect for electrons is even larger. A ~20 times higher mobility is found with impedance spectroscopy than obtained from the DC transfer curves. We have to note that this value may still be underestimated due to a gate leakage current. The leakage may cause some accumulated charges to leak away, effectively decreasing the accumulated charge density. Nonetheless, it clearly shows that due to the contact resistance the electron mobility was highly

underestimated by extracting the mobility from the transfer characteristics. With impedance spectroscopy on the finger-gate system, the mobility measurement is decoupled from charge injection and the true mobility in the transistor channel could be extracted. In some devices where record mobilities are measured, also a contact resistance is present.[4] Likely these mobilities are therefore underestimated and higher values may be obtained with the method presented in this chapter.

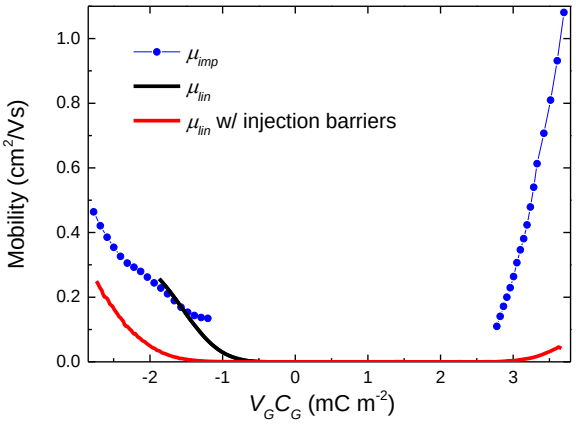

Figure 4.5: Extracted charge mobilities using impedance spectroscopy (symbols) as function of gate bias. The mobilities extracted from the transfer curves of Figure 4.1b are presented as solid lines.

4.5 Conclusion

We have presented a general applicable method to measure charge carrier mobilities in organic field-effect transistors, independent of contact resistance. By using capacitive generation and detection of alternating currents there is no need to inject and/or extract charges during the mobility measurement and contact resistance effects are avoided. For that, two additional finger gates were positioned near the accumulation channel. By performing impedance spectroscopy on the finger gates the true mobility could be determined. Comparison to mobilities measured in a conventional (DC) manner confirmed that due to contact resistance the latter present a lower limit. For our devices, the underestimation of the actual mobility went up to a factor 20 for electrons in an ambipolar device. Expressions are provided to allow application of the method to systems with arbitrary dimensions.

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Chapter 5

Light emission in the unipolar regime of ambipolar OFETs

Abstract

Light emission from ambipolar organic field-effect transistors (OFETs) is often observed when they are operated in the unipolar regime. This is unexpected, the light emission should be completely suppressed, because in the unipolar regime only one type of charge carrier is accumulated. Here, we investigate an electroluminescent diketopyrrolopyrrole copolymer. Local potential measurements by scanning Kelvin probe microscopy reveal a recombination position that is unstable in time due to the presence of injection barriers. The electroluminescence and electrical transport have been numerically analyzed. We show that the counterintuitive unipolar light emission is quantitatively explained by injection of minority carriers into deep tail states of the semiconductor. The density of the injected minority carriers is small. Hence they are relatively immobile and they recombine close the contact with accumulated majority carriers. The unipolar light output is characterized by a constant efficiency independent of gate bias. We argue that light emission from OFETs predominantly originates from the unipolar regime when the charge transport is injection limited.

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5.1 Introduction

Light-emitting organic field-effect transistors (OFETs) are being investigated as a potential light source.[1-4] For light emission holes and electrons need to recombine, hence both have to be present in the semiconductor. In the ambipolar regime both charges are accumulated simultaneously by biasing the gate in between the source and drain voltage. The charge carriers meet in the channel of the transistor, where electrons and holes recombine to form excitons and decay by the emission of light. The light output depends on the recombination rate which is proportional to the product of accumulated electron and hole density, on the singlet-triplet formation ratio, and on the photoluminescence efficiency of the semiconductor. The advantage of an OFET for light emission is the control of the recombination zone. By choosing appropriate biases, this zone can be shifted away from the source and drain contacts.[5-8] Quenching by the contacts is thereby avoided and high external quantum efficiencies have been reported.[1] Recently developed electroluminescent ambipolar polymers with increasingly high and balanced electron and hole mobilities further enhance the opportunities for the use of OFETs as light sources.[9-11]

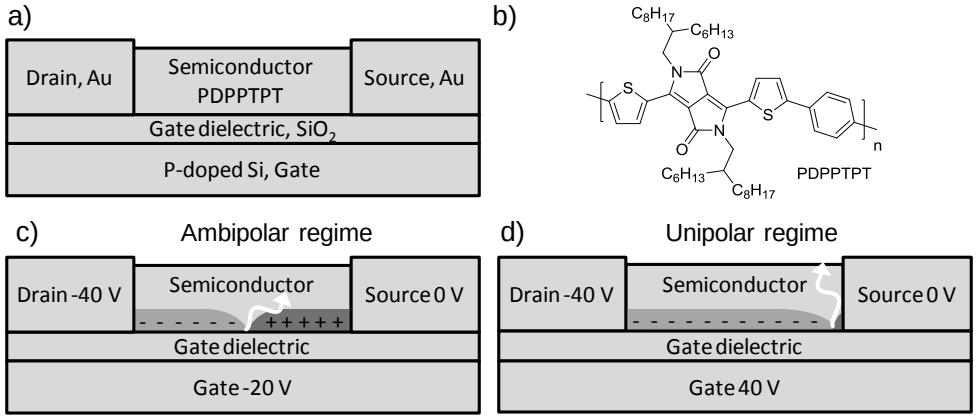

Figure 5.1: a) Schematic representation of the OFET used in this work. b) Chemical structure of PDPPTPT. c) Schematic of a transistor in the ambipolar regime. Light emission originates from the location where electrons and holes meet. d) Schematic of a transistor in the unipolar *n*-type regime. Light emission originates from the source, where the majority carriers are extracted.

The highest light output is expected when the transistor is operated in the bipolar regime, where the gate bias is in between the source and drain bias, such that simultaneously electrons are injected at the source contact and holes are injected from the drain contact (Figure 5.1c). Remarkably however, there are many examples in literature where electroluminescence is observed when the transistor is operated in one of the unipolar regimes (Figure 5.1d). In these examples a high light output has been obtained when the gate bias is not in between the source or the drain bias.[5, 12-14] Even light emission from entirely unipolar transistors has been reported.[3, 15-17] This is

unexpected, the light emission should be completely suppressed in the unipolar regime, because then only one type of charge carrier is accumulated. No satisfactory explanation has been given for this peculiar light emission.

In our investigations on charge transport of diketopyrrolopyrrole-type polymers (DPP), we observed light emission from field-effect transistors. The highest electroluminescence intensity was obtained when the transistor was biased in the two unipolar regimes. In order to determine whether and where electrons and holes are present in the channel, we performed spatially resolved scanning Kelvin probe microscopy (SKPM) measurements. We show that the transistor behaves unstably in time when both electrons and holes are accumulated. Using device modeling we show that the instability is a result of the presence of injection barriers. As a consequence of the barrier, minority carriers cannot be injected into the transport level, but only in the tail of the density of states (DOS), which is present due to disorder in the semiconductor. We argue that the unipolar light emission is due to the recombination of the accumulated majority charge carriers with the minority carriers injected in the tail of the DOS at the contact.

5.2 Experimental

Field-effect transistors were prepared on heavily doped Si wafers acting as common gate, with thermally grown SiO_2 as gate dielectric and lithographically pre-patterned gold electrodes with a 2 nm Ti adhesion layer. The resulting finger transistors have a channel length and width of 10 µm and 1 cm, respectively, and a gate capacitance of C_G = 17 nF/cm^2. To reduce gate bias stress, the gate dielectric was passivated with vapor deposited hexamethyldisilazane (HMDS). The organic semiconductor PDPPTPT was applied by spincoating from chloroform and annealed at 150 °C in vacuum for 24 hours. The chemical structure of PDPPTPT is presented in Figure 5.1b.[18] Transfer characteristics of the OFETs were measured in a high-vacuum (10^{-6} mbar) probe station with a Keithley 4200 source-measure unit. Light emission was probed by a Si photodiode (Siemens SFH 206 K) placed directly above the sample and connected to the Keithley 4200 and the EL efficiencies were derived by dividing the detected EL intensity by the source-drain current. Non-contact atomic force microscopy (AFM) and scanning Kelvin probe microscopy (SKPM) measurements were performed with an Omicron VT-SPM connected to a Nanonis controller in ultra-high vacuum (10^{-9} mbar). Pt-Ir coated AFM-tips (PPP-EFM, Nanosensors, f_{res} ~70 kHz) were used. For SKPM a 1 V AC-tip voltage (~650 Hz) was applied during scanning.

5.3 Results and discussion

5.3.1 Electrical and optical characterization

Typical transfer curves of the ambipolar OFETs are presented in Figure 5.2a. The gate bias was swept between -40 and 40 V and the drain bias was fixed at -20 , -40, and -60 V. The transfer curves show ambipolar behavior; the current is enhanced at negative gate biases due to accumulation of holes and at positive gate biases due to accumulation of electrons. The extracted saturated electron and hole mobilities are around 0.02 cm^2/Vs, similar to those obtained earlier on a SiO_2 dielectric.[18] The mobilities extracted in the linear regime are strongly dependent on the gate bias due to disorder and due to the presence of injection barriers, especially for electrons. Mobilities extracted in the saturated regime at high gate biases are only slightly underestimated.[19] The presence of an energy barrier for injection is expected since the bandgap of PDPPTPT is around 1.5 eV and electrons and holes are both injected from gold electrodes. From the HOMO and LUMO level energies as determined by cyclic voltammetry measurements[18] and by using an estimated work function of gold of 4.7 eV, we arrive at a hole injection barrier of 0.7 eV and an electron injection barrier of 1.1 eV.[20] The injection barriers are manifest in the output curves as an S-shaped curve at low drain bias.

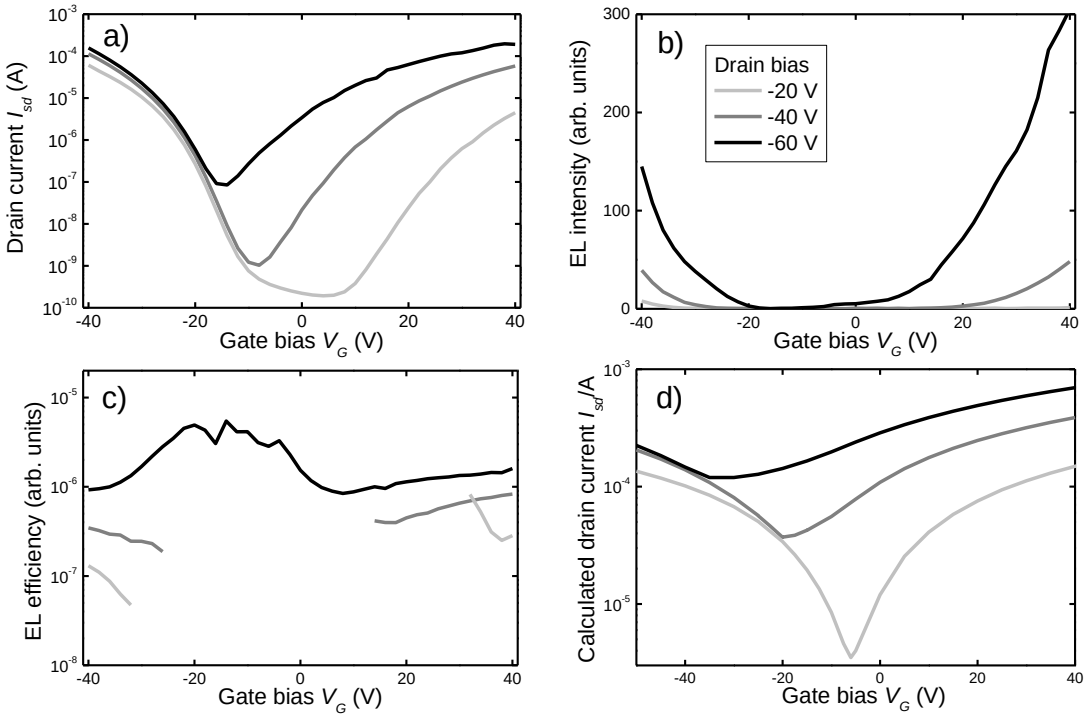

Figure 5.2: a) Transfer characteristics of an ambipolar organic transistor, measured at drain biases of -20, -40, and -60 V. b) The corresponding light emission of the transistor and c) the EL efficiency. d) Calculated transfer characteristics of a transistor with a constant mobility and an injection barrier for holes and electrons.

The electroluminescence (EL) intensity probed by the photodiode increases with both the drain and the gate bias, presented in Figure 5.2b. The highest light output is obtained

in the two extreme unipolar regimes. This implies that the recombination zone is located either at the source or the drain contact. The detected EL intensity is divided by the source-drain current to obtain a measure for the EL efficiency. This efficiency is presented in Figure 5.2c as a function of gate bias. The EL efficiency is low due to the low photoluminescence efficiency of the semiconductor. At drain biases of -20 and -40 V, the electroluminescence efficiency at low gate bias cannot be determined, because the light output is below the detection limit of the photodiode used. At higher gate biases the efficiency does not depend on the gate bias. Similarly, at a drain bias of -60 V the EL efficiency is constant for all gate biases. We note that a constant efficiency is not expected for a bipolar light emitting transistor. The efficiency should actually peak when the gate bias is halfway the source and drain bias and the recombination zone is in the middle of the channel, as experimentally verified.[7] The constant EL efficiency is characteristic for a unipolar light emitting transistor; its origin will be elucidated below.

5.3.2 Local channel potential

To determine the location of the recombination zone we probed the local channel potential, $V(x)$, in the channel with SKPM, with x the position in the channel. We define the effective gate potential, V_{eff}, in the channel as the gate bias, V_G, with respect to the local surface potential, *i.e.* $V_{eff} = V_G - V(x)$. The locally accumulated surface charge density ρ is equal to the product of the effective gate bias and the gate capacitance, $\rho = -C_G \times V_{eff}$. Electrons are induced in the channel for a positive effective gate potential and holes are induced for a negative effective gate potential. At the recombination zone, the position where the charges recombine, there is no net accumulated charge and consequently the effective gate potential is zero. The measured channel potentials for fixed gate biases are presented in Figure 5.3a, with the drain bias set at + 14 V. We first discuss the black line which is measured for a gate bias of 10 V. At small x, close to the drain electrode, the channel potential is larger than the applied gate potential. The effective gate potential is negative, which implies that holes are accumulated. The effective gate potential is zero at about x = 5 μm, so the recombination zone is close to the source contact, and predominantly holes are accumulated in the channel. The dark gray curve represents the surface potential measured at an only slightly higher gate bias of 10.5 V. The effective gate potential is now zero at about x = 0.8 μm, which implies that the recombination zone is now located close to the drain contact. Now predominantly electrons are accumulated in the channel. The light gray line represents a single measurement at an intermediate gate bias. However, the measurement is unstable; the recombination zone cannot reliably be determined. The position varies in time and oscillates between the two extremes. It is remarkable that the transistor switches from

an almost unipolar electron channel to an almost unipolar hole channel when changing the applied gate bias by only 0.5 V.

We note that in all cases a voltage drop is observed at the contacts, which indicates the presence of a large injection barrier.[21] The largest voltage drop or the biggest barrier is observed at the source where electrons are injected, in agreement with the estimation from the energy levels.

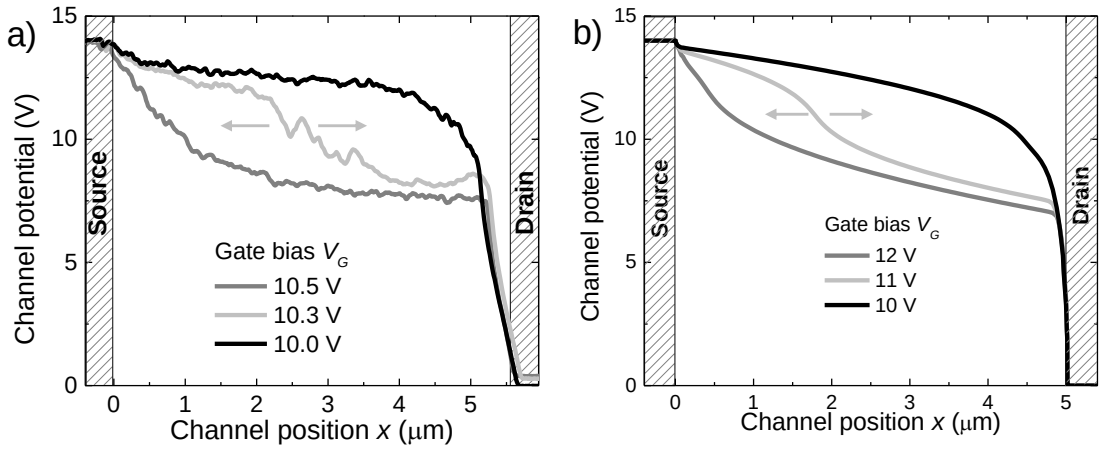

Figure 5.3: a) Measured surface potential in the channel of an operating ambipolar OFET. The gate of the transistor is biased in the ambipolar regime. At a gate bias of 10 V (black line) the effective gate potential is mainly positive, while at 10.5 V (dark gray line) the effective gate potential is mainly negative. The line in between in light gray is not time-stable. b) Simulated potential in an ambipolar transistor with a 0.39 eV injection barrier for holes and a 0.58 eV injection barrier for electrons. The arrows indicate the instability of the recombination zone.

5.3.3 Drift-diffusion calculations

To explain the origin of the instability of the recombination zone, drift diffusion calculations were performed. The electrical transport model is based on the coupled drift-diffusion, Poisson, and current continuity equations that are numerically solved on a 2D rectangular grid. A density dependent mobility will decrease the conductivity of the minority channel in the transistor with respect to the majority channel, which destabilizes the recombination position. In order to disentangle the effect of injection barriers from effects due to a field- and density dependent mobility we use a constant mobility in the simulations. We note however that this approximation does not affect the generality of the conclusions. The charge injection is described by classical thermionic emission. The Emtage O'Dwyer model is used to take lowering of the injection barrier by the image force into account.[22] This makes the charge injection field dependent. Electrons and holes are assumed to recombine via the Langevin mechanism. No loss mechanisms as exciton quenching are incorporated. The calculation method is described in detail in Appendix A.

As a first step we calculated the electrical transport. The transfer curves obtained are presented in Figure 5.2d. As input parameters we used the experimentally extracted saturated mobilities and an injection barrier for holes and electrons of 0.39 eV and 0.58 eV, respectively. We note that these values are lower than estimated above, since disorder lowers the effective injection barriers.[22] The simulated results qualitatively agree with the measured transfer curves of Figure 5.2a. At high positive and negative gate biases, in the unipolar regimes, the absolute current values are dominated by the saturated mobility of 0.02 cm2/Vs, which is used as input in the calculations. In the ambipolar regime, where the drain bias is larger than the gate bias, the calculated current is higher than the measured current. The origin is that in the calculations we use a constant mobility while the mobility is actually gate bias dependent.

It may seem counterintuitive that despite a large injection barrier charges can be injected, but in fact a field-effect transistor is tolerant for injection barriers. The origin is image-force lowering of the barrier due to the high electric field at the injecting contact. In a transistor under accumulation the electric field at the injecting contact progressively increases with increasing gate bias. Hence, at low gate bias the current is injection limited, but by increasing the gate bias injection barriers up to 1 eV can be surmounted.[23]

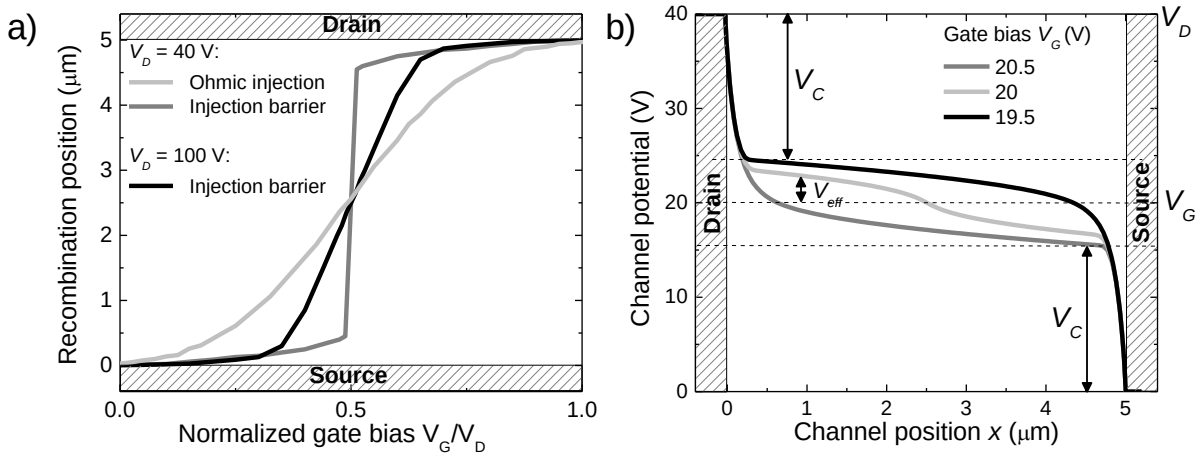

Figure 5.4: a) The position where recombination takes place in an ambipolar OFET as function of the gate bias normalized by the drain voltage for three situations. In dark gray the situation with injection barriers of 0.65 eV for both holes and electrons and 40 V at the drain, in black the situation with identical injection barriers and 100 V at the drain, and in light gray the situation with Ohmic injection. b) The potential in the channel of an OFET with injection barriers of 0.65 eV for both holes and electrons and 40 V at the drain for three different gate biases. The effective gate potential, V_{eff} , in the channel is reduced due to the voltage drop at the contacts.

5.3.4 Unstable recombination position

The calculated surface potentials as a function of gate bias are presented in Figure 5.3b. We used the same input parameters as used for the calculation of the transfer curves, viz. the extracted saturated mobilities and an injection barrier for holes of 0.39 eV and for electrons of 0.58 eV. Comparison of Figures 5.3a and 5.3b shows that a good

qualitative agreement between measured and calculated potentials is obtained. The black line represents an almost unipolar *p*-type channel and the dark gray curve an almost unipolar *n*-type channel. The position of the recombination zone close to either the source or the drain contact is reproduced. Within a bias window of 2 V the transistor operation switches from unipolar hole to unipolar electron transport. For intermediate gate biases the position of the recombination zone strongly depends on the input parameters. Note that the heights of the barriers are chosen such that the calculated potential drop in Figure 5.3b corresponds with the measured potential drop in Figure 5.3a. The exact values of the injection barriers are not critical for the behavior of the transistor as will be explained below. If the barriers are increased to, for example, 0.65 eV the same unstable behavior is observed, as shown in Figure 5.4b.

The experimentally and numerically established extreme sensitivity of the recombination zone position on gate bias can be understood as follows. We distinguish three regions in the transistor, two interfacial regions near the contacts and one bulk region in between. The total applied source-drain bias V_D is distributed over these three regions. In absence of injection barriers V_D entirely drops over the bulk region. In this situation, the recombination zone position can be gradually moved across the bulk region by varying the effective gate bias between 0 and V_D. The position of the recombination zone as function of gate bias calculated without injection barriers is presented with the light gray line in Figure 5.4a. Note that we so far tacitly assumed identical source and drain contacts which, in combination with zero hole and electron injection barriers (Ohmic contacts), implies a zero bandgap semiconductor. For a semiconductor with a finite bandgap E_g, significant ambipolar transport only sets in when $V_D \gg E_g$. Assuming a symmetric device, the recombination zone position moves across the bulk region when the effective gate bias is between $E_g/2$ and $V_D - E_g/2$. We now drop the Ohmic contact assumption. Part of the source-drain bias, V_C, will now fall across the interfacial region at both the source and the drain. Then only $V_D - 2V_C$ will fall over the bulk region. An example of such a situation is depicted in Figure 5.4b where 0.65 eV injection barriers are used for both holes and electrons. The recombination zone position moves across the bulk region for effective gate biases between $V_C + E_g/2$ and $V_D - V_C - E_g/2$, still assuming symmetry. This condition can be understood by regarding the bulk region as a separate ambipolar channel with Ohmic contacts, albeit with a lower applied source-drain bias of $V_D - V_C$. Hence, it is clear that with increasing importance of injection barriers (increasing V_C) the sensitivity of the recombination zone position on gate bias increases, i.e. it runs from one side of the bulk to the other in an increasingly narrow window of the effective gate voltage, c.f. the black and dark gray lines in Figure 5.4. The ultimate situation is reached when the device is fully injection limited. In that case,

ambipolarity still demands both electron and hole accumulation on either side of the recombination zone, so the voltage drop over the bulk must at least remain equal to, roughly, E_g, so $V_C = V_D - E_g$. In this limit, the gate voltage window in which the recombination zone transits the entire bulk region goes to zero: any small change affecting the electrostatics in the device may completely shift the recombination zone. The recombination zone is unstable.

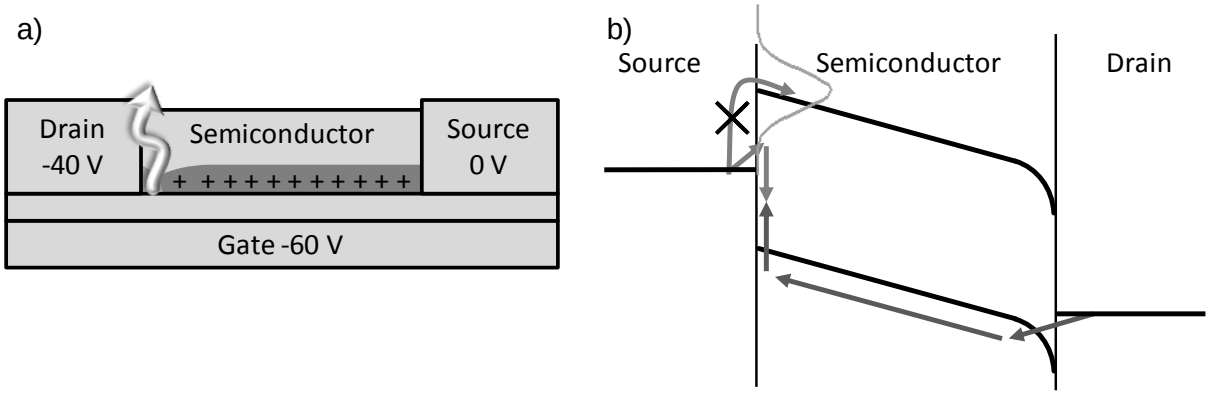

Figure 5.5: a) Schematic of an OFET biased in the unipolar *p*-type regime. b) Schematic of the corresponding band diagram. The Gaussian depicts the broadened density of states. The dark gray arrows represent the movement of holes and the light gray arrows the movement of electrons. The injection barrier is too high for the minority carriers, the electrons, to be injected in mobile states.

5.3.5 Description of unipolar light emission

The light output is proportional to the recombination current. Hence we calculated the recombination current as a function of gate bias, with similar input parameters used for the simulation of Figure 5.2d, viz. a constant mobility. Irrespective of the injection barrier, the highest light output is obtained in the ambipolar regime, when the gate bias is about in between the source and drain bias. The light output decreases with increasing gate bias. In the limiting case of the unipolar regime when the gate bias is close to either the source and drain bias the light output is negligible. The experimental data of Figure 5.2b cannot be reproduced; the reason being that the density of minority carriers in the calculations is too low. The explanation is elucidated in Figure 5.5. A transistor is biased in the unipolar *p*-type regime. Holes are injected by the drain and accumulated in the channel. The band diagram shows an injection barrier. Due to the accumulated holes in the channel, a large fraction of the source-drain bias drops near the drain contact. The resulting high electric field leads to strong image forces, effectively eliminating the injection barrier for holes. This mechanism does not apply for the minority carriers, here electrons from the source. Since the gate does not accumulate electrons there is no significant electric field near the source, hence no image force barrier lowering. In the calculations electrons have to overcome an insurmountable energy barrier and the density of injected electrons is negligible. Consequently there is no recombination.

To explain the experimentally observed light output the injection mechanism has to be adapted. So far we have assumed injection into a single transport level with a well-defined energy. For semiconducting polymers the energy bands are broadened by disorder. As illustrated in Figure 5.5, minority carriers can be injected into the tail states that are lower in energy. Both the density and the mobility of the tail states is low.[24] The current is therefore still dominated by the majority carriers; the minority carrier current density can be disregarded. The calculations are adjusted by introducing a low density of tail states at a lower energy than the mobile states. Transport between tail states only occurs by thermal activation via the mobile states. We note that the outcome of the calculations is independent of the mobility of the tail states, as long as the density and mobility of the tail states is significantly lower than the states higher in energy.

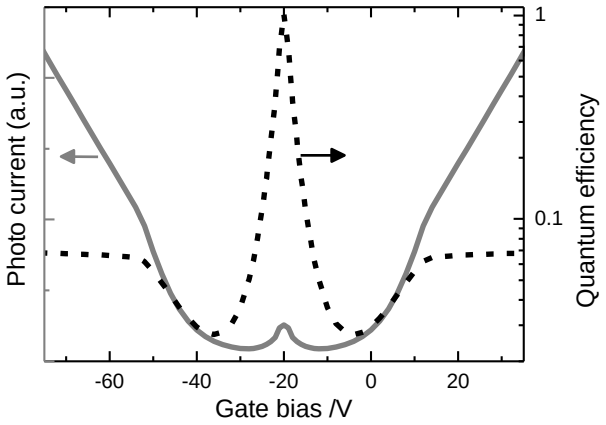

Figure 5.6: Solid line (left axis): the calculated EL intensity as function of gate bias when injection in tail states is incorporated in the simulation. Dashed line (right axis): the corresponding efficiency. The drain bias was set at 40 V.

The adapted description of minority carrier injection does not affect the calculated charge-transport results of Figures 5.2d and 5.3b. In the ambipolar regime minority carriers do not play a role for charge transport and its density is low. The calculated electroluminescence intensity, which is proportional to the recombination current, is presented in Figure 5.6 as a function of gate bias. The highest light output is obtained in the two extreme unipolar regimes, when the gate bias is close to either the source or the drain potential. A good qualitative agreement with the experimental data of Figure 5.2b is obtained. In this description light is mainly emitted from tail states. The spectrum of the emitted light at the contacts will therefore probably be red shifted compared to light emitted from the middle of the transistor channel. However, since charge transport already occurs via the lowest energy states, the red shift may be very marginal. Care has to be taken that a shifted spectrum has no different origin such as e.g. varying cavity effects.[2]

The quantum efficiency, calculated by dividing the total recombination current by the source-drain current, is presented as the dashed line in Figure 5.6. In the unipolar regimes the efficiency is constant. The reason is that the efficiency only depends on the density of minority carriers, which does not change with gate bias. Quenching at the contacts, out-coupling and photoluminescence efficiencies are being ignored. The absolute value of the minority density depends on the local field at the majority extracting contact, the energy levels and density of the tail states. Effectively, the calculated efficiency strongly depends on the magnitude of the injection barrier. Figure 5.6 shows that the efficiency has a maximum in the ambipolar regime. However, the source-drain current is then low, and the electroluminescence intensity is much smaller than the unipolar light output. In the measurements the source-drain current is even lower in the ambipolar regime due to the density dependent mobility and, therefore, the peak is not observed. We note that a different injection mechanism for minority carriers has been reported by Santato et al.[16] They need a potential drop at the minority carrier injecting contact. As explained above, this is highly unlikely.

5.4 Conclusions

The light emission in organic ambipolar field effect transistors is investigated. SKPM measurements have shown that the recombination zone is unstable in the ambipolar regime. Numerical calculations have shown that this instability is a direct consequence of the presence of injection barriers. The highest light output is observed when the transistor is biased in the unipolar regime, where just one type of charge carrier is accumulated. This counterintuitive light emission is quantitatively explained by taking injection of minority carriers into tail states into account. This injection starts to dominate when substantial injection barriers are present. The density of the injected minority carriers is small. Hence they are relatively immobile and they recombine close the contact with accumulated majority carriers. Field-effect transistors based on luminescent ambipolar semiconductors emit in the ambipolar regime when the contacts are Ohmic. However, when the charge transport is injection limited, unipolar light emission is obtained.

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Chapter 6

Fundamental limitations for electroluminescence in OFETs

Abstract

Optically excited lasing and amplified spontaneous emission have been observed in a wide range of organic semiconductors. However, the lasing threshold for electronically pumped lasers has not been reached in organic light-emitting diodes. Light emission is quenched by the metal electrodes and the injected free charge carriers annihilate the formed excitons. To compensate for these recombination losses and to reach population inversion a higher current density is required. A suggested and promising alternative device is a light-emitting dual-gate ambipolar field-effect transistor, in which one gate accumulates electrons and the other gate accumulates holes. The high field-effect mobility yields extremely high current densities in the separate channels. When the electron and hole currents can be forced to recombine the recombination current could easily exceed the lasing threshold. Here we confine both electrons and holes in a single semiconducting film. For thick films two independent channels are formed, however, these are physically and electrically separated from each other. For thin films we show that only one type of charge carrier can be injected. It is concluded that independent hole and electron accumulation is mutually exclusive with vertical recombination and light emission.

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6.1 Introduction

Since the demonstration of the optically pumped organic laser,[1-2] there has been a quest to create an electrically pumped organic laser.[3-5] An organic laser is potentially compact, wavelength and power tunable and may be manufactured at low cost.[6-10] The electrical currents in organic light-emitting diodes (OLEDs) have been pushed to their limits to reach population inversion. The lower limit for the current density needed for lasing is about 100 A/cm^2 as estimated from an optically pumped organic laser.[5] These currents have been reached in OLEDs and light-emitting electrochemical cells (LECs).[8-10] The lasing threshold however has not yet been reached. The bottlenecks have recently been reviewed.[3] The first source of losses associated with electrical pumping is the presence of the charge carriers themselves. The polarons have broad absorption bands that overlap with the emission bands and therefore lead to absorption of laser photons or to quenching of excitons.[4, 11-12] Second, under optical excitation triplets are formed only by intersystem crossing and their presence is not deleterious. However, under electrical excitation triplet excitons are more abundant than singlet excitons due to their creation probability ratio of 3 to 1 and due to their long lifetimes of up to milliseconds. The triplets will lead to optical losses by absorption of laser photons and or by quenching of the singlet emission.[11, 13-14] Finally, the electrodes in an OLED are problematic because light generated close to the electrode is quenched. Since the charge carrier mobility in an OLED is relatively low, thin films are needed to obtain high current densities for population inversion. The recombination then occurs close to the electrodes leading to enhanced unfavorable electrode quenching.[15]

An ambipolar organic field-effect transistor (OFET) offers an elegant way to obtain high current densities and to diminish the exciton quenching by the electrodes.[16] By biasing the gate in between the source and the drain voltage both electrons and holes are accumulated. The charge carriers meet in the channel of the transistor where they recombine to form excitons which then decay by the emission of light. By choosing appropriate biases the recombination zone can be set away from the contacts whereby exciton quenching is eliminated.[17-19] High external quantum efficiencies for light-emitting OFETs have been reported.[4, 20]

Recently developed polymers offer field-effect mobilities for both holes and electrons exceeding 1 cm^2/Vs.[7, 21-22] Current densities in the OFET channel in the order of 100 kA/cm^2 can then be obtained, definitely exceeding the lasing threshold estimated from the optically pumped laser. However, these current densities can only be realized in the unipolar regime of the transistor, where the gate bias is larger than the drain bias. Unfortunately light emission is then impeded, because only one type of charge carrier is accumulated. In short, the highest recombination efficiency is obtained when the

transistor is biased in the ambipolar regime where the current is inherently low. On the other hand, a high current density is obtained when the transistor is biased in the unipolar regime but then the efficiency is inherently low. This fundamental problem might be solved by adding a second gate yielding an ambipolar dual-gate transistor. As schematically shown in Figure 6.1, two accumulation layers are then formed which allows accumulating holes and electrons independently. Holes can be accumulated in one channel and electrons in the other. The two gates can both be biased in the unipolar regime yielding high field-effect mobilities. Here we will address the recombination and the prospects for light emission. To this end we investigate experimentally and theoretically dual-gate ambipolar field-effect transistors as a function of semiconductor layer thickness. For thick semiconductor films two accumulation layers can be formed but they are physically and electrically separated from each other, whereas for thin films only one type of charge carrier can be accumulated. Hence, we will show that it is fundamentally impossible to make two accumulation layers that are close enough to each other to force the charge carriers to recombine. Independent hole and electron accumulation is mutually exclusive with vertical recombination and light emission. The operation mechanism will be compared to that of conventional light-emitting diodes.

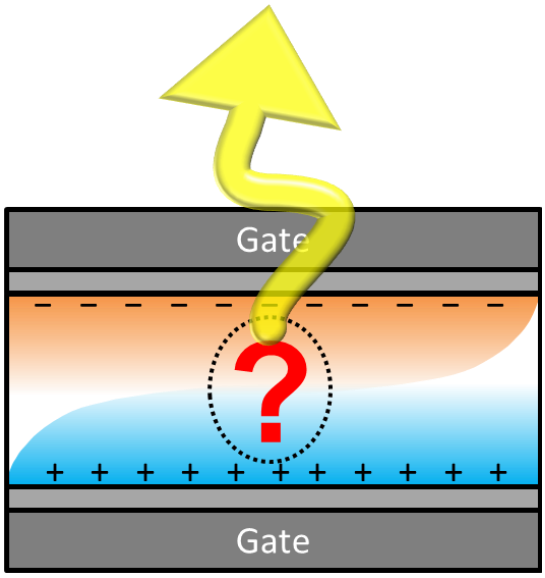

Figure 6.1: Schematic of a light-emitting ambipolar dual-gate field-effect transistor. Holes and electrons are independently accumulated by the bottom gate and top gate respectively. The question addressed is whether the electrons and holes can be forced to vertically recombine yielding stimulated emission.

6.2 Experimental

The ambipolar dual-gate transistors were prepared on heavily doped Si wafers acting as a common bottom gate, with 200 nm thermally grown SiO_2 as bottom gate dielectric and lithographically patterned 50 nm gold source drain electrodes on top of a 2 nm Ti adhesion layer. The interdigitated electrodes yield a channel length and width of 10 µm and 1 cm respectively. The bottom gate capacitance, C_{BG}, amounts to 17 nF/cm^2. The

SiO_2 gate dielectric was passivated with vapor deposited hexamethyldisilazane to reduce gate bias stress. The organic semiconductor PDPPTPT (Figure 6.2b) was applied by spincoating from chloroform. The concentration and spin speed were adjusted to vary the layer thickness from 8 to 57 nm as measured with atomic force microscopy. The top gate dielectric was a spincoated 750 nm thick Cytop layer (C_{TG} = 2.4 nF/cm^2). Subsequently, the stack was annealed at 150 °C in vacuum for 24 hours. Finally, as transparent top gate electrode indium tin oxide (ITO) was applied by sputter deposition. Transfer characteristics of the OFETs were measured in a high vacuum (10^{-6} mbar) probe station with a Keithley 4200 source-measure unit. The electroluminescence (EL) was probed by a Si photodiode (Siemens SFH 206 K) placed directly above the device and was measured along with the electrical characteristics.

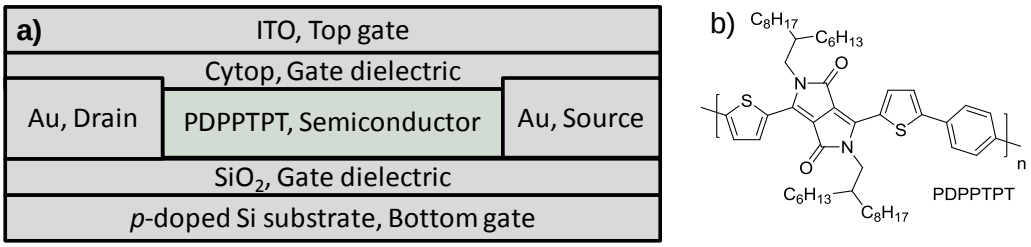

Figure 6.2: a) Schematic representation of the investigated dual-gate ambipolar OFETs. b) Chemical structure of the ambipolar semiconductor.

6.3 Results and discussion

6.3.1 Electrical characterization

The device lay-out of the fabricated dual-gate organic field-effect transistor is schematically presented in Figure 6.2a. The semiconductor film thickness was varied between 57 nm and 8 nm. Transfer curves for the transistors with the 57 nm and 8 nm thick film are presented in Figure 6.3a and b respectively. Transistors with other layer thicknesses yield transfer curves in between these two extreme cases. The bottom gate is swept between -40 and +40 V at fixed top-gate biases between –100 and +100 V in steps of 10 V. The transfer curves show ambipolar behavior; the current is enhanced at negative gate biases due to accumulation of holes and at positive gate biases due to accumulation of electrons. The extracted saturated hole and electron mobilities are around 0.02 and 0.01 cm^2/Vs, respectively, similar to the values found in Chapter 5. By sweeping the top gate bias, not shown here, a similar ambipolar behavior is observed. The extracted saturated hole and electron mobilities are then slightly higher, around 0.03 and 0.02 cm^2/Vs.

The transfer curves for the 57 nm thick semiconductor film, Figure 6.3a, show that, irrespective of the bottom gate bias, the drain current increases with increasing top-gate bias. This holds both for positive top-gate bias, in green, and for negative top-gate bias,

in purple. Effectively, the transfer curve shifts up and down with the set value of the top gate bias.

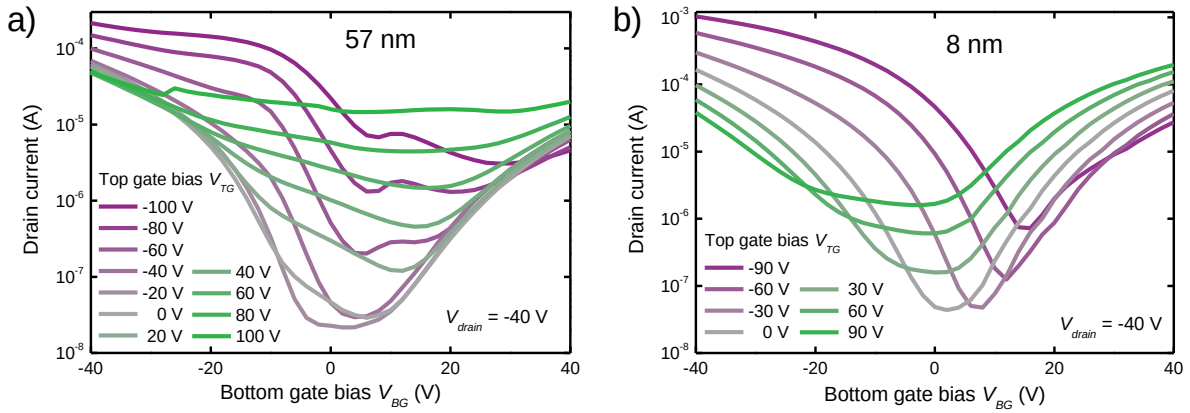

Figure 6.3: a,b) Experimental transfer curves of the dual-gate ambipolar transistor with an organic semiconductor thickness of a) 57 nm and b) 8 nm.

The transfer curves for the thin semiconductor, Figure 6.3b, show a completely different phenomenological behavior. For positive top gate biases, in green, the drain current is enhanced for positive biases on the bottom gate, but is suppressed for negative biases on the bottom gate. Similarly, for negative top gate biases, in purple, the drain current is enhanced for negative biases on the bottom gate and is suppressed for positive biases on the bottom gate. Effectively the shape of the transfer curve remains the same, but the threshold voltage shifts with applied top gate bias.

6.3.2 Operational mechanism

The different behavior of the transfer curves of the thick and thin semiconductor layer can phenomenologically be understood as follows. When the semiconducting layer is thick enough, two parallel accumulation layers are created, as schematically shown in Figure 6.4c. The field of each gate is compensated by the accumulated charge carriers in the nearest channel and therefore electrically decoupled from the other accumulation layer. The top and bottom channel then behave independently, as shown by the equivalent circuit of Figure 6.4a. When the bottom gate is swept the current through the top channel is set by the fixed top gate bias. The current through the top channel leads to a constant offset of the transfer curve. In contrast, when the semiconductor film is thin apparently only one ‘effective’ accumulation layer can be created, as schematically shown in Figure 6.4d. The current is controlled by both gates simultaneously as schematically depicted in the equivalent circuit of Figure 6.4b. The shape of the transfer curve remains the same, only the threshold voltage shifts. A similar difference in the transfer curves between a thick and a thin semiconducting layer was previously observed in unipolar hole-only transistors.[23-25]

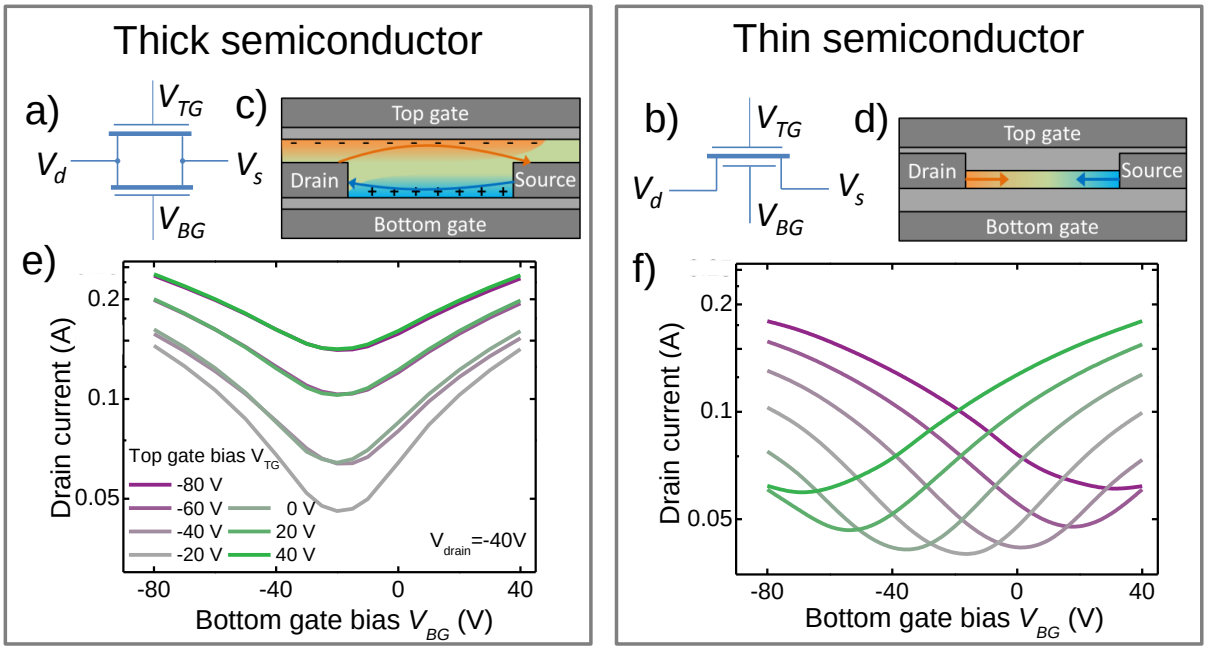

Figure 6.4: a,b) Schematic of the electrical equivalent circuit of a dual-gate transistor with a a) thick semiconducting layer and b) a thin semiconducting layer. c,d) Schematic operation mechanism of a dual-gate transistor with c) a thick semiconducting layer and d) a thin semiconducting layer. The top and bottom gate independently regulate the current in the parallel accumulation layers for thick layers. For thin layers the gates jointly regulate the current in the single accumulation layer. e,f) Calculated transfer curves of a dual-gate transistor with a semiconductor thickness of e) 55nm and of f) 5 nm.

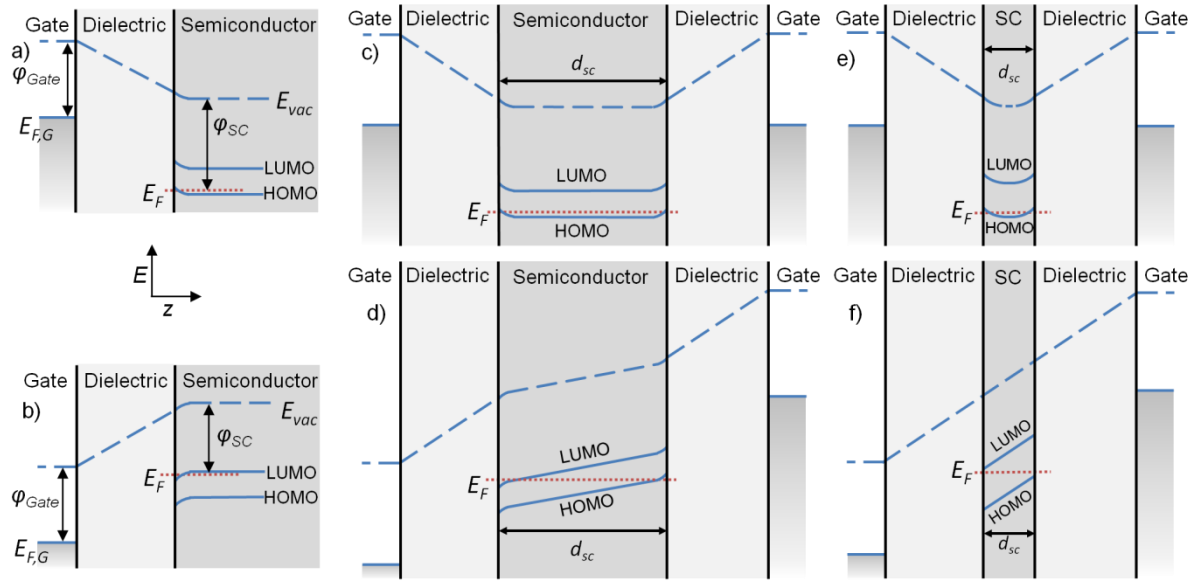

Figure 6.5: Schematic band diagrams for a, b) a single gate *p*- and *n*-type OFET and a dual-gate OFET where the two gates are c,e) equally biased and d,f) oppositely biased, with a semiconducting layer that is c,d) thick and e,f) thin. φ_{SC} indicates the local ionization potential.

To elucidate the implications for device operation and light emission in case of an ambipolar semiconductor we first look at the band diagrams of the two extreme cases of a thick and a thin semiconductor layer. The band diagrams for hole and electron accumulation by a single gate are presented in Figure 6.5a and b respectively. When a

bias is applied to the gate, charge carriers accumulate in the semiconductor and screen the gate field. The Fermi level is fixed by the source and drain contacts. The HOMO level has to bend towards the Fermi level when holes are accumulated, while the LUMO level has to bend towards the Fermi level when electrons are accumulated.[26] Note that as a consequence the semiconductor ionization potential is larger in hole accumulation than in electron accumulation; the ambipolar semiconductor appears to be *p*-type or *n*-type depending on the applied gate bias.

In a dual-gate transistor the two accumulation layers influence each other via the shared semiconductor. The thickness of the semiconductor, d_{sc}, determines the strength of the electrostatic interaction. At zero source-drain bias, *i.e.* thermal equilibrium, the Fermi level is constant in the semiconductor. The (related) situations of nonzero source-drain bias and of separate source-drain contacts for each accumulation layer will be discussed later on. In Figure 6.5c the situation is shown when the bias on both gates is of equal sign, here negative. The ionization potentials of the two accumulation layers are equal and the accumulation layers have no electrostatic interaction. However, the ionization potentials are unequal when the bias on both gates is of opposite sign (Figure 6.5d). An electric field is then present in the semiconductor since *n*- and *p*-type regions are formed in a single semiconductor. Note that the origin of the electric field is equivalent to the built-in field in diodes, where also *p*- and *n*-type regions are brought in contact. The magnitude of the built-in electric field, F_{BI}, is related to the bandgap of the semiconductor, E_g, and the thickness of the organic layer as

$$F_{BI} \cong \frac{E_g}{qd_{sc}}, \tag{6.1}$$

with q the elementary charge.

The appearance of the built-in field in the semiconductor has several important implications. First, the presence of a field in the semiconductor implies that the gate field is incompletely screened, which in turn implies a reduced density of accumulated charges in the accumulation layer(s). Secondly, when the electric field, F, created by the gates is smaller than the built-in field, $F < F_{BI}$, the HOMO and LUMO levels cannot both cross the Fermi level E_F, as illustrated in Figure 6.5e. Hence, when the gate field is lower than F_{BI}, two accumulation layers of opposite polarity will not be formed. Lastly, the built-in field drives electron and hole accumulation layers vertically apart.

In a dual-gate transistor with a thick semiconducting film the field F_{BI} is low with respect to the applied gate fields and the reduction of the accumulated charge density is negligible. Consequently, the gates with their corresponding accumulation layers will behave independently. In the limit of an infinitely thick semiconducting film the source-

drain current I_D can therefore be written as the sum of the current of two independent transistors, each controlled by their own gate:

$$I_D = I(V_{TG}) + I(V_{BG}). \tag{6.2}$$

When the semiconducting film thickness is decreased, for instance to force the electron and hole accumulation layers together, the field in the semiconductor increases and its effect on the accumulation layers can no longer be neglected. For thin enough semiconducting films the required field F_{BI} will even exceed the maximum applicable gate fields. The situation of oppositely biased gates in a thin-film device is depicted in Figure 5f. The gate field does not lead to charge accumulation since the HOMO and LUMO levels do not cross the Fermi level. Consequently, the gate field is unscreened and continues into the semiconductor. When a fixed bias is applied to the bottom gate, an opposite bias applied to the top gate will therefore first deplete the bottom channel, as shown in Figure 5f, before it will lead to charge accumulation of the opposite sign. This inhibits the simultaneous creation of a hole and an electron accumulation layer.

The above-discussed restriction for charge accumulation in a dual-gate OFET with a thin semiconducting film is reflected in the transfer characteristics. When varying the bias of one gate of the OFET, accumulated charge density is lowest when the gates are oppositely biased. The minimal source-drain current is reached when the gate field of one gate is exactly counteracted by that of the other gate, *cf*. Figure 6.3b. Changing either of the gate voltages beyond this (tunable) threshold induces a single accumulation layer. Effectively this situation is equal to a shift in the threshold voltage of a single gate OFET. This threshold voltage shift, ΔV_{th}, depends on the capacitive coupling between the two gate dielectrics as

$$\Delta V_{th} = -\frac{C_{TG}}{C_{BG}} V_{TG}, \tag{6.3}$$

with V_{TG} the top gate bias, C_{TG} the capacitance of the top dielectric and C_{BG} the capacitance of the bottom dielectric.[25] Hence, in the limit of an infinitely thin semiconducting film the current can be written as the current in an ambipolar transistor with just one gate, of which the threshold voltage can be shifted by the second gate:

$$I_D = I\left(V_{BG} - \Delta V_{th}\right). \tag{6.4}$$

So far we have assumed a constant Fermi level throughout the semiconductor. The situation becomes more complicated when a bias is applied between the source and the drain electrode and therefore the electron and hole quasi Fermi levels will vary along the channel. In particular, this variation will be different for electrons and holes. The dual-gate transistor is therefore calculated using a numerical drift-diffusion model. The model is described in Appendix A. In brief, it solves the coupled drift-diffusion, Poisson and continuity equations on a rectangular grid by forward integration in time until steady

state is reached. The calculated transfer curves are shown in Figure 6.4e and f for a thick and thin semiconducting layer respectively. The on/off ratio of the simulations is lower than in the experiments because a constant mobility of 0.02 cm^2/Vs is used, whereas the experimental mobility is gate bias dependent. Essentially the same behavior is found as in the experiments for both thin and thick semiconducting layers. More importantly, the quantitative results are fully consistent with the qualitative arguments given above.

6.3.3 Light emission from the dual-gate ambipolar OFETs

Figure 6.6 shows the measured EL for the transistors with a 57 nm and 8 nm thick semiconducting layer. In both transistors light emission is observed in the two unipolar regimes, similarly as observed in Chapter 5. In the transistor with the thick semiconductor enhanced light emission is observed when the top gate bias is increased to positive voltages (Figure 6.6a). The light emission then peaks at intermediate bottom gate biases, i.e. in the ambipolar regime. We attribute this effect to an enhanced electron injection that is facilitated by the top gate bias.[27] Both a strong accumulation of charges and a large gate field are known to lower injection barriers.[28] Since in the transistor with the thick semiconductor two accumulation layers can be created simultaneously, the extra accumulation layer can help to lower the injection barrier. The lowering of the injection barrier results in the emission of light in the ambipolar regime.

In the transistor with the thin semiconductor the light emission is maximal when the gates are biased with the same polarity (Figure 6.6b). In this situation the highest current is reached in the transistor. Importantly, by biasing the two gates with opposite polarity no enhanced light emission is observed. The reason is that in the thin film it is impossible to simultaneously accumulate electrons and holes. The bias applied to the top gate only changes the effective threshold voltage of the transistor and thereby shifts the curve of the light emission.

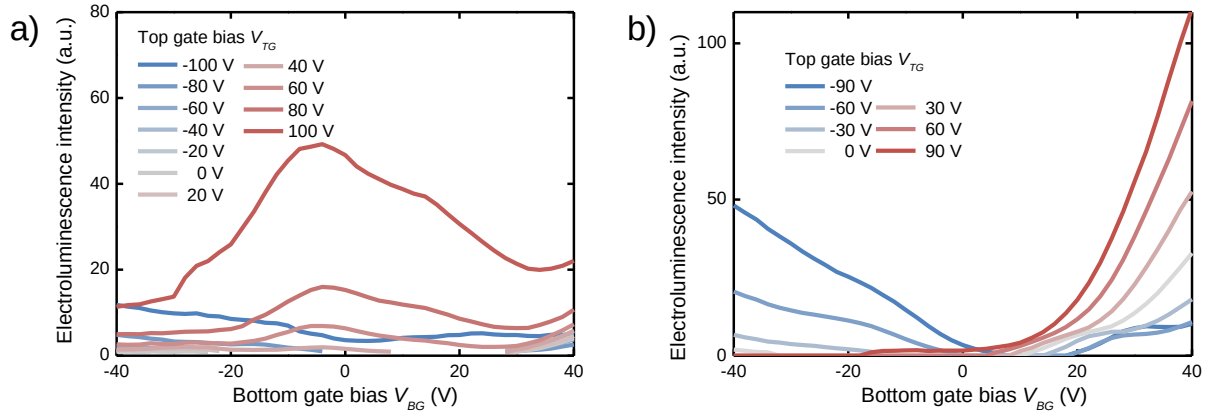

Figure 6.6: Electroluminescence characteristics of the ambipolar dual-gate transistor with an organic semiconductor thickness of a) 57 nm and b) 8 nm.

6.3.4 Fundamental limitations for recombination

Above we explained that in a dual-gate OFET either two independent, and therefore disconnected, accumulation layers are formed, or just a single one. The impossibility to create independent accumulation layers that at some position connect to yield electron-hole recombination is fundamental. One could argue that, even for very thin layers, it is always possible to simultaneously accumulate charges of opposite sign by just increasing the gate bias enough. However, then charges in the semiconductor are still separated from each other by a large field F_{BI}. This prevents the electron and hole accumulation layers to connect and recombine. Having accumulation layers of opposite polarity is therefore mutually exclusive with efficient electron-hole recombination, *i.e.* light emission.

In 2000, Schön et al. reported that the accumulated holes and electrons can be forced to vertically recombine yielding laser action.[29] This paper was later retracted,[30] however the presented ideas are still considered reasonable.[31-32] In order to have a recombination current flowing between the two accumulation layers, the field F_{BI} has to be cancelled at some position in the channel. For a dual-gate transistor this requires a potential difference between the electron and the hole accumulation layers that, at some place, exceeds the bandgap. Control over the position can in principle be achieved by employing two separate sets of source and drain electrodes, one on either side of the active layer.[29] However, applying a potential difference between the accumulation layers is fully equivalent to the situation commonly encountered in light-emitting diodes where the built-in potential has to be surmounted to have current flowing, as illustrated in Figure 6.7. At the position of recombination, the dual-gate transistor then functions as a conventional light-emitting diode, the only difference being that the role of the charge injecting contacts is played by the accumulation layers. In such a configuration recombination is obtained via a bipolar space charge limited current between the accumulation layers. In this case the recombination current density in the dual-gate OFET can never be as high as in the equivalent OLED: after injection from the contacts of the OFET the charges have to travel to the recombination zone through the accumulation layer, instead of being directly injected into the same recombination zone from the OLED contacts. Hence there is no fundamental advantage of using a dual-gate ambipolar transistor over a regular OLED when designing electronically pumped organic lasers.

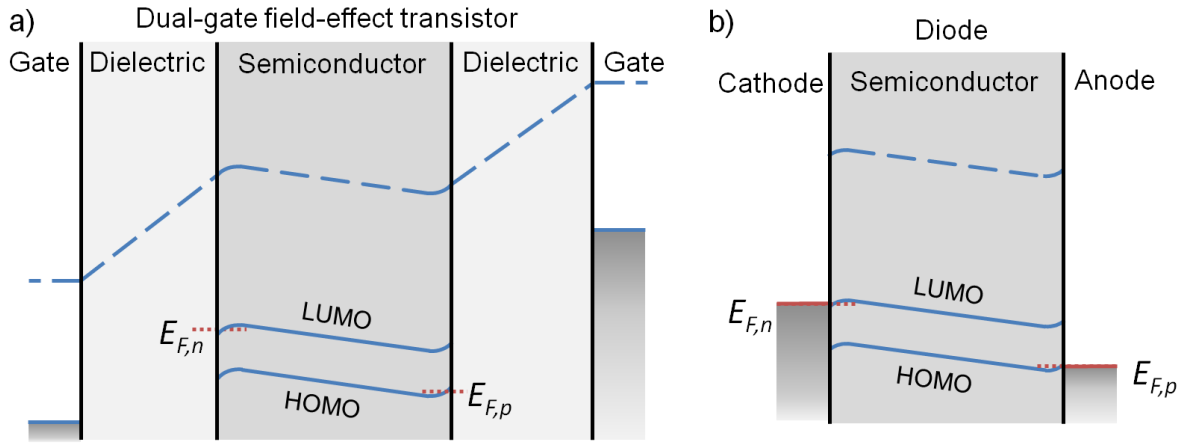

Figure 6.7: a) Band diagram of a dual-gate ambipolar field-effect transistor, with a potential difference between the two accumulation layers. The potential difference cancels the built-in field in the semiconductor. The HOMO and LUMO levels close to the dielectric are curved to form the accumulation layers due to the gate fields. b) Band diagram of a light-emitting diode in forward bias. The Ohmic contacts curve the HOMO and LUMO levels close to the cathode and anode.

6.4 Conclusion

In the quest for an organic electronically driven laser ambipolar dual-gate transistors have been investigated. We have addressed the fundamental question whether the accumulated holes and electrons can vertically be forced together to recombine. To this end we have experimentally measured and numerically modeled the charge transport as a function of semiconductor layer thickness. For thick films two independent accumulation layers are formed that do not electrically communicate. For thin films however only one type of charge carrier can be accumulated at a time. The fundamental reason is the constraint put by the continuity of the electrostatic potential within the semiconductor.

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Chapter 7

Fast ambipolar integrated circuits

Abstract

Ambipolar integrated circuits were prepared with poly(diketopyrrolopyrrole-terthiophene) (PDPP3T) as the semiconductor. The field-effect mobility of around 0.02 cm^2/Vs for both electrons and holes allowed for fabrication of functional integrated CMOS-like inverters and ring oscillators. The oscillation frequency was found to have a near quadratic dependence on the supply bias. The maximum oscillation frequency was determined to be 42 kHz, which made this ring oscillator the fastest ring oscillator on the date of publication.

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7.1 Introduction

Copolymers with diketopyrrolopyrrole (DPP) units are emerging as attractive semiconducting materials for organic solar cells and transistors.[1-10] In DPP based bulk-heterojunction solar cells power conversion efficiencies over 8% are obtained and high hole mobilities are found in field-effect transistors (FETs).[4-11] For FETs even ambipolar operation is observed.[2, 7-10] Efficient injection and transport of both electrons and holes allows for the fabrication of CMOS logic based on ambipolar transistors, i.e. CMOS-like logic, which combines the robustness and good noise margin of truly complementary logic with the ease of processing of unipolar logic. CMOS-like logic has been demonstrated,[12-13] but the availability of an ambipolar semiconductor that exhibits both high and balanced electron and hole mobilities has been the main bottleneck to manufacture complementary-like logic that competes in performance with its unipolar counterpart. The polymer PDPP3T (Figure 7.1a) exhibits nearly balanced electron and hole mobilities.[4] Here, we show the first integrated circuits based on DPP-copolymers. CMOS-like ring oscillators operating at frequencies up to 42 kHz are demonstrated. These were the fastest organic CMOS-like circuits at the date of publication in 2011 and even higher speeds were obtained by Kronenmeijer et al. in 2012.[14] The frequencies obtained in CMOS-like circuits approach the speeds obtained in state-of-the-art organic CMOS[15] and organic unipolar circuits.[16-18] This makes DPP-copolymers viable candidates to act as the semiconductor in high performance organic logic.

7.2 Experimental

Integrated circuits were fabricated from FETs with patterned gates on a monitor wafer in a bottom-gate bottom-contact architecture (Figure 7.1a). To build the transistor gates and a first interconnect layer a phosphorous doped polycrystalline silicon layer (250 nm) was applied via chemical vapor deposition, structured by conventional photolithography, and thermally oxidized to yield the gate oxide (206 nm) with a gate capacitance of 17 nF/cm^2. Then vertical interconnects were defined by photolithography. Next titanium/gold was sputtered and patterned creating the source and drain electrodes and the second layer of interconnects. Finally, PDPP3T was applied by spin coating, after which the stack was annealed at 140 °C in vacuum for 24 h.

7.3 Results and discussion

The SiO_2 gate dielectric is thermally grown on the polycrystalline gate, which is notoriously rough. The resulting rough dielectric surface could hamper charge transport. The AFM topography of the bare gate dielectric and gold source and drain contacts is presented in Figure 7.1b. The root-mean-square roughness of the bare SiO_2 dielectric is

very large, about 9 nm. To study the impact of this roughness on the charge transport, we fabricated 16 identical transistors, all with a channel length, *L*, of 5 μm and a width, *W*, of 1000 μm. In Figure 7.1c transfer curves of these transistors are plotted for different drain biases. The transistors exhibit similar electrical characteristics; the standard deviation in the drain current is only 10%. The averaged electron and hole mobility amounts to 0.02 cm^2/Vs and 0.04 cm^2/Vs respectively, comparable to the mobility in FETs made using atomically smooth SiO_2.[4] The hysteresis is slightly larger than observed before, which we tentatively ascribe to a more hydrophilic gate dielectric surface.[19]

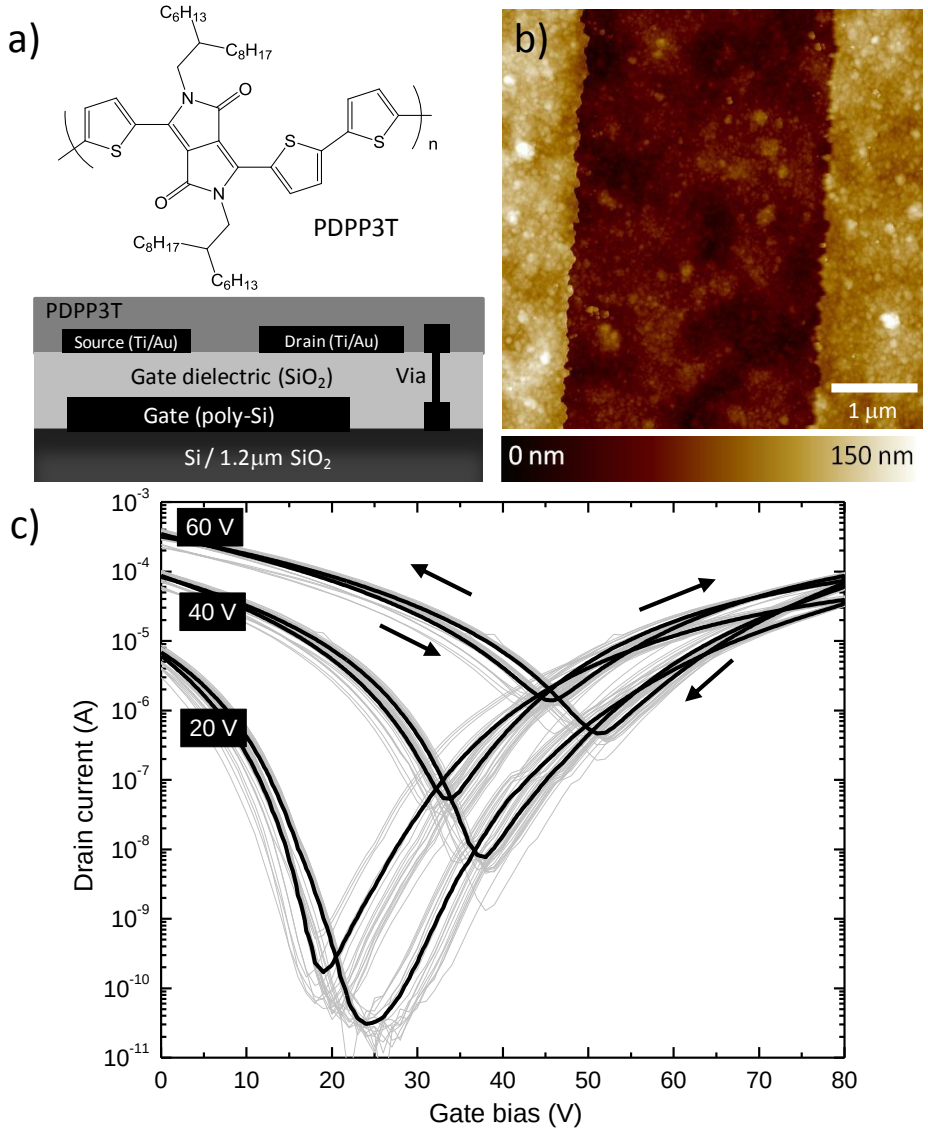

Figure 7.1: a) Structure of PDPP3T and cross-section of the transistor and vias. b) AFM topography of the bare SiO_2 gate dielectric on polycrystalline silicon (middle) with source and drain contacts (left and right). c) Gray: transfer characteristics of 16 identical PDPP3T transistors (*L* = 5 μm; *W* = 1000μm) measured at drain biases of 20, 40, and 60 V. Black: average of the 16 transfer characteristics.

The apparent insensitivity of the charge carrier mobility in PDPP3T to the gate dielectric surface roughness is remarkable in view of earlier findings where pentacene or pBTTT films were used.[20-23] There, a mobility decrease by two orders of magnitude was reported for a similar surface roughness of 9 nm. We conjecture that the insensitivity of the charge carrier mobility in PDPP3T to the surface morphology of the dielectric is due to the amorphous nature of the film, in contrast to pentacene and pBTTT which are polycrystalline. The high mobility and uniformity of the fabricated PDPP3T transistors enables integration of multiple transistors into more complex circuits.

7.3.1 Inverter

FETs made with PDPP3T are ambipolar, *i.e.* both electrons and holes can be injected using a single electrode material, here gold. The transistors allow for fabrication of integrated circuits not based on unipolar logic, but on complementary-like logic instead. In CMOS-like logic an inverter is created by combining two ambipolar transistors as depicted in the Figure 7.2a. Both gates are shorted and the source of the first transistor is connected to the drain of the second. The input bias, V_{in}, is then applied to the shorted gates, while the output voltage, V_{out}, is read from the point where the source and drain of both transistors are connected. In Figure 7.2b a typical static input/output characteristic is shown of an inverter based on two identical transistors with L = 5 μm and W = 100 μm. Voltage inversion is demonstrated for both negative and positive supply biases, V_{DD}, as expected for an ambipolar inverter.

The operation mechanism of a CMOS-like inverter working in the first quadrant is schematically depicted in Figure 7.2c. An inverter is basically a voltage divider with two transistors acting as tunable resistors, controlled by the input voltage. When the input bias is low (V_{in} = 0 V, region 1) more holes are accumulated in OFET1 than in OFET2, making the resistance of OFET1 lower than that of OFET2. As a consequence, V_{out} approaches V_{DD}. When the input bias is increased to about half the supply bias V_{DD}, OFET1 and 2 work in *p*- and *n*-type modes, respectively, with about equal charge density and resistivity. Hence, the output voltage is about half the input voltage. When the input bias is increased even further and approaches the supply bias (V_{in} = V_{DD}, region 3), more electrons are accumulated in OFET2 than in OFET1. The resistance of OFET2 is therefore lower than that of OFET1 and V_{out} approaches zero. The steepness of the slope of the inverter curve indicates the gain of the inverter. The present PDPP3T-based inverters have a gain around 20, which is comparable to that of state-of-the-art CMOS-like inverters and to organic inverters made on atomically smooth SiO_2.

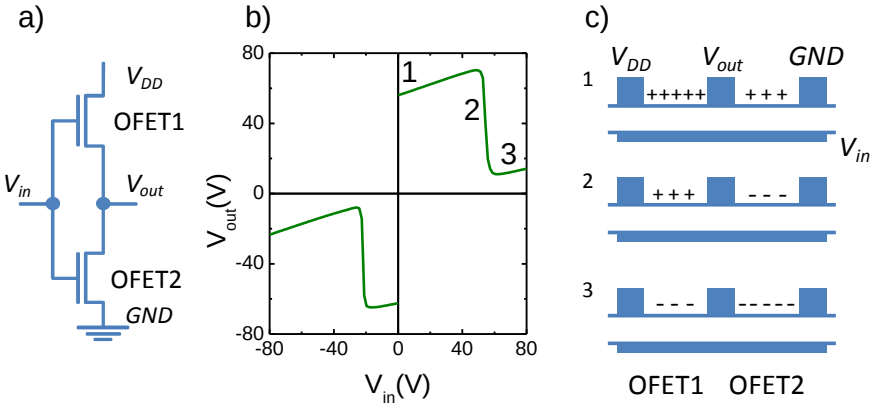

Figure 7.2: . a) CMOS-like logic inverter schematic. b) Typical input-output characteristic of an inverter based on two identical transistors (L = 5 µm, W = 100 µm) measured at a supply bias V_{DD} of -80 and 80 V. (c) Schematic diagram of the operation mechanism of a CMOS-like inverter in 3 regions as indicated in b): (1) V_{in} = 0 V, (2) $V_{in} \approx V_{DD}/2$, and (3) $V_{in} = V_{DD}$.

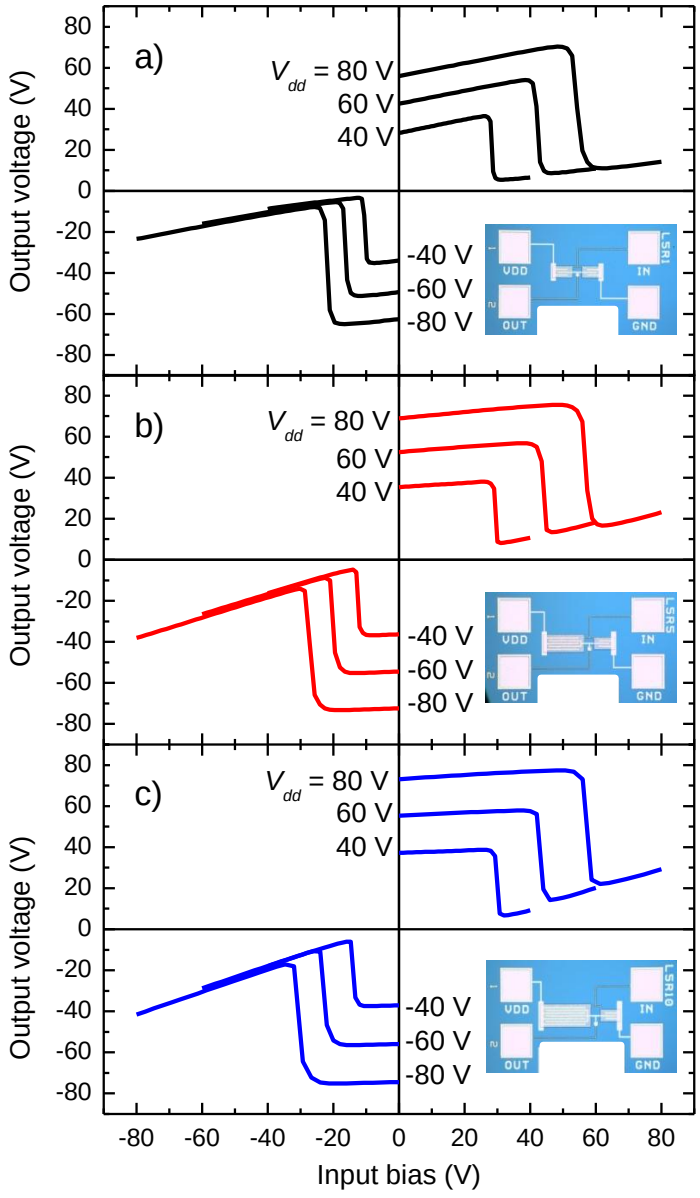

Figure 7.3: . Input-output characteristics of three inverters. The width of OFET1 is increased from a) 100 µm to b) 500 µm and c) 1000 µm. The inset shows an optical micrograph of each inverter.

Ambipolar transistors can never be switched off completely (Figure 7.1c). Due to the accumulation of charge carriers in the transistors at input voltages close to 0 V and V_{DD}, the inverter is consuming power in both states. This is a drawback of CMOS-like logic as compared to truly CMOS logic where the transistors can be switched off and the power consumption is minimal in these states. The undesirable current is reflected in a positive slope of the inverter characteristics in region 1 and 3. The slope depends on the mobility of electrons and holes and on the lateral dimensions of the two transistors. To optimize the characteristics of the inverter we changed the geometry of the composing transistors. Figure 7.3a-c shows input-output characteristics for different supply biases as the width of OFET1 in the inverter is increased from 100 to 500, and 1000 μm. When OFET1 is enlarged, a decrease of the positive slope is observed in region 1 while the slope in region 3 is increased. In this way the width of the transistors is a handle to optimize the inverter characteristics.

7.3.2 Ring oscillator

Five inverters were connected in series to create an integrated CMOS-like ring oscillator (Figure 7.4a,b). To read out the state of the ring oscillator a buffer stage was implemented. Three kinds of fully functional five stage ring oscillators were fabricated based on the inverters presented above. We focus on the ring oscillator comprising identical transistors, because it outperformed the other ring oscillators. The output of the oscillator as a function of time is depicted in the inset of Figure 7.4c. An oscillation frequency of about 42 kHz was obtained at a supply bias of 130 V. The device geometry may be enhanced in future work to decrease the required supply bias.

The oscillation frequency is found to have a quadratic dependence on the supply bias for values of V_{DD} larger than about 80 V (Figure 7.4c). A tentative explanation follows from the waveform of the measured output voltage of the ring oscillator, V_{out}, which exhibits a saw-tooth shape (Figure 7.4c inset). This shape implies that the pull-up and pull-down transistors are always in saturation (like in Figure 7.2b – region 2). The saturated current of one inverter stage is used to charge the capacitance, C_L, of the next inverter stage. Current conservation then yields:[24]

$$\frac{\mu C_{ox} W}{2L}(V_{DD} - V_{th})^2 = -C_L \frac{dV_{out}}{dt}, \tag{7.1}$$

where V_{th}, μ and C_{ox} are the threshold voltage, the electron and hole mobility and the gate oxide capacitance, respectively. The charging time or stage delay time can then be calculated by integrating Equation (7.1). The oscillation frequency, f, which is proportional to the inverse of the stage delay time, is then given by:

$$f \sim \frac{\mu C_{ox} W}{4LC_L \Delta V_{out}}(V_{DD} - V_{th})^2 C_{ox}, \tag{7.2}$$

with $\Delta V_{out} = \int_{V_{min}}^{V_{max}} dV_{out}$, where V_{max} and V_{min} are the maximum and minimum output voltages during the oscillation, respectively. The effective mobility for electrons and holes was measured to be nearly constant at gate biases larger than 80 V. Hence for large biases a quadratic dependence is found in good agreement with Figure 7.4c. For smaller gate biases the mobilities are not constant but depend on the gate bias yielding a more than quadratic dependence of oscillation frequency on bias.

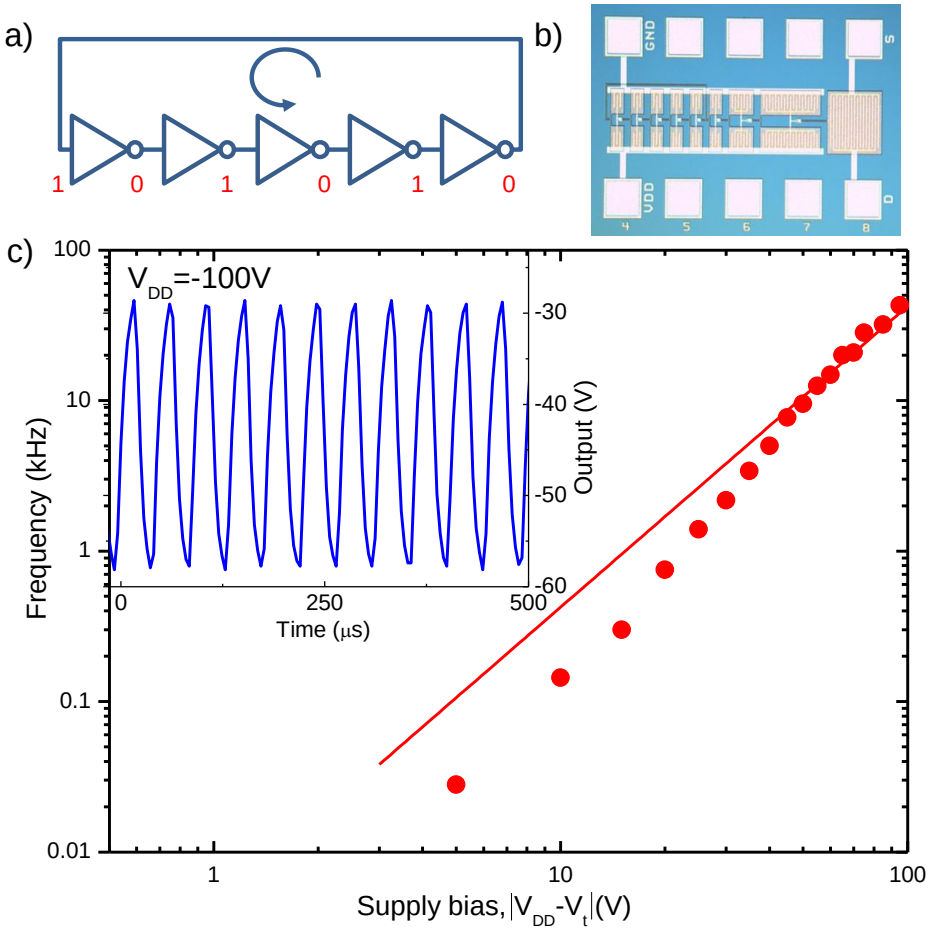

Figure 7.4: a) CMOS-like logic ring oscillator schematic. b) Optical micrograph of the integrated ring oscillator. c) Log-log plot of the oscillation frequency vs. supply bias (markers) with quadratic fit (line), V_{th}=35V. Inset: output of the ring oscillator vs. time at V_{DD} = 100 V, determined by measuring the current through a transistor in the buffer stage.

7.4 Conclusion

We demonstrated ambipolar transistors, integrated CMOS-like inverters, and ring oscillators with PDPP3T as semiconductor. The obtained oscillation frequency in ring oscillators was determined to be 42 kHz, which made this ring oscillator the fastest ring oscillator on the date of publication.

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Chapter 8

Outlook

Abstract

In an ambipolar dual-gate transistor, electrons and holes can be accumulated independently. Although no recombination between independent accumulation layers takes place in a dual-gate transistor, still high densities of electrons and holes are present in close vicinity. The distance between the electron and hole accumulation layers is only the semiconductor film thickness. A pulsed driving scheme applied to the gates can enforce recombination of the accumulation layers. The computer simulations show that a singlet exciton density may be obtained that exceeds the lasing threshold. Moreover, quenching mechanisms introduced by electrically pumping are minimized in this device concept.

8.1 Introduction

Electrically pumped lasing has not yet been obtained in organic semiconductors. To obtain lasing in organic semiconductors, the singlet exciton density needs to exceed a threshold to achieve population inversion. The electrical currents in organic light-emitting diodes (OLEDs) have been pushed to their limits to reach this threshold. The lower limit for the current density needed for lasing is about 100 A/cm^2 as estimated from an optically pumped organic laser. These currents have been reached in OLEDs and light-emitting electrochemical cells. The lasing threshold however has not yet been reached. The problem is that electrical pumping inevitably introduces additional losses as discussed in Chapter 6.[1] Singlets and triplets are formed in a 1:3 ratio and polarons are evidently unavoidable.[1,2] Triplets and polarons absorb laser photons or quench excitons and consequently increase the lasing threshold. With optical pumping, these losses are limited; only singlet excitons are generated by optical excitation and electrodes, polarons, and triplet excitons and are initially not present. The light-emitting field-effect transistor (LEFET) is a good candidate to achieve organic lasing, because they perform well at high current densities. However ideally excitons are formed with a low density of charges, which is not the case in a LEFET.

8.2 Driving scheme for dual-gate OFET

The dual-gate organic field-effect transistor introduced in Chapter 6 offers independent control over a hole and an electron accumulation layer. However, in Chapter 6 we found that independent hole and electron accumulation is mutually exclusive with vertical recombination and light emission in steady state. Here we propose a novel pulsed driving scheme for a dual-gate field-effect transistor to enforce recombination of the accumulation layers and to simultaneously minimize polaron quenching.

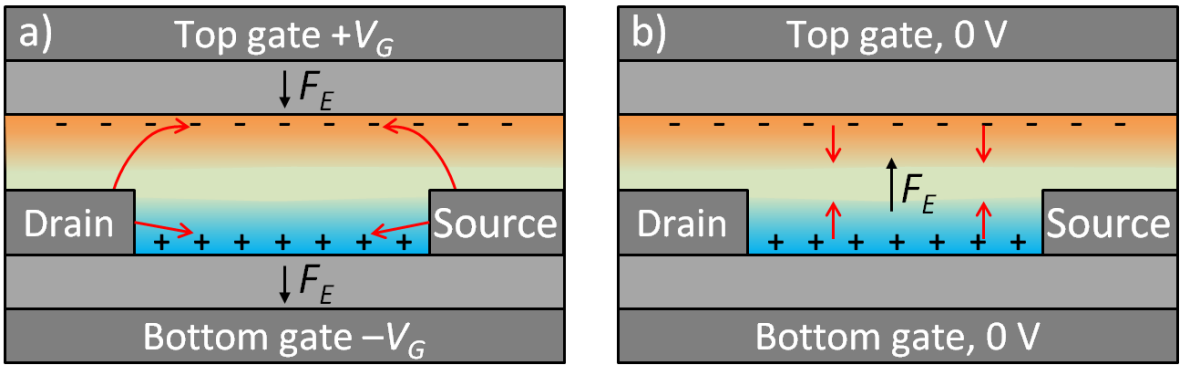

Figure 8.1: Novel driving scheme of a dual-gate transistor. a) By applying a negative bias to the bottom gate and a positive bias to the top gate, giving rise to the electric gate fields F_E, holes and electrons accumulate at the bottom and top gate dielectric, respectively. b) After removing the gate fields, the accumulated electrons and holes are attracted to each other and might recombine.

By applying biases of opposite polarity to the gates, electrons and holes are injected in the organic semiconductor and accumulation layers are formed, as depicted in Figure 8.1a. The electrons and holes are electrically and physically separated from each other by the electric gate fields, hence no excitons are formed. Nonetheless, high densities of electrons and holes are present in close vicinity. The distance between the electron- and hole accumulation layer is only the semiconductor film thickness. When all electrons and holes would be instantaneously forced to meet, all charges can recombine and transform into excitons. In order to let the charges meet, they have to be released from the gate fields. The release can be achieved by just removing the gate biases. The situation directly after removing the gate bias is depicted in Figure 8.1b. Since the charges are of opposite sign an electric field is present that drives the charge carriers towards each other. The charges will meet each other in the semiconductor and recombine to form excitons. This will create a high exciton density in a short time period, potentially leading to lasing. The excitons will subsequently decay by the emission of light. This process can be divided in the following steps:

1. Apply gate fields to fill the accumulation layers with charge carriers
2. Remove gate field
3. Charges recombine to form triplet and singlet excitons
4. Singlet excitons decay by emission of light
5. Triplet excitons decay

8.2.1 Singlet density calculation

The gate field switching experiment is simulated to get an indication of the singlet density that may be reached. The experiment is simulated using a numerical drift-diffusion model on a 2D grid, which is described in Appendix A. The calculation starts with filled accumulation layers of opposite sign and with equal charge density. The gate fields are subsequently removed and the charge and exciton densities are tracked in time. Poisson's equation is used to calculate the electric fields and Langevin recombination is assumed. A charge density independent mobility is assumed to keep the model as simple as possible.

First a simulation is performed with parameters as input comparable to the material properties of F8BT.[3] F8BT has one of the highest mobilities of the organic semiconductors that has been proven to work in an optically pumped laser. In the simulation the semiconductor thickness was taken 22 nm, the mobility 10^{-3} cm^2/Vs, the singlet (fluorensence) lifetime 5 ns and the triplet (phosphorescence) lifetime 1 μs. The gate fields were instantaneously switched from 400 to 0 V/μm.

The resulting singlet and triplet density as function of time are presented on a double logarithmic scale in Figure 8.2a. Charge and exciton densities are calculated by averaging over the volume of the semiconductor. Singlet densities are higher in the middle of the semiconductor layer and are therefore this density is shown separately. The polaron density is calculated by adding together the electron and hole density. Initially the semiconductor contains a high charge density, caused by the charges accumulated by the gates. After about 0.5 ns the polaron density decreases and the triplet and singlet exciton densities increase. Charge carriers then recombine forming excitons. The singlets already decay shortly after they were formed, because of their lifetime of 2 ns. However, for a short period a large singlet density is created in the semiconductor. The lasing threshold estimated from optically pumped lasers is around 10^{17} cm^{-3}.[4] This threshold is exceeded in this calculation, meaning that lasing may be obtained. However, loss mechanisms due to triplet and polaron quenching are not taken into account. These mechanisms likely increase the singlet threshold value or decrease the singlet lifetime.

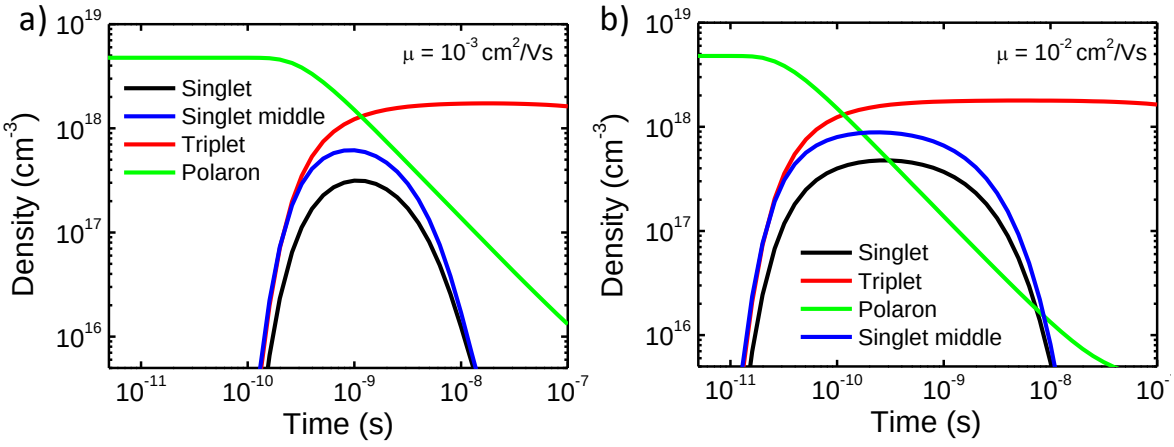

Figure 8.2: Simulation result of the switch experiment in a dual-gate OFET, with a) a mobility of 10^{-3} cm^2/Vs and b) 10^{-2} cm^2/Vs. A step in the electric field from 400 to 0 V/µm is applied at t = 0.

The singlet density that can be reached is determined by the initial accumulated charge density and by the charge recombination time. The initial gate field sets the amount of accumulated charge. Therefore this gate field has to be high enough to accumulate enough charge to reach the lasing threshold. The formation of excitons by charge recombination is competing with the singlet exciton decay rate. Recombination therefore has to be faster than the singlet exciton decay. The recombination rate is mainly determined by the mobility of the charges. With an increasing mobility, charges will meet faster, leading to higher recombination rates. Note that for the fast recombination also a fast release of the charge carriers is required. This involves a removal of the gate field that is faster than the recombination rate. This means RC charging time of the gate has to be less than 1 ns, which may be an experimental

complication. If the gate field is removed slower than charge recombination rate, this will be the recombination time limiting step.

The polaron density has to be minimized to avoid quenching. The initial accumulated hole and electron densities therefore need to be well balanced. Otherwise a surplus of one of the charge will remain after recombination. Also a fast charge recombination is required. Polarons are then transformed quickly in excitons. A simulation is performed where the mobility is increased to 10^{-2} cm^2/Vs, which is a realistic value for state-of-the-art semiconducting polymers. Charges then recombine 10 times faster as shown in Figure 8.2b. Singlets are already formed after 0.1 ns and the relative ratio of singlets and polarons becomes more favorable, especially after ~1 ns.

Lastly the triplet exciton density has to be minimized. Triplets are formed in a singlet:triplet ratio of 1:3 when electrons and holes recombine. Formation of these triplet excitons is unavoidable. However, the triplet density is lower than in a device that is operated using a continuous direct current. Triplet excitons have a lifetime that is generally a few orders of magnitude larger than that of singlet excitons. In direct current operation, singlet and triplet excitons are continuously formed. Since the singlets decay much faster than triplets, the triplets will accumulate in time. This leads to a situation where the singlet:triplet ratio is mainly determined by the lifetime of the two species, rather than their formation ratio. In our experiment excitons are not formed continuously. Triplet excitons can be given the time to decay before new excitons are formed. Important is the singlet:triplet ratio directly after a recombination event, which is at that moment determined by their formation ratio.

8.2.2 AC light-emitting device

Perumal *et al*. have published a light-emitting device which is very similar to the dual-gate transistor discussed in this Chapter.[5] However, instead of using source and drain contacts, in their device *n*- and *p*-type doping layers are used to inject charges. They sandwiched a light-emitting layer (EML) in between two (one *n*- and one *p*-type) doping layers and two electrically isolated electrodes, as schematically depicted in Figure 8.3. Indeed light-emission could be obtained by applying an alternating bias to the electrodes. When a field is created over the doped regions, electrons and holes will be extracted from the *n*- and *p*-type regions and they will drift to each other and recombine.

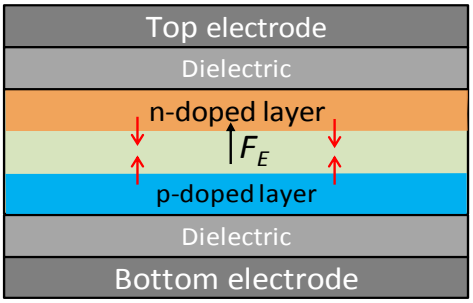

Figure 8.3: Schematic of the light emitting device with doping layers.

The difference with the dual-gate transistor is that now charges from doped regions are first injected in the EML and start to drift after applying an electric field. In the dual-gate OFET charges were already injected and start to drift from the accumulation layers after removing the gate field. The recombination process in the device is calculated using the drift-diffusion model to get an indication of the implications of these differences. The same mobility and exciton lifetime parameters are used as previously. Furthermore the same electric field is used for a fair comparison. The two doping layers and the EML all have a thickness of 20 nm and have the same energy levels. The density of free charges in the doping layers is assumed 10^{19} cm^{-3}.[5]

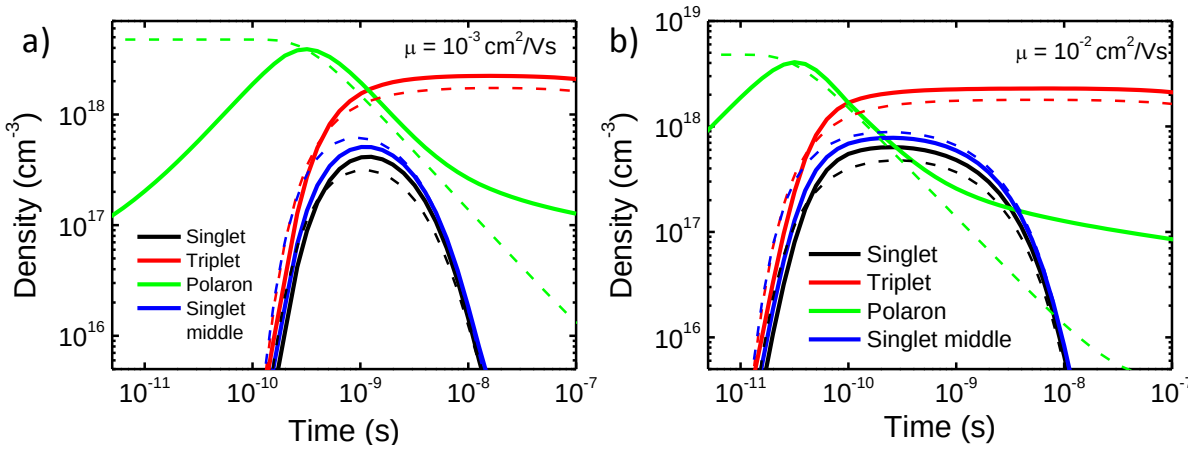

Figure 8.4: Straight lines: simulation result of the switch experiment in a light-emitting device with doping layers, with a) a mobility of 10^{-3} cm^2/Vs and b) 10^{-2} cm^2/Vs. A step in the electric field from 0 to 400 V/μm is applied at t = 0. Dashed lines: result of Figure 8.2 for comparison.

In Figure 8.4 the simulation result is shown with the drawn lines. The dashed lines represent the result obtained for the dual-gate OFET for comparison. Initialy, the polaron density increases due to charge injection from the doped layers into the emissive layer. Subsequently the polaron density peaks and decays because of recombination. The initial and final polaron density is caused by charges diffusing from the doped layers into the emissive layer. Since the electric field is in this example not high enough to push all charges out of the doped regions the layers stay doped after recombination. Importantly, a similar result is obtained in the device with the doped layers as for the dual-gate

transistor. The time required for recombination of electrons and holes is the same and about the same singlet density can be obtained. Hence, the calculations indicate that electrically pumped lasing may be feasible in dual-gate OFETs.

The required materials for the device with doped layers are however different than for the dual-gate transistor. By using doping layers, additional materials are introduced that have to match with the emissive layer. The doping layers need to have comparable charge transport properties, i.e. mobility, as the emissive semiconductor. Also the energy level alignment between the layers must be well tuned to facilitate proper injection from the doped layers into the EML. Furthermore, charges recombining in the doped layers are lost. In the simulation electrons and holes were perfectly balanced and recombination occurred in the emissive semiconductor. However the recombination zone may shift to one of the doped layers when electrons and holes are not balanced, e.g. due to a slightly different mobility or different injection properties. Nonetheless, by using doping layers the production of contacts is avoided, simplifying device processing. Therefore it is worthwhile to investigate the effect of non-ideal material properties in this AC light-emitting device for lasing.

8.3 Conclusion

By driving the dual-gate transistor in a pulsed way, a singlet exciton density may be obtained that exceeds the lasing threshold. Moreover, exciton loss mechanisms introduced by electrically pumping are minimized. The polaron density can be minimized, since all polarons are converted into excitons. For a fast conversion mobilities should be around or higher than 10^{-2} cm^2/Vs. The formation of triplet excitons cannot be avoided with electrical pumping, but the pulsed driving scheme minimizes the triplets to the singlet:triplet formation ratio of 1:3. Crucial for the experiment is that the conversion of charges into excitons is faster than the singlet lifetime. The ability to exceed the lasing threshold and simultaneously minimizing the exciton losses makes the dual-gate transistor a promising device for electrically pumped lasing in organic semiconductors.

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Summary

Charge transport and light emission in organic field-effect transistors

Organic semiconductors offer an attractive alternative for the use of silicon in large area electronics. Major advantages of organic semiconductors are their easy processing, e.g. spin coating, inkjet or silk-screen printing, and their mechanical flexibility. The performance of solution-processed organic transistors has steadily increased during the last two decades. Nowadays the organic field-effect transistor (OFET) meets mobility and stability requirements to be applied in simple integrated circuits. Moreover, field-effect transistors have emerged as a promising device lay-out to reach bright light emission. The reason is the very high current density that can be reached, and that in fact may be even high enough to reach the threshold for electrically pumped lasing. Lasing has, however not been reached. Also the stability of light-emitting field-effect transistor (LEFETs) is still limited.

To further improve the transistor performance, the charge transport needs to be described in detail. Besides intrinsic charge transport, also the injection of charges into the semiconductor is essential for the operation of organic transistors. The aim of the research described in this thesis is to enhance the description of charge transport in transistors and to improve light-emission from organic transistors.

The width and shape of the density of states (DOS) are important parameters to describe the charge transport in disordered organic semiconductors. These parameters are typically fitted to describe the measurements in existing models. In Chapter 2 it was shown that the DOS can also be measured directly. The DOS can be extracted by probing the channel potential with 'scanning Kelvin probe microscopy' (SKPM) as a function of gate bias. The energy range over which the DOS can be determined accurately is restricted by the semiconductor thickness. The method is pushed to its fundamental limit by measuring a semiconductor of only a single monolayer thick. The current in the OFET is calculated using the measured DOS in existing models. A perfect agreement between measured and calculated OFET current is obtained. This shows that detailed knowledge of the density of states is a prerequisite to consistently describe the charge transport in OFETs.

Scanning tunnelling microscopy (STM) has previously been proven to be a powerful technique to characterize semiconductors with great spatial resolution. However, the full potential of STM and scanning tunneling spectroscopy (STS) for in-situ characterization of

organic semiconductors has so far not been accessible. The underlying problem is the low intrinsic conductivity. In Chapter 3 this problem is overcome by working in a field-effect transistor. In an OFET a conducting channel can be created by the gate. This channel acts as back contact, collecting the tunneling current. Stable and high resolution STM images could be obtained on pentacene organic field-effect transistors. The tunneling current measured as a function of tip bias (STS) showed a rectifying behavior due to the unipolar behavior of the transistor used. It was shown that intrinsic organic semiconductors can be in-situ characterized with high spatial and energetic resolution in functional devices.

A key parameter to indicate the performance in organic transistors is the charge carrier mobility. However, an accurate measurement of carrier mobilities is obstructed when the charge transport is injection limited. In Chapter 4 a method is presented to measure mobilities in organic field-effect transistors, independent of contact resistance. The method uses two additional finger-shaped gates that capacitively generate and probe an alternating current in the OFET channel. The time lag between drive and probe can directly be related to the mobility. This method is fundamentally insensitive to contact resistances, since the uptake or injection of charges is not required during the measurement. Indeed higher values were found when extracting the mobility independent of the contact resistance.

In Chapter 5 the stability of light emission in organic transistors is investigated. Local potential measurements probed by SKPM reveal a charge recombination position that is unstable in time due to the presence of injection barriers. The injection barriers prevent simultaneous transport of holes and electrons in the transistor channel, hence there is only unipolar transport of the majority carriers. However, still light emission is observed when the transistor is operated in one of the unipolar regimes. This is unexpected, because in the unipolar regime only one type of charge carrier is accumulated and the light emission should be completely suppressed. The light emission is quantitatively explained by injection of minority carriers into deep tail states of the semiconductor. The density of the injected minority carriers is small. Hence they are relatively immobile and they recombine close the contact with accumulated majority carriers. From the research was concluded that light emission from OFETs predominantly originates from the unipolar regime when the charge transport is injection limited.

In Chapter 6, a dual-gate field-effect transistor is investigated for bright light emission to ultimately create an organic electrically-pumped laser. The formation of a conductive channel in field-effect transistors makes that very high current densities can be reached, but these current densities can only be realized in the unipolar regime of the transistor. Unfortunately light emission is then impeded, because only one type of charge carrier is

accumulated. On the other hand, the highest recombination efficiency is obtained when the transistor is biased in the ambipolar regime where the current is inherently low. The challenge in organic LEFETs is to find a way to utilize the high current densities found in the unipolar regime and combine this with the high EL efficiencies found in the ambipolar regime. In the dual-gate transistor, one gate accumulates electrons and the second gate accumulates holes. The two gates can both be biased in the unipolar regime yielding currents of both electrons and holes. The charges were confined in a single semiconducting film. For thick films two independent channels are formed, but these are physically and electrically separated from each other. For thin films only one type of charge carrier can be injected. It was found that independent hole and electron accumulation is mutually exclusive with vertical recombination and light emission.

In Chapter 8 an outlook is presented with an alternative pulsed driving scheme for the dual-gate transistor. Although no recombination between independent accumulation layers takes place in a dual-gate transistor, still high densities of electrons and holes are present in close vicinity. The distance of the electron hole separation is only the semiconductor film thickness. The electrons and holes are separated from each other by the gate fields. By quickly removing the gate bias, the charges can be released from their fields and be forced to recombine. In this way a singlet exciton density may be obtained that exceeds the lasing threshold. Moreover, light-quenching mechanisms introduced by electrically pumping are minimized.

In Chapter 7 transistors were integrated to create logic circuits based on an ambipolar polymer as semiconductor. The polymer has a balanced mobility of around 0.02 cm^2/Vs for both electrons and holes. This allows for fabrication solution-processed integrated CMOS-like inverters and ring oscillators. The oscillation frequency showed a near quadratic dependence on the oscillator's supply bias, with a maximum record high frequency of 42 kHz.

Samenvatting

Ladingstransport en lichtemissie in organische veldeffectransistors

In dit proefschrift worden verschillende fysische aspecten van organische veldeffecttransistors behandeld. Traditioneel wordt silicium gebruikt voor de productie van transistors. Echter, het gebruik van monokristallijn silicium op grote oppervlakken is erg kostbaar en daarom wordt er gezocht naar alternatieve materialen, zoals organische halfgeleiders. Belangrijke voordelen van organische materialen zijn dat ze met eenvoudige productietechnieken vanuit oplossing verwerkt kunnen worden en hun mechanische flexibiliteit. De afgelopen twee decennia zijn de prestaties van organische transistors snel verbeterd. Op dit moment kunnen de transistoren al toegepast worden in eenvoudige elektrische circuits. Naast circuits is het genereren van licht met hoge intensiteit een veelbelovende toepassing van organische veldeffecttransistors. Door het ontwerp van de transistors kunnen hoge stroomdichtheden gecreëerd worden. Deze stroomdichtheid kan potentieel zelfs hoog genoeg zijn om een elektrisch gepompte laser te maken van organische halfgeleiders –iets wat tot nu toe nog niet gelukt is en om dit te bereiken zal eerst de stabiliteit van de lichtgevende transistors verbeterd moeten worden.

Om de prestaties van de transistors verder te verbeteren is het cruciaal om het ladingstransport in organische transistors in detail te begrijpen. Naast het intrinsiek ladingstransport zijn ook de contacten die zorgen voor stroominjectie in en -extractie uit de halfgeleider van belang. Het doel van het onderzoek dat in dit proefschrift beschreven wordt, is het verbeteren van de beschrijving van ladingstransport in organische halfgeleiders en het verbeteren van lichtgevende transistors.

Belangrijke parameters voor de beschrijving van het ladingstransport in wanordelijke organische halfgeleiders zijn de breedte en de vorm van de toestandsdichtheid. Meestal worden deze parameters indirect afgeleid uit metingen aan ladingstransport. In Hoofdstuk 2 is de toestandsdichtheid direct bepaald met behulp van ‘scanning Kelvin probe microscopy’ (SKPM). Het bereik van de meetmethode wordt gelimiteerd door de dikte van de halfgeleidende laag. Door de dunst mogelijke laag, een monolaag, als halgeleider te gebruiken, kan de toestandsdichtheid worden gemeten over een groot energiebereik. De stroom in de transistor is berekend door de gemeten

toestandsdichtheid te gebruiken in modellen voor ladingstransport. De berekende stroom in de transistor komt uitstekend overeen met de gemeten waarden. Dit laat zien dat gedetailleerde kennis van de toestandsdichtheid in organische halfgeleiders een voorwaarde is om het ladingstransport consistent te beschrijven. Scanning tunneling microscopy (STM) heeft zich bewezen als een krachtige techniek om halgeleiders te karakteriseren met hoge laterale resolutie. Echter, doordat organische halfgeleiders een lage geleiding hebben kon STM tot nu toe niet gebruikt worden om de halfgeleiders rechtstreeks in het device te karakteriseren. In Hoofdstuk 3 is dit probleem opgelost door met een veldeffecttransistor te werken. In de transistor kan een geleidend kanaal gemaakt worden met behulp van de gate. Dit kanaal fungeert als elektrode om de tunnelstroom af te voeren naar de contacten. Het oppervlak van een transistor met pentaceen als halfgeleider is op deze manier stabiel gescand en een hoge resolutie is behaald. Dit laat zien dat een intrinsieke halfgeleider kan met hoge resolutie worden gekarakteriseerd ter plekke in de transistor.

De ladingsmobiliteit is een belangrijke parameter om het vermogen van een transistor uit te drukken. De mobiliteit kan echter niet goed bepaald worden wanneer het ladingstransport in een transistor gehinderd wordt door injectiebarrières. In Hoofdstuk 4 is een methode gepresenteerd waarmee de mobiliteit bepaald kan worden zonder dat contactweerstanden hier invloed op hebben. In de methode zijn twee vingervormige elektroden gebruikt die capacitair verbonden zijn met het transistorkanaal. De ene elektrode wordt gebruikt om een stroom in het kanaal te genereren en de andere om de stroom te meten. Het tijdverschil tussen het genereren en het meten van de stroom is direct gerelateerd aan de mobiliteit. Met deze methode is geen ladingsinjectie nodig tijdens de meting en de methode is daarom fundamenteel ongevoelig voor injectiebarrières. Op deze manier zijn inderdaad hogere waarden voor de mobiliteit gemeten in een transistor met contactweerstand.

In Hoofdstuk 5 is de stabiliteit van lichtgevende transistors onderzocht. Met behulp van SKPM-metingen in het transistorkanaal is gevonden dat de recombinatiezone instabiel is als er injectiebarrières zijn. Door de barrières kunnen elektronen en gaten niet gelijktijdig in het transistorkanaal geaccumuleerd worden. Hierdoor vindt er alleen unipolair ladingstransport in de transistor plaats. Toch wordt er in het unipolaire regime vaak licht uitgezonden. Dit is merkwaardig omdat recombinatie van elektronen en gaten nodig is voor lichtemissie, terwijl in het unipolaire regime maar één type ladingsdrager is geaccumuleerd. De emissie van licht kan verklaard worden door aan te nemen dat er een kleine fractie van de niet geaccumuleerde ladingsdragers wordt geïnjecteerd in laag-energetische toestanden. De dichtheid van deze toestanden is klein en de mobiliteit van de ladingen zal daardoor relatief laag zijn. Als gevolg zullen de ladingsdragers

recombineren met de geaccumuleerde ladingen aan het injecterende contact. Het onderzoek heeft uitgewezen dat wanneer het ladingstransport gelimiteerd wordt door de contacten lichtemissie vooral in het unipolaire regime plaatsvindt.

In Hoofdstuk 6 is een 'dual-gate transistor' onderzocht voor lichtemissie, met het ultieme doel om een organische elektrisch gepompte laser te maken. In een transistor kunnen erg hoge stroomdichtheden behaald worden, maar dit lukt alleen in het unipolaire regime. Echter, voor efficiënte recombinatie en lichtemissie moeten beide landingsdragers geaccumuleerd worden in het ambipolaire regime, maar in dit regime is de stroomdichtheid lager. De extra gate in een dual-gate transistor kan gebruikt worden om twee onafhankelijke accumulatielagen te maken. Elektronen en gaten kunnen dan gelijktijdig geaccumuleerd worden in het unipolaire regime in dezelfde halfgeleidende laag. In dikke lagen kunnen onafhankelijke accumulatielagen worden gevormd, maar de accumulatielagen zijn dan fysiek en elektrisch van elkaar gescheiden. Daarentegen kan in dunne lagen maar één type ladingsdrager tegelijk geaccumuleerd worden. Het onderzoek heeft uitgewezen dat onafhankelijke accumulatie van elektronen en gaten de verticale recombinatie en lichtemissie uit sluit.

In Hoofdstuk 8 is een alternatief concept gepresenteerd om elektronen en gaten te recombineren in een dual-gate transistor. In een dual-gate transistor kunnen hoge dichtheden van gaten en elektronen dicht bij elkaar geaccumuleerd worden. De afstand tussen de twee accumulatielagen is slechts de dikte van de halfgeleidende laag, maar de elektronen en gaten blijven van elkaar gescheiden door het elektrische gateveld. Door plotseling het gateveld weg te halen kunnen de ladingen vrij naar elkaar bewegen en recombineren. Computersimulaties hebben uitgewezen dat op deze manier een hoge dichtheid aan singlet excitonen verkregen kan worden die mogelijk hoog genoeg is voor gestimuleerde lichtemissie. Bovendien worden op deze manier van elektrisch pompen ook verliezen voor lichtemissie beperkt.

In Hoofdstuk 7 zijn organische transistors geïntegreerd in logische circuits. De transistors zijn gebaseerd op een ambipolair polymeer als halfgeleider met een gebalanceerde mobiliteit van 0.02 cm^2/Vs voor zowel elektronen als gaten. Hiermee kunnen inverters en ringoscillatoren gemaakt worden vanuit een oplossing. De oscillatiefrequentie hangt kwadratisch af van de aangelegde spanning en de maximale frequentie van de oscillator is 42 kHz, wat de hoogste frequentie is die tot dan toe gerapporteerd was voor organische ambipolaire transistors

Appendix A

Numerical drift diffusion calculations

A.1 Drift diffusion model

In Chapters 5, 6 and 8 calculations are performed based on a drift diffusion model. The drift-diffusion model calculates drift, diffusion and displacement currents by forward integration in time on a 2D grid. Using the continuity equation the charge carrier density in each grid cell is calculated for each time step. The continuity equation reads for the electron density *n* and the hole density *p*, respectively:

$$\begin{aligned} q\frac{\partial n}{\partial t} &= \vec{\nabla}\vec{j}_n + q(G - R_L) - qU_n \\ q\frac{\partial p}{\partial t} &= \vec{\nabla}\vec{j}_p + q(G - R_L) - qU_p \end{aligned}, \tag{A.1}$$

with q the elementary charge, n the electron density, j_n the electron current, p the hole density, j_p the hole current, G the generation rate (which is here set to zero), R_L the Langevin recombination rate, U_p the net hole capture into tail states and U_n the net electron capture rate into tail states. The electron and hole currents follow from the drift-diffusion equation:

$$\begin{aligned} \vec{j}_n &= -q\mu_n n\vec{F} + qD_n\vec{\nabla}n \\ \vec{j}_p &= q\mu_p p\vec{F} + qD_p\vec{\nabla}p \end{aligned}, \tag{A.2}$$

with μ_n the electron mobility, μ_p the hole mobility, F the electric field, D_n the electron diffusion coefficient and D_p the hole diffusion coefficient. The Einstein relation is used to determine the diffusion coefficient:

$$D_n = \mu_n k_B T / q\,, \tag{A.3}$$

with k_B Boltzmann's constant and T the temperature.

In the cells where the semiconductor is neighboring a source or drain cell, the electron density in the cell is given by thermionic emission from the contacts:

$$n = N_0 \exp\left(-\frac{q\varphi_n'}{k_B T}\right), \tag{A.4}$$

here N_0 is the electron density of states and φ_n' is the energy barrier for electron injection lowered by the image force. In Chapter 5 image force lowering is taken into account. The lowering of the injection barrier ϕ_n by the image force of the electric field in the direction of injection is calculated as:

$$\varphi_n' = \varphi_n - \sqrt{\frac{q\left|\vec{F}\right|}{4\pi\varepsilon_0\varepsilon_r}}, \tag{A.5}$$

with ε_o the permittivity of vacuum and ε_r the dielectric constant of the semiconductor. Equations (3) to (5) are calculated completely analogous for holes and electrons. Electrons and holes are assumed to recombine via Langevin recombination:

$$R_L = \frac{q}{\varepsilon_0\varepsilon_r} np(\mu_n + \mu_p). \tag{A.6}$$

In Chapter 5 calculations are performed with taking tail states below the LUMO or above the HOMO into account. The density of electrons in tail states n_t follows from the capturing rate U_n and recombination rate in tail states $R_{t,n}$:

$$\frac{\partial n_t}{\partial t} = U_n - R_{SRH,n}, \tag{A.7}$$

with $R_{SRH,n}$ the Shockley Read Hall recombination rate for electrons in tail states:

$$R_{SRH,n} = \frac{q}{\varepsilon_0\varepsilon_r} n_t p \mu_p. \tag{A.8}$$

For simplicity the electron tail states are assumed to be located at a single fixed energy $E_{t,n}$ below the LUMO with a density N_t. Similarly, holes tail states are located at an energy $E_{t,p}$ above the HOMO with a density P_t. The net electron capture rate U_n follows from the capture rate C_n and the emission rate E_n , viz.:

$$U_n = C_n - E_n, \tag{A.9}$$

The rate for electrons to be captured is proportional to the density of electrons and the number of empty tail states:

$$C_n = c_0\left(1 - f_{t,n}\right)N_t n, \tag{A.10}$$

with $f_{t,n}$ the fraction of filled tail states and c_0 a capture coefficient, here set to 10^{-18} m^3/s. The emission rate is related to the capture coefficient via detailed balance:

$$E_n = c_0 f_{t,n} N_t N_0 \exp(-E_{t,n} / k_B T). \tag{A.11}$$

Injection in tail states is calculated similarly to the injection in the HOMO and LUMO levels with the injection barrier lowered by E_t. The hole density in tail states p_t is calculated completely analogous to the calculation of the electron density in tail states.

Finally, the electric fields and electric potentials are calculated with Poisson's equation:

$$\vec{\nabla}\cdot\vec{F}=\vec{\nabla}\cdot(\vec{\nabla}V)=\frac{q(p-n+p_t-n_t)}{\varepsilon_0\varepsilon_r}. \tag{A.12}$$

A.2 Grid definitions

The equations are solved on a 2D grid. The grid used in Chapter 5 is defined in Figure A.5. To be able to accurately calculate the electric fields close to the contacts smaller grid spacing is used there, since this is important for injection. The grids used in Chapter 6 and 8 are defined in Figures A.2 and A.3, respectively.

Cell width (nm)		50	2	2	2	2	2	10	10	10	10	50	50	...	50	50	10	10	10	10	2	2	2	2	2	50
Cell height (nm)		1	2	3	4	5	6	7	8	9	10	11	12	...	109	110	111	112	113	114	115	116	117	118	119	120
5	1	Source	Semiconductor																							Drain
5	2																									
5	3																									
5	4																									
5	5																									
5	6																									
50	7	Dielectric																								
50	8																									
50	9																									
50	10																									
50	11	Gate																								

Figure A.5: Definition of the grid used in the simulation of Chapter 5.

a)

Cell width (nm)		200	200	200	200	...	200	200	200	200
Cell height (nm)		1	2	3	4	...	22	23	24	25
50	1	Gate 2								
50	2	Dielectric 2								
50	3									
50	4									
50	5									
5	6	Source	Semiconductor							Drain
5	7									
5	8									
...	...									
5	14									
5	15									
5	16									
50	17	Dielectric 1								
50	18									
50	19									
50	20									
50	21	Gate 1								

b)

Cell width (nm)		200	200	200	200	...	200	200	200	200
Cell height (nm)		1	2	3	4	...	22	23	24	25
50	1	Gate 2								
50	2	Dielectric 2								
50	3									
50	4									
50	5									
1	6	Source	Semiconductor							Drain
1	7									
1	8									
1	9									
1	10									
50	11	Dielectric 1								
50	12									
50	13									
50	14									
50	15	Gate 1								

Figure A.6: Definition of the grid used in the simulation of Chapter 6 for a) a semiconductor thickness of 55 nm and b) 5 nm.

a)

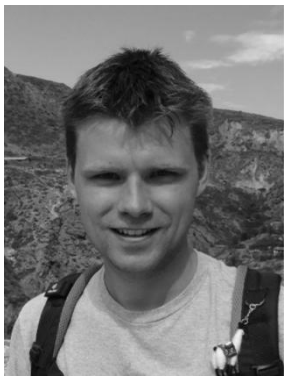
Cell width (nm)		50	50	50	50	50	50	50	50	50
Cell height (nm)		1	2	3	4	…	17	18	19	20
50	1	Gate 2								
50	2	Dielectric 2								
50	3									
50	4									
50	5									
2	6	Source	Semiconductor							Drain
2	7									
2	8									
…	…									
2	14									
2	15									
2	16									
50	17	Dielectric 1								
50	18									
50	19									
50	20									
50	21	Gate 1								

b)

Cell width (nm)		50	50	50	50	50	50	50
Cell height (nm)		1	2	3	…	8	9	10
50	1	Gate 2						
50	2	Dielectric 2						
50	3							
50	4							
50	5							
4	6	p-doped layer						
4	…							
4	10							
4	11	Semiconductor						
4	…							
4	15							
4	16	n-doped layer						
4	…							
4	20							
50	17	Dielectric 1						
50	18							
50	19							
50	20							
50	21	Gate 1						

Figure A.7: Definition of the grid used in the simulation of Chapter 6, for a) the dual-gate transistor and b) the light-emitting device with doped layers.

Curriculum vitae



Christian Roelofs was born on April 18, 1987 in Stadskanaal, the Netherlands. In 2005, he obtained his pre-university secondary education at the Peellandcollege in Deurne, after which he started to study Applied Physics at the Eindhoven University of Technology (TU/e). He obtained his bachelor's degree in 2008 followed by his master's degree in 2010. His master thesis describes the use of Kelvin probe microscopy on organic ferroelectrics and organic transistors. In 2010 Christian started his PhD focusing on light-emitting field-effect transistors. The research was carried out at the TU/e in the group "Molecular Materials and Nanosystems" of prof.dr.ir. R.A.J. Janssen under daily supervision of prof.dr.ir. M. Kemerink and at Philips Research under supervision of prof.dr. D.M. de Leeuw. The results obtained with this work are presented in this thesis. All results have been published in peer-reviewed journals and have been presented at international conferences in Atlanta, San Francisco, Boston, Barcelona, London, Barga, and Turku.

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The work presented in Chapters 2-7 is based on the following publications:

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