Dynamic multi-path WDM routing in a monolithically integrated 8 × 8 cross-connect

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Abstract: We demonstrate for the first time WDM multi-path routing through a monolithically integrated InP/InGaAsP 8 × 8 space and wavelength selective cross-connect. Data channels are dynamically routed from four input ports to the same output port with excellent OSNR from 27.0 to 31.1 dB. Representative data paths are evaluated in terms of optical power penalty. Data routing experiments are performed using round-robin scheduling with nanosecond time-scale switching times.

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OCIS codes: (250.5300) Photonic integrated circuits; (250.5980) Semiconductor optical amplifiers; (250.6715) Switching.

References and links


1. Introduction

The combination of increasing bandwidth and connectivity in high-performance computing applications, data-communications [1] and telecommunication networks [2] is leading to a relentless pressure in network switching technologies. MEMS and liquid crystal optical switching engines are increasingly deployed in telecommunication networks [3, 4]. However the assembly complexity for such free space optical systems and the relatively slow switching speeds become a concern as increasing levels of packet-based traffic permeate the network [5].

Experimental packet-compliant optical switch fabric demonstrators have previously been reported using sophisticated combinations of discrete photonic components and semiconductor optical amplifier gates. The highest connectivity systems have exploited the combination of both space- and wavelength-selective-routing [1, 6, 7]. The OSMOSIS demonstrator provided 64 channel connections by using multiplexes of eight wavelengths on each of eight input ports [7]. However the use of discrete photonic components incurs losses, delays, size, control plane complexity and energy overhead. The optical switching engines also become impractical to manufacture. A viable reconfigurable interconnection solution now requires considerable photonic integration. Recently we have reported the first 8 × 8 space- and wavelength-selective cross-connect [8–10]. This represents a radical step forward in switch integration complexity and an opportunity for considerably simplified switch fabric control.

![Architecture and photograph of the fabricated 8 × 8 cross-connect.](image)

In this paper we implement a test-bed to perform the first multi-path WDM routing experiments in such a monolithically integrated 8 × 8 cross-connect. Sixteen channels are routed from four independent inputs to the same output. Round-robin scheduling is applied
for each channel of each input port. Dynamic multi-path multi-channel provisioning is performed.

2. Integrated 8 × 8 cross-connect

The architecture for the monolithic integrated 8 × 8 space- and wavelength-selective cross-connect is shown in Fig. 1(a). It consists of a combination of broadband port select and wavelength or color select stages. Eight colorless input ports connect to an array of eight pre-amplifying semiconductor optical amplifiers (SOAs). A broadcast shuffle network maps each of the inputs to all eight output ports. A first stage of 64 broadband SOA gates is used for input port select. The broadband port-select SOAs then connect to eight independent cyclic arrayed waveguide gratings (AWGs). The AWGs route the different wavelength channels to the second stage array of broadband SOAs to perform wavelength selection. The selected channels are aggregated with a broadband fan-in comprising three multimode interference 2 × 1 couplers to provide the eight colorless outputs. The grey layers in Fig. 1(a) show the seven additional identical planes implemented in the integrated circuit. Further switching planes may also be implemented to optimize the blocking probability [11].

Tables 1 and 2 show the correspondence between SOA gate labeling scheme in Fig. 1(a), the optical port connections and wavelength mapping. Groups of eight broadband port select SOAs route the different inputs to each output as shown in Table 1. A group of wavelength select SOAs selects from the eight incoming wavelengths from each input in Table 2, routing them to output O0, which is the assessed output in this work. The paths used in this study are highlighted in both Tables with a bold typeface: The four broadband port select SOAs and eight wavelength select SOAs which route the inputs to output O0. The cross-connect supports all wavelengths on the grid of the cyclic router. The precise grid is defined by the AWG router channel spacing \( \Delta \lambda_{spaces} \) which is designed to be 3.2 nm (400 GHz) and by the number of unique wavelength paths which is defined by the free spectral range of the cyclic router at \( 8 \times \Delta \lambda_{spaces} \). The use of a cyclic router additionally allows waveband routing and therefore more than eight wavelengths to be routed. The upper and lower limits for the wavelengths are constrained only by the multi-Terahertz bandwidth of the SOA gates.

Table 1. Broadband Port Select SOA Connections

<table>
<thead>
<tr>
<th>Input</th>
<th>Output</th>
<th>O0</th>
<th>O1</th>
<th>O2</th>
<th>O3</th>
<th>O4</th>
<th>O5</th>
<th>O6</th>
<th>O7</th>
</tr>
</thead>
<tbody>
<tr>
<td>I0</td>
<td>B[0,0]</td>
<td>B[0.1]</td>
<td>B[0.2]</td>
<td>B[0.3]</td>
<td>B[0.4]</td>
<td>B[0.5]</td>
<td>B[0.6]</td>
<td>B[0.7]</td>
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</tbody>
</table>

Gate B[0,0] is used in the WDM routing experiments in section 5. Gates B[0,0], B[1,0], B[5,0] and B[6,0] are used in the dynamic routing experiments in section 6.

The circuit is fabricated on a re-grown active-passive epitaxial wafer. The active regions are used for SOA gates and preamplifiers and include four InGaAsP/InP quantum wells which are optimised for TE polarization. The passive regions for the waveguide wiring, splitters and cyclic routers use the same 500 nm-thick confining hetero-structure but do not include the quantum wells. Both active and passive confinement layers are sandwiched between InP cladding layers. The SOA elements are 1mm long and 2 µm wide. Deep-etched, high side-wall verticality, 1.5 µm-wide waveguides are used for the low-radius curved-waveguides, the power splitters and the curved waveguides within the arrayed waveguide gratings. Deep-etched multi-mode-interference devices are used for power splitters and combiners. Shallow-etched, low-loss, 2 µm-wide ridge-waveguides are used for most of the circuit layout to minimize losses. SOA gates and shuffle network waveguide crossings are also implemented as shallow waveguides.
A programmable gate array (FPGA) provides time-slotted control signals to the nano-second-current level adjustment and schedule selection for the integrated cross-connect. The 10GHz bit clock in the pattern generator generates a 50 MHz common reference to synchronise the 200 MHz FPGA clock and the clock generator between the FPGA and the bit error rate (BER) test equipment. This is achieved between the routed data and the switch controller by means of a common reference within the FPGA. The FPGA also generates synchronised trigger signals for test equipment.

A Stanford delay generator is used for signal conditioning prior to connection to test equipment such as the oscilloscope for time trace visualization. Bit-level synchronization is achieved between the routed data and the switch controller by means of a common reference signal is amplified and then filtered for broadband noise rejection at a pre-amplified DC level. The data plane below. The grey blocks and the chip define the optical plane. A multiplex of four waveguide crossings. The SOAs appear in five columns. The left-most column shows the preamplifiers, the central pair of SOA columns performs broadband port-select and the right-most pair of SOA columns perform the wavelength-select. The array of cyclic routers are placed between the two SOA select stages. The input waveguides are perpendicular to the facet and are separated by a 250 µm pitch on the input side to allow input port access with a fiber lens array. The chip is 14.6 mm long between the uncoated facets and 6.7 mm wide. The chip is attached with conductive epoxy to a water-cooled heatsink, and 136 p-side electrodes are wire-bonded to neighboring printed circuit boards.

### 4. Test-bed

An experimental test-bed is implemented to demonstrate multi-path WDM data routing. This is schematically shown in Fig. 2 and showing an electrical control plane above and an optical data plane below. The grey blocks and the chip define the optical plane. A multiplex of four wavelengths with a nominal channel separation of 3.2nm (400GHz) is modulated with the same 10 Gb/s on-off keyed modulator. The signals are amplified with a fiber amplifier and de-correlated with a 10km length of standard dispersion fiber. The wavelength multiplexed data are launched with polarization control at the input side of the circuit. Four to sixteen wavelengths with a nominal channel separation of 3.2nm is modulated with the same 10 Gb/s on-off keyed modulator. The signals are amplified with a fiber amplifier and de-correlated with a 10km length of standard dispersion fiber. The wavelength multiplexed data are launched with polarization control at the input side of the circuit. Four to sixteen channels are routed within the 8 × 8 integrated circuit to output port O0. The WDM data signal is amplified and then filtered for broadband noise rejection at a pre-amplified DC coupled lightwave converter. Time traces are also analysed on an oscilloscope.

The electrical plane comprises fast current drivers and programmable logic. A multiple current source provides DC currents to the pre-amplifying SOAs. Fast current drivers connect to the SOA selector gates of the integrated cross-connect to enable path and channel selection. The current levels for each of the SOA selector gates is separately programmed by means of digital-to-analog converters (DACs) and a central microcontroller. An Altera Stratix III field programmable gate array (FPGA) provides time-slotted control signals to the nano-second-rise-time current drivers for optical path selection. A round robin schedule is implemented within the FPGA. The FPGA also generates synchronised trigger signals for test equipment. A Stanford delay generator is used for signal conditioning prior to connection to test equipment such as the oscilloscope for time trace visualization. Bit-level synchronization is achieved between the routed data and the switch controller by means of a common reference clock generator between the FPGA and the bit error rate (BER) test equipment. This generates a 50 MHz common reference to synchronise the 200 MHz FPGA clock and the 10GHz bit clock in the pattern generator. The PC shown at the top right of Fig. 2 is used for current level adjustment and schedule selection for the integrated cross-connect.

### Table 2. Wavelength Mapping to Output O0

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<tbody>
<tr>
<td>B[0,0]</td>
<td>λ5</td>
<td>λ6</td>
<td>λ7</td>
<td>λ2</td>
<td>λ3</td>
<td>λ4</td>
<td>λ5</td>
<td>λ6</td>
</tr>
<tr>
<td>B[1,0]</td>
<td>λ2</td>
<td>λ3</td>
<td>λ4</td>
<td>λ5</td>
<td>λ6</td>
<td>λ7</td>
<td>λ8</td>
<td>λ9</td>
</tr>
<tr>
<td>B[2,0]</td>
<td>λ3</td>
<td>λ4</td>
<td>λ5</td>
<td>λ6</td>
<td>λ7</td>
<td>λ8</td>
<td>λ9</td>
<td>λ10</td>
</tr>
<tr>
<td>B[3,0]</td>
<td>λ4</td>
<td>λ5</td>
<td>λ6</td>
<td>λ7</td>
<td>λ8</td>
<td>λ9</td>
<td>λ10</td>
<td>λ11</td>
</tr>
<tr>
<td>B[4,0]</td>
<td>λ5</td>
<td>λ6</td>
<td>λ7</td>
<td>λ8</td>
<td>λ9</td>
<td>λ10</td>
<td>λ11</td>
<td>λ12</td>
</tr>
<tr>
<td>B[5,0]</td>
<td>λ6</td>
<td>λ7</td>
<td>λ8</td>
<td>λ9</td>
<td>λ10</td>
<td>λ11</td>
<td>λ12</td>
<td>λ13</td>
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<tr>
<td>B[6,0]</td>
<td>λ7</td>
<td>λ8</td>
<td>λ9</td>
<td>λ10</td>
<td>λ11</td>
<td>λ12</td>
<td>λ13</td>
<td>λ14</td>
</tr>
<tr>
<td>B[7,0]</td>
<td>λ8</td>
<td>λ9</td>
<td>λ10</td>
<td>λ11</td>
<td>λ12</td>
<td>λ13</td>
<td>λ14</td>
<td>λ15</td>
</tr>
</tbody>
</table>

k represents a band of wavelengths for the cyclic router. For the free spectral range studied in this work \( \lambda_6 \) corresponds to 1543.1 nm and \( \lambda_7 \) corresponds to 1568.1 nm. Wavelength channels are separated by 3.2nm.

Gates W[0,0], W[1,0], W[2,0] and W[3,0] are used in the WDM routing experiments in section 5.

Gates W[0,0], W[1,0], W[2,0], W[3,0], W[4,0], W[5,0], W[6,0] and W[7,0] are used in the dynamic routing experiments in section 6.
5. WDM routing

A multiplex of four wavelengths is implemented with center wavelengths $\lambda_0 = 1543.1$ nm, $\lambda_1 = 1546.3$ nm, $\lambda_2 = 1549.8$ nm and $\lambda_3 = 1552.7$ nm. The third channel is shifted 0.3 nm to longer wavelength as the preferred multiplexed channel was unavailable at the WDM source. The wavelength multiplexed data is launched into port I0 for the WDM routing experiments.

The WDM routing assessment is performed for path I0 → O0. The injected current to the on-state first-stage broadband port-select SOA B[0,0] is 60mA, while currents injected at the second wavelength-select SOA stage are independently optimized to 40mA, 45mA, 55mA and 47mA. Figure 3 shows the spectra recorded for all four output wavelengths at output O0. Four channels are input at I0 and one is selected at O0 for each measurement for the corresponding wavelength-select SOA W[0,0], W[1,0], W[2,0] and W[3,0]. The upper dashed grey line is the WDM signal input at port I0. The difference in peak power between the input and the output signals for the selected wavelengths in Fig. 3 shows a fiber-to-fiber loss of 26.4 dB to 27.2 dB. Component level analysis predicts an on-chip loss of 33.6 dB for this path and fiber-chip coupling losses of 13.5 dB [10]. This suggests that each SOA is operated with a gain of 7 dB. Higher gain should be feasible if anti-reflection coatings are applied to the facets. In-fiber optical signal to noise ratio (OSNR) is recorded in the range from 27.0 dB to 31.1 dB/0.1nm for the channels shown in Fig. 3. A crosstalk level below $-19$ dB is found for the three aligned wavelength channels. The amplified spontaneous emission attending the four channels in Fig. 3 indicates a 3dB pass-bandwidth of 170 GHz to 200 GHz for the cyclic router.

Data integrity for multiple simultaneously routed wavelengths is further evaluated by bit error rate measurement. The output signal is filtered and sent to the pre-amplified receiver. Figure 4 shows the measured bit error rates as a function of input power. Moderate power penalties are shown in the range from 3.6 to 4.0 dB for three of the four filtered output wavelength data signals for a 10 Gb/s $2^{31}-1$ pseudo random sequence. Power penalty is expected to be dominated by amplified spontaneous emission from the transmitter side amplifier and the cross-connect. The third channel remains compromised by the pass-band misalignment imposed at the WDM source multiplexer.
Fig. 3. Spectra for 10Gb/s WDM at the input I0 (dashed) and at the output O0 (solid).

Fig. 4. BER measurements for 10Gb/s WDM data from input I0 to output O0.

6. Dynamic multi-path WDM routing

The wavelength multiplexed data is split into four copies using broadband splitters and these data streams are launched into four input ports: I0, I1, I5 and I6 for dynamic multi-path WDM reconfigurability studies. The input pre-amplifier current values are now in the range 29 mA to 43 mA. The port-select currents are within the range 61 to 80 mA for the on-state. The second-stage wavelength-select SOAs are enabled with fixed, path-specific current levels which range from 29 mA to 41 mA. The current values are chosen to best equalize the power at the output. The first-stage broadband port-select SOAs B[0,0], B[1,0], B[5,0] and B[6,0] are enabled sequentially with a four time-slot round-robin schedule. These SOAs are cyclically driven by periodic 0.940 μs pulses with 60 ns guard-bands which are also
programmed via the FPGA. The SOAs select the data signals coming from the corresponding input ports I0, I1, I5 and I6 to output O0.

![Round Robin Scheduling](image)

**Fig. 5.** (a) Control signal for the cyclically enables B-SOAs for input port selection. (b) Time traces for all the wavelength of the 4 WDM input signals and (c) corresponding falling and rising time for λ1 at time slot 5→0.

Figure 5(a) shows the control signals between the FPGA and the current drivers for the broadband port select SOAs. Each wavelength is sequentially routed through different paths from input I0, I1, I5 and I6 to output O0 from time slot to time slot and time traces are recorded. The four sets of wavelengths are isolated using external optical filtering and are displayed as four separate graphs in Fig. 5(b). The time traces appear to be clean and well resolved. The optical power is levelled for each wavelength to within 2 dB, as the current values have been optimised for equalized output power from time-slot to time-slot. There are difference in mean output wavelength power levels. The most pronounced drop in amplitude is for the case of λ2, which is attributable to the off-chip WDM multiplexer.
Figure 5(c) shows detail for the falling and rising time for the output signal taken for λ1 when moving from one time slot to the next one: The rise and fall times are recorded to be 3.8 and 2.8 ns, respectively. The response time is slower than the specified driver performance of 1.0 ns, indicating some parasitic bandwidth limitations between the driver and photonic circuit.

7. Discussion

The ultimate performance for the space and wavelength select cross-connect is determined by crosstalk, losses and path bandwidth. The −19 dB crosstalk level observed in Fig. 3 is primarily due to imperfect wavelength channel discrimination in the cyclic routers. Higher precision lithography tools are therefore expected to improve crosstalk performance further [12] and also to enable lower-loss designs [13]. The high fiber-chip coupling losses, with a total value of −13.5 dB, may be reduced to less than −2 dB with integrated spot-size converters [14] and anti-reflection coatings. The losses inherent to the broadcast and select architecture, namely 18 dB from the six 3 dB splitter/combiners, are compensated by the on-chip gain in the current circuit. Much of the remaining loss may be removed through component optimisation and a maturing fabrication technology.

The scaling properties for the cross-connect are defined by the broadcast and select architecture. Optical loss and electrical power are both expected to scale as log₂N for N input connections. For every doubling in connectivity, more than 6 dB of extra loss is introduced, requiring an additional stage of amplification. The amplifiers in this work operate with typical currents and voltages of 50 mA and 1.25 V respectively, leading to a maximally stressed chip power consumption of 8.5 W in the unlikely situation where all 136 SOAs are in the on-state. End-to-end line-rates may be scaled further to fully exploit the pass-bandwidth of the cyclic routers. Differential phase shift keyed data modulation may also be feasible, with evidence for wide optical dynamic range operation for short-range SOA-based systems [15].

8. Conclusions

A WDM multi-path routing test-bed is implemented and is used to demonstrate a monolithically integrated 8 × 8 cross-connect for the first time. Four inputs are loaded with four wavelength multiplexed signals. Sixteen channels are routed to the same output port by means of a programmable controller. The ease of control and connectivity of the demonstrated circuit offers considerable promise for further capacity scaling in packet-compliant photonic optical switching.