Flexible multilevel converters using four-switch extended commutation cells

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Flexible Multilevel Converters using 4-Switch Extended Commutation Cells

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Abstract—The extended commutation cell is a 4-port, 4-switch cell that allows for bidirectional energy transport in two orthogonal directions throughout the cell. By cascading multiple cells a multilevel converter can be constructed with a high number of cells. The voltage across each cell capacitor can be adjusted independently of the load, resulting in high flexibility in output levels. In this paper the general theoretical analysis for this cell, including the necessary design tools is detailed. Experimental results of a 2-cell 8-level dc-ac converter are given. The outcomes in good agreement with the analysis and simulation results.

Index Terms—Buck-boost, ECC, multicell, multilevel, switched capacitor.

I. INTRODUCTION

With the rapid development of electronics one can find electric power converters, such as dc-dc and ac-dc converters almost everywhere. In the search for an increasing power density, the switching frequency is being raised [1] and multilevel converters are being used, reducing the size of passive filtering components.

The filtering components use a great portion of the volume of a power converter. To further reduce the size much effort is made in the development of (new) multilevel and multicell converter topologies [2]–[5], and modular converter structures [6]–[9]. By using a higher number of levels, opposed to only two, the ripple, and consequently the volume of filtering components is reduced. Most popular examples of such multilevel/multicell converters are the flying capacitor converter, neutral-point clamped converter, cascaded cell multilevel converter and modular multilevel converter [10]–[12]. However, current multilevel topologies have poor (linear) scaling of the levels, and adding cells in parallel enables single-fault safe operation. This new commutation cell, designated as the extended commutation cell (ECC), leads to power converter topologies such as high-ratio converters and multilevel converters. The switching cell is modular and can be cascaded, adding a factor of two more levels with each cell. Within the converter, the voltage rating of all switches is only determined by the capacitor voltages of the neighboring cells. The voltage across each cell capacitor is controlled independently of the load and can be adjusted in real-time, directly changing the output levels. The basic cell introduced in this paper can isolate a switch fault without additional switches. Therefore fault tolerance can be implemented by simply placing cells in parallel.

In this paper an innovative commutation cell is introduced, shown in Fig. 1, that allows for more flexibility. Adding multiple cells in series results in a rapid increase in the number of levels, and adding cells in parallel enables single-fault safe operation. This new commutation cell, designated as the extended commutation cell (ECC), leads to power converter topologies such as high-ratio converters and multilevel converters. The switching cell is modular and can be cascaded, adding a factor of two more levels with each cell. Within the converter, the voltage rating of all switches is only determined by the capacitor voltages of the neighboring cells. The voltage across each cell capacitor is controlled independently of the load and can be adjusted in real-time, directly changing the output levels. The basic cell can be considered as an extension of the flying inductor converter in [19], which was developed only for buck-boost operation.

This paper provides an introduction of the ECC and the necessary tools to design and analyze a multilevel converter using this cell. In the next section the basic ECC is introduced and explained. In section III converter examples, constructed with the basic ECC, are illustrated. Next, in section IV a general N-level converter is elaborated in more detail, followed by an analysis of the component stress in section V. Experimental results for a specific converter are shown in section VI and

Fig. 1. Basic circuit diagram of the extended commutation cell. Connection terminals are indicated with a, b, c and d.

Adding another six switches and drivers, and replacing each switch with two parallel branches of two series switches [18]. This high cost for single-fault safe operation, also applies to the known multilevel converters such as the flying capacitor and neutral-point clamped converter, making it generally not interesting to implement except for special applications, such as aerospace ones. The basic cell introduced in this paper can isolate a switch fault without additional switches. Therefore fault tolerance can be implemented by simply placing cells in parallel.
Fig. 2. Circuit diagram of a single extended commutation cell constructed with MOSFET switches.

Fig. 3. ECC direct input-to-output operation. (a) Direct connection between \( S_{4\eta-3} \) and \( S_{4\eta-1} \). (b) Direct connection between \( S_{4\eta-2} \) and \( S_{4\eta} \).

section VII, and finally, conclusions are drawn in section VIII.

II. EXTENDED COMMUTATION CELL

The extended commutation cell is a 4-port, 4-switch cell that allows for energy transfer in two orthogonal directions throughout the cell. Due to this property, a whole new group of power converters can be constructed, enabling versatile, reliable and efficient power conversion.

The basic ECC is shown in Fig. 1 where the connection terminals are indicated with letters \( a, b, c \) and \( d \). This cell is a 4-switch voltage-to-voltage converter where terminals \( a \) and \( b \) are supposed to operate as a first pair, and, terminals \( c \) and \( d \) as the second one. An example of the ECC assembled with MOSFET switches is presented in Fig. 2.

Operation of the ECC consists of two isolated modes. The first mode is the input-to-output direct connection, using switches \( S_{4\eta-3} \) and \( S_{4\eta-1} \) turned on simultaneously, as illustrated in Fig. 3 (a), or with switches \( S_{4\eta-2} \) and \( S_{4\eta} \) turned on as given in Fig. 3 (b). With the first pair of switches, terminal \( a \) is connected to \( c \), and with the second pair, terminal \( b \) is connected to \( d \).

The second mode is the buck-boost operation. As shown in Fig. 4 energy can be transferred between a voltage source, connected to terminals \( a \) and \( b \), and the capacitor \( C_\eta \) in two stages. In the case of energy flow from the input voltage source to the capacitor, the inductor is charged from the input in Fig. 4 (a) and discharged to the capacitor in Fig. 4 (b). Assuming continuous conduction mode (CCM) for the buck-boost operation, the capacitor voltage is given by

\[
U_{C_\eta} = U_{ab} \cdot \frac{D_{\eta}^+}{1 - D_{\eta}^-}
\]

where \( D_{\eta}^+ \) is the buck-boost duty ratio for switches \( S_{4\eta-3} \) and \( S_{4\eta-1} \) and \( S_{4\eta-2} \) and \( S_{4\eta} \) being complementary. \( \eta \) is used as a general identifier of an ECC. The peak voltage across all switches in the switching cell is \( U_{C_\eta} + U_{ab} \).

Operation of the ECC, with both input-to-output direct connection and buck-boost operation combined, is shown in Fig. 5. Clearly, with ideal components, the input-to-output direct connection and the buck-boost operation do not influence each other.

III. CONVERTER EXAMPLES

Using the extended commutation cell, a number of novel converter topologies can be constructed. In the subsections below a few examples are given.

A. 4-Level converter

The most elementary multilevel converter that can be constructed on the basis of the ECC is a 4-level converter. This
The circuit diagram of the 4-level converter is shown in Fig. 6. The output states of the 4-level converter under input-to-output operation mode are shown in Fig. 7. The corresponding output levels are given in Table I. In Fig. 7 the buck-boost operation is not drawn for the sake of clarity.

In steady state the voltage across the capacitor \( C_1 \) is defined by (1) with \( \eta = 1 \) and \( U_{ab} = U_{DC} \).

### B. N-Level converter

In the previous section an ECC is used in a 4-level converter, consisting of a single extended commutation cell followed by a half-bridge. By using the series connection of multiple ECCs, the number of levels is exponentially related to the number of switches. As an example, a 2-ECC converter with 8 output levels is shown in Fig. 8. In section IV the N-Level converter is presented in more detail.

### C. Fault-tolerant converter

Using the ECC, multiple cells can be placed in series also also in parallel. With the parallel modules, the converter becomes tolerant to a single fault occurring in any of the cells, as long as a parallel path exists. A converter structure with series and parallel cells, is shown in Fig. 9 in a \( 3 \times 4 \) configuration. This converter has 3 cells in parallel \( (\rho = 3) \) and 4 cells in series \( (\sigma = 4) \), resulting in a 32-level converter.

In this example, multiple switches may fail before the converter is unable to keep supplying the load. In two of three adjacent parallel ECCs a random switch may fail. In adjacent series cells, a switch may fail in each cell without fully disabling the converter. In the half-bridge (HB) cells, at
the end of each row, multiple open-switch failures are allowed but only a single failure to short. A single failure to short-circuit in one of the half bridge cells reduces the number of output levels by a factor of 2.

Besides the advantages of redundancy, the fault-tolerant converter also provides a mean to reduce the current stress in the cell capacitors. By performing interleaved buck-boost operation in each of the parallel cells, the current ripple in the capacitors could be significantly reduced.

IV. N-LEVEL CONVERTER

In the N-level converter, each additional cell in the converter multiplies the number of available output voltage levels by 2. Therefore, the number of levels as a function of the number of ECCs is given by

\[ N = 2^{\sigma + 1} \] (2)

where \( \sigma \) is the number of cells cascaded in series and \( N \) is the number of levels. For a given number of cells the required number of switches, denoted by \( n_S \), is given by

\[ n_S = 4\sigma + 2 \] (3)

Combining (3) and (2), after some manipulations gives the number of switches, \( n_S \), required for a number of levels, \( N \), as

\[ n_S = 2 \frac{2 \ln(N) - \ln(2)}{\ln(2)} \] (4)

For comparison, \( n_S \) for a flying capacitor converter [11], [13] is given by

\[ n_S = 2(N - 1) \] (5)

which is also valid for the neutral-point clamped and cascaded cell multilevel converter.

The resulting number of switches for both the ECC and flying capacitor converter for an arbitrary number of levels, is shown in Fig. 10. Note that for visualization a continuous line is plotted in spite of the fact that (4) and (5) only hold for specific values of \( N \). At 2 or 4 levels the number of switches for the flying capacitor and ECC multilevel converter are equal. For higher numbers of levels the number of switches in the flying capacitor converter strongly increases.

It should be emphasized that each of the ECCs in an \( N \)-level converter has decoupled buck-boost and direct input-to-output operation modes. Therefore, the buck-boost operation is independent. If it is required each of the cells could be operated at a different switching frequency or phase.

A. Output levels

The output levels that can be achieved with the 8-level converter from Fig. 8 are listed in Table II. Depending on the capacitor voltages \( U_C_1 \) and \( U_C_2 \), a set of output voltage levels is defined, indexed with

\[ \ell \in \{N/2, \ldots, 1, -1, \ldots, -N/2\} \] (6)

In case a 0-level is required \( (u_{out} = 0\text{V}) \), two switch states will result in a 0V output and a maximum of 7 unique active
The capacitor voltage for capacitor voltages and

Using this fact, a general expression can be derived for the observed in the numerator of the capacitor voltage fractions.

and step size between adjacent levels is also given.

The set of levels for a 4-level converter can be deducted from Table II by removing output levels will remain. The set of levels for a 4-level converter can be deduced from Table II by removing $u_{C_2}$ and filtering away the resulting double outcomes. For converters with a higher number of levels, the pattern from Table II repeats.

An example of a capacitor voltage choice, for the 1, 2, 3, 4 and 5-cell converter, is shown in Table III. The capacitor voltages are chosen such that an even number of equidistant output levels is obtained. The resulting output voltage range and step size between adjacent levels is also given.

In Table III, the Jacobsthal integer sequence [20] can be observed in the numerator of the capacitor voltage fractions. Using this fact, a general expression can be derived for the capacitor voltage and $\Delta u_{out}$ (the output voltage step size). The capacitor voltage for $C_\eta$ is represented by

$$U_{C_\eta}(\sigma) = \frac{(\sigma)^{\eta} + 2^{\sigma+1-\eta}}{(-1)^\eta + 2^{\sigma+1}} \quad (7)$$

The resulting level step size is calculated with

$$\frac{\Delta u_{out}(\sigma)}{U_{DC}} = \frac{3}{(-1)^\eta + 2^{\sigma+1}} \quad (8)$$

The corresponding peak output voltage is given by

$$\frac{\hat{u}_{out}(\sigma)}{U_{DC}} = \frac{3}{2} \cdot 2^{\sigma+1} - 1 \quad (9)$$

which converges to $\frac{3}{2}$ as $\sigma \to \infty$.

B. Gating signals

In this section the relation between the different gating signals and the output levels is elaborated. First a direct input-to-output gating signal $g_\eta^-$ is defined as

$$g_\eta^- = \begin{cases} 0 & \text{then } S_{4\eta-2} \text{ and } S_{4\eta} \text{ on} \\ 1 & \text{then } S_{4\eta-3} \text{ and } S_{4\eta-1} \text{ on} \end{cases} \quad (10)$$

for $\eta = 1 \ldots \sigma$, and the output gating signal of the half-bridge is defined as

$$g_{\eta+1}^- = \begin{cases} 0 & \text{then } S_{4\eta+2} \text{ on} \\ 1 & \text{then } S_{4\eta+1} \text{ on} \end{cases} \quad (11)$$

In Table IV the gating signals are given for each of the levels of an 8-level converter. The set of columns containing the gating signals form a $3 \times 8$ matrix. This matrix is referred to as the gating matrix and is indicated with $Q$. The 3 rightmost columns indicate the contribution of $\frac{1}{2}U_{DC}$ and $u_{C_0}$ to the output voltage. This $3 \times 8$ matrix summarizes the relation between the gating signals and the output levels. This matrix is referred later as level matrix and is indicated with $P$ (see (14) further on).

Similar to $g_\eta^-$ a gating signal can be defined for the buck-boost operation mode. This gating signal $g_\eta^+$ is defined as

$$g_\eta^+ = \begin{cases} 0 & \text{then } S_{4\eta-1} \text{ and } S_{4\eta} \text{ on} \\ 1 & \text{then } S_{4\eta-3} \text{ and } S_{4\eta-2} \text{ on} \end{cases} \quad (12)$$

The gating of the switches in each cell is eventually controlled by both $g_\eta^-$ and $g_\eta^+$. The gating vector per cell $g_\eta$ is defined as

$$g_\eta = \begin{bmatrix} g_{4\eta-3}^- \quad g_{4\eta-2}^- \quad g_{4\eta-1}^- \quad g_{4\eta}^- \\ g_{4\eta}^+ \quad g_{4\eta-1}^+ \quad g_{4\eta-2}^+ \quad g_{4\eta-3}^+ \end{bmatrix} = \begin{bmatrix} g_{4\eta}^- \quad 1 \quad g_{4\eta}^+ \quad 1 \\ g_{4\eta}^+ \quad 1 \quad g_{4\eta}^- \quad 0 \\ g_{4\eta}^- \quad 0 \quad g_{4\eta}^+ \quad 1 \\ g_{4\eta}^+ \quad 0 \quad g_{4\eta}^- \quad 0 \end{bmatrix} \quad (13)$$

![Fig. 10. Required number of switches $n_S$ versus number of levels $N$ for an ECC based converter and flying capacitor converter.](image)
where the corresponding switch is “on” if the indicated condition is true. For the half-bridge switches the state is solely defined by $g_{\sigma+1}$.

C. General expression for levels

In this section, a general expression is derived to obtain the values for the capacitor voltage for a specific set of desired output voltages. First, a vector $\bar{y}_{\text{out}}$, containing the levels of an $\sigma$-cell converter, is described. This vector is defined as

$$\bar{y}_{\text{out}} = PU_C$$

with $\bar{y}_{\text{out}}$ being the level vector containing the output voltage per level, obtained as

$$\bar{y}_{\text{out}} = \begin{bmatrix} y_{\text{out},-N/2} & \cdots & y_{\text{out},1} & y_{\text{out},-1} & \cdots & y_{\text{out},-N/2} \end{bmatrix}^T$$

of length $N$, and $U_C$ being the capacitor voltage vector introduced as

$$U_C = \begin{bmatrix} 1/2U_{\text{DC}} & U_{C_1} & U_{C_2} & \cdots & U_{C_\sigma} \end{bmatrix}^T$$

of length $\sigma + 1$. The structure of $P$ is given in Table IV.

The target is to find a solution for $U_C$ for an arbitrary set of values for $\bar{y}_{\text{out}}$. Therefore, (14) is rewritten as

$$PU_C - I_{\text{out}} = 0$$

where $I$ is the identity matrix. This equation is then transformed into

$$\begin{bmatrix} P & I \end{bmatrix} \begin{bmatrix} U_C \\ -\bar{y}_{\text{out}} \end{bmatrix} = 0$$

Performing the reduced row echelon form operation, indicated with $\text{rref}$, a matrix is obtained as

$$\text{rref} \begin{bmatrix} P & I \end{bmatrix} = \begin{bmatrix} I & W \\ 0 & C \end{bmatrix}$$

and thus

$$\begin{bmatrix} I & W \\ 0 & C \end{bmatrix} \begin{bmatrix} U_C \\ -\bar{y}_{\text{out}} \end{bmatrix} = 0$$

with $I$ being an identity matrix of size $\sigma + 1$, $0$ the zero matrix, $W$ describing the solutions for capacitor voltages and $C$ providing additional constraints for $\bar{y}_{\text{out}}$. Rewriting (20) gives the set of equations to solve $U_C$ as a function of a specified $\bar{y}_{\text{out}}$ as

$$U_C = W\bar{y}_{\text{out}}$$

$$0 = C\bar{y}_{\text{out}}$$

V. COMPONENT STRESS

In this section, an analytical method is given to determine the current and voltage stress in the components of a converter constructed with extended commutation cells.
and
\[
\langle i_{\text{in},n}^+ \rangle = \langle i_{s_{n-3}} - i_{s_{n-2}} \rangle
\]
(26)
for the direct cell input current. The buck-boost input current is given by
\[
\langle i_{\text{out},n}^+ \rangle = -\frac{1}{2} \left[ \langle i_{s_{n-1}} + i_{s_{n}} \rangle - I_{\text{out}} \left( 2g_{n}^- - 1 \right) \right]
\]
(27)
and the cell direct output current by
\[
\langle i_{\text{out},n}^- \rangle = \langle i_{s_{n-1}} - i_{s_{n}} \rangle
\]
(28)
where, by definition,
\[
i_{\text{in},n}^+ = i_{\text{out},n}^- = i_{\text{out},n}
\]
(29)

D. Average inductor current

To estimate the average value of the inductor current in each cell, first, the buck-boost input current of each cell is calculated. The average buck-boost input current, for an ideal lossless system, can be expressed in terms of the output current by
\[
\langle i_{\text{in},n}^- \rangle = \frac{\langle i_{\text{out},n}^+ \rangle \ D_{n}^+}{1 - D_{n}^+}
\]
(30)
The average input current value of the last cell is given by
\[
\langle i_{\text{in},N}^+ \rangle = k_{\sigma} P_{\ell,\sigma + 1}
\]
(31)
for the other cells in the converter the average input current is given by
\[
\langle i_{\text{in},n}^+ (\ell) \rangle = k_{n} \left( \langle i_{\text{in},n+1}^+ (\ell) \rangle + P_{\ell,\eta + 1} \right)
\]
(32)
where \(k_{n}\) is the cell-to-cell voltage gain defined by
\[
k_{n} = \frac{D_{n}^+}{1 - D_{n}^+}
\]
(33)
Rewriting (31) and (32) into a matrix form gives
\[
\langle i_{\text{in},n}^+ \rangle = P \left[ 0 \ 1 \right]^T A I_{\text{out}}
\]
(34)
with \(A\) being an ancillary matrix describing the inter-cell buck-boost gain as
\[
A_{p,q} = \prod_{n=q}^{p} k_{n} \quad \text{if } p \geq q \quad \text{else } A_{p,q} = 0
\]
(35)
The resulting ancillary matrix has the following structure
\[
A = \begin{bmatrix}
    k_1 & 0 & 0 & \ldots & 0 \\
    k_1 k_2 & k_2 & 0 & \ldots & 0 \\
    k_1 k_2 k_3 & k_2 k_3 & k_3 & \ldots & 0 \\
    \vdots & \vdots & \vdots & \ddots & \vdots \\
    k_1 k_2 \ldots k_\sigma & k_2 \ldots k_\sigma & k_3 \ldots k_\sigma & \ldots & k_\sigma
\end{bmatrix}
\]
(36)

The obtained matrix \(\langle i_{\text{in},n}^- \rangle\) from (34) contains the average buck-boost input current value of each of the cells for each level as
\[
\langle i_{\text{in},1}^- (N/2) \rangle \ldots \langle i_{\text{in},\sigma}^- (N/2) \rangle \\
\vdots \quad \quad \vdots \\
\langle i_{\text{in},1}^- (1) \rangle \ldots \langle i_{\text{in},\sigma}^- (1) \rangle \\
\langle i_{\text{in},1}^- (-1) \rangle \ldots \langle i_{\text{in},\sigma}^- (-1) \rangle \\
\vdots \quad \quad \vdots \\
\langle i_{\text{in},1}^- (-N/2) \rangle \ldots \langle i_{\text{in},\sigma}^- (-N/2) \rangle
\]
(37)

Using \(I_{\text{in}}^+\), the average inductor current value is calculated in matrix form. Using only the buck-boost currents, the cell can be treated as a standard buck-boost converter. Therefore, for a single cell the average inductor current is given by
\[
\langle i_{L_{\text{in}}} \rangle = \langle i_{\text{in},n}^- \rangle + \langle i_{\text{out},n}^+ \rangle
\]
(38)
since
\[
\langle i_{\text{in},n}^- \rangle = k_{n} \langle i_{\text{out},n}^+ \rangle
\]
(39)
it follows that
\[
\langle i_{L_{\text{in}}} \rangle = \langle i_{\text{in},n}^- \rangle / (1 + k_{n}^-)
\]
(40)
Converting this into matrix form gives
\[
\langle i_{L_{\text{in}}} \rangle = \langle i_{\text{in},n}^- \rangle \left[ I + K^{-1} \right]
\]
(41)
where \(K\) is a square matrix with the buck-boost gains on the diagonal as
\[
K = \begin{bmatrix}
k_1 & 0 & \ldots & 0 \\
0 & k_2 & \ldots & 0 \\
\vdots & \vdots & \ddots & \vdots \\
0 & 0 & \ldots & k_\sigma
\end{bmatrix}
\]
(42)
and \(\langle i_{L_{\text{in}}} \rangle\) is a matrix containing the average inductor current value for all cells and levels.

The worst case average current through the inductor, with a constant output current, occurs at levels \(N/2\) and \(-N/2\). Then, each of the buck-boost converters is supplying power to the load and following cells.

E. Average switch current

With the inductor current and level matrix, the current in each of the switches can be calculated for each cell and level. First, a matrix is introduced containing the buck-boost duty ratios, given by
\[
D^\perp = \begin{bmatrix}
    D^\perp_1 & 0 & \ldots & 0 \\
    0 & D^\perp_2 & \ldots & 0 \\
    \vdots & \vdots & \ddots & \vdots \\
    0 & 0 & \ldots & D^\perp_\sigma
\end{bmatrix}
\]
(43)
The average switch current value, considering the output constant current, is calculated with
\[
\langle i_{s_{n-3}} \rangle = \langle i_{L_{\text{in}}} \rangle D^\perp + Q \left[ I \ 0 \right]^T I_{\text{out}}
\]
(44)
and for $S_{4\eta-2}$

$$I_{S_{4\eta-2}} = \sqrt{(1 - D_{\eta}^+)} \left(1 - g_{\eta}^\perp\right) I_{out}^2 +$$

$$D_{\eta}^+ \left[I_x^2 + 2I_x \Delta i_{L\eta} + \frac{4}{3} \Delta i_{L\eta}^2\right]$$

(49)

with

$$I_x = -\left(1 - g_{\eta}^\perp\right) I_{out} + \langle i_{L\eta}\rangle - \Delta i_{L\eta}$$

similar for $S_{4\eta-1}$

$$I_{S_{4\eta-1}} = \sqrt{(1 - D_{\eta}^+)} \left(1 - g_{\eta}^\perp\right) I_{out}^2 +$$

$$\left(1 - D_{\eta}^+\right) \left[I_x^2 - 2I_x \Delta i_{L\eta} + \frac{4}{3} \Delta i_{L\eta}^2\right]$$

(50)

with

$$I_x = -\left(1 - g_{\eta}^\perp\right) I_{out} - \langle i_{L\eta}\rangle + \Delta i_{L\eta}$$

and, finally, for $S_{4\eta}$

$$I_{S_{4\eta}} = \sqrt{(1 - D_{\eta}^+)} \left(1 - g_{\eta}^\perp\right) I_{out}^2 +$$

$$D_{\eta}^+ \left[I_x^2 - 2I_x \Delta i_{L\eta} + \frac{4}{3} \Delta i_{L\eta}^2\right]$$

(51)

with

$$I_x = -\left(1 - g_{\eta}^\perp\right) I_{out} - \langle i_{L\eta}\rangle + \Delta i_{L\eta}$$

The RMS current value in the half bridge switches is only dependent on the output current and output state. The RMS current value for $S_{4\sigma+1}$ is, therefore, given by

$$I_{S_{4\sigma+1}} = g_{\sigma+1}^\perp I_{out}$$

(52)

and for $S_{4\sigma+2}$ the RMS current value is

$$I_{S_{4\sigma+2}} = \left(1 - g_{\sigma+1}^\perp\right) I_{out}$$

(53)

VI. SIMULATION RESULTS

As an example, simulated waveforms of a 2-cell 250 W dc-ac converter are presented. The circuit diagram of this 2-cell converter is shown in Fig. 8, whose simulation parameters are given in Table V. The capacitor voltage set-points chosen are according to Table III, such that a set of eight equidistant output levels is obtained. The sinusoidal set-point has a modulation-depth of 0.9 ($M_{\text{sync}} = 0.9$).

The capacitor voltages are controlled in closed loop. The buck-boost operation is controlled by a current-mode controller and a first order linear voltage controller. Both buck-boost controllers, of cells one and two, are completely independent.

All components used in the simulation are ideal. The resistive load is connected to the output without any additional filtering. The resulting output voltage in steady-state is plotted in Fig. 13. The corresponding switch-gating signals for all 10 switches are presented in Fig. 14.
TABLE V
2-CELL, 8-LEVEL CONVERTER SIMULATION PARAMETERS.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$U_{DC}$</td>
<td>300 V</td>
</tr>
<tr>
<td>$\hat{u}_{out}$</td>
<td>$\pm 350$ V</td>
</tr>
<tr>
<td>$f_{sw}$</td>
<td>10 kHz</td>
</tr>
<tr>
<td>$C_1, C_2$</td>
<td>1 mF</td>
</tr>
<tr>
<td>$L_1, L_2$</td>
<td>210 $\mu$H</td>
</tr>
<tr>
<td>$U_{C1}^<em>, U_{C2}^</em>$</td>
<td>100 V</td>
</tr>
<tr>
<td>$f_{sine}$</td>
<td>50 Hz</td>
</tr>
<tr>
<td>$M_{sine}$</td>
<td>0.9</td>
</tr>
<tr>
<td>$R_l$</td>
<td>210 $\Omega$</td>
</tr>
</tbody>
</table>

Fig. 13. Simulation results: 2-cell, 8-level converter output voltage, $u_{out}$.

Fig. 14. Simulation results: switch-gating signals of switches $S_1$ to $S_{10}$.

Fig. 15. Experimental setup.

Fig. 16. Experimental results of a 2-cell, 8-level converter with 210 $\Omega$ load. Output voltage $u_{out}$ (200 V/div), output current $i_{out}$ (2 A/div) and capacitor voltages at (50 V/div).

Fig. 17. Inductor currents and capacitor voltages ripples.

VII. EXPERIMENTAL RESULTS

A prototype was constructed to experimentally test the principle of operation of an ECC based converter. The 2-cell prototype converter, with circuit diagram as shown in Fig. 8, comprises of five SKM100GB12T4 half-bridge IGBT modules with isolated drivers. The experimental setup, as shown in Fig. 15, operates in open-loop with the same parameters as in Table V. The measured output voltage and output current, together with the capacitor voltages, are shown in Fig. 16. On the same time-scale the inductor currents and capacitor voltage ripples are illustrated in Fig. 17. In Fig. 18 the inductor current and capacitor voltage ripple are detailed on a shorter timescale.

The obtained experimental results show a good coherence with the analysis and simulation results. The converter is stable in open-loop and the eight output levels can be clearly observed. Due to the absence of an output filter the stepping between levels is almost instantaneous. The small spikes between some level transitions are caused by blanking times, since during these short time intervals the output level is determined by the output current. In Fig. 17 a 5 V ripple can be seen on the capacitor voltage of $u_{C1}$ due to the absence of voltage control.
A proof-of-concept 2-cell 8-level dc-ac converter was designed, simulated and built. The obtained experimental results demonstrate the operation principle of the ECC, showing a clear 8-level output voltage waveform. All measured quantities are in good agreement with the analysis and simulation results.

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