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A Design Methodology for Power-efficient Reconfigurable SC $\Delta\Sigma$ Modulators

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SUMMARY

This paper presents a methodology to design reconfigurable switched-capacitor (SC) delta-sigma modulators ($\Delta\Sigma$ Ms) capable of keeping their corresponding power efficiency figures constant and optimal for a set of resolutions and signal bandwidths. This method is especially suitable for low-bandwidth, medium-to-high resolution specifications, which are common in bio-medical application range. The presented methodology is based on an analytic model of all different contributions to the power dissipation of the $\Delta\Sigma$ M. In particular, a novel way to predict the static power dissipated by integrators based on class-A and class-AB OTAs is presented. The power-optimal solution is found in terms of filter order, quantizer resolution, oversampling ratio and capacitor dimensions for a targeted resolution and bandwidth. As the size of the sampling capacitors is crucial to determine power consumption, three approaches to achieve reconfigurability are compared: sizing the sampling capacitors to achieve the highest resolution and keep them constant, change only the first sampling capacitor according to the targeted resolution or program all sampling capacitors to the required resolution. The second approach results in the best trade-off between power efficiency and simplicity. A reconfigurable $\Delta\Sigma$ M for bio-medical applications is designed at transistor-level in a 0.18 μ m CMOS process following the methodology discussed. A comparison between the power estimated by the proposed analytic model and the transistor implementation shows a maximum difference of 17%; validating thus the proposed approach.

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KEY WORDS: analog-digital converter, switched-capacitor, sigma-delta modulator, power optimization, reconfigurable.

1. INTRODUCTION

Low-bandwidth (up to few tens of kHz) high-resolution (>12 bits) Analog-to-Digital Converters (ADCs) are becoming more and more needed in a wide range of application fields, such as bio-medical and environmental monitoring [1]-[2]. In these kinds of applications, the signal carrying information needs a flexible and complex processing which is difficult and power-hungry to implement in the analog domain. The use of high-resolution ADCs helps to simplify the signal acquisition chain, making possible to shift most of the processing to the digital domain and relaxing the requirements on the analog front-end [3]. Because of the limited power budget available in autonomous sensor nodes [4], these ADCs should have excellent power

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efficiency and adapt their resolution and speed to the characteristics of the different possible input signals. Bio-potential signals have a spectrum between few hundreds of Hertz and few kilohertz, with an amplitude range between few tens of μV and few mV. A reconfigurable ADC can cope with many of these signals while minimizing area and power in the corresponding readout system. This component must be able to satisfy different resolution and bandwidth requirements keeping a minimum and constant figure-of-merit (*FoM*) in each mode of operation [5]. In this paper, *FoM* is calculated as in [6]:

$$FoM = \frac{P_{TOT}}{2 \cdot BW \cdot 2^{ENOB}} [\text{J/conv.s.}] \quad (1)$$

where P_{TOT} is the total power consumption and BW is the input signal bandwidth; $ENOB = \frac{SNDR_{dB} - 1.76}{6.02}$ is the effective number of bits and $SNDR_{dB}$ is the peak signal-to-noise-and-distortion ratio (in dB).

$\Delta\Sigma$ Ms are good candidates for reconfigurability because of their inherent bandwidth resolution trade-off [7]. Reducing the oversampling lowers indeed P_{TOT} , while decreasing the resulting $ENOB$. Continuous-time (CT) $\Delta\Sigma$ modulators are sometimes favoured over their SC counterparts because of their potential lower power consumption but their coefficients are determined by time-constants rather than capacitor ratios. Therefore, their integrator coefficients need to be changed depending on the clock frequency. On the contrary, switched-capacitor (SC) reconfigurable $\Delta\Sigma$ Ms do not suffer from this and their corresponding poles and zeros of the NTF scale automatically with the clock frequency [8]. SC modulators can thus be clocked at virtually any rate allowed by the gain-bandwidth product of the opamps that they use. Moreover, SC modulators are robust against process and temperature variations as their transfer functions rely on capacitor ratios, which are quite accurate in modern technologies. CT $\Delta\Sigma$ Ms, however, need calibration on their passives to compensate for process variations. For all these reasons, the proposed method for the design of power-optimal reconfigurable $\Delta\Sigma$ Ms is focused on SC implementations.

The most power efficient $\Delta\Sigma$ architecture is identified for each mode of operation among single-loop topologies with different loop order N , oversampling ratio OSR and quantizer resolution B , using an analytic model for the power consumption [9]. Three different strategies to achieve reconfigurable $\Delta\Sigma$ Ms are identified and compared in terms of power efficiency using the proposed design methodology.

Single-loop $\Delta\Sigma$ Ms have been chosen here because of the relaxed specifications on their analog blocks [10]. Moreover, this class of $\Delta\Sigma$ M is suitable for high-accuracy low-to-moderate bandwidth applications, including the ones in the case study presented in this paper. Our approach, however, can be extended to cascade architectures if high-order noise-shaping is needed and stability becomes a constraint [11].

In this paper, we also improve several aspects of the analytic power model presented in [9]. In particular, the power dissipated by the OTAs in the integrators (called “static power” in our model) is estimated here taking into account:

- Both the small-signal and the large-signal behavior of the OTAs
- Both class-A and class-AB OTA implementations.

Finally, we have applied and validated our method designing a reconfigurable $\Delta\Sigma$ for bio-potential (EEG, ECG, EMG) and audio signals able to work in the operation modes described in Table I.

A constant FoM (see Table I) cannot be achieved simply as a consequence of the reduced BW and increased $ENOB$: going from the medium to the high resolution mode, the $ENOB$ increases by 2 bits (factor 4) while the bandwidth decreases by a factor 10. Therefore, the total power P_{TOT} has to decrease at least 2.5 times for a constant FoM .

The paper is organized as follows: Section II presents a high-level overview of the design methodology. Section III describes the procedure for sizing the first-integrator sampling capacitors $C_{s,i}$. Section IV describes the analytic model used to estimate the power consumption of a single-loop $\Delta\Sigma$ for a required $ENOB$ and BW , focusing on an improved description of the static power consumption. In Section V, the proposed design methodology is applied to design a power-optimal reconfigurable $\Delta\Sigma$ modulator satisfying the requirements in Table I. Results are validated by comparing the model estimations with post-extracted simulations of the reconfigurable modulator. Some conclusions are drawn in Section VI.

2. OVERVIEW OF THE METHODOLOGY

As the resolution of a $\Delta\Sigma$ is mainly determined by N , B , OSR , and the sampling capacitors of each integrator¹ $C_{s,i}$, several combinations of these parameters can provide the targeted dynamic range (DR). A structured design approach has been proposed in [9] to find the power optimal solution. In this paper, the methodology in [9] is extended to address the design of power-efficient *reconfigurable* $\Delta\Sigma$ s.

The size of the sampling capacitors $C_{s,i}$ is crucial in determining the power consumption of the complete $\Delta\Sigma$. For this reason, three approaches to reconfigurability are possible: a *fixed- $C_{s,i}$* approach, a *variable- $C_{s,1}$* approach and a *variable- $C_{s,i}$* approach. In the *fixed- $C_{s,i}$* approach, the sampling capacitors in all working modes are the same as the ones calculated for the highest resolution mode. This strategy allows a simple and area-efficient design that does not require the use of switchable passives. However, as shown already in [7], this approach leads to poor power optimization and it is mostly avoided in state-of-the-art literature. Therefore, it will not be considered in the rest of this paper. In the *variable- $C_{s,1}$* strategy, the size of the first-integrator capacitor $C_{s,1}$ is adapted to the targeted resolution of each working mode, while the capacitors of the following integrators are kept equal to those used in the highest resolution mode. As shown in [9], adapting $C_{s,1}$ to the targeted resolution is crucial in optimizing the power consumption. On the other hand, the power dissipation due to the capacitors of the following integrators is normally negligible thanks to the noise filtering provided from the integrator stages following the first one. The *variable- $C_{s,i}$* approach consists in programming the sampling capacitors of all the integrators according to the required resolution, deriving a specific size for each capacitor in each $\Delta\Sigma$ working mode. These strategies for reconfigurability are compared in terms of power efficiency following the proposed structured design approach.

¹ The index i ($1 \leq i \leq N$) indicates the position of each integrator in the $\Delta\Sigma$ loop starting from the input.

For a targeted resolution equal to $ENOB$ bit, the $SNDR$ of the $\Delta\Sigma$ is defined as :

$$SNDR = 3 \cdot 2^{2 \cdot ENOB - 1} = \frac{V_{in,MAX}^2}{P_{Th} + P_Q + P_{HD}} \quad (2)$$

where P_{Th} , P_Q and P_{HD} are the power of the in-band thermal noise, quantization error, and harmonics, respectively. $V_{in,MAX}$ is the maximum input range of the modulator, defined as $V_{in,MAX} = OL \cdot V_{in,FS}$, being the overload level OL the maximum amplitude relative to the input full scale $V_{in,FS}$ at which the modulator reaches its peak $SNDR$ [12]. The derivation of OL values in this work will be discussed in Section 3. As suggested above, the power term P_{HD} is related to the non-linearities in the $\Delta\Sigma$. In SC implementations, the main causes of distortion are the non-linear OTA gain, the non-linear settling of the integrators, non-linear capacitances and the non-linearities of the switches [13]. P_{Th} and P_Q in (2) are defined for a fully-differential $\Delta\Sigma$ implementation as [9]:

$$P_{Th} = \frac{2kT}{OSR \cdot C_{s,1}} \quad (3)$$

$$P_Q = \frac{(2V_{in,FS})^2}{12} \frac{\pi^{2N}}{(2N+1) \cdot OSR^{2N+1} (2^B - 1)^2} \quad (4)$$

where $C_{s,1}$ is the first-integrator sampling capacitor, variables k and T stand for the Boltzmann constant and the absolute temperature, respectively. In (3) only the thermal noise coming from sampling operation of the switches is considered [14]. This is based on the assumption that the contribution of the OTA noise is negligible with respect to the noise of the switches. This assumption needs to be verified a posteriori by other means, such as behavioral simulations.

As starting point of the design methodology, we consider the highest resolution mode of the reconfigurable $\Delta\Sigma$ modulator (e.g. HR/LB mode in Table I).

a) Firstly, we identify the combinations of (N, B, OSR) that are able to achieve the specified $ENOB$ within the given BW . The selection is based only on quantization noise requirements. Therefore, we combine (2) and (4) by temporarily neglecting both the term P_{Th} and P_{HD} in (2). When doing so, a design margin of 10 dB is added to the $SNDR$ on top on the specification value. This margin guarantees that the quantization noise is well below the thermal noise P_{Th} and takes into account sources of distortion P_{HD} that are not included in the analytical model [15]. This noise-budget strategy aims at making the thermal noise dominant in the modulator and is common for power-efficient designs, as suppressing the thermal noise costs a lot of power [16].

b) The minimum value of $C_{s,1}$ which satisfies the $SNDR$ requirement in terms of thermal noise is calculated. This is done by using together (2) and (3) for all the combinations of (N, B, OSR) in the solution space selected in step a). In (2), the term P_{HD} is neglected assuming that $SNDR = SNR$, i.e. considering $P_{HD} \ll P_{Th}$. Note that this assumption is validated a posteriori with transistor-level simulations. The full procedure used to determine all the sampling capacitors is better described in Section 3.

c) We estimate the total power consumption of the $\Delta\Sigma\text{M}$ for all the combinations in the (N, B, OSR) solution space found in Step a) using the values of $C_{s,i}$ found in Step b). The power is calculated using the analytic model presented in Section IV and the combination of (N, B, OSR) granting the lowest power solution is annotated.

We proceed then with the lower-resolution operation modes of the reconfigurable $\Delta\Sigma\text{M}$ (e.g. MR/MB and LR/HB modes in Table I).

d) First, we identify the possible solutions in the (N, B, OSR) space following Step a). New combinations of (N, B, OSR) are selected based on the set of requirements (ENOB, BW) for each mode of operation.

e) We calculate the sampling capacitors $C_{s,i}$ for the lower resolution modes in a similar way to what is done in Step b). The size of the capacitors in the integrators following the first one will depend on the strategy chosen for reconfigurability (*fixed- $C_{s,i}$* approach, *variable- $C_{s,1}$* approach and *variable- $C_{s,i}$* approach). In the *variable- $C_{s,1}$* approach, $C_{s,1}$ is sized based on the new target resolution, while the capacitors of the following integrators are kept equal to those found for the highest resolution mode. In the *variable- $C_{s,i}$* approach, the sampling capacitors of all the integrators are calculated again according to the required ENOB .

f) Finally, we apply Step c) and select the most power-efficient combinations of (N, B, OSR) for the lower resolution modes, both in *variable- $C_{s,1}$* and in *variable- $C_{s,i}$* approaches.

Based on the results of Step c) and f), we determine the power-optimal design of the reconfigurable $\Delta\Sigma\text{M}$.

3. SAMPLING CAPACITORS SIZING

For all the combinations of (N, B, OSR) in the solution space, the sampling capacitor $C_{s,1}$ of the first-integrator in the loop filter is calculated from thermal noise requirements according to [9]:

$$C_{s,1} = \frac{2kT}{\text{OSR}} \cdot \frac{\text{SNR}}{(V_{\text{ref}} \cdot \text{OL})^2} \quad (5)$$

where V_{ref} is the reference voltage of the quantizer. V_{ref} is assumed to coincide with the supply voltage V_{DD} in both feedback (FB) and feed-forward (FF) topologies. As aforementioned, OL is overload level and we assume here that $\text{SNR} = \text{SNDR}$.

A specific value of OL must be assigned to each combination of (N, B, OSR) . This decision requires careful consideration.

This decision requires careful consideration. The OL is indeed a function of the infinity norm $\|H_\infty\|$, a parameter which strongly affects the stability of the loop and thus the final $\Delta\Sigma\text{M}$ performance. In the case of a single-bit quantizer, the infinity norm is traditionally chosen to be 1.5. In the case of a multi-bit quantizer, $\|H_\infty\|$ can be increased to improve the signal-to-quantization noise ratio (SQNR). However, this cannot be pushed too far, because then the OL starts to decrease. In [10] specific values of infinity norm have been chosen for the different combinations of filter orders and quantizer bits to maximize the SQNR while minimizing the decrease of the OL . In this work we adopt the same choice for $\|H_\infty\|$, while the signal transfer function (STF)

and the noise transfer function (NTF) are determined using [17]. More specifically, the optimal NTF is determined using the `synthesizeNTF` function in [17], to find out the corresponding *OL* values. Finally, the modulator stability is verified by means of long-term transient simulations in the transistor-level design phases.

Matching requirements also set a lower boundary for $C_{s,1}$. The total capacitance implementing a B -bit feedback DAC has indeed the same sizing as the correspondent input sampling capacitor $C_{s,i}$. A B -bit feedback DAC is implemented as a capacitive array of 2^B-1 unit elements C_u so that $C_{s,i} = (2^B-1) \cdot C_u$. A linearity higher than the targeted *ENOB* is required for the DAC. To achieve this goal we assume in this paper that a first-order data weighted averaging (DWA) is used in the feedback loop. The minimum size of the first sampling capacitor $C_{s,1}$ can thus be calculated from the requirements of DAC linearity and capacitor matching, assuming a first-order DWA, according to [9]:

$$C_{s,1} = 2^{2 \cdot ENOB} \cdot \pi^2 \cdot K_\sigma^2 \cdot \left(\frac{2^B - 2}{2^B - 1} \right)^2 \cdot \frac{C_A}{3 \cdot OSR^3} \quad (6)$$

where K_σ is the matching constant of capacitors and C_A is the capacitance per unit area for the given technology ($K_\sigma \approx 2.5\%$ and $C_A \approx 2 \text{ fF}/\mu\text{m}^2$ for a $0.18\mu\text{m}$ CMOS technology). $C_{s,1}$ is sized to be the maximum of the values given by (5) and (6).

The sampling capacitors $C_{s,i}$ in the integrators following the first one ($i > 1$) can be sized from thermal noise requirements as [9], taking into account the noise filtering introduced by the previous integrators in the $\Delta\Sigma$ M:

$$C_{s,i} = C_{s,1} \frac{\pi^{2i-2}}{OSR^{2i-2} (2i-1)} \prod_{k=2}^i \frac{1}{a_{k-1}^2}; \quad (7)$$

where a_k are the in-loop coefficients of single-loop $\Delta\Sigma$ Ms. The coefficients a_k are shown in Fig. 1 (a) and (b) for FB and FF $\Delta\Sigma$ M architectures, respectively [9].

Fig. 1. Conventional FB (a) and FF (b) single loop $\Delta\Sigma$ modulators. The blocks $I(z)$ represent the SC integrators.

The performance of single-loop architectures is also influenced by the in-loop coefficients (a_i and c_i) as they need to provide a stable operation in the whole input range [18]. In SC architectures, these coefficients are implemented as ratios of capacitors. Due to process variations, these capacitors will be slightly different from their intended value. Extensive behavioral simulations have shown that variations as large as 2% do not degrade the performance of the $\Delta\Sigma$ M in the resolution range studied in this paper. Considering the matching properties of capacitors in a $0.18\mu\text{m}$ CMOS technology, the minimum size for the sampling capacitors $C_{s,i}$ ($i > 1$) has been

set accordingly to 50 fF. This constraint is far less stringent than the one for $C_{s,i}$, given by (6), as errors introduced by the subsequent integrators are shaped by the transfer function of the previous ones.

4. ANALYTIC MODEL FOR THE POWER CONSUMPTION OF SC SINGLE-LOOP $\Delta\Sigma$ S

Once the minimum value of the sampling capacitors $C_{s,i}$ is known as a function of (N, B, OSR) , it is possible to estimate the $\Delta\Sigma$ total power dissipation P_{TOT} .

The total power consumption consists of four main contributions: the static power of the OTAs P_{STAT} , the dynamic power for charging the capacitors in the modulator P_{DYN} , the power dissipated by the quantizer P_{QUANT} and the power dissipated by the DWA digital circuitry P_{DWA} . Thus [9],

$$P_{TOT} = P_{STAT} + P_{DYN} + P_{QUANT} + P_{DWA} \quad (8)$$

As anticipated, the models for P_{STAT} and P_{DWA} are improved in this section with respect to [9]. Indeed, in this paper a more accurate model of the OTA power consumption is provided and the expression for P_{DWA} is modified to fit the DWA implementation chosen in Section V.

A. Static Power

The $\Delta\Sigma$ static power was calculated in [9] taking into account only small-signal settling requirements and did not include the slewing behavior of the OTAs. This is a rather coarse approximation for OTAs in $\Delta\Sigma$ modulators, especially in single-bit topologies, where the feedback signal is inherently large. Moreover, the study in [9] was limited to the simple case of a class-A folded-cascode OTA. In this paper, we address these issues and improve the analytic model of OTA static power by:

- Considering both the small-signal and the large-signal behavior of the OTAs;
- Finding an expression for the OTA power consumption during the time interval in which the OTA has a large-signal behavior which is a function of the feedback signal, and thus of the number of bits B of the quantizer;
- Deriving specific expressions for several class-A and class-AB OTA topologies.

This improved model enables an accurate estimation of P_{STAT} and makes possible to compare the power consumption of different circuit implementations of the OTA. This way, we can choose the most power efficient OTA implementation for each $\Delta\Sigma$ architecture having different (N, B) . For simplicity, the comparison does not take into account OTAs non-idealities such as OTAs noise and DC gain. We assume that all the topologies are able to satisfy the design requirements both in terms of noise and DC gain. This hypothesis needs to be finally verified by means of behavioral simulations.

The static power model is based on the analysis described in [19]. However, the method presented in that paper is only valid for single-bit SC $\Delta\Sigma$ architectures. This paper derives an expression for the feedback signal which is a function of the quantizer number of bits B and thus allows extending the power estimation to multi-bit architectures.

Large-signal and small-signal behavior

The single-ended implementation of an SC integrator is represented in Fig. 2. ϕ_1 and ϕ_2 are two non-overlapping phases, ϕ_1 the sampling phase and ϕ_2 the integration phase. The analysis of a single-ended OTA is chosen for simplicity. Note that all formulae can be derived in a similar way for the fully differential implementations. During ϕ_1 , the input signal V_{in} is sampled on the input capacitor C_s and the feedback signal is generated by the corresponding sampling of the references. The reference voltages $+V_{ref,j}$ or $-V_{ref,j}$ are sampled on each of the 2^B-1 unit elements C_u depending on the feedback signals $L_{p,j}$ and $L_{n,j}$ generated by the DWA ($j=1, \dots, 2^B-1$).

Fig. 2. Single-ended implementation of an SC integrator. The feedback signals $L_{p,j}$ and $L_{n,j}$ are controlled by the digital output code of the modulator quantizer.

During ϕ_2 , the charge stored in these capacitors is transferred to the integrating capacitor C_I . In this phase, the OTA shows two different behaviors: large-signal and small-signal, depending on the voltage at the inverting input node of the OTA V_m . As long as V_m is larger than the input-pair threshold voltage, the OTA is in large-signal behavior and its output slews. When V_m becomes lower than the differential-pair threshold voltage, the OTA has a small-signal behavior and its gain-bandwidth GBW determines the settling performance. The integrating phase ϕ_2 is consequently divided into two periods, called large-signal period and small-signal period, respectively [19]. The average power $\bar{P}$ dissipated in one clock period T by the OTA can be calculated as a weighted sum of the power consumed during the large-signal period P_{la} and of the power consumed during the small-signal period P_{sm} :

$$\bar{P} = \alpha\theta \cdot P_{la} + \beta\zeta \cdot P_{sm} \quad (9)$$

where variables α and β are parameters dependent on the OTA topology. Until now we have considered just the power dissipated by the OTA during the integrating phase, during the large-signal period P_{la} and during the small-signal period P_{sm} , respectively. ζ and θ are corrective terms which are added to take into account the power dissipated by the OTA during the sampling phase ϕ_1 (see Table III). The calculation of P_{sm} is derived as in [9] assuming that the transistors of the input stage are biased in weak inversion and that the settling of the amplifier is completed before the subsequent sampling moment if $GBW = 5 \cdot f_s$:

$$P_{sm} = 5 \cdot 2\pi \cdot n \cdot V_{Th} \cdot C_{eq} \cdot V_{DD} \cdot f_s \quad (10)$$

where V_{Th} is the thermal voltage ($V_{Th}=26$ mV at 300K), n is the weak inversion slope factor (1.3-1.5) and f_s is the sampling frequency $f_s = 2BW \cdot OSR$. C_{eq} is the equivalent load capacitance which can be expressed, for both FB and FF topologies, as [9]:

$$C_{eq} = C_s + C_p + C_L \left(1 + \frac{C_s + C_p}{C_I} \right) \approx C_s + C_L \left(1 + \frac{C_s}{C_I} \right) \quad (11)$$

Note that C_{eq} corresponds to the effective closed loop capacitive load of an SC integrator during the integration phase. Here, C_p is the OTA input parasitic capacitance and C_L is the integrator output load. C_p is assumed negligible since its value is normally minimized by design.

The power for charging the capacitors during the large-signal period P_{la} is function of both the input signal V_{in} and the reference voltages and can be expressed as [19]:

$$P_{la}(V_{in}, \pm V_{ref}) = \left(C_s \cdot V_{in} + \sum_{j=1}^{2^B-1} C_u \cdot (\pm V_{ref,j}) \right) V_{DD} \cdot f_s \quad (12)$$

Please note that this contribution is input-signal dependent as the first term in (12) is the charge stored on C_s and C_u at the beginning of the integrating phase ϕ_2 .

If we now assume x to be the normalized input signal with respect to the reference voltage V_{ref} , i.e. $x = V_{in}/V_{ref}$, the notation $P_{la}(V_{in}, \pm V_{ref})$ can be rewritten as:

$$\begin{aligned} P_{la}(V_{in}, \pm V_{ref}) &= \left(C_s \cdot x \cdot V_{ref} + \sum_{j=1}^{2^B-1} C_u (\pm V_{ref,j}) \right) V_{DD} \cdot f_s = \\ &= \left| \frac{k(t)}{2^B - 1} \mp x \right| \cdot C_s \cdot V_{ref} \cdot V_{DD} \cdot f_s \end{aligned} \quad (13)$$

where $\frac{k(t)}{2^B - 1}$ is the B -bit DAC feedback signal normalized with respect to V_{ref} , and,

again, $C_s = (2^B - 1) \cdot C_u$.

$P_{la}(V_{in}, \pm V_{ref})$ is the minimum power consumption for the combination of the input signal and the reference voltage during the large-signal period. $P_{la}(V_{in}, \pm V_{ref})$ is both dependent on the number of bits of the feedback DAC B and the input signal as it includes $k(t)$. The feedback signal $k(t)$ is a B -bit representation of V_{in} . Depending on the amplitude of the input signal, $k(t)$ ranges between 0 and $2^B - 1$ and its value corresponds to the number of DAC elements C_u connected to $+V_{ref}$ (see Fig. 2).

Overall static power for different OTA topologies

The overall power dissipation of sinusoidal inputs can now be derived for the different OTA topologies. Let us first assume a high OSR , so that any sampled value of the sinusoidal signal can be treated as a quasi-static input [19]. We will consider the input signal to be $x = b + a \sin \omega t$, where b is the DC bias set to $V_{ref}/2$ ($b = 1/2$), and a is the amplitude ($a = OL/2$), with OL standing for the overload level.

The power consumption is divided by the factor $C_s \cdot V_{ref} \cdot V_{DD} \cdot f_s$, to simplify the formulae and obtain the normalized power $\hat{P}(x)$. The final static power model is derived in the following sub-sections for both class-A OTAs and class-AB OTAs.

Static power model of class-A OTAs

Since the supply current in a class-A OTA is fixed, the OTA should be designed to handle the largest charge transfer. Therefore, the minimum power required during the large-signal period is equal to the largest of the two values that the expression (13), i.e.:

$$\begin{aligned}\hat{P}_{la,A}(x, k(t)) &= \max\left(\left|\frac{k(t)}{2^B-1} - x\right|, \left|\frac{k(t)}{2^B-1} + x\right|\right) = \\ &= \frac{k(t)}{2^B-1} + |x|\end{aligned}\quad (14)$$

If the maximum value of the sinusoidal signal x is $b + |a| = \frac{1}{2} + \frac{OL}{2}$, the corresponding power will be:

$$\hat{P}_{la,A} = \frac{k(t)}{2^B-1} + \frac{1}{2} + \frac{OL}{2} \quad (15)$$

The total normalized power consumption of a class-A OTA can thus be found from (9), (10) and (15):

$$\hat{P}_A = \alpha\theta \cdot \left(\frac{k(t)}{2^B-1} + \frac{1}{2} + \frac{OL}{2}\right) + \beta\zeta \cdot \left(\frac{5 \cdot 2\pi \cdot n \cdot V_{Th} \cdot C_{eq}}{V_{ref} \cdot C_s}\right) \quad (16)$$

Static power model of class-AB OTAs

Class-AB OTAs adaptively adjust their output current depending on the required output voltage, and thus to the needed charge transfer in an SC circuit. Therefore, their average power dissipation during the large-signal period will be a function of the actual signal x and of the normalized DAC feedback signal $\frac{k(t)}{2^B-1}$. Given a certain

sampled value of x , the output of the $\Delta\Sigma$ will toggle between two digital values with a certain statistics. The statistics will be different depending on where x is with respect to the two closest quantization levels. As a result, the DAC feedback will toggle, with the same statistics as the $\Delta\Sigma$ output, between the two DAC levels, $k1$ and $k2$, which are the closest to x , above and below. We can thus express the average power dissipation in (13) as:

$$\begin{aligned}\hat{P}_{la,AB}(x, k(t)) &= P_{la,AB}(x, k1) \cdot f(x, k1) + \\ &+ P_{la,AB}(x, k2) \cdot f(x, k2)\end{aligned}\quad (17)$$

where $P_{la,AB}(x, k1)$ and $P_{la,AB}(x, k2)$ are the power consumptions associated to the DAC feedback values $k1$ and $k2$, respectively. $f(x, k1)$ and $f(x, k2)$ are the probability of $k1$ and $k2$ given the value of x . The values of $f(x, k1)$ and $f(x, k2)$ can be found as a function of x and B^2 . The average power dissipation during the large-signal period can thus be expressed for a certain sampled value of x as:

² In the appendix of [18] the expressions of $f(x, k1)$ and $f(x, k2)$ are derived for single-bit modulators. We follow the same procedure here to derive $f(x, k1)$ and $f(x, k2)$ for multi-bit $\Delta\Sigma$ s.

$$\hat{P}_{la,AB}(x, k(t)) = \frac{k(t)}{2^B - 1} - (2^B - 1) \cdot x^2 \quad (18)$$

The normalized average power dissipation is finally obtained by time-averaging (18) over one signal period T :

$$\begin{aligned} \hat{P}_{la,AB} &= \frac{1}{T} \int_0^T (2^B - 1) \cdot \left[\frac{k(t)}{2^B - 1} - (b + a \sin \omega t)^2 \right] dt = \\ &= (2^B - 1) \cdot \frac{1}{T} \int_0^T \left[\frac{k(t)}{2^B - 1} - \left(\frac{1}{2} + \frac{OL}{2} \sin \omega t \right)^2 \right] dt \end{aligned} \quad (19)$$

This equation allows us to average over all the possible values of the sinusoidal signal x . Please note that, contrary to [19], a closed form cannot be found for this integral as it includes the feedback signal $k(t)$, which varies during the period T . $k(t)$ is indeed a B -bit representation of V_{in} . The total normalized power consumption of a class-AB OTA is finally derived from (9), (10) and (19) as:

$$\begin{aligned} \hat{P}_{AB} &= \alpha \theta \cdot (2^B - 1) \cdot \frac{1}{T} \int_0^T \left[\frac{k(t)}{2^B - 1} - \left(\frac{1}{2} + \frac{OL}{2} \sin \omega t \right)^2 \right] dt + \\ &+ \beta \zeta \cdot \left(\frac{5 \cdot 2\pi \cdot n \cdot V_{Th} \cdot C_{eq}}{V_{ref} \cdot C_s} \right) \end{aligned} \quad (20)$$

The total normalized power dissipations in (16) and (20) are summarized in Table II.

Static power comparison of class-A and class-AB topologies

We can now compare the power dissipation of different OTA topologies to determine the power-optimal OTA to be used in an architecture with given (N, B) . Current-mirror and folded-cascode OTAs are listed here as examples of class-A OTAs while the Castello topology [20] is used as a representative example of a class-AB OTA. Telescopic OTAs are not considered, despite their power efficiency, because they are not suitable for low-voltage operation, which is one of the main points of this work. Fig. 3 shows the simplified circuit schematics of current-mirror, folded-cascode and Castello topologies.

Table III provides the constants α , β , θ , ζ corresponding to each circuit. M is the current mirror ratio in Table III and Fig. 3 (a) and (c). F is defined as $F = I_{bias} / I_{tail}$ where I_{bias} is the extra current used for biasing the class-AB output branch and I_{tail} is the OTA tail current (Table III and Fig. 3 (c)). We assume that the minimum value of I_{bias} and I_{tail} is 50nA for matching purposes. F is always set to 0.25, 0.5 or 1 and considers the aforementioned matching constraint. The ratio between the sampling and the integrating time is γ , with $\gamma = T_{sam} / T_{int}$ ($\gamma=1$ in this work).

Fig. 4 illustrates the behavior of the normalized static power with respect to B (number of bits in the quantizer) for $N=3$. In the single-bit configuration, the class-AB OTA is power-optimal: as B grows, class-A current-mirror OTAs become more and more power efficient. In multi-bit topologies, indeed, the difference between the input and the feedback signals is smaller and class-AB OTAs mostly show small-signal behaviour. With respect to class-A OTAs, they thus pay the power penalty of the extra current used for biasing the class-AB output branch. Class-A folded-cascode

topologies always show the worst power performance in the comparison, as it is expected considering the values of α and β shown in Table III.

Fig. 3. Simplified circuit schematic for current-mirror (a) OTA, folded-cascode OTA (b) and Castello OTA (c) [20].

Fig. 4. Normalized power dissipation of class-A and class-AB topologies as a function of B for $N=3$.

B. DWA Power

The power penalty to correct for capacitor mismatch errors is calculated considering a data weighted averaging approach (DWA) as used in the case study shown below.

Following the same approach as in [9], the dynamic power dissipation of CMOS digital gates can be expressed as:

$$P_{DWA} = \sum_{m=1}^K \psi_m \cdot C_{in,m} \cdot V_{DD}^2 \cdot f \quad (21)$$

where K is the number of the internal nodes, ψ_m is the switching activity of each node m , and $C_{in,m}$ is the parasitic capacitance of each internal node m [21].

The DWA architecture contains a binary-to-thermometer converter which is implemented by means of logic gates, a (2^B-1) bit-barrel shifter and a B -bit accumulator. The barrel shifter is implemented using $2^B \cdot \log_2 2^B = B \cdot 2^B$ multiplexers (MUXs) and 2^B inverters [22]. Each MUX is equivalent to two switching inverters. The B -bit accumulator comprises a B -bit adder and a B -bit register. Assuming each internal node loaded only by the gates connected to that specific point and expressing the equivalent load of any logic gate as a multiple of the inverter equivalent load, the power dissipated can be approximated as ($\psi_m \approx 1$):

$$P_{DWA} = V_{DD}^2 \cdot C_{inv} (2BW \cdot OSR) \cdot \left[(2^B - 1)(B + 1) + \sum_{n=0}^{B-1} (2^B - 2^n) + 8B \right] \quad (22)$$

where C_{inv} is the equivalent input capacitance of a minimum size inverter. If we estimate the switching energy of a minimum-size 0.18 μ m CMOS inverter to 5 fJ [23], the corresponding capacitance C_{inv} will become 10 fF per logic node. Note that this contribution is not added to the total power consumption for architectures with $B=1$, as linearity is not a concern in single-bit designs and DWA is therefore not needed.

C. Total Power consumption

The updated formulae to estimate P_{STAT} and P_{DWA} are summarized in Table IV together with the other contributions to power consumption already analyzed in [9].

In the expression for the dynamic power P_{DYN} , C_{TOT} is the total capacitance switching in the $\Delta\Sigma$ M, which can be expressed for FB and FF topologies respectively as:

$$C_{TOT,FB} = 2 \sum_{i=1}^N C_{s,i} \left(1 + \frac{1}{a_i} \right) \text{ and } C_{TOT,FF} = 2 \cdot C_{s,l} \left(1 + \frac{1}{a_l} \right).$$

In P_{COMP} , V_{eff} is defined as the effective voltage of the circuit, $V_{eff} = \delta V_{DD} - \varepsilon V_{SW}$. V_{SW} is the input signal swing; η is a power efficiency parameter and L_{min} is the gate length for the used technology. The parameters δ , ε , η are derived from transistor level simulations in [10] ($\delta=0.6$, $\varepsilon=0.3$, $\eta=32100$).

In P_{FLASH} and P_{SAR} , $C_{in,ADC}$ and C_{SAR} are the capacitance of the SC level shifter placed at the input of the flash-ADC, and the unit capacitor of the SAR DAC array, as it is described in [9].

5. CASE STUDY: DESIGN OF A RECONFIGURABLE $\Delta\Sigma$ FOR BIOMEDICAL APPLICATIONS

In this Section, the method outlined in Section II is applied to design a reconfigurable $\Delta\Sigma$ with the operation modes specified in Table I. According to the general methodology, Step a) is applied to find all values of (N, B, OSR) which satisfy the specifications of the HR/LB mode ($ENOB=16$, $BW=256$ Hz). Step b) is used then to define the corresponding values of the sampling capacitors $C_{s,i}$. The order of the loop filter has been limited to 4, the resolution of the internal quantizer to 5 bits, while OSR is swept between 16 and 128. When choosing the actual OSR value for implementation, only powers of 2 will be considered, to simplify the design of the decimation filter. Note that first-order architectures are not considered as they do not reach the targeted resolution for this OSR range. According to Step c) the power dissipation is calculated using the analytic power model for each $\Delta\Sigma$ architecture satisfying the HR/LB specs. The results are shown for FB and FF implementations in Fig. 5 (a) and (b), respectively. The power consumption is shown as a function of OSR and for different combinations of (N, B) . Missing or incomplete curves represent combinations of (N, B, OSR) with insufficient resolution. A supply voltage of 1V has been assumed and a SAR ADC has been chosen to calculate P_{QUANT} , as this approach enables power-efficient multi-bit quantization [22].

As the power optimization here described is based on the $SNDR$ requirement, the power curves in Fig. 5 (and Fig. 6) should be considered as a lower limit, obtained for single loop designs that are not limited by linearity issues. The same considerations about non-linearity as in [9] can be applied here.

Fig. 5. Estimation of P_{TOT} for HR/LB mode ($ENOB=16$, $BW=256$ Hz) as a function of OSR in FB (a) and in FF (b) implementations.

In both feedback (FB) and feedforward (FF) topologies, the power efficiency is higher for low-order $\Delta\Sigma$ and the minimum power consumption (marked with an asterisk) is obtained with a second-order modulator. P_{STAT} and P_{DYN} values are indeed minimized for a small number of integrators.

The power consumption is also inversely proportional to B as the use of a multi-bit quantizer in the $\Delta\Sigma$ modulator reduces the quantization noise and improves the stability of the loop. The allowed OL levels in (5) thus become larger, reducing the

size of the minimum $C_{s,l}$ as well as the power. The only exception to this general trend is for single-bit FB topologies, for which we used class-AB OTAs (see Fig. 4).

Fig. 5 finally shows that it is possible to reach a good trade-off between thermal noise and quantization noise power contributions (the local minimum in the curves) for low OSR s. The OTA static power increases with OSR through its GBW (see Table IV); at the same time, it includes $C_{s,l}$ and $C_{s,i}$ (see (23) and (24)). At low OSR , $C_{s,l}$ and $C_{s,i}$ decrease with OSR increasing. At low OSR , if (5) is used to calculate $C_{s,l}$, the proportionality of the static power to OSR can be approximated as:

$$P_{STAT} \propto OSR \cdot \left(C_{s,l} + \sum_{i=2}^N C_{s,i} \right) \quad (23)$$

$$\propto k + \frac{1}{OSR^{2i-2}}$$

At high OSR , $C_{s,l}$ and $C_{s,i}$ reach the minimum value determined by matching requirements. Therefore, in this case they are constant and:

$$P_{STAT} \propto OSR \cdot \left(C_{s,l} + \sum_{i=2}^N C_{s,i} \right) \quad (24)$$

$$\propto OSR \cdot k$$

The best power optimization is achieved for values of $N=2$, $B=5$ and $OSR=64$ in both FB and FF topologies. In general, FF architectures exhibit lower power consumption.

For the other modes of operation, we will follow either the *variable- $C_{s,l}$* or the *variable- $C_{s,i}$* approach. The former will be investigated first.

The *variable- $C_{s,l}$* strategy allows reconfiguring the $\Delta\Sigma M$ in a relatively simple way. It requires only 4 switchable capacitor arrays in a fully differential SC architecture. After applying Steps d), e) and f), the achieved values of P_{TOT} for the MR/MB and the LR/HB modes are shown in Fig. 6 for FF topologies. Note that FF topologies are indeed, also in these modes, more power efficient than FB.

Fig. 6. *Variable- $C_{s,l}$* approach: P_{TOT} as a function of OSR using FF implementations for (a) MR/MB mode ($ENOB=14$, $BW=2$ kHz) and (b) LR/HB mode ($ENOB=12$, $BW=16$ kHz).

As in HR/LB mode, low-order topologies are more power efficient than those with higher order. In low resolution modes, it turns out that the minimum value of $C_{s,l}$ is limited by matching requirements. Also, the best power efficiency is achieved with multi-bit configurations in MR/MB and LR/HB modes. The power-optimal choice is $N=2$, $B=4$ in both MR/MB and LR/HB cases. As a result of the selection in Step f), the

best values of power consumptions and $FoMs$ are reported in Table V for FF implementations. Varying the first-integrator sampling capacitors according to the required resolution keeps FoM values almost constant among the three different $\Delta\Sigma$ operation modes. The FoM is comparable in HR/LB and LR/HB modes (around 0.2 pJ/conv.s.) while is slightly lower in MR/MB mode (0.13 pJ/conv.s.). In MR/MB mode, neither high-resolution (which demands large sampling capacitors) nor high- BW (which requires a high-frequency sampling rate) is required, making it simpler to decrease the power of the $\Delta\Sigma$.

The *variable- $C_{s,l}$* approach to reconfigurability applied to the operation modes of Table I requires changing the quantizer resolution between HR/LB mode on the one hand, and MR/MB, LR/HB cases on the other (Table V). This results in a complex circuit implementation that can be further simplified as shown in next subsection.

We can now apply Steps d), e) and f) to the *variable- $C_{s,i}$* approach for comparison. The dependency of the total power consumption on the design parameters N , B and OSR obtained with this approach is similar to the one shown in Fig. 6. Also in this case FF topologies are more power efficient than FB $\Delta\Sigma$ architecture. P_{TOT} is generally minimized for low N and low OSR while power decreases for high-resolution quantizers. The power-optimal values of P_{TOT} and FoM using the variable $C_{s,i}$ approach are annotated in Table VI for FF implementations according to the results of Step f). The results for the *variable- $C_{s,l}$* approach are very similar to the ones obtained using the *variable- $C_{s,i}$* strategy for the operation modes of Table I, because in MR/MB and LR/HB modes the sampling capacitors of the integrators are limited by matching, as in the higher resolution HR/LB mode. More details on this will be given in next subsection.

A. Selection of the Reconfigurable $\Delta\Sigma$ Architecture for Transistor-Level Implementation

The *variable- $C_{s,l}$* approach is the best compromise between power efficiency and simplicity as shown in the comparison between Table V and Table VI. Indeed:

- Sizing all the sampling capacitors according to the targeted resolution generates optimal power values which are only slightly lower than those obtained with the *variable- $C_{s,l}$* approach. The difference is just 1 μ W in both MR/MB and LR/HB modes. As mentioned above, the $C_{s,i}$ in all the back-end integrators should ideally scale according to (7). However, as explained in Section III, the minimum size for $C_{s,i}$ is assumed in this work to be 50 fF to avoid that capacitor mismatch affects the $\Delta\Sigma$ performance. The values of $C_{s,i}$ in the *variable- $C_{s,i}$* approach are thus limited by matching to values close to the ones obtained under the *variable- $C_{s,l}$* strategy, and the *variable- $C_{s,i}$* approach allows only minimal power benefits in our case study.
- Implementing the *variable- $C_{s,i}$* approach would require additional circuit complexity. $4N$ capacitor arrays that are suitably switched for each ADC mode would be necessary. Indeed, 2 sampling capacitors and 2 integrating capacitors arrays must be used for each integrator in *variable- $C_{s,i}$* approach.
- Even if the minimum power for HR/LB mode is given by the FF combination ($N=2$, $B=5$, $OSR=64$), Fig. 5 shows that a power efficient scalable $\Delta\Sigma$ can be obtained also by choosing ($N=2$, $B=4$, $OSR=128$). For this choice, the values of the first sampling capacitor, the total power and FoM in HR/LB mode become $C_{s,l}=16$ pF, $P_{TOT}=11$ μ W, and $FoM=0.23$ pJ/conv.s., respectively. This means just a small power penalty with respect to the optimal solution. It is thus possible to avoid changing the resolution of

the quantizer between the different modes with a minor power penalty. This further simplifies the implementation of the *variable- $C_{s,1}$* approach as power efficiency can be guaranteed just by changing the *OSR* and the size of the first-integrator sampling capacitances for the different modes.

The final architectural choices and expected performances are listed in Table VII for the three operational modes mentioned above.

B. Comparison between the analytic model and transistor-level simulations

To validate the results obtained with the described analysis, a second order FF $\Delta\Sigma$ with a 4-bit quantizer has been designed and implemented at transistor-level in a standard 0.18 μm CMOS process, using a 1 V supply. To meet the required *BW* and resolution, the sampling frequency is tuned between 65 kHz and 1.05 MHz, implementing *OSRs* between 128 and 32. The size of the sampling capacitors in the first integrator is adjusted to implement reconfigurability according to the *variable- $C_{s,1}$* strategy. Fig. 7 illustrates the block diagram of the modulator, drawn as a single-ended circuit for simplicity (the actual implementation is fully differential).

Fig. 7. Simplified SC implementation of the reconfigurable $\Delta\Sigma$ M.

As a result of the design choices in the previous section, $C_{s,1}$ is tuned according to the targeted *ENOB* to minimize the equivalent load of the first integrator. The values of the in-loop coefficients have been here selected using the tool in [17] as $a_1=3$, $a_2=9/5$, $c_1=6/15$, $c_2=3/15$. They have being adjusted so that the integrators output range is 30% of the integrators reference voltage. This makes the design of the OTAs easier and less power-hungry as it relaxes the OTAs requirements in terms of output swing and slewing [6].

To validate the analytic power model and the reconfigurability approach, Fig. 8 compares the power breakdown for the theoretical model and for the post-layout extracted (PEX) simulations of the reconfigurable $\Delta\Sigma$ M in Fig. 7.

Fig. 8. Power consumption breakdown: comparison between theoretical model and transistor-level implementation in HR/LB, MR/MB and LR/HB modes.

The values of P_{STAT} in the practical implementation fit well the contributions predicted by the model. Small differences in MR/MB and LR/HB modes are related to the real implementation of the OTAs. Issues with the OTAs stability made indeed necessary to spend a little more power in the OTAs (P_{STAT}) than expected from the model. The dynamic power consumption in HR/LB mode is the same in the behavioral model and in simulation since the capacitances have been dimensioned following the procedure described in this paper. In MR/MB mode, P_{DYN} is slightly higher in PEX simulations due to the parasitic capacitance in the first integrator which is determined by the $C_{s,1}$ configuration switches. In LR/HB mode, the difference is even higher as the size of $C_{s,1}$ had to be increased with respect to the minimum bound provided by the model (see Table VII) due to constraints on the minimum unit capacitor in the employed technology. As mentioned above, $C_{s,1}$ coincides with the input DAC capacitor, which is here composed by 15 minimum size elements. The minimum capacitor size available in the CMOS 0.18- μm process is 36 fF, resulting in $C_{s,1} = 15 \cdot 36 fF \approx 0.5 pF$, which is indeed the value used in the simulations, but is higher than the value requested by the design methodology. The quantization power in the model is larger than that from PEX simulations. This is mostly due to the dynamic power for switching the SAR internal DAC. The SAR DAC considered in the model uses a binary-weighted capacitor array, while the SAR DAC implemented at transistor level is a segmented architecture with a central coupling capacitor to reduce the total capacitance. An analytic model of the implemented DAC could be used to better match the SAR power but this has not been done as the quantization power is a small part of the total power consumption. The values of P_{DWA} obtained in the real implementation are close to the theoretical estimation, as the model calculations have been updated to match the actual design. This power contribution is negligible in all the modes. We assumed in Section IV that the requirement on the matching of the DAC unit elements is satisfied by using a first-order DWA algorithm. The power result shows that we would even have room for a more complex DWA algorithm in the power budget. Contributions of the clock generator circuit and of the analog switches used for reconfiguring $C_{s,1}$ determine additional (but still negligible) power consumption in the simulated version.

Table VII summarizes the final $\Delta\Sigma M$ design choices and power performance. The

good agreement between the values of P_{TOT} obtained from the model and from PEX simulation confirms the validity of the presented methodology.

The maximum error is limited to roughly 17% (LR/HB mode) and is due to second-order effects in the transistor-level implementation (capacitive parasitics, trade-off between GBW and stability in the OTAs). The FoM is kept almost constant (between 0.15 and 0.21 pJ/conv.s.) over the whole conversion range confirming the validity of the chosen *variable- $C_{s,i}$* approach. The *variable- $C_{s,i}$* approach, which requires making all the capacitor switchable, would increase the problems related to the implementation of the reconfigurable $\Delta\Sigma$. Tuning the size of all the $C_{s,i}$ would indeed result in larger parasitic capacitances due to the configuration switches.

6. CONCLUSION

A structured methodology for the design of energy-efficient SC single-loop $\Delta\Sigma$ s has been presented. The proposed method finds, for the given resolution and bandwidth, the combination of filter order N , quantizer resolution B , oversampling ratio OSR and capacitor sizes that results in minimum power using an analytic model of the power consumption. To achieve this goal, the model of the static power contribution has been extended with respect to the previous work in [9]. The power-optimization procedure has addressed the design of reconfigurable $\Delta\Sigma$ s, scalable in resolution and bandwidth, for biomedical applications.

The *variable- $C_{s,i}$* approach offers the best compromise between power efficiency and simplicity as requires changing only the size of the first-integrator capacitors. A second-order feed-forward $\Delta\Sigma$ topology featuring a 4-bit SAR quantizer has been adopted. The reconfigurable $\Delta\Sigma$ has been implemented at transistor-level, featuring tunable sampling capacitors in the first integrator. The $\Delta\Sigma$ is configurable for 16 to 12 bits and 256Hz to 16kHz BW . $FoMs$ ranging from 0.15 to 0.21 pJ/conv.s. are obtained from simulations after parasitic extraction of the whole $\Delta\Sigma$. The simulated results validate the proposed design approach to reconfigurability and the analytic model proposed for the total power consumption. The comparison between power model and PEX simulations show differences of only 9%, 16% and 17% in HR/LB, MR/MB, and LR/HB, respectively.

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Table I. Specifications for Reconfigurability

ADC mode	ENOB	BW [Hz]	Target application
High resolution/ low BW (HR/LB)	16	256	EEG, ECG
Medium resolution and BW (MR/MB)	14	2048	EMG
Low resolution/ high BW (LR/HB)	12	16 k	Hearing-aids

Table II. Static Power Dissipation for Sinusoidal Inputs

OTAs	Normalized power dissipation
<i>Class-A</i>	$\hat{P}_A = \alpha\theta \cdot \left(\frac{k(t)}{2^B - 1} + \frac{1}{2} + \frac{OL}{2} \right) + \beta\zeta \cdot \left(\frac{5 \cdot 2\pi \cdot n \cdot V_{Th} \cdot C_{eq}}{V_{ref} \cdot C_s} \right)$
<i>Class-AB</i>	$\hat{P}_{AB} = \alpha\theta \cdot (2^B - 1) \cdot \frac{1}{T} \int_0^T \left[\frac{k(t)}{2^B - 1} - \left(\frac{1}{2} + \frac{OL}{2} \sin \omega t \right)^2 \right] dt + \beta\zeta \frac{10\pi \cdot n \cdot V_{Th} \cdot C_{eq}}{C_s \cdot V_{ref}}$

Table III. Coefficients for Various OTAs

Topology	α	β	θ	ζ
<i>Current-mirror</i>	$\frac{1+M}{M}$	$\frac{1+M}{M}$	$1+\gamma$	$1+\gamma$
<i>Folded-cascode</i>	2	2	$1+\gamma$	$1+\gamma$
<i>Castello</i> [20]	$\frac{1+M+F}{M}$	$\frac{1+M+F}{M}$	1	$1+\gamma$

Table IV. $\Delta\Sigma$ Power Contributions

P_{STAT}	<i>Class-A</i>	$P_{STAT-A} = V_{DD} \cdot (2BW \cdot OSR) \cdot V_{ref} \cdot \sum_{i=1}^N C_{s,i} \cdot \hat{P}_{A,i}$
	<i>Class-AB</i>	$P_{STAT-AB} = V_{DD} \cdot (2BW \cdot OSR) \cdot V_{ref} \cdot \sum_{i=1}^N C_{s,i} \cdot \hat{P}_{AB,i}$
P_{DYN}		$P_{DYN} = V_{ref}^2 \cdot C_{TOT} \cdot (2BW \cdot OSR)$
P_{QUANT}	<i>Single-bit comparator</i>	$P_{COMP} = \frac{V_{off}}{\eta} V_{DD} L_{min} (2BW \cdot OSR)$
	<i>Multi-bit Flash-ADC</i>	$P_{FLASH} = (2^B - 1) \cdot P_{COMP} + V_{DD}^2 (B+1) \cdot C_{in,ADC} \ln(2) \cdot (BW \cdot OSR)$
	<i>Multi-bit SAR-ADC</i>	$P_{SAR} = B \cdot P_{COMP} + 2V_{DD}^2 (2^B - 1) \cdot 1.5C_{SAR} (2BW \cdot OSR)$
P_{DWA}		$P_{DWA} = V_{DD}^2 \cdot C_{inv} (2BW \cdot OSR) \cdot \left[(2^B - 1)(B+1) + \sum_{n=0}^{B-1} (2^B - 2^n) + 8B \right]$

Table V. Power Optimal Solutions for Variable- $C_{s,i}$ Approach

	HR/LB	MR/MB	LR/HB
N	2	2	2
B	5	4	4
OSR	64	64	32
$C_{s,i}$ [pF]	28	2	0.2
P_{TOT} [μ W]	9.5	12	34
FoM [pJ/conv.s.]	0.2	0.13	0.18

Table VI. Power Optimal Solutions for Variable- $C_{s,i}$ Approach

	HR/LB	MR/MB	LR/HB
N	2	2	2
B	5	4	4
OSR	64	64	32
$C_{s,i}$ [pF]	28	2	0.2
P_{TOT} [μ W]	9.5	11	33
FoM [pJ/conv.s.]	0.2	0.12	0.17

Table VII. $\Delta\Sigma M$ Design and Performance Summary

	HR/LB		MR/MB		LR/HB	
	MODEL	PEX	MODEL	PEX	MODEL	PEX
N	2		2		2	
B	4		4		4	
OSR	128		64		32	
$C_{s,i}$ [pF]	16	16	2	2.1	0.2	0.5
P_{TOT} [μ W]	11	10	12	14	34	40
FoM [pJ/conv.s.]	0.23	0.21	0.12	0.15	0.18	0.21