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ASIVA14: Multi-Rate, MOR and Sensitivity in Circuit Simulation

Introduction

Faster and smaller electronic devices are more and more required by, e.g., the health care industry, the scientific research community and by the field of entertainment. There is a constant request to increase the simulation speed while keeping a high accuracy and reliability of the simulation. Here, we describe a number of important technical gaps that currently are being addressed within the ASIVA14 project (Analog SIMulation and Variability Analysis for 14nm designs).

Three targets: accelerating the transient simulation for general, VLSI complex circuits (s.a. ICs and Printed Circuit Boards (PCBs)) and for nearly-periodic circuits (s.a. Phase-Locked Loop (PLL), Switching Power Supply (SPSs)), and speeding up the analysis of the effects of variability and uncertainty (originating from manufacturing, parasitics, etc…).

The methodologies we are using, which can be also combined together, are: Multi-Rate, Model Order Reduction (MOR) to speed up the transient simulation, and Fast Adjoint techniques for the sensibility analysis (eventually, together with MOR for parametric models).

MOR methods

During the numerical integration, the most expensive routines are in solving a set of \( n \) linear equations in \( n \) variables (dimension of the Full Order Model (FOM)) for each Newton’s iteration, and in evaluating nonlinearities (for the Jacobian and the Right-Hand Side (RHS)). We apply the Proper Orthogonal Decomposition (POD) method, combined with the Discrete Empirical Interpolation Method (DEIM) [1]. The idea (originally from [3]) is to compute the solutions of the FOM at selected discrete time points, for a certain period of the transient (say, from \( t = 0 \) to \( t_{\text{TRAIN}} = 1/3 \) of the stopping time), then we employ a Singular Value Decomposition (SVD) on the collected solutions, choose the order of reduction \( r \) and the number \( m \) of DIEM points (related to the nonlinearities to be updated/evaluated), based on a user-specified accuracy of the dynamics (e.g., \( \text{tol}_{\text{POD-DEIM}} = 10^{-9} \)), and we use the Reduced Order Model (ROM) for the remaining transient period. Fig.21 plots the dynamic of a node’s potential. One can see that the accuracy (RelErr) is satisfactory, achieving a speedup of around 2.5.

Challenges: how to choose the training period (\( t_{\text{TRAIN}} \)) and how to dynamically check for the ROM’s accuracy; we need for a reliable time and space complexity analysis, since the ROM is characterized by having dense matrices; the SVD may be expensive for very large circuits: hierarchical partitioning of the whole circuit, for a sub-blocks (parallel) analysis; this methodology has to be tested on more complex circuits.

Multi-Rate methods

For circuits having signals with widely different time constants (e.g., PLLs and SPSs), usually fast transitions in the \( ns \) or \( ps \) range, and slow ones in the \( ms \), a huge number of time points are calculated during the simulation. It can take even weeks. These circuits are called nearly-periodic. Besides, the operation of the fast signals is highly non-linear, and crude linearization of the whole system is not “safe-enough” for most users. Multi-rate methods can be used, based on appropriately splitting time scales, using a large time-step for the slow-varying dynamics (envelope), saving computations.

Challenges: develop a method easily adaptable to existing circuit simulators, allowing a dynamic partitioning of the variables with different rate of variation; MOR techniques can be applied in this context also.

Variability Analysis

One of the biggest challenges in analog/mixed-signal IC design is uncertainty in electrical behavior and reliability. Existing solutions become too expensive due to an increasing demand for low-failure rates, augmented with even more reliability and variability problems. The research is focused on fast adjoint techniques to speed up the Monte Carlo runs, in order to analyze uncertainties in the output of the system with respect to different uncertainties in the input.

Challenges: fast adjoint methods; MOR techniques for parametric circuits (e.g., extracting the most dominant parameters for the evaluation process) [2].

References


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