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The full potential of scanning tunnelling microscopy (STM) and scanning tunnelling spectroscopy for in-situ characterization of organic semiconductors has so far not been accessible. Here, we demonstrate that the underlying problem, the low intrinsic conductivity, can be overcome by working in a field-effect geometry. We present high resolution surface topographies obtained by STM on pentacene organic field-effect transistors (OFETs). By virtue of the OFET geometry, the hole accumulation layer that is present at sufficiently negative gate bias acts as back contact, collecting the tunnelling current. The presence of a true tunnelling gap is established, as is the need for the presence of an accumulation layer. The tunnelling current vs. tip bias showed rectifying behaviour, which is rationalized in terms of the tip acting as a second gate on the unipolar semiconductor. An explanatory band diagram is presented. The measurements shown indicate that intrinsic organic semiconductors can be in-situ characterized with high spatial and energetic resolution in functional devices. © 2014 AIP Publishing LLC. [http://dx.doi.org/10.1063/1.4886155]

Scanning tunnelling microscopy (STM) has proven to be a powerful technique to characterise semiconductors with a resolution down to that of a single molecule, defect, or impurity level. STM not only provides the surface topography but also information is obtained about the local density of states by measuring the tunnelling current as a function of bias as in scanning tunneling spectroscopy (STS). The additional information on the energy levels makes STS the indicated technique to study organic semiconductors. They are typically disordered and the charge transport is due to hopping between the inherently localised states. STM and STS are preferably performed in-situ, i.e., in the actual device itself, allowing to directly relate the microscopic findings to the macroscopic material properties. In-situ measurements have the additional advantage that the measurements can be followed during device operation to examine, for instance, the device reliability or the potential distribution in the device. Charge transport in organic semiconductors is often investigated in organic field-effect transistors (OFETs), where the charge mobility is extracted as a function of the carrier density. STM and STS could deliver important microscopic information, such as the density of states, to unravel the semiconductor charge transport mechanism. In-situ STM measurements on organic semiconductors in transistors, however, have not been reported. The reason is that the bulk resistance of the intrinsic semiconductor is too high. Consequently, there is no tunnelling gap and the tip crashes on the surface of the semiconductor.

An in-situ STM measurement in an OFET is schematically depicted in Fig. 1. The conduction of charge carriers involves three steps: (1) tunnelling from the tip to the semiconductor, (2) transportation of the charges to the accumulation layer at the gate dielectric, and (3) conduction via the accumulation layer of the transistor to the source or drain contacts. The sample resistance, $R_s$, is the series resistance of the sample, $R_t$, is much lower than the tunnel resistance, $R_{tun}$. The applied tip bias, $V_{tip}$, then drops only over the tunnelling gap. When the sample resistance cannot be disregarded, the feedback system will decrease the tip height to reach the set tip current, $I_{set}$, but if the set current cannot be obtained the tip crashes. In other words, STM requires fulfilling the following condition:

$$V_{tip}/I_{set} = R_s + R_{tun} \gg R_t$$

FIG. 1. Schematic of an in-situ STM measurement on a field-effect transistor, with the applied biases indicated. The tip current has to cross the tunnel gap (1), reach the accumulation layer (2) and finally reach the contacts via the accumulation layer (3). Inset: chemical structure of pentacene.
paths 2 and 3. The resistivity of path 2 can be minimized by decreasing the thickness of the organic layer. When the gate is biased above the threshold voltage no charges are accumulated in the channel. For an intrinsic semiconductor, the channel resistance, path 3, then is prohibitively large. Equation (1) is not fulfilled, a tunnel gap cannot be formed and the tip crashes. Here, however, we demonstrate in-situ STM topography and spectroscopy measurements in a functional OFET. By adjusting the gate bias an accumulation layer is formed. The channel resistance decreases and the requirement Eq. (1) is fulfilled. A tunnel junction is formed and the current can be measured as a function of applied tip bias. We show that the rectifying current voltage characteristics obtained are a direct consequence of the tip acting as a dual gate on a unipolar semiconductor. An explanatory band diagram is presented.

Pentacene-based OFETs were prepared on a highly doped Si substrate, acting as bottom gate. A 200 nm thick thermally grown SiO₂ layer on top acts as a gate dielectric. Bottom source and drain Au/Ti (25 nm/5 nm) contacts were defined by standard I-line photolithography. The channel length, L, and width W, amounted to 5 μm and 1000 μm, respectively. Prior to pentacene deposition, the dielectric surface was treated with hexamethyldisilazane (HMDS) to reduce bias stress. Pentacene was evaporated at 150 °C in high vacuum (10⁻⁷ mbar) at 0.4 Å/s. The resulting pentacene layer has an average thickness of 25 nm and fully covered the substrate. The full coverage is needed to avoid tip crashes on the non-conducting SiO₂. STM measurements were performed with an Omicron SPM driven by a Nanonis controller in UHV (10⁻⁹ mbar), using a mechanically cut Pt/Ir-wire as tip. The STM measurement to study the tip crash (Fig. 3) was performed in ambient conditions using a Veeco Multimode with Nanoscope IIIA controller in STM mode. Electrical characterization of the transistors was done in-situ using a Keithley 2636 low-current source-measure unit.

A typical transfer curve, where the source-drain current is plotted as a function of gate bias is shown in Fig. 2(a). Forward and backward scans are superimposed; there is no hysteresis. The threshold voltage \( V_{th} \), taken as the onset of current flow, is around 0 V. The transistor shows unipolar p-type behaviour, where the current is enhanced at negative gate biases due to hole accumulation. At positive gate biases, the current is low since no electrons are accumulated. The extracted field-effect hole mobility is 0.3 cm²/V s.

STM images were obtained under bias conditions as shown in Fig. 1. The source and drain contacts were grounded, \( V_{SD} = 0 \) V, and a gate bias of \( V_G = -10 \) V was applied to assure the presence of an accumulation layer. The bias on the STM tip was set at \(-1\) V. STM images of the pentacene transistor with increasing spatial resolution are shown in Figs. 2(b)–2(d), respectively. In the large-scale image of Fig. 2(b), the source and drain electrodes are visible as the brighter parts on the left and right hand side. Stable images are obtained both on top of the electrodes and in the transistor channel. The morphology of the pentacene on top of the contacts and in the channel is clearly different. Grains formed on top of the electrode are smaller than the ones formed in the channel. We note that the morphology being a function of the type of surface underlines the need to perform in-situ measurements. Fig. 2(c) shows a zoom-in on the transistor channel. Terraces are clearly visible, which are typical for evaporated pentacene. The step height of 1.7 ± 0.2 nm corresponds to the c-axis lattice constant of a pentacene.

A further zoom-in of the top of a pentacene terrace is presented in Fig. 2(d). Remarkable circular features with a height of 0.5 ± 0.1 nm are observed on the terraces. Both the height and the monodisperse size distribution strongly suggest that these features are related to pentacene molecules lying flat on the surface. The absence of any visible elongation and the fact that the lateral feature size is larger than that of a single molecule can, in view of the overall good resolution, not easily be uniquely attributed to convolution with the STM tip. Likely, changes in the electronic structure surrounding the surface species determine their apparent shape. Importantly, the close to molecular resolution and the fact that the surface could be scanned multiple times without
noticeable changes shows that true tunnelling to the pentacene film is achieved in the OFET. We note that Gross et al. have imaged a pentacene molecule with sub-molecular resolution. However, in order to achieve that high resolution they required a well defined tip terminated with a CO molecule and an atomically flat metal substrate.

In order to demonstrate the crucial presence of an accumulation layer, we slowly increased the gate bias from accumulation at \(-15\) V to depletion at \(+6\) V while continuously scanning the tip. The STM images are presented in Fig. 3. As can be seen from the transfer curve in Fig. 2(a), the channel resistance increases with increasing gate bias. The tip crashes just before the threshold voltage, \(V_{th}\), of the transistor is reached. The channel resistance is then so large that the STM requirement of Eq. (1) is not any longer fulfilled. The impossibility to scan without the accumulation layer present shows that the charges are conducted via this layer. Charge transport via other possible pathways, for example, via the bulk due to possible unintended doping, is therefore ruled out.

STM not only provides the surface topography as shown in Fig. 2 but also information can be obtained about the local density of states by measuring the tunnelling current as a function of bias. The states probed in the scanning tunneling mode (STS) depend on the tip bias. When the Fermi level of tip, \(E_{F,t}\), is larger than the Fermi level of the pentacene top surface with negative tip biases, electrons from the tip can tunnel to empty states of the pentacene. When the Fermi level of the tip is lower than that of the top pentacene layer with positive tip biases, electrons from the filled pentacene states can tunnel to the tip. A first measurement is presented in Fig. 4. The tip bias was swept from \(-1.5\) V to \(+1.5\) V with the feedback loop disabled, i.e., the current was recorded at constant tip height. Interestingly, only current was observed at negative tip biases and not at positive tip biases. This rectifying behaviour is a direct consequence of the unipolarity of the pentacene transistor. The tip will effectively act as a local second gate, since it is a metal contact separated from the pentacene semiconductor by a vacuum gap. At negative tip biases, the electric field created by the tip attracts holes to the pentacene top surface, effectively accumulating locally extra holes. At positive tip biases, the electric field created by the tip cannot attract electrons to the pentacene top surface because the transistor is unipolar. Instead, holes shall be pushed away, even locally depleting the accumulation layer at the bottom gate SiO\(_2\) dielectric interface.

Band diagrams for the situation of negative and positive tip biases are presented in Figs. 5(a) and 5(b), respectively. The gate is biased negatively such that holes are accumulated in the channel and the resistance of path 3 is low. At a negative tip bias, holes are accumulated at the pentacene top surface near the tip due to the local gate effect. The holes will screen the electric field of the tip and therefore this electric field is mainly restricted to the vacuum gap. Electrons from the tip tunnel to the empty states in the highest occupied molecular orbital (HOMO) level at the pentacene top surface. In contrast, at positive tip bias, no electrons are attracted to the pentacene top surface due to the unipolarity of the transistor. The applied electric field is now distributed between the tip and the accumulation layer. As a result, only a small fraction of the tip bias falls over the tunnelling gap, since the semiconductor thickness (~25 nm) is much larger than the tunnel gap (<1 nm). The effective electric field falling over the vacuum gap is too low to get the tip Fermi level below the HOMO level of the semiconductor. As a result no electrons can tunnel from the filled HOMO to the tip.

We note that in metals the density of states can be extracted from the derivative of the tunnel current. However, this technique assumes a constant Fermi level. Here, the Fermi level is not constant due to the local gate effect of the tip. The position of the semiconductor Fermi level changes

![Graph](image)

**Fig. 4.** Scanning tunnelling spectroscopy in the transistor channel at a gate bias of \(-10\) V. The tip bias was swept from \(-1.5\) V to \(+1.5\) V, at constant tip height. Tunnelling current was observed for negative tip biases only.

![Diagram](image)

**Fig. 5.** Band diagram of the STS measurement experiment for (a) a negative tip bias and (b) a positive tip bias. In both cases, the bottom gate bias is biased negative, in accumulation, and the semiconductor is grounded, fixing the accumulation layer Fermi level, \(E_F\).
with respect to the semiconductor HOMO level, when holes are accumulated by the tip. Consequently, the density of states of the semiconductor in an OFET cannot directly be extracted from the tunnel current.

In conclusion, in-situ STM and STS measurements are performed on a functional OFET. As a semiconductor a 25 nm thick pentacene film was used. When the transistor is biased in depletion, the channel resistance is large and as a consequence the tip crashes. When the transistor is biased in accumulation, stable and high resolution STM images could be obtained. The tunnelling current measured as a function of tip bias showed a rectifying behaviour due the tip acting as a second gate on a unipolar semiconductor. An explanatory band diagram is presented. The STM and STS measurements presented indicate that intrinsic organic semiconductors can be characterized with high spatial and energetic resolution in-situ in functional devices.

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