On-chip antenna integration for single-chip millimeter-wave FMCW radars

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On-Chip Antenna Integration for Single-Chip Millimeter-Wave FMCW Radars

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Abstract— The feasibility of on-chip antennas for single-chip millimeter-wave FMCW radar has been investigated. The FMCW radar is configured to have one transmitting and two receiving monopole antennas. The performance of each antenna (matching, gain, isolation and surface wave suppression) is improved by adding a cavity backed wide slot on a PCB ground plane for each antenna, optimizing the PCB packaging environment, grinding the silicon substrate below 350 μm to reduce the substrate modes and optimizing the thickness of the environmental hazard protection globe top layer. Simulation results show that the on-chip antenna integrated on a 200 μm thick, 20 Ωcm silicon IC and mounted on an optimized PCB environment has more than 30% impedance bandwidth. In addition, the proposed approach suppresses surfaces waves, resulting in a relative high gain of 5 dBi with an overall efficiency of 41% at center frequency of 60 GHz. Furthermore, it meets the specific FMCW-radar requirements such as high isolation (more than 25 dB) between transmitting and receiving antennas and a ripple-free broadside radiation pattern.

Index Terms—millimeter wave, on-chip antenna, FMCW radar, printed circuit board (PCB)

I. INTRODUCTION

The millimeter-wave frequency bands assigned for radar applications and short-range wireless communications offer various advantages. For example, the 7 – 9 GHz bandwidth at 60 GHz provides high image resolution in radar applications. In addition, in this frequency band the effective wavelength is only a few millimeters and offers the possibility of integrating the antenna together with the front-end receiver and transmitter circuits in a single chip. This results in a low-cost solution and avoids interconnect losses [1]-[3]. Next to this, standard wire-bonding assembly and RF-testing can be applied during mass-production.

The preferred technologies for low-cost design, the standard main-stream silicon processes of CMOS and BiCMOS, are not ideal for antenna design. Because of the low resistivity and high dielectric constant of the silicon substrate the overall efficiency is low. For example, 200 μm silicon substrate with a dielectric constant of $\varepsilon_r=11.9$ and a resistivity of 20 Ωcm results in a best-case radiation efficiency of 50 % [4]-[5]. With the increase in thickness, both the Ohmic and surface-wave losses increase significantly, reducing the efficiency drastically. In order to reduce losses special measures have to be taken into account. Some of techniques reported in literature include the use of high-resistivity silicon, reducing the thickness by grinding below 350 μm [4], or post processing it. These techniques can improve the antenna performance, but at increased cost. In addition, on-chip antennas often radiate a lot of power towards the substrate which increases the back radiation [6]. This backward radiation can be used as the main lobe antenna pattern for some applications, but it is not suitable for many other applications. For example, in [2] the backward radiated power is the main lobe radiation pattern of the antenna.

In this paper, we present the design and optimization of efficient on-chip antennas and the in-package integration for millimeter-wave FMCW radar applications. We use the PCB environment of the package to improve matching, gain, efficiency and to suppress substrate modes that can exist in the lossy silicon substrate. Furthermore, we want to minimize the backradiated power, which is unwanted for our radar application.

In section II, we explain the FMCW radar antenna requirements and configuration. In section III, our antenna concept is presented including the use of the PCB and packaging environment to improve the antenna performance. In section IV, the obtained results are presented.

II. RADAR ANTENNA REQUIREMENTS

Radar transmitters and receivers can be designed and configured in various ways depending on their application. For applications that require angle-of-arrival measurements, there should be at least two receiving antennas. Typically, these antennas are separated by half a wavelength in order to avoid uncertainties in the angle-of-arrival determination. The radiation pattern of the antenna in the 3 dB beam width region should be ripple free, as ripple in the amplitude pattern results in a phase error signal which causes errors in the angle-of-arrival measurement. Furthermore, for FMCW radars, the isolation between the transmitting and receiving antennas should be high. Limited isolation makes it difficult to distinguish the reflected (wanted) signal from the (unwanted) coupled transmit signal [7]. In our application we require an isolation of more than 25 dB.

In Figure 1, the configuration of the on-chip radar antennas is shown. It consists of one transmitting (Tx) and two receiving antennas (Rx1 and Rx2), all integrated in a single silicon BiCMOS die. The center area of the silicon chip is used for the frontend electronic circuits. The two receiving antennas are placed half-wavelength apart. This configuration increases the isolation between the transmit and receiving antennas. Furthermore, the two receiving antennas are aligned for angle-of-arrival determination along the x-axis. The die is mounted on a PCB with a size of 7 mm by 7 mm and covered by a globe top layer to protect it from the environmental hazard. The final prototype of the complete single-chip radar with the three antennas is shown in Figure 2.
Fig. 1. Single-chip antenna configuration for FMCW radar application that includes angle of arrival measurement.

Fig. 2. Single-chip radar with three antennas integrated with the frontend circuit. The total size of the chip-package is 7 mm by 7 mm.

III. Antenna Design

In this section we will investigate the antenna design on the lossy silicon chip mounted on a PCB substrate. An optimized design of the PCB environment can improve the matching, suppress surface waves, reduces back radiation and improves the overall efficiency.

In our design, we used printed quarter-wave monopole antennas as shown in Figure 3. The three antennas are printed on the top metal layer of the back end of line (BEOL) process. The ground plane of the antenna in the simulation model is a sheet of metal as shown in the Figure 3. However, practically, it is impossible to manufacture it. Note that IC-manufacturing rules of CMOS and BiCMOS exclude the use of a fully metalized large ground plane. An equivalent ground plane on a chip to a sheet metal ground plane can be achieved: 1) by printing metal strips very close together; 2) using readily available dense metal interconnects of the front-end circuits. Use of the former requires additional silicon area, therefore, increases the cost. Use of the latter does not add any additional cost. Therefore, we used the second approach in our design and approximated it as a sheet of metal in our simulation model. This simplification reduces modelling complexity and, hence, significantly reduces simulation time.

In order to reduce the losses in the silicon special measures were taken in the design process, because the silicon with a dielectric constant of $\varepsilon_r=11.9$ and a resistivity of 20 $\Omega\cdot$cm resulting in high substrate losses. First of all, in order to avoid higher-order substrate modes, the silicon thickness should be grinded back to a thickness below 350 $\mu$m. If the silicon with a thickness less than 350 $\mu$m is mounted on a grounded PCB, only the TM$_0$ mode can exist. Further reduction in thickness reduces the TM$_0$ surface wave and ohmic losses. We were able to grind the thickness of the silicon back to 200 $\mu$m.

The radar chip is mounted on a PCB of 0.5 mm thick material with dielectric constant of 3.66 and loss tangent of 0.0037. The top of the PCB is a ground plane with three wide slots directly underneath each antenna, see Figure 4. Each slot is backed by a cavity with via walls around it. The depth of the cavity is approximately quarter wave length from the antenna. The mounted silicon die on the PCB is shown in Figure 5. The combined effect of the planar monopole antenna with the cavity backed wide slots increases the radiation efficiency, improves matching, isolation and significantly increases front-to-back ratio.

For standard wirebonding assembly of the chip with the PCB, a modification of the top ground plane on the PCB was required. The modified ground plane includes the low frequency interconnects to the external signal sources (power supply and control) and vias connecting the top ground plane to the backside ground plane in order to create a heat sink. Furthermore, the chip has an environmental hazard protection, globe top layer of thickness of 0.7 mm with dielectric constant of 3.7 and loss tangent of 0.012.
Fig. 5 Mounting the silicon die on the PCB. The three antennas are directly above the slots.

IV. RESULTS

In this section we present the simulation results of the on-chip antenna, modelled in the CST software tool [8]. We compare the results of the on-chip antenna with and without PCB environment in order to demonstrate that the optimization of the PCB environment improves the overall efficiency of the on-chip antenna. The antenna without the PCB is a quarter-wave monopole printed on a 200 μm silicon substrate as shown in Figure 3 without any additional structures. The antenna with PCB environment includes the monopole antenna printed on a 200 μm silicon, mounted on a PCB and with the addition of the globe top layer. The length of the monopole in both cases is quarter wavelength in terms of the effective wavelength; so the resulting physical length is not exactly the same in both cases. This adjustment was required to compensate for the effect the PCB environment.

Figure 6 shows the matching of the antenna with and without the PCB environment. Without the PCB, the antenna shows a poor matching. This was expected, since the monopole is not the same as a conventional monopole where the ground plane is perpendicular to the quarter wavelength pin. Using the PCB environment, the matching has been improved to a -10 dB impedance bandwidth of more than 30%. Figure 7 shows the mutual coupling between the transmitting and receiving antennas. In this case, we can also clearly observe that the mutual coupling is reduced by the supporting PCB environment, resulting in an isolation of more than 28 dB at 60 GHz. Figure 8(a) and 8(b) show the radiation pattern of the transmitting antenna in the E- and H-plane. The use of the PCB environment significantly increases the gain in the broadside direction along the z-axis. For example, at 0° the gain is improved by 10 dB. In addition, there is no radiation towards the back of the chip and the pattern is ripple free within the 3 dB beam-width region. The simulated radiation efficiency of the antenna is shown in Figure 9. The radiation efficiency of the antenna with the PCB environment is 41% at 60 GHz and 30% better as compared to the antenna without the PCB environment.

Fig. 6. Reflection coefficient of the monopole antennas with and without PCB environment.

Fig. 7. Mutual coupling between transmitting and receiving monopole antennas with and without PCB environment.

Fig. 8. Gain pattern of the monopole antenna with and without PCB environment; (a) E-plane (b) H-plane.
V. CONCLUSIONS

On-chip integration of multiple antennas for FMCW radar is feasible. Proper design of the supporting PCB environment significantly improves the performance of the on-chip monopole antennas. The simulation results show an impedance bandwidth of 33%, 5 dBi gain, 27 dB isolation between Tx and Rx and an efficiency of up to 41%.

REFERENCES

[8] https://www.cst.com/Products/CSTMWS