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Electronics for Cellular Neural Networks

by P.P.F.M. Bruin

Coach: dr. J.A. Hegt
Supervisor: prof.dr.ir. W.M.G. van Bokhoven
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Bruin, P.P.F.M.

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Abstract

In the design of Artificial Neural Networks a great deal of progress has been made. Some of the problems still remaining is the large number of connections needed between neurons and the large amount of memory needed to store weights. To solve these problems Cellular Neural Networks (CNNs) where proposed by Chua and Yang in 1988. All neurons, now called cells, are placed on a grid and communicate with their neighbours only. Furthermore the weights for all connections are the same per cell.

This report discusses the design of electronics for this form of networks. After analyzing several kinds of system structures and circuits in detail a design of a prototype cell is implemented on chip and tested.

An up to simulation working cell has been designed which can be used in CNNs. The chosen structure and the choice of subcircuits combines to a circuit that has all the properties needed to function as a CNN cell and in the layout several measures have been taken to be able to compile a CNN from the cell easily.

Measurements on the chip proved successfull up to the dynamic behaviour. It showed that the cell's inner loop was not stable and the problems remains to be solved in a future design.
Chapter 1: Introduction

While more and more digital computers are used to solve problems nowadays, the human brain still remains superior in some fields. They are capable of dealing with incomplete and inconsistent data, less sensitive to errors in data or the system itself, capable of learning, and they make use of massive parallelism to process huge amounts of data.

Since the end of the 40's researchers, with the aid of the long but extensive knowledge of biologic neural networks, try to implement artificial neural networks, that should have the same properties. This research has led to structures, resembling more or less biologic neural networks, that indeed show the above mentioned properties.

Two problems coming up in artificial neural networks are the large number of communication lines between cells, that has to be realized and the memory needed to store the weights belonging to these lines. That is why in 1988 cellular neural networks were proposed. In these networks cells only communicate with their nearest neighbour cells and the weights belonging to communication lines between cells can be the same for every cell. Therefore much less communication line and much less memory is needed.

During the project integrated electronics have been designed that can be used in cellular neural networks. Areas of interest were chip area, power dissipation, speed, and sensitivity to errors during fabrication. The result is a design which has been realized on an integrated circuit which has been tested.
Chapter 2: Cellular neural networks

2.1 Basics

2.1.1 Definition

Basically Cellular Neural Networks (CNNs) consist of cells $C(i,j)$ organized in a regular grid of dimension $n$, where $n$ is normally 2. This grid is mostly square or sometimes hexagonal, but also other varieties are possible. For each cell on a 2 dimensional $MxN$ square grid an $r$-neighbourhood $N_r(i,j)$ is defined according to formula (2.1).

$$N_r(i,j) = \{C(k,l) | \max\{|k-i|,|l-j|\} \leq r; 1 \leq k \leq M; 1 \leq l \leq N\} \quad (2.1)$$

All cells in the CNN communicate with cells belonging to their neighbourhood only. Figure 2.1 shows a $4x4$ grid of cells with a 1-neighbourhood of cell $2,2$ marked in grey.

![figure 2.1: A 4x4 CNN with 1-neighbourhood of 2,2 marked in grey](image)

Individual cells are multiple input single output dynamical systems. Their output $y(t)$ is defined by the input $u(t)$, the state $x(t)$ an offset $i(t)$, a feedback operator $A(t)$ and a control operator $B(t)$ according to formulas (2.2) and (2.3).
\[
\Delta x^c(t) = g[x^c(t)] + \sum_{d \in N_c(c)} d_d[c(y^d(t);\tau) + \sum_{d \in N_c(c)} b_d[u^d(t);\tau]] + i^c(t)
\] (2.2)

\(x^c(t)\) is the state of cell \(c\) in time and \(d_d\) is the feedback operator from cell \(d\) to cell \(c\). Both operators are calculated from all values of \(y^d(t)\) and \(u^d(t)\) between \(t-\tau\) and \(t\). \(\Delta\) stands for a differential operator.

The output \(y^c(t)\) is calculated from the state \(x^c(t)\) according to a nonlinear saturation function as in formula (2.3).

\[
y^c(t) = f[x^c(t);\tau]
\] (2.3)

Within this definition of CNNs many different varieties have been proposed in which all kinds of constraints have been put on the parameters presented in this section. A review of some kinds of CNNs can be found in [Cim93].

### 2.1.2 Linear Cloning Template CNN

In section 2.1.1 a general definition for CNNs has been given. When Chua and Yang [Chu88a] proposed CNNs in 1988 they were thinking of a structure called Linear Cloning Template CNNs (LCT-CNNs). In these networks the control and feedback operators are continuous in time and they are the same for all cells, furthermore all signal are continuous in time. Formula (2.2) then becomes formula (2.4).

\[
\frac{dx^c(t)}{dt} = -x^c(t) + \sum_{d \in N_c(c)} A_d y^d(t) + \sum_{d \in N_c(c)} B_d u^d(t) + I^c
\] (2.4)

Furthermore \(f(x^c(t))\) is a piece wise linear saturation function according to formula (2.5).

\[
y^c(t) = f(x^c(t)) = \frac{1}{2}(x^c(t) + 1) - |x^c(t) - 1|
\] (2.5)

Graphically this saturation function is shown in figure 2.2.
In their article [Chu88a] Chua and Yang have proved some important properties belonging to LCT-CNNs. First of all these networks will be stable when constraints (2.6) are met.

\[
\begin{align*}
|x^c(0)| &\leq 1 \\
|u^c(t)| &\leq 1 \\
A_c^c &> 1 \\
A_d^c & = A_c^d
\end{align*}
\] (2.6)

Furthermore they have shown that in this case the final output values for all cells will be binary as in formula (2.7). This makes it easy to process outputs from CNNs.

\[
y(\infty) \in \{-1, 1\}
\] (2.7)

The last important property for LCT-CNNs is that the value of the state variable \(x^c(t)\) is limited according to formula (2.8). This is important for electronic implementation of CNNs because electronic signal values in electronic circuits are also limited due to for example the supply voltage.

\[
|x^c(t)| \leq 1 + \sum_{d \in N(C)} |A_d^c| + \sum_{d \in N(C)} |B_d^c| + |I|
\] (2.8)

For this kind of CNN Chua and Yang also proposed an electronic circuit implementation of which the structure is very easy. It consists of a capacitor for the dynamic element, a resistor to implement the therm \(-x^c(t)\) and voltage controlled current sources (VCCSs) for the control and feedback operators \(A\) and \(B\) and the offset \(I\). This circuit can be found in figure 2.3.
The gains of the VCCSs are according to formulas (2.9).

\[
\begin{align*}
I_{xy,c,d} &= A_d^c v_{y,d} \\
I_{sx,c,d} &= B_d^c v_{u,d} \\
I_c &= i^c \\
I_{y,c} &= \frac{1}{2R_x} (|v_{x,c} + 1| - |v_{x,c} - 1|) 
\end{align*}
\]  

This means that the dynamic state equation now becomes formula (2.10).

\[
R_x C \frac{dv_{x,c}(t)}{dt} = -v_{x,c}(t) + R_x \sum_{d \in N_j(c)} A_d^c v_{y,d}(t) + R_x \sum_{d \in N_j(c)} B_d^c v_{u,d}(t) + R_x i_c 
\]  

This is apart from the factors \( R_x C \) and \( R_x \) the same formula as formula (2.4) and thus a correct electronic implementation of a CNN is given. With this structure only efficient (VLSI) implementations for VCCSs and \( R_x \) have to be found to complete the CNN design.
2.1.3 Applications

After the definition and the structure of CNNs this section will treat some of the application possibilities of CNNs. The type of action performed by a CNN depends on the elements of the feedback and control operators $A$ and $B$ and the offset $l$. The data input to a network can be supplied through the normal inputs $u$ and through the initial states $x(0)$ of each cell.

Since the introduction many possible applications have been proposed which can be found mainly in three areas: image processing, simulation of physical systems, and associative memories. Especially the field of image processing has found many applications which can be performed by CNNs, because of the two-dimensional structure and the local interaction between cells, two properties of many image processing algorithms. Some examples are: noise removal, hole filling, corner and edge detection, shadowing, line detection, thinning, peeling, shadowing, and connected component detection (CCD). The last one will explained in more detail.

The aim of connected component detection is to find connected components, essentially pixels with the same colour. Starting with an image of black and white pixels, the result of CCD will be a picture with alternating black and white pixels for every black and white connected component found. For horizontal CCD the cloning templates are according to formula (2.11)

$$A = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 2 & -1 \\ 0 & 0 & 0 \end{bmatrix}; B = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}; I = 0 \quad (2.11)$$

In this case the $B$ matrix is empty, and thus this is an example in which the input pattern is formed by the initial states in the network. In figure 2.4 an example of an input pattern and the resulting output pattern is given.

![Input and output pattern](image-url)

Figure 2.4: Example input and resulting output pattern for horizontal CCD
The result of CCD is that all connected components in the '9' are shifted right and reduced to one pixel of the corresponding colour each. More lists of applications, mostly image processing, and worked out examples can be found in [Chu88b], [XX], and [Bon93]. Some work on physical systems simulation and associative memories can be found in [Fer91] and [Tan90].

2.2 Full range approach

One of the disadvantages of the LCT-CNN described in section 2.1.2 is the fact that the state variable $x^c(t)$, although limited, can reach much larger values than the output $y^c(t)$ depending on the values of the control and feedback operators. For the electronic implementation proposed in the same section this means that the dynamic range of $y^c$ can be far less than the dynamic range of $x^c$. To overcome this problem Rodriguez-Vazquez et al. [Rod93] proposed a slightly different approach called the full range approach. They altered the dynamic state equation of formulas (2.4) and (2.5) into formulas (2.12) and (2.13).

\[
\frac{dx^c(t)}{dt} = -g(x^c(t)) + \sum_{d \in N_c} A_d y^d(t) + \sum_{d \in N_c} B_d u^d(t) + I^c
\]  
(2.12)

\[
g(x^c(t)) = \begin{cases}  
-\left[\left(x^c(t) + 1\right) + 1 \right] & \text{if } x^c(t) < -1 \\
-x^c(t) & \text{otherwise} \\
-\left[\left(x^c(t) - 1\right) - 1 \right] & \text{if } x^c(t) > 1
\end{cases}
\]  
(2.13)

In this case $g(x^c(t))$ ensures that the state $x^c$ will always have a value between its boundaries -1 and 1. Therefore also no need for a nonlinear saturation function exists, which could imply that less hardware is needed to implement the cell.

2.3 Feedback loop approach

In 1992 Nossek et al. proposed a basic electronic implementation for CNNs consisting of an opamp with a feedback as the core of a cell [Nos92]. They make use of the fact that the state of a cell is bounded (see formula (2.8)). When the states are scaled to make sure that they remain within the saturation voltage of an ideal opamp $V_{sat}$ and $V_{sat}^+$, this opamp, together with a resistor and a capacitor to form a lossy integrator, could be used to hold the state voltage. The original and resulting circuit can be found in figure 2.5.
All parameters in these circuits marked by an overbar have been modified to ensure that the state voltage \( \overline{V}_{x,c} \) does not exceed the saturation voltage of the opamp. The rightmost circuit in figure 2.5 holds two major advantages over the left one. Firstly all incoming currents \( S \) are no longer injected to a node with varying potential, but they are drawn from a virtual ground node. This means that instead of VCCSs resistors can be used. Secondly the voltage \( \overline{V}_{x,c} \) is maintained regardless of the load current \( I_{load} \). To complete the cell two more opamps can be used to form the nonlinear saturation function \( f(x) \) as shown in figure 2.6.

Figure 2.6: Cell circuit with feedback loop and nonlinear saturation function
In figure 2.6 the factor $\bar{r}$ is added to compensate for the modifications in $C$ and $G_x$. Furthermore both $-v_{yc}$ and $+v_{yc}$ are needed to be able to realize both positive and negative template elements with just resistances. So, concluding, a cell can be realized with three opamps, a capacitor and some resistances.

Further improvement from this can be accomplished by using balanced signals and opamps. In this case only one opamp is needed to form the nonlinear saturation function and the conductances used within the cell and for the interconnections between cells can be formed by simple CMOS circuits. The circuit with balanced opamps and signals can be found in figure 2.7.

In this circuit programmability is introduced by using variable conductances. These conductances could be implemented in CMOS by some kind of 4-quadrant multiplier circuit, which will be treated in more detail in chapter 3. The nodes $I_{nc,-}$ and $I_{nc,+}$ are the equivalent of the input node in figure 2.6 and are used to sum all incoming currents from the neighbouring cells. For the interconnection of cells again variable conductances can be used.

2.4 Fullrange CNN with feedback loop and 2-quadrant multipliers

In this section the ideas of sections 2.2 and 2.3 will be combined with the fact that unipolar signals can be used to get to the structure of the CNN cell which is going to be implemented. In 1994 Perfetti published an article [Per94] in which he more or less combines the ideas of Rodriguez-Vazquez and Nossek. He uses the electronic implementation with a feedback loop and the full range approach to save the opamp(s) needed for the saturation function. The state voltage $v_{xc}$ will be confined between $V_{sat-}$ and $V_{sat+}$ of the opamp. With balanced signals this would result in the circuit of figure 2.8.
Furthermore Van Engelen [Eng95] showed that it is possible to scale all template elements, the saturation function and the offset in such a way that all output and input signals from and to cells will be unipolar. This would mean that normal opamps can be used and 2-quadrant multipliers instead of 4-quadrant ones. These two things would mean reduction of the hardware needed. Chapter 4 will treat different possibilities to implement this structure.
Chapter 3: Analog MOS multipliers

3.1 Introduction

Multipliers, the most numerous building blocks used in Artificial Neural Networks (ANNs), are also used in large numbers in CNNs. Because they consume large portions of chip area and power consumption and greatly influence the further design of a neural network implementation, the selection of appropriate multipliers is significant in both ANN and CNN design.

Of the many possible topologies for analog MOS multipliers, the most relevant designs have voltage inputs and current outputs (because the output signals of many multipliers have to be added and a neuron's or cell's output has to be connected to many multiplier inputs) and have been designed more for simplicity than for accuracy (because neural nets can deal with inaccuracies). Six potentially suitable multiplier designs are compared here in terms of chip area, power dissipation, input and output impedance, and linearity.

3.2 Multipliers

Chip area, the first topic, has been estimated by counting the number of transistors. This is better than multiplying widths and lengths of all transistors and adding them up, because the borders around transistors are quite large.

Power dissipation will be related to the ratio of the maximum total current in the circuit and the maximum signal current (or current difference) at the output, that has been obtained by simulations with HSpice. To simulate the multipliers under conditions approximating their use and to make a fair comparison, these simulations were done for input ranges of 1V and output ranges of 1mA. This means that all transistors have been sized to get the right transconductance of 1μA/V and that only PMOS transistors were used because of their smaller transconductance parameter.

Input and output impedances have not been calculated exactly but a qualitative measure will be given according to which pins of a transistor are used, in what mode the transistor is, and what its size is.

Finally linearity has been measured with the aid of the characteristics obtained by the HSpice simulations. These characteristics' starting and ending points have been connected by a straight line and the maximum relative deviation from this line will be used as a measure for linearity. Whenever this deviation is only positive or only negative, the number has been divided by two.

-16-
3.2.1 Two transistor multiplier

The two transistor multiplier is shown in figure 3.1.

\[ I_+ = \beta \left( V_{in2+} - V_{in1} - V_T (V_{out} - V_{in1}) - \frac{1}{2} (V_{out} - V_{in1})^2 \right) \]  
\[ (3.1) \]

\[ I_- = \beta \left( V_{in2+} - V_{in1} - V_T (V_{out} - V_{in1}) - \frac{1}{2} (V_{out} - V_{in1})^2 \right) \]  
\[ (3.2) \]

\[ I_+ - I_- = \beta (V_{in2+} - V_{in2-}) (V_{in1} - V_{out}) \]  
\[ (3.3) \]

Advantages:

- Only two transistors are needed which means little area.
- One input has a high impedance.
- One input is single ended.
- The linearity of this circuit is good.
Disadvantages:

- Long transistors \((W/L = 4.8\mu m/48\mu m)\) are needed to get a transconductance of \(1\mu \Omega^{-1}\) which increases chip area.

- Also both output voltages have to be kept constant regardless of the output currents. To do this, current conveyors are needed, which will increase chip area too.

- Furthermore these conveyors can only be implemented reasonably easily when currents are flowing in one direction only, which means that the multiplier can only be used in two quadrants. This is not a real problem for CNNs however.

- Power dissipation is quite high.

- One input has a low impedance.

- The output has a low impedance.

- One input is differential.

- The output is differential.

With the two transistor multiplier one can trade area for power dissipation and dynamic range. With longer transistors and smaller input ranges currents will decrease.

Furthermore, because \(V_{sb}\) is varying, this multiplier suffers from the bulk effect which decreases its linearity. This can be improved by increasing the mean value of \(V_{gs}\) which however increases power consumption as well. Another possibility is to have \(V_{out}\) higher than \(V_{in}\) thus making \(V_{out}\) the source voltage which is now constant. This improves the multiplier's linearity significantly, but a disadvantage of this configuration is that \(V_{out}\) will be closer to the supply voltage, making it harder to implement a current conveyor.
3.2.2 Four transistor multiplier

Figure 3.2 presents the four transistor multiplier.

Again all transistors are equal and working in linear range:

\[
I_+ = \beta \left\{ (V_{in2} - V_{in1} + V_T)(V_{out} - V_{in1} + ) - \frac{1}{2} (V_{out} - V_{in1} + )^2 + \right. \\
\left. (V_{in2} + V_{in1} - V_T)(V_{out} - V_{in1} - ) - \frac{1}{2} (V_{out} - V_{in1} - )^2 \right\} 
\]

(3.4)

\[
I_- = \beta \left\{ (V_{in2} + V_{in1} - V_T)(V_{out} - V_{in1} + ) - \frac{1}{2} (V_{out} - V_{in1} + )^2 + \right. \\
\left. (V_{in2} - V_{in1} - V_T)(V_{out} - V_{in1} - ) - \frac{1}{2} (V_{out} - V_{in1} - )^2 \right\} 
\]

(3.5)

\[
I_+ - I_- = \beta (V_{in2} - V_{in1} - V_{out}) + (V_{in2} + V_{in1} - V_{out}) + (V_{in1} + V_{in1} - V_{out}) \\
= \beta (V_{in2} - V_{in2} - ) (V_{in1} + V_{in1} - ) 
\]

(3.6)
Advantages:

- The output voltages do not have to remain constant but just equal, so no current conveyors are needed.

- This means that both output currents can be bidirectional without causing great problems and thus four quadrants can be used. Moreover the second differential input $V_{in}$ makes four quadrants usable anyway.

- It also means that power dissipation can be no higher than with the two transistor multiplier, regardless of the fact that two more transistors are needed. This is because $V_{in}$ is differential, so in order to have an input range for $V_{in+} - V_{in-}$ of 1V both inputs need only have a swing of 0.5V. This decreases the currents through all transistors without decreasing the resulting current difference at the output.

- One input has a high impedance.

- The linearity of this circuit is very good.

Disadvantages:

- The output voltages have to be kept equal. Although this is more easy than keeping them constant as with the two transistor multiplier, at least something like an opamp is needed.

- Long transistors are needed to get a transconductance of $1\mu\Omega^{-1}$

- Power dissipation is quite high.

- Input $V_{in1}$ has a low impedance.

- The output has a low impedance.

- All inputs and outputs are differential.

With the four transistor multiplier it is only possible to get rid of the bulk effect by sacrificing the major advantage over the two transistor multiplier, being the fact that $V_{out}$ does not have to be fixed. Therefore it is probably no better except when the two differential inputs or four quadrant operation are explicitly needed.
3.2.3 Differential pair multiplier

Figure 3.3 shows the differential pair multiplier.

When all transistors are in saturation and the Early effect is disregarded the following formulas hold:

\[ I = \frac{1}{2} \beta (V_{in1} - V_{dd} - V_T)^2 \]  
\[ I_+ = \frac{1}{2} \beta (V_{in2-} - V_T - V_Y)^2 \]  
\[ I_- = \frac{1}{2} \beta (V_{in2+} - V_T - V_Y)^2 \]

(3.7), (3.8), and (3.9) are combined to get \( V_T + V_Y \):

\[ I_+ + I_- = I \Rightarrow \]

\[ V_Y + V_T = \frac{1}{2} (V_{in2+} - V_{in2-}) + \frac{1}{2} \sqrt{\frac{B_1}{B_2}} (V_{in1} - V_{dd} - V_T)^2 - (V_{in2+} - V_{in2-})^2 \]

With this we can calculate the output signal:

\[ I_+ - I_- = \frac{1}{2} \beta_2 (V_{in2+} - V_{in2-}) \sqrt{\frac{B_1}{B_2}} (V_{in1} - V_{dd} - V_T)^2 - (V_{in2+} - V_{in2-})^2 \]
\[ I_+ - I_- = -\sqrt{\frac{\beta_1 \beta_2}{2}} (V_{in2+} - V_{in2-})(V_{in1} - V_{dd} - V_T) \]

when \[ 2\frac{\beta_1}{\beta_2} (V_{in1} - V_{dd} - V_T)^2 > (V_{in2+} - V_{in2-})^2 \]

Advantages:

- This multiplier only needs three transistors.
- Power dissipation is fairly low.
- It has two high impedance inputs.
- The output has a high impedance.
- One input is single ended.

Disadvantages:

- Long transistors are needed to keep the tail current low (± 3μA) for input ranges of 1V.
- This multiplier operates in two quadrants only.
- One input is differential.
- The output is differential.
- '0' is not reachable for input \( V_{in} \).
- Linearity decreases when \( V_{in2+} - V_{in2-} \) increases.

This multiplier's characteristics rapidly decrease, when the tail current is made very low. That is why a real '0' is impossible for input \( V_{in1} \).

Furthermore \( \beta_1 \) and \( \beta_2 \) should be the same to keep both input ranges equally large.

When using a supply voltage of 5V it becomes hard to fit two input ranges of 1V into it, while keeping all transistors working in saturation. There is no room for shifting these ranges a bit, which could hamper the design of surrounding circuitry.
3.2.4 Double differential pair multiplier

With a second differential pair multiplier the circuit of figure 3.4 results.

To calculate the current difference at the output, formula (3.11) can be used:

\[
I_+ - I_- = \frac{1}{2} \beta_2 (V_{in2+} - V_{in2-}) \left\{ \sqrt{ \frac{2 \beta_1}{\beta_2} (V_{in1+} - V_{dd} - V_T)^2 - (V_{in2+} - V_{in2-})^2} - \right. \\
\left. \sqrt{ \frac{2 \beta_1}{\beta_2} (V_{in1+} - V_{dd} - V_T)^2 - (V_{in2+} - V_{in2-})^2} \right\}
\]

(3.13)

\[
\Rightarrow I_+ - I_- \approx \sqrt{ \frac{\beta_1 \beta_2}{2} (V_{in2+} - V_{in2-}) (V_{in1+} - V_{in1-})}
\]

(3.14)
Advantages:

- Four quadrants can be used.
- It has two high impedance inputs.
- The output's impedance is high.
- Linearity is quite good.

Disadvantages:

- This circuit needs six transistors.
- Long transistors are needed to keep the total tail current low (± 5μA) for input ranges of 1V.
- Power dissipation is a bit high.
- Both inputs are differential.
- The output is differential.
- Linearity decreases when $V_{in2} - V_{in1}$ increases.

When comparing the double differential pair multiplier with a single one, the result would be that linearity has improved while power dissipation and area have increased. Furthermore four quadrant operation is possible with this multiplier and $V_{in1}$ can be '0' again. Regarding the ranges one can state exactly the same as for the single differential pair.
3.2.5 Gilbert multiplier

The Gilbert multiplier is almost the same as the one in the previous section except for an extra current source, as in figure 3.5.

From (3.8), (3.9), and (3.10) we can calculate $I_1$ and $I_2$:

$$I_1 = \frac{1}{2} \beta_1 \left( \frac{1}{2} (V_{in1} + - V_{in1} -) - \frac{1}{2} \frac{4I}{\beta_1} - (V_{in1} + - V_{in1} -)^2 \right)$$  \hspace{1cm} (3.15)

$$I_2 = \frac{1}{2} \beta_1 \left( \frac{1}{2} (V_{in1} - - V_{in1} +) - \frac{1}{2} \frac{4I}{\beta_1} - (V_{in1} + - V_{in1} -)^2 \right)$$  \hspace{1cm} (3.16)
From (3.11) and (3.16) follows:

\[
I_+ - I_- = \frac{1}{2} \beta_2 \left( (V_{in2_-} - V_{in2_+}) \cdot \sqrt{\frac{4I_2}{\beta_2}} - (V_{in2_-} - V_{in2_+}) \right)^2 \\
+ \frac{1}{2} \beta_2 \left( (V_{in2_-} - V_{in2_-}) \cdot \sqrt{\frac{4I_1}{\beta_2}} - (V_{in2_-} - V_{in2_-}) \right)^2
\]

\[
\approx \frac{1}{2} \beta_2 \left( (V_{in2_-} - V_{in2_+}) \cdot \sqrt{\frac{4I_2}{\beta_2}} + (V_{in2_-} - V_{in2_-}) \cdot \sqrt{\frac{4I_1}{\beta_2}} \right)
\]

\[
\Rightarrow I_+ - I_- \approx \sqrt{\frac{\beta_1 \beta_2}{2}} (V_{in2_+} - V_{in2_-})(V_{in1_+} - V_{in1_-})
\] (3.17) (3.18)

Advantages

- Four quadrants can be used.
- Power dissipation can be very low.
- It has two high impedance inputs.
- The output's impedance is high.
- Linearity is very good.

Disadvantages:

- This circuit needs seven transistors
- Long transistors are needed to get a transconductance of $1 \mu\Omega^{-1}$
- Both inputs are differential.
- The output is differential.

Although formula (3.18) yields the same result as for the double differential pair multiplier, the Gilbert multiplier's performance is much better in terms of linearity and especially power dissipation. However a problem may arise using the Gilbert multiplier with low supply voltages, due to stacking of threshold voltages.
3.2.6 Saxena multiplier

The multiplier proposed by Saxena is based on formula (3.19).

\[(x + y)^2 - x^2 - y^2 = 2xy\]  

(3.19)

To realize this, one can use the quadratic relation between \(V_{gs}\) and \(I_d\) for a transistor in saturation. This is done by the circuitry in figure 3.6.

\[I_1 = \frac{1}{2} \beta (V_{in1} - V_{dd} - V_T)^2\]
\[I_2 = \frac{1}{2} \beta (V_{in2} - V_{dd} - V_T)^2\]
\[I_3 = \frac{1}{2} \beta (V_{in1} + V_{in2} - V_{dd} - V_T)^2\]
\[I_4 = \frac{1}{2} \beta (- V_{dd} - V_T)^2\]

(3.20)

\[\Rightarrow I_{out} = I_1 + I_2 - I_3 - I_4\]
\[= \beta V_{in1} V_{in2}\]
Advantages:

- Four quadrants can be used.
- The output's impedance is high.
- Inputs are single ended.
- The output is single ended.
- Linearity is very good.

Disadvantages:

- Even when some current mirrors would be shared by more than one multiplier, this circuit needs at least eight transistors.
- Because the threshold voltages of all five PMOS transistors should be equal, this circuit is very sensitive to the bulk effect. Therefore three N-wells are needed to keep $V_{sb}$ equal to $DV_{th}$ for all transistors and this takes a lot of chip area.
- Power dissipation is high.
- One input has a low impedance.
- It is hard to make this circuit work correctly with a supply voltage of 5V.

When using this multiplier one should take care that all transistors are in saturation. Therefore the ranges of $V_{in1}$ and $V_{in2}$ are more or less fixed. With a supply voltage of 5V this means ranges from -0.3V to 0.3V.

Furthermore this circuit was the only one which showed an easily perceptible offset in both inputs even during simulation with perfectly matched transistors. However this is due to the fact that the current mirrors suffer from the Early effect so the other multipliers will show the same offsets when these basic current mirrors are going to be used.
3.3 Summary and conclusions

After describing all multipliers in detail and summing up their particular advantages and disadvantages, this section will present a survey of simulation results and from this conclusions will be drawn. Table 3.1 sums up all results and gives some qualitative properties for all circuits.

Table 3.1: Survey of multiplier properties

<table>
<thead>
<tr>
<th>Kind of multiplier</th>
<th>$V_{in1}$ (V)</th>
<th>$V_{in2}$ (V)</th>
<th>#T</th>
<th>$\frac{W}{L}$ ((\mu\m))</th>
<th>quad</th>
<th>$\frac{s}{b}$</th>
<th>$Z_{in}$</th>
<th>$Z_{out}$</th>
<th>in</th>
<th>out</th>
<th>lin (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Two transistor multiplier</td>
<td>3.5 .. 4.5</td>
<td>1 .. 2</td>
<td>2</td>
<td>$48$</td>
<td>2</td>
<td>$\frac{1}{32}$</td>
<td>-</td>
<td>+</td>
<td>s,d</td>
<td>d</td>
<td>8.5</td>
</tr>
<tr>
<td></td>
<td>3.5 .. 4.5</td>
<td>0.5 .. 1.5</td>
<td>2</td>
<td>$48$</td>
<td>2</td>
<td>$\frac{1}{32}$</td>
<td>-</td>
<td>+</td>
<td>s,d</td>
<td>d</td>
<td>4.3</td>
</tr>
<tr>
<td></td>
<td>4 .. 5</td>
<td>0.5 .. 1.5</td>
<td>2</td>
<td>$48$</td>
<td>2</td>
<td>$\frac{1}{32}$</td>
<td>-</td>
<td>+</td>
<td>s,d</td>
<td>d</td>
<td>1.6</td>
</tr>
<tr>
<td>With $V_{sb}$ constant ...</td>
<td>3.5 .. 4.5</td>
<td>1.5 .. 2.5</td>
<td>2</td>
<td>$48$</td>
<td>2</td>
<td>$\frac{1}{32}$</td>
<td>-</td>
<td>+</td>
<td>d,d</td>
<td>d</td>
<td>10.4</td>
</tr>
<tr>
<td></td>
<td>3.5 .. 4.5</td>
<td>1 .. 2</td>
<td>2</td>
<td>$48$</td>
<td>2</td>
<td>$\frac{1}{32}$</td>
<td>-</td>
<td>+</td>
<td>d,d</td>
<td>d</td>
<td>3.8</td>
</tr>
<tr>
<td>Four transistor multiplier</td>
<td>3.5 .. 4.5</td>
<td>1.5 .. 2.5</td>
<td>4</td>
<td>$48$</td>
<td>4</td>
<td>$\frac{1}{32}$</td>
<td>-</td>
<td>-</td>
<td>d,d</td>
<td>d</td>
<td>3.6</td>
</tr>
<tr>
<td>Differential pair multiplier</td>
<td>2.5 .. 3.5</td>
<td>0.5 .. 1.5</td>
<td>3</td>
<td>$48$</td>
<td>2</td>
<td>$\frac{1}{33}$</td>
<td>+</td>
<td>+</td>
<td>s,d</td>
<td>d</td>
<td>2.5</td>
</tr>
<tr>
<td>Double differential pair multiplier</td>
<td>2.5 .. 3.5</td>
<td>0.5 .. 1.5</td>
<td>6</td>
<td>$48$</td>
<td>4</td>
<td>$\frac{1}{33}$</td>
<td>+</td>
<td>+</td>
<td>d,d</td>
<td>d</td>
<td>5.5</td>
</tr>
<tr>
<td>Gilbert multiplier</td>
<td>2.5 .. 3.5</td>
<td>0.5 .. 1.5</td>
<td>7</td>
<td>$48$</td>
<td>4</td>
<td>$\frac{1}{33}$</td>
<td>+</td>
<td>+</td>
<td>d,d</td>
<td>d</td>
<td>1.0</td>
</tr>
<tr>
<td></td>
<td>2.5 .. 3.5</td>
<td>0.5 .. 1.5</td>
<td>7</td>
<td>$48$</td>
<td>4</td>
<td>$\frac{1}{33}$</td>
<td>+</td>
<td>+</td>
<td>d,d</td>
<td>d</td>
<td>0.5</td>
</tr>
<tr>
<td>With small input ranges ...</td>
<td>2.2 .. 2.8</td>
<td>0.7 .. 1.3</td>
<td>7</td>
<td>$48$</td>
<td>4</td>
<td>$\frac{1}{33}$</td>
<td>+</td>
<td>+</td>
<td>d,d</td>
<td>d</td>
<td>1</td>
</tr>
<tr>
<td>Saxena multiplier</td>
<td>3.2 .. 3.8</td>
<td>3.2 .. 3.8</td>
<td>10</td>
<td>$48$</td>
<td>4</td>
<td>$\frac{1}{33}$</td>
<td>+</td>
<td>-</td>
<td>s,s</td>
<td>s</td>
<td>1</td>
</tr>
</tbody>
</table>
Explanation:

#T: Number of transistors.

quad: Number of quadrants that can be used.

\[ \frac{s}{b} \]: To give a measure for the power dissipation the ratio between the maximum signal current and the maximum total current in a circuit is given.

\( Z_{\text{in}} \): The impedance of both inputs is assessed: '-' means a low impedance; '..' means high impedance.

\( Z_{\text{out}} \): See \( Z_{\text{in}} \); '-' means very low impedance.

in, out: 's' Stands for single ended; 'd' means differential

lin: This is the maximum relative deviation from an ideally linear characteristic.

The two transistor multiplier and the differential pair multiplier need only a few multipliers and thus will use little chip area. Furthermore CNNs only need two quadrant multiplication, which means that there is no need to use the four transistor multiplier or the double differential pair multiplier, which are just four quadrant versions of the first two. Finally the Saxena multiplier seems a bit too complex and does not hold a real advantage over any of the other, simpler ones.

The two transistor multiplier has to be used in combination with some circuit to keep \( V_{\text{out}} \) constant. Furthermore the differential pair multiplier seems to be a good option because of its simplicity and its high impedance inputs and outputs. The high impedance outputs make that a basic current mirror can be used to subtract the output currents.

With respect to power consumption the Gilbert multiplier scores best. Furthermore in CNNs about nineteen multipliers will be connected to one node. This means all bias currents will be added, which could imply large offsets when the subtraction of currents is not perfect due to for example mismatch. Therefore also the signal bias ratio is an important feature of multipliers and thus the Gilbert multiplier, which also shows very good linearity, seems to be a good choice for CNNs too.
Chapter 4: Cell core circuitry

In section 2.4 a structure has been proposed to implement a full range CNN with an opamp, a capacitor and some kind of variable conductance. For this conductance some of the 2-quadrant multipliers discussed in chapter 3 can be used. Chapter 3 did not make a definitive choice for a two transistor multiplier or a three transistor multiplier. This choice will mainly depend on the surrounding circuitry and therefore this chapter will treat some possibilities with the two types.

4.1 Feedback loop cell with two transistor multipliers

This section will treat a possible CNN implementation with the discussed structure making use of the two transistor multiplier to form the interconnections between cells. For an implementation with two transistor multipliers some constraints have to be met. Firstly the output signal of this multiplier is differential consisting of two currents. This means that the state will be a differential signal too, kept on two capacitors, or the two currents will have to be subtracted. The latter case will be the subject of the next section. Secondly the multiplier’s output voltage has to be constant and the same for both outputs. In [Eng95] a CNN circuit is proposed which makes use of two current conveyors to do this. Figure 4.1 shows this circuit.
Figure 4.1: CNN circuit with two transistor multipliers and current conveyors

On nodes \( v_{\text{conv}+} \) and \( v_{\text{conv}-} \) all input multipliers and the feedback multiplier will be connected. The four transistor multiplier is used as a voltage to current converter and together with the two capacitors \( C \) and resistors \( R \) closes the feedback loop to form the lossy integrator. When an opamp with gain \( A \) and one dominant time constant \( \tau_{\text{OA}} \) is used the cell’s state equation becomes formula (4.1).

\[
\left( C + \frac{\tau_{\text{OA}}}{A \cdot R} \right) \frac{d(v_{\text{out}} - V_0)}{dt} = -\beta(v_{\text{out}} - V_0)(v_{x+} - v_{x-}) + i_{\text{in}+} - i_{\text{in}-} \tag{4.1}
\]

\( \beta \) is the transconductance parameter of the transistors in the four transistor multiplier. In this circuit the use of a four transistor multiplier adds an extra input \( v_{x+} - v_{x-} \) which can be used to scale all template elements. This however changes the cell’s time constant too. When \( i_{\text{in}+} - i_{\text{in}-} \) is written as the sum of the input multiplier outputs, connected to nodes \( i_{\text{in}+} \) and \( i_{\text{in}-} \) to form the template elements, this formula becomes formula 4.2.

\[
\left( C + \frac{\tau_{\text{OA}}}{A \cdot R} \right) \frac{d(v_{\text{out}} - V_0)}{dt} = -\beta(v_{\text{out}} - V_0)(v_{x+} - v_{x-}) + \sum_m \beta(v_{w+,m} - v_{w-,m})(v_{\text{in},m} - V_{\text{conv}}) \tag{4.2}
\]

In this \( m \) stands for all multipliers connected to the input nodes \( v_{\text{conv}+} \) and \( v_{\text{conv}-} \). To get the original state equation (2.4) again some multipliers will function as control operator elements, some as feedback operator elements and one as offset.

The current conveyors can be implemented very simply like in figure 4.2.

![Figure 4.2: A simple current conveyor implementation](image-url)
$I_c$ is a control current to set the output voltage $v_{out}$. The two transistors both are in saturation and form a loop with negative feedback. When the Early effect is disregarded $v_{out}$ can be calculated from formula (4.3).

$$v_{out} = -\frac{2}{B} \sqrt{I_c} + V_{dd} + V_T$$  \hspace{1cm} (4.3)

So $v_{out}$ is independent of $I$ as long as the loop gain is greater than one.

More details on this circuit and on the implementation of the opamp, the current conveyors, and resistances $R$ can again be found in [Eng95]. Also results from HSpice simulations can be found there.

### 4.2 Feedback loop cell with two transistor multipliers and current mirror

Instead of storing the state differentially on two capacitors it is also possible to store the state on one capacitor by first subtracting the currents from the input multipliers. When an active input current mirror is used [Ser94] the input voltage of this current mirror is virtually constant which means that it does not suffer from the Early effect and that one output of a two transistor multiplier could be connected directly without current conveyor. For the other multiplier output one can make use of the fact that the feedback loop approach forms a virtual ground node at its input, with also a nearly constant voltage. The resulting circuit is shown in figure 4.3.
Opamp $A1$ and transistors $M1$ and $M2$ form the current mirror with node $v_1$, a virtual ground node. Opamp $A2$ with resistor $R$ and capacitor $C$ forms the feedback loop with node $v_2$ a virtual ground node. With ideal opamps the state equation becomes formula (4.4).

$$C \frac{v_{out}}{dt} = -\frac{1}{R} v_{out} + \sum_m \beta (v_{w+,m} - v_{w-,m}) v_{in,m}$$  \hspace{1cm} (4.4)

When $R$ is replaced by a four transistor multiplier again like in section 4.1, a scaling input is added and the state equation becomes formula (4.5).

$$C \frac{dv_{out}}{dt} = -\beta v_{out} (v_{sc+} - v_{sc-}) + \sum_m \beta (v_{w+,m} - v_{w-,m}) v_{in,m}$$  \hspace{1cm} (4.5)

When this circuit is compared to the one in section 4.1 the differences are firstly that no current conveyors are needed. Instead of this the active input current mirror and the feedback loop make sure that voltages $v_1$ and $v_2$ are the same and constant. At the same time this is also very advantageous for the current mirror, because it will not suffer from the Early effect. The amount of hardware will be approximately the same for both cases because the extra opamp can be kept simple due to the fact that it's loaded by gates only. Secondly only one capacitor is needed to store the state. This could save a lot of chip area because on-chip capacitors normally are quite big. The last and maybe most important difference is that the circuit in this section suffers less from stacking of threshold voltages. Series of only two transistors form
the core of the circuit which makes it suitable for low supply voltages.

Both circuits from sections 4.1 and 4.2 suffer from a disadvantage introduced by the two transistor multiplier, being the fact that it has a low output impedance (see chapter 3). When for example due to offsets in the opamps the voltages $v_1$ and $v_2$ are not the same an offset in the output signal occurs. This shown in formula (4.6) where the output signal for one two transistor multiplier is calculated when the output voltages are wrong.

$$v_1 = v_{out} + \Delta v_{out}; v_2 = v_{out} - \Delta v_{out} \Rightarrow$$

$$i_{out+} - i_{out-} = \beta((v_{in2+} - v_{in2-})(v_{in1} - v_{out}) + 4\Delta v_{out}(v_{in1} - v_{out}) - \Delta v_{out}(v_{in2+} - v_{in2-}) + \Delta v_{out}(-2v_{in2-} + 2v_{out} + 2V_T))$$

(4.6)

The first term is the normal multiplication, the rest are added because of the error $\Delta v_{out}$. Especially the last term in formula (4.6) can grow quite large. The problem becomes even worse when more than one multiplier is connected to the same node, which will be the case in the CNN circuit. With a 1-neighbourhood nign multipliers are needed for both the control and feedback operators and one more for the offset. With even a small offset in one multiplier of a few percent, nineteen multipliers will make this a total offset of a few tens of percents. So the offset $I_c$, an important parameter for CNN cells, can not be controlled accurately and can be different for each cell.

### 4.3 Feedback loop cell with differential pair multipliers

To overcome the problems with the low output impedance of the two transistor multiplier one can also make use of the differential pair multiplier instead (see chapter 3). In this multiplier all transistors work in saturation and thus the output impedance will be high. This will also mean that no active input current mirror is needed. The resulting circuit is shown in figure 4.4.
It is clear that using the differential pair multiplier means more chip area. This however gets compensated a bit because a normal current mirror can be used. The differential pair multiplier has a high output impedance and thus will not suffer a lot from the fluctuations in $V_1$.

In this configuration the high output impedance of the circuits connected to node $V_2$ brings along another problem. When the opamp gets saturated the loop gain will drop and node $V_2$ will no longer be a virtual ground node. The voltage on this node will drop or fall according to wether $i_{in+}$ is smaller than $i_{in-}$ or not and will saturate to $V_{out} - R(i_{in+} - i_{in-})$. When the current difference $i_{in+} - i_{in-}$ comes near zero again $V_2$ will slowly return to the virtual ground state again with a rate indicated in formula (4.7).

$$RC \frac{dv_2}{dt} = v_{out} - v_2 - R(i_{in+} - i_{in-})$$ \hspace{1cm} (4.7)

When $i_{in+} - i_{in-}$ is small this rate could be very slow and as long as $v_2$ is not a virtual ground node the type of action performed by the cell is no longer correct. Another way to look at this problem is to say that the time constant of the cell is no longer $1/RC$ when the opamp gets saturated.
4.4 Differential pair multipliers with inhibition

Another way to bound the state voltage is to add extra transistors to the differential pair multiplier, which cut off or clip the output current whenever it gets too high (positive or negative). This offers a new way to limit the cell's output. A multiplier with this extra feature is shown in figure 4.5.

![Differential pair multiplier with clipping transistors](image)

Figure 4.5: Differential pair multiplier with clipping transistors

In this figure all transistor widths and lengths, that were used in HSpice simulation later this section, are added. The multiplier transistors have been sized to get a transconductance of $1 \mu \text{S}$ to be able to compare with the ones discussed in chapter 3. More details on the sizing and on other parameters used in HSpice can be found in section 5.1.
It is important to notice that both clipping transistors should be working in linear range. Otherwise the transistor pair intended for just inhibiting the multiplier will become a differential pair in saturation. This could even mean that the transconductance of the multiplier changes sign. To achieve linear range for both clipping transistors two measures where taken. Firstly the current mirror has been cascaded to ensure high voltages on the drains of the clipping transistors. And secondly these are quite long so that they start inhibiting for low values of $V_{cl}$ or $V_{cl+}$ already. In this manner $V_{gs}$ can be kept below the threshold voltage.

Figure 4.6 shows simulation results multiplier's characteristic for different values of $V_{cl}$. 

![Figure 4.6: Simulation of multiplier with clipping transistors.](image)

As can clearly be seen the voltage $V_{cl}$ offers a way to increase the output current of the multiplier, especially when it is at its lower limits. The opposite holds true for $V_{cl+}$. 

-39-
With the multiplier introduced in this section the following circuit would result for a complete cell:

![Cell Circuit with New Multipliers](image)

Figure 4.7: Cell circuit with new multipliers

The two extra opamps will raise $V_{cl}$ or $V_{cl+}$ whenever $V_{out}$ gets above $V_{sat+}$ or below $V_{sat-}$. More details on the implementation of the opamps, resistor R, on simulation results for the complete circuit, on the layout, and on measurements on the resulting circuit can be found in chapters 5 and 6.
Chapter 5: Total cell design

This chapter will treat in detail the design of all circuits needed to complete one cell, the layout needed to implement this design on chip, and finally the simulation results of an extraction from this layout.

5.1 Imec MOS process

Before all, the used IC process will be discussed. The chip will be fabricated by Imec on a 2.4μm double-poly double-metal n-well CMOS process. Because two poly layers can be used, poly-poly, thus floating, capacitors are possible.

The minimum measure for any transistor is 2.4μm. However using this minimum length (or width) will lead to relatively high inaccuracies and therefore all transistors of which the size contributes to the accuracy of the circuit will have minimum sizes of twice the minimum, thus 4.8μm. Other sizes than 2.4μm (or 4.8μm) can be obtained in steps of 0.4μm.

HSpice level 2 parameters for PMOS and NMOS transistors with minimum widths and lengths can be found in appendix A. When proportions are changed W and L have to be changed accordingly and furthermore LAMBDA has to be altered to account for the Early effect. The new value for LAMBDA, needed when a different length than 2.4μm is used, can be found with formula (5.1). In this the Early voltage \( V_{Early} \) is the same for transistors of one type (PMOS or NMOS) with whatever length.

\[
V_{Early} = \frac{1}{\lambda \cdot L} \Rightarrow \lambda_L = \lambda_{2.4\mu m} \cdot \frac{2.4\mu m}{L} \quad (5.1)
\]

For dynamic simulations also parasitic capacitances have to be calculated. This can be done via parameters AS, AD, PS, and PD. They stand for the area and perimeter of source and drain. Figure 5.1 shows the layout of a minimum sized transistor and two contact holes to connect it.

From this AS, AD, PS, and PD can be calculated according to formulas (5.2).

\[
\begin{align*}
AS &= AD = (5.6\mu m)^2 + W \cdot 1.6\mu m \quad \text{if } W \leq 5.6\mu m \\
PS &= PD = 25.6\mu m \\
AS &= AD = W \cdot 7.2\mu m \quad \text{if } W > 5.6\mu m \\
PS &= PD = 2 \cdot (W + 7.2\mu m)
\end{align*}
\quad (5.2)
\]

When no contact hole is connected but another transistor these formulas change depending on the layout of the circuit.
Figure 5.1: Layout of a minimum size transistor with two contact holes.

More details on the meaning of all level 2 parameters can be found in the Spice manual [Spi91]. A list of all minimum sizes and distances between different kinds of material on the chip can be found in [Ime00].

5.2 Circuit design and HSpice simulation

To implement the cell, the structure proposed in section 4.4 will be used. This means that the following building blocks are needed: differential pair multipliers with clipping transistors, some kind of multiplier (implementing R in the backward path), a buffer (for the forward path), and amplifiers to control the clipping transistors.

A supply voltage of 5v has been chosen. This is needed because some circuits suffer from the stacking of threshold voltages. All multipliers have been designed to have a transconductance of $1\mu \Omega^{-1}$. Furthermore a time constant of about 1$\mu$s for the complete cell has been aimed for. This means that buffers and amplifiers have to be sufficiently fast.

Some of the subcircuits need bias voltages or bias currents. In order not to use up a lot of pins from the chip just for these bias inputs, they were all scaled to voltages of 1.5v, 2.5v, or 3.5v. Bias currents can be made by using these voltages in combination with a transistor.

5.2.1 Differential pair multiplier with inhibition

The differential pair multiplier with clipping transistors will be used as input multipliers with input $V_{in1}$ used for output signals $v_{yd}$ from other cells or input signals $v_{ud}$ to the CNN. Input $V_{in2}$ will be used for feedback operators $A_j^e$ and control operators $B_j^e$. The multiplier has already been introduced in section 4.4 and can be found in figure 4.5.
All multiplication transistors have been sized to get a tranconductance of $1\mu\Omega^{-1}$. The transistors in the current mirror have been sized to keep the voltage on the drains of the clipping transistors approximately 2.2v. This high voltage is needed to keep these transistors in linear mode. For this also the clipping transistors were made long (see section 4.4).

Figure 4.6 already showed the effect of the clipping transistors. Figures 5.2 and 5.3 show the multipliers characteristics without clipping.

![Graph showing the multiplier's output current as a function of $V_{in1}$](image)

**Figure 5.2: Multiplier’s output current as a function of $V_{in1}$**

$V_{in2+} - V_{in2-} = 0.5\nu$

$V_{in2+} - V_{in2-} = -0.5\nu$
In both figures the nonlinearity which is present in this multiplier can clearly be seen. Input $V_{in2+} - V_{in2-}$ is not evenly balanced because the drain voltages of the transistors forming the differential pair are not equal.

### 5.2.2 Gilbert multiplier

To implement resistor R of figure 4.7, some kind of four quadrant multiplier is needed. Furthermore, because it will be connected to a node with varying voltage, it needs to have a high output impedance. This leaves the double differential pair multiplier and the Gilbert multiplier as good options. The latter was chosen because it scores far better with respect to power consumption while adding only one transistor. The stacking of threshold voltages due to this extra transistor also poses no problem.
Figure 5.4 shows the implemented Gilbert multiplier. Again all multiplying transistors have been sized to obtain the proper transconductance.

The transistors in the current mirror are shorter than those in the input multipliers due to the fact that the Gilbert multiplier needs smaller branch currents to obtain the same output current $I_{out}$. Figure 5.5 shows this multiplier's characteristic.
Figure 5.5: HSpice results for Gilbert multiplier; $I_{out}$ as a function of $V_{in1+}-V_{in1-}$; $V_{out}=2.2\,\text{v}; V_{in2+}-V_{in2-}=-0.5\,\text{v..0.5v}$

The figure shows that this multiplier shows good linearity and that four quadrants can be used.

**5.2.3 Forward buffer**

The forward buffer controls the output voltage of a cell and sets the voltage at the virtual ground node where all multipliers will be connected. As all multipliers have very high output impedances (long transistors and cascoded current mirrors) this voltage does not have to be defined with very good accuracy and some change during the operation of the cell is allowed. The output of the buffer will drive a chip pin, so it should have a low output impedance. A simple way to achieve both goals is to make use of a two stage amplifier with a CMOS inverter, with current source load in the first stage and a source follower in the output stage. This configuration can be found in figure 5.6.
This circuit has been simulated dynamically with a load of 3pF and a DC input voltage 2.5v. Figure 5.7 shows the bode plot.

Figure 5.6: Forward buffer circuit

Figure 5.7: Bode plot for forward buffer
The UGB for the circuit is about 10MHz so it will pose no problem in meeting the 1µs time constant for the complete cell. The double pole just above 1MHz will be compensated by the feedback capacitor which will be present in the cell anyway.

Other properties which have been tested are DC and transient behaviour. No further simulation results will be shown here, but the tests showed that the circuit is nicely linear over the total range it will be used in. This means outputs between 2.5v and 3.5v. Furthermore the slew rate proved to be high enough to ensure a step response time of 1/UGB.

5.2.4 Clipping amplifiers

To control the gate of the clipping transistors two amplifiers are needed. It is important that the saturation voltages of the cell are well defined and remain accurate while the cell is in operation so a differential amplifier with a gain of about 40dB is chosen. The output load will be about 19 transistor gates, summing up to a total of about 0.5pF. Later extraction showed that wiring did not substantially alter this number. Therefore the amplifier’s output impedance needs not to be as low as for the forward buffer. In fact no second stage is needed. The resulting circuit can be found in figure 5.8.

![Clipping Amplifier Circuit](image)

Figure 5.8: Clipping amplifier circuit

Again for this circuit a dynamic simulation has been done and the resulting bode plot can be found in figure 5.9. This simulation results were obtained with a load of 0.5pF.
The UGB for this circuit also is well above 1MHz. Again linearity and slew rate are sufficient.

5.2.5 Total cell

When all the building blocks discussed in the previous sections are put together the total cell circuit results. This can be found in appendix B. The two capacitors C_{cl+} and C_{cl} have been added for stability reasons discussed in section 5.2.5.2.

5.2.5.1 Static analysis

At first the multiplication characteristic of one multiplier will be shown when it is connected to the cell core. This means that of all nineteen multipliers actually present in the circuit only one is used. The template inputs of all others were set to '0'. With this figure 5.10 results.
Figure 5.10: HSpice simulation of total cell; $V_{out}$ as a function of $V_{in}$ of one cell; $V_{sc} = 0.5v$; $V_{w} = -0.5v$.

As can clearly be seen this figure is more or less the same as figure 5.2 except that now the output voltage of the cell is being shown and that this output voltage clips at 3.5v.

Another simulation is shown in figure 5.11 where the weight or template input is varied for different values of the scaling input.
Figure 5.11: Scaling behaviour of cell; $V_{out}$ as a function of $V_{w+}-V_{w-}$ of one cell; $V_{in}=3.0\,V; V_{sc+}-V_{sc-}=0.1 \ldots 0.5\,V$

This figure shows the scaling of multiplier input $V_{w+}-V_{w-}$ by using cell input $V_{sc+}-V_{sc-}$. This scaling will, of course, be the same for all multipliers connected to the cell.

### 5.2.5.2 Dynamic analysis

After statically analysing the cell circuit this section will take a closer look at the dynamic behaviour. For this, the cell's response to changes in input $V_{in}$ of one multiplier for different values of input $V_{w+}-V_{w-}$ is tested. The first simulations showed that the circuit became instable whenever the output voltage saturated. Analysis of this problem proved to be very difficult due to the complex transfer function from the clipping input of the multipliers to their output. All nineteen multipliers have independent inputs and thus have an independent working range. Therefore a complex sum of poles and zeros results which changes whenever one of the cell's inputs changes.
Because there was not enough time left to search for other ways to inhibit the multiplier's output current a crude solution has been used by adding to capacitors of 5pF to nodes $V_{cl+}$ and $V_{cl}$. This makes the circuit slower of course, but it does not add a lot of chip area because the capacitors make up for less than 10% of the cell's area. The simulation results are shown in figure 5.12.

\begin{center}
\includegraphics[width=\textwidth]{figure512.png}
\end{center}

Figure 5.12: Dynamic simulation of cell; one multiplier is used

In this figure the output voltage follows changes in the input voltage and the weight voltage. Whenever the output saturates one of the clipping voltages rises. This however takes time, so some overshoot is present in the output voltage.

### 5.3 Layout design in Dali

While designing the layout of the chip many constraints have to be taken into account. For example minimum sizes of transistors are 2.4\(\mu\)m and other measures can only be obtained in steps of 0.4\(\mu\)m. The minimum width of metal1 is 2.4\(\mu\)m; the minimum width of metal2 is 3.2\(\mu\)m. An n-well, used for implementing PMOS transistors, has large boundaries around it and thus it is advantageous to put all PMOS transistors together in one n-well as much as possible. Connections made by
poly material or doped substrate should be as short as possible, because of their high resistance.

Many more of these constraints, which are a result of the fabrication process, exist and they can be found in [Ime00].

5.3.1 CNN

The cell designed in the previous chapters will be used in a LCT-CNN with a square grid. This means that all template elements are the same for each cell and that one cell should be approximately square itself. Rectangular designs will lead to rectangular chips to which may not be as effective with respect to total area.

All template elements will be distributed over the cells by vertical metal2 lines and other common signals, like reference voltages, will be distributed by horizontal metal1 wires. This means that, in order not to interfere with these global connection lines, in the cell also, metal1 should be used for horizontal connections and metal2 for vertical ones as much as possible. This leads to a layout structure as in figure 5.13.

![Figure 5.13: Layout structure for the complete CNN](image)

The goal is, to find some standard instance, consisting of a cell and all wires to connect it to the outside world, which just has to be put in a grid to form the CNN. This means that also a standard way of connecting the cells together has to be found.
Output and input signal to the cells will be connected with or without multiplexing, depending on the number of cells in the CNN chip. The design presented is a prototype and all inputs and outputs will be connected to pins, to be able to test it correctly. Therefore it will consist of one cell only and no multiplexing will be needed.

5.3.2 One cell

Each cell is designed for a 1-neighbourhood and thus should have nineteen multipliers in it. Furthermore the inputs to these multipliers will be supplied by vertical lines, so they should be placed horizontally next to each other. Keeping this in mind the topology of figure 5.14 has been used.

![Figure 5.14: Topology for one cell](image)

The multipliers have been arranged in two rows of which one has been shifted about half the width of one multiplier. This allows for the nineteen lines supplying the template values, to be straight. Furthermore all multipliers are long rectangles to be able to have a square cell.

A full layout of the cell can be found in appendix C. The design of most of the subcircuits presented in section 5.2 is straightforward. The most important one, the input multiplier, will be discussed in the next section.

5.3.3 Differential pair multiplier with inhibition

The differential pair multiplier should be rectangular with a width:length ratio of about 1:3. On horizontal lines will be connected: the output current, the input of the current mirror, the reference weight voltage \( V_{w+} \), and the clipping voltages, \( V_{cl+} \) and \( V_{cl-} \). Vertically the weight voltage \( V_{w-} \) and the input \( V_{in} \) will be connected. Furthermore there will be a dummy vertical line which is used to feed through the weight input for a multiplier on the other side of the cell (see section 5.3.2).
This leads to the layout presented in figure 5.15.

Figure 5.15: Layout of differential pair multiplier with clipping transistors

In the figure it seems as if the three long metal2 lines are connected to almost everything by contact holes. This however is a result of showing all contact holes on top. Only via's connect metal2 (to metal1).

In the top half the n-well can clearly be seen in which all PMOS transistors are put. Two contact holes in the V_{dd} line are used to connect this n-well. In the bottom half a contact hole is used to connect the substrate.
The multiplier’s tail transistor is folded between the differential pair and also the cascoded current mirror is folded, to allow for a width length ratio of 1:3. The rest of this layout should be fairly clear. As one can see, these multipliers just have to be put next to each other to form a fully interconnected row.

5.3.4 Cell and pads

To complete the chip the cell of section 5.3.2 has to be connected to pins. For this purpose some pads will be needed. To connect all input gates so-called PFPPDR pads are used which have protection diodes and a resistor in them to protect the gates from high voltages, which can easily occur due to static charge. The cell’s output and the supply voltages will not suffer from static charge because of their low impedance and will be connected through PFPAD pads, just a large metal1 area. Finally two more pads (PFVDD and PFVSS) will be needed to provide the protection pads with supply voltages. The layout of one cell and pads is presented in appendix C. The squares on the corners of the chip are standard instances used to interconnect the pads next to them.

Because the number of pads is quite large (50), the chip area is much larger than that needed for one cell. This chip however is just a prototype and with more cells, to form a CNN, this problem will no longer occur.

5.4 Layout extraction

To test the layout before fabrication an extraction has been drawn from the cell without the pads. For reference the resulting HSpice listing can be found in appendix D.

Two simulations, which have already been done in sections 5.2.5.1 and 5.2.5.2, will be repeated here based on the extraction file. Firstly the scaling behaviour of the cell is tested by printing $V_{out}$ as a function of $V_w$ for different values of $V_{sc}$. This is shown in figure 5.16.
Figure 5.16: Scaling simulation of extracted layout; $V_{out}$ as a function of $V_{w+}-V_{w-}$:

- $V_{w+} = 1.5v$; $V_{sc+}-V_{sc-} = 0.1v .. 0.5v$

Except for being mirrored around the y-axis this figure is the same as figure 5.11. The mirroring occurs because $V_{w+}$ is used as reference voltage so in fact $-V_{w}$ is shown along the x-axis.

Secondly the dynamic test has been repeated. The results of this can be found in figure 5.17 and are nearly the same as in figure 5.12.
The cell is a bit slower because of the parasitic capacitances which are present in the HSpice file now. Again instead of $V_{\text{w+}}$, $V_{\text{w-}}$ is shown.
Chapter 6: Measurements

6.1 Measurement setup

This section will discuss how all measurements were performed. The chip is housed in a 68 pin Leadless Chip Carrier (LCC) package. Because only 51 pins are needed (50 pads and a cavity connection) pins 27 until 43 are not used. The meaning of all other pins can be found in figure 6.1.

The names of the pins correspond with those in the extracted HSpice file, presented in appendix D. A figure showing the bonding of the chip can be found in appendix C.

PFVdd and Vdd have been connected to 5V, PFVss, Vss, and the cavity have been connected to 0V. To supply all inputs with some signal, potentiometers were used. Furthermore all input have been decoupled with a capacitor of 10nF. Schematically this is shown in figure 6.2.
Because all inputs are formed by gates, the resistances of 10kΩ are low enough.

### 6.2 Static results

Firstly the multiplication characteristic of the cell with one multiplier has been measured. The results of this can be found in figure 6.3.

As can be seen, the angle of both lines is much lower than in figure 5.10. This could be due to a small error in the threshold voltage $V_T$ of the multiplier's tail transistor. Furthermore there appears to be an offset of about 40mV in the output voltage. This could the result of an offset in input $V_0 - V_{out}$ of the Gilbert multiplier.

In this figure already the effects of $V_{in}$ nearing $V_{dd}$ can be seen. When the tail transistor goes into weak inversion mode the multiplication formulae (3.12) no longer hold.
Figure 6.3: Multiplication characteristic with one transistor; $V_{out}$ as a function of $V_{in}$:

$V_{w^+} - V_{w^-} = -0.5V$

$V_{w^+} - V_{w^-} = 0.5V$

Secondly the scaling behaviour of the chip has been tested. Again only the inputs of one multiplier have been used. The results can be found in figure 6.4.
As can clearly be seen there seems to be an offset present in $V_{w+} - V_{w-}$. Furthermore, keeping in mind the offset of 40mV present in the output voltage, as shown in figure 6.3, this offset changes as the scaling input changes.

Several simulations based on the extraction file have been done to find the offset's cause. The threshold voltages and some other important transistor parameters have been changed, the voltage on the cell's central node has been changed by varying $V_{sc}$, and parasitic resistances have been added in the extraction. However, none of these proved to be a plausible cause for the offset in $V_{w}$. Another possibility lies in the layout of the multipliers. As can be seen in figure 5.15, several metal wires stretch out above transistors, also the differential pair transistors. The voltage on these wires could influence the behaviour of these transistors. When one multiplier is faulty due to this, they will all be thus the resulting error can be quite big.
Also in figure 6.4 errors in the cell's saturation voltages can be seen. This is very likely due to offsets in the clipping amplifiers, which could also result from metal crossing over transistors.

Results of another test of the error in weight voltage can be seen in figure 6.5.

Figure 6.5: Multiplication behaviour of chip with one transistor; $V_{out}$ as a function of $V_{w+} - V_{w-}$.

$V_{in} = -0.5V .. 0.5V$; $V_{sc+} - V_{sc-} = 0.2V$

Again the offset in the weight input changes when other signals ($V_{in}$) change. In future designs a check should be done by not letting metal lines cross over transistors. This however will cost chip area.
6.3 Dynamic results

After testing the chip statically, dynamic tests have been done. They showed that the cell is instable whenever it goes into saturation. So the capacitors added for stability have not been large enough. In simulations however the circuit, also the extraction, proved to be stable. The phase marging was about 70° which should be more than enough.

The cause of this instability lies probably in the transfer functions from $V_{cl+}$ and $V_{cl-}$ to the cell's central node. Because it is formed by many transistors, all set in different working ranges, it can have all kinds of forms. This pleads for another way of inhibiting the multipliers, having a simpler transfer function, preferably with only one pole. This would be far easier to control. Furthermore the changes in this transfer function due to changes in the cell's state or inputs, should thoroughly be analysed.
Chapter 7: Conclusions and recommendations

Drawing conclusions from the previous chapters the following remarks can be made. Firstly combining the full range approach, feedback loop approach, and two quadrant operation, as presented in chapter 2, leads to efficient CNN implementations. Furthermore of the two most promising multipliers from chapter 3 the differential pair multiplier has been chosen because of its high output impedance. This however can lead to a slow cell circuit and therefore a modification has been done, as presented in chapter 4. This modification costs however some extra hardware.

Simulations with this design promised good results and therefore it has been implemented in hardware. The layout has been designed keeping in mind of course the process parameters, the possibility of easily implementing complete CNNs with multiple instances of the designed cell, and further the accuracy of the circuit by not using minimum sizes for transistors where this was called for. A possibility for lowering chip area could be to combine some parts of the input multiplier which they have in common (for example their current mirrors).

Static measurements on the realized chip showed some offsets for which the cause could not be found definitively. A likely option seems to be the fact that in some parts of the chip metal lines cross over transistors frequently and this could influence the behaviour of these transistors. In future the design could be adapted not to have metal above transistors to test this. This would however cost chip area.

Dynamic measurements showed that the chip’s cell becomes instable whenever it goes into saturation. This instability was not present in the simulations from the extraction file so some poles or zeros coming from the loop formed by the forward buffer, the clipping amplifiers, and the clipping transistors, must have shifted. In future work this loop should be analyzed thoroughly or other ways of clipping the cell should be searched for. Maybe some solution can be found, which does not show as complex a set of poles and zeroes and which costs somewhat less hardware.

As a final, remark one could say that some of the structures presented in chapter 4, which are not suitable for CNNs (especially the two transistor multiplier circuit with active input current mirror from section 4.2), could be used for other types of ANNs which do not suffer from their disadvantages as much as CNNs.
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# Appendix A:

## HSpice level 2 parameters

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Appendix B: Total cell circuit

Figure B: Total cell circuit with one input multiplier shown
Appendix C: Total Layout
Appendix D: Extracted HSpice listing

cell1

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* 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45
* 46 47 48 49 50

* 1 pbulk 2 nbulk 3 model 4 out 5 V_3v5
* 6 sc_min 7 vdd 8 wref 9 V_1v5 10 V_2v5
* 11 w0[3] 12 v0 13 w0[0] 14 w0[1] 15 w0[2]

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m2 3 92 93 1 penh w=2.4u l=12u
m3 91 91 94 2 nenh w=4.8u l=20u
c1 89 0 12.12f
m4 95 13 89 1 penh w=4.8u l=40u
m5 93 8 96 1 penh w=4.8u l=40u
c2 93 0 12.12f
m6 97 98 3 2 nenh w=4.8u l=20u
c3 13 0 11.424f
m7 94 94 2 nenh w=4.8u l=20u
m8 97 99 0 2 nenh w=4.8u l=20u
c4 97 0 32.8896f
m9 95 23 7 1 penh w=4.8u l=40u
m10 7 42 96 1 penh w=4.8u l=40u
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m11 94 100 2 nenh w=4.8u l=20u
m12 99 99 0 2 nenh w=4.8u l=20u
c6 94 0 40.9472f
c7 23 0 11.6224f
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m14 98 90 102 1 penh w=2.4u l=12u
m15 3 91 100 2 nenh w=4.8u l=20u
c8 101 0 12.12f
m16 95 8 101 1 penh w=4.8u l=40u
m17 102 33 96 1 penh w=4.8u l=40u
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c11 95 0 73.3728f
c12 96 0 73.3728f
c13 99 0 40.9472f
c14 33 0 11.424f
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Vpbulk 1 0 5V
Vnbulk 2 0 0V

V_1v5 9 0 1.5V
V_2v5 10 0 2.5V
V_3v5 5 0 3.5V

V0 12 0 3V
Vwref+ 8 0 1.7V
Vsc- 6 0 1.5V

Vsc+ 11 6 0.5V

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Vin03 25 12 0V
Vin04 26 12 0V
Vin05 27 12 0V
Vin06 28 12 0V
Vin07 29 12 0V
Vin08 30 12 0V
Vin09 31 12 0V
Vin10 32 12 0V
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+ .OPTION POST OP
+ .END

-79-