Design of a calibrated 12-bit current-steering Digital-to-Analog Converter

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Design of a calibrated
12-bit current-steering
Digital-to-Analog Converter

Georgi Ivanov Radulov

A TWAIO Thesis
January 2004

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Abstract

A goal of this project is to design a calibration algorithm for Digital-to-Analog Converters (DACs) that relaxes their design requirements and improves their static performance. To demonstrate and implement the algorithm, a secondary goal is defined to design a 12-bit current-steering DAC core with 6-6 segmentation.

This thesis presents the design of a 12-bit 400MS/s current-steering DAC with calibration. The converter is designed in UMC 0.25µm CMOS process.

The proposed calibration algorithm adjusts the individual contributions of the thermometer currents. It is applied once, the results are memorized and used during normal DAC operation without deteriorating the dynamic performance of the DAC core. Calibration makes it possible to combine elements with relaxed specifications into a system the performance of which is not sacrificed. In addition, calibration reduces DAC’s performance dependancies on the variations of the process parameters.

This thesis is divided into four chapters. The first chapter is an introduction to the field of DACs. A survey of 34 recent academic and industrial DAC works is presented. The second chapter covers the system level design of the DAC core and the calibration algorithm. The theoretical background of the calibration algorithm is also elaborated there. The third chapter presents the transistor level design of the 12-bit Current-Steering DAC with calibration. Simulation results are presented. The fourth chapter briefly describes the layout design of the DAC system. Particular layout aspects for the design of DACs are discussed.
Background

This thesis is submitted in partial fulfillment of the requirements for the degree of Professional Doctorate in Engineering (PDEng) to the Stan Ackermans Institute, a part of the Technical University of Eindhoven (TU/e), the Netherlands.

This thesis is a result of a 10 month project, the academic side of which is represented by Stan Ackermans Institute and MsM group at TU/e and the industrial side of which is represented by Xilinx, Ireland.

The supervisors in this project are prof.dr.ir. A.H.M. van Roermund and dr.ir. J.A. Hegt (direct supervisor) in Eindhoven and ir. Patrick Quinn in Dublin. Prior to his current professional engagement, in the first 3 months of this project, ir. Konstantinos Doris was also involved as a direct supervisor. His PhD studies and work elaborated principles for design of the DAC core, which served as a basis for the development of the current project.

This project is developed in MsM group and in Xilinx, Ireland. It involved several work visits to the industrial partner in Ireland. Thus, the results presented here reflect also the knowledge and the experience of the engineers working on both places.

An invaluable contribution during the development of this project came from Stan Ackermans Institute. The courses and workshops followed there considerably improved the management and time planning of the project.
TABLE OF CONTENTS

Abstract 2
Background 3
TABLE OF CONTENTS 4
List of abbreviations 6
Preliminary 7

1.0 Introduction ..............................................................................................................8
  1.1 Specifications. Sources of errors .............................................................................8
  1.1.1 Digital-to-Analog Conversion ........................................................................... 8
  1.1.2 Input-output characteristic ............................................................................. 8
  1.1.3 Static errors and specifications ........................................................................ 8

Offset and Gain error 9
DNL and INL errors and specifications 9
  1.4 Dynamic specifications .................................................................................. 10

SNDR, SNR, and THD 10
SFDR 11
Output Frequency Spectrum of a DAC converted Single Sinewave. 12
  1.5 Dynamic errors ................................................................................................ 12

Glitch impulse 12
Output slewing 12
Digital feedthrough 12
  1.6 References ..................................................................................................... 13

1.2 DACs in comparative perspective ....................................................................... 14
  1.2.1 DAC Architectures ........................................................................................ 14

1.2.2 DAC Families ................................................................................................ 16

Binary-weighted architecture 14
Thermometer Encoded architecture 14
Segmented architecture 15

1.3 Calibration techniques for Current-Steering DACs .............................................. 19
  1.3.1 Calibration of current cells. 1A ..................................................................... 20
  1.3.2 Correction of the output current. 1B ............................................................. 21

Current-Based DAC 16
Charge redistribution DAC 17
R-2R Ladder DAC 17
  1.4 Brief DAC literature overview ........................................................................... 23
  1.4.1 References ................................................................................................... 28

2.0 System Level Design .............................................................................................31
  2.1 Concepts ............................................................................................................ 31
  2.1.1 Current based DAC ..................................................................................... 31
  2.1.2 Current-Steering Binary, Thermometer, and Segmented DACs .................. 32
  2.1.3 Intrinsic and Calibrated CS DACs ............................................................... 33

2.2 Architecture ......................................................................................................... 35

2.3 Requirements for the converter core sub-blocks ................................................. 37
  2.3.1 Finite output impedance .............................................................................. 37
<table>
<thead>
<tr>
<th>Section</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.3.2 Unit-current sources matching</td>
<td>40</td>
</tr>
<tr>
<td>2.4 Calibration Method</td>
<td>43</td>
</tr>
<tr>
<td>2.4.1 Calibration requirements</td>
<td>43</td>
</tr>
<tr>
<td>2.4.2 Calibration algorithm</td>
<td>44</td>
</tr>
<tr>
<td>2.4.3 Calibration implementation</td>
<td>47</td>
</tr>
<tr>
<td>2.4.4 Calibration algorithm simulations</td>
<td>50</td>
</tr>
<tr>
<td>2.5 System level decisions</td>
<td>52</td>
</tr>
<tr>
<td>3.0 Transistor Level Design</td>
<td>53</td>
</tr>
<tr>
<td>3.1 DAC Core</td>
<td>53</td>
</tr>
<tr>
<td>3.1.1 Thermometer Decoder</td>
<td>53</td>
</tr>
<tr>
<td>3.1.2 Master-Slave Latch</td>
<td>54</td>
</tr>
<tr>
<td>3.1.3 Current Switching Cell</td>
<td>56</td>
</tr>
<tr>
<td>3.1.4 Unit-element approach</td>
<td>57</td>
</tr>
<tr>
<td>3.1.5 DAC Core Dynamic Performance</td>
<td>58</td>
</tr>
<tr>
<td>3.2 Calibration Add-on</td>
<td>61</td>
</tr>
<tr>
<td>3.2.1 CALDAC</td>
<td>61</td>
</tr>
<tr>
<td>3.2.2 Temporary Current source &amp; CALDAC</td>
<td>63</td>
</tr>
<tr>
<td>3.2.3 Current Comparator</td>
<td>63</td>
</tr>
<tr>
<td>3.2.4 Calibration simulations</td>
<td>65</td>
</tr>
<tr>
<td>3.3 Transistor level decisions</td>
<td>67</td>
</tr>
<tr>
<td>4.0 Layout Design</td>
<td>68</td>
</tr>
<tr>
<td>4.1 Layout considerations</td>
<td>68</td>
</tr>
<tr>
<td>4.2 Chip floorplan</td>
<td>69</td>
</tr>
<tr>
<td>4.3 DAC components</td>
<td>71</td>
</tr>
<tr>
<td>4.3.1 Array of unit current sources</td>
<td>71</td>
</tr>
<tr>
<td>4.3.2 Array of CALDACs</td>
<td>72</td>
</tr>
<tr>
<td>4.3.3 Array of cascodes</td>
<td>72</td>
</tr>
<tr>
<td>4.3.4 Current comparator</td>
<td>73</td>
</tr>
<tr>
<td>4.3.5 Master-Slave latches and Current Switches</td>
<td>73</td>
</tr>
<tr>
<td>4.3.6 DAC layout</td>
<td>74</td>
</tr>
</tbody>
</table>

Conclusions 76
Recommendations 77
Bibliography 78
Acknowledgments 82
## List of abbreviations

<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADC</td>
<td>Analog-to-Digital Converter</td>
</tr>
<tr>
<td>CALDAC</td>
<td>Calibrating Digital-to-Analog Converter</td>
</tr>
<tr>
<td>CB</td>
<td>Current Based</td>
</tr>
<tr>
<td>CS</td>
<td>Current Steering</td>
</tr>
<tr>
<td>CVSL</td>
<td>Cascode Voltage Switch Logic</td>
</tr>
<tr>
<td>DAC</td>
<td>Digital-to-Analog Converter</td>
</tr>
<tr>
<td>DNL</td>
<td>Differential Non-Linearity</td>
</tr>
<tr>
<td>INL</td>
<td>Integral Non-Linearity</td>
</tr>
<tr>
<td>FPGA</td>
<td>Field Programmable Gate Array</td>
</tr>
<tr>
<td>FS(R)</td>
<td>Full Scale (Range)</td>
</tr>
<tr>
<td>FSM</td>
<td>Finite-State-Machine</td>
</tr>
<tr>
<td>LSB</td>
<td>Least Significant Bit</td>
</tr>
<tr>
<td>LVDS</td>
<td>Low Voltage Differential Signal</td>
</tr>
<tr>
<td>PDF</td>
<td>Probability Density Function</td>
</tr>
<tr>
<td>MSB</td>
<td>Most Significant Bit</td>
</tr>
<tr>
<td>MsM</td>
<td>Mixed Signal Microelectronics</td>
</tr>
<tr>
<td>MSps</td>
<td>Mega Samples Per Second</td>
</tr>
<tr>
<td>SFDR</td>
<td>Spurious Free Dynamic Range</td>
</tr>
<tr>
<td>SN(D)R</td>
<td>Signal-to-Noise-(and Distortion)-Ratio</td>
</tr>
<tr>
<td>THD</td>
<td>Total Harmonic Distortion</td>
</tr>
</tbody>
</table>
Preliminary

The exponential development of CMOS processes is continuously driving the development of digital micro-electronics forward. One of the many beneficiaries of that process are the Field-Programmable-Gate-Array (FPGA) chips that significantly increased in market share for the past ten years. Within this period, the FPGAs have improved in speed and complexity tens of times and in size hundreds of times. However, the observed functional development is only along the digital axis: DLL, Memory blocks, Multiplier units, etc. There is no true functional advance along the analog axis, except some interface features. On the other hand, the growth of digital circuits also leads to an increased demand for mixed-signal interface, which for now is not offered by the FPGA platforms.

These considerations motivated the start-up of the joint-venture project "Flexible AD/DA conversion" between the MsM group at TU/e and Xilinx. An objective of the project is to research and develop smart, reconfigurable AD/DA techniques, which might well survive in the hostile digital environment of a FPGA, and which lead to the creation of a novel mixed-signal FPGA-based platform. In this framework, the TWAIO project "Design of a 12-bit Calibrated Current-Steering Digital-to-Analog Converter" was undertaken. It addresses the design of a high speed Digital-to-Analog Converter (DAC) in a standard 0.25 µm digital CMOS process. A particular emphasis is given to the research and design of calibration capabilities, which improve the DC accuracy without deteriorating the dynamic performance. In that context, an extensive literature survey was elaborated, a DAC Core was designed and a calibration algorithm was developed and implemented for that core. It is planned to tape-out a prototype chip in May 2004.

The results of this project, in particular the acquired knowledge and experience in calibration, will extensively be used in the broader “Flexible AD/DA conversion” project, since calibration is one of its fundamental aspects.
1.0 Introduction

This chapter reviews the terminology, the definitions, and the figures of merit used in the field of Digital-to-Analog Converters (DAC). It provides an overview of the basic DAC architectures and implementations. A survey of more than 30 academic and industrial DAC works is presented.

1.1 Specifications. Sources of errors.

1.1.1 Digital-to-Analog Conversion

Digital-to-Analog Converters (DACs) are interfacing circuits between the digital and the analog electronics. They receive digital code words and produce discrete analog output levels according to some code-word/output level correspondence [Tewsbury 78]. The conversion of digital values to proportional analog values is a necessary task in order that results of digital computations can be used and easily understood in the analog world [Hnatek 76]. Various techniques, realizing this conversion are known from literature: PWM converters, Integrating converters, R2R ladder network based converters, Switched-capacitor converters, Sigma-Delta converters, Current steering converters, etc. [Plassche 94, Jespers 2001, Hnatek 76]. Every major group of these has further subdivisions, but all of them obey similar terminology, specifications, and evaluation techniques.

1.1.2 Input-output characteristic

The vast majority of DACs feature a linear input-output characteristic that may be summarized as:

$$V_{\text{out}} = \sum_{m=0}^{n-1} B_m 2^m R_{\text{ref}}$$  \hspace{1cm} (EQ 1)

EQ 1 describes DA conversion: $V_{\text{out}}$ represents the analog output value, $R_{\text{ref}}$ is a reference value, $n$ is the converter’s resolution, $m$ is a particular bit between 0 and $n$, and $B$ is the value of this particular bit - either 1 or 0 [Plassche 94].

The number of bits $N$ sets the number of discrete levels $2^N$ of the converter, the so-called converter’s resolution, which determines the smallest step $V_{\text{FS}}/2^N$ that can be discriminated. The full-scale of the converter, $V_{\text{FS}}$, is the analog value, which corresponds to the maximal input digital word. The smallest step, referred to as 1 Least Significant Bit (LSB), is the difference in the analog output between two consequent digital input words.

An ideal model of a DAC features similar input-output characteristics as the one given by EQ1. However, a real implementation of a DAC always suffers from particular non-idealities due to various types of unavoidable errors. To evaluate the impact of these errors onto DAC’s performance, sets of figures of merit are defined. These can be split in two main groups: static and dynamic errors and specifications [TI 95, Plassche 94, Hendriks 97].

1.1.3 Static errors and specifications

Static errors are those errors that affect the accuracy of the converter when it is converting static (dc) signals. These can be completely described by just four terms: offset error, gain error, integral non-
linearity, and differential nonlinearity. Each can be expressed in LSB units or sometimes as a percentage of the full-scale range (FSR) [TI 95].

1.1.3.1 Offset and Gain error

Input amplifiers, output amplifiers, and comparators in practical systems inherently have a built-in offset voltage and offset current. This offset is caused by the finite matching of components. The offset results in a non-zero output voltage or current, although a zero signal is applied to the converter [Plassche 94]. The offset error, as shown in Figure 1 a), is defined as the difference between the nominal and actual offset points. It is the DAC’s output value when its digital input is zero [TI95].

The gain error characterizes the divergence of the actual transfer characteristic slope from the ideal one [Jespers 2001]. It is shown in Figure 1 b) and defined as the difference between the nominal and actual gain points on the transfer function after the offset error has been corrected to zero. Thus, it is the value between the nominal and the actual output when the digital input is full scale [TI 95].

1.1.3.2 DNL and INL errors and specifications

Differential nonlinearity (DNL) error describes the difference between two adjacent analog signal values compared to the step size (LSB weight) of a DAC, generated by the transitions between adjacent pairs of digital code numbers over the full range of the converter [Plassche 94].

The DNL error shown in Figure 2a) is the difference between an actual step height and the ideal value of 1 LSB. Therefore if the step height is exactly 1 LSB, then the differential nonlinearity error is zero. If DNL exceeds 0.5 LSB, there is a possibility that the converter becomes non-monotonic. This means that the magnitude of the output gets smaller for an increase in the magnitude of the input [TI 95]. EQ 2 describes the DNL error analytically:

$$DNL_k = A_k - A_{k-1} - \Delta$$

EQ 2

DNL_k is the differential nonlinearity error for a particular code k, A_k is the analog output for the code k, A_{k-1} is that for k-1, and \Delta is the quantization step of the DAC, i.e. 1 LSB.
Integrated nonlinearity expresses the total deviation of an analog value from the ideal value, when the offset and gain errors are nullified. The precise definition of the INL given by IEEE Standard 746-1984 reads: “The integral linearity error is the peak difference between the actual and ideal quantization levels after appropriate adjustments have been made for gain and offset errors”[IEEE84].

The INL error shown in Figure 2 b) is the deviation of the values on the actual transfer function from a straight line. This straight line can be either a best-fit straight line, which is drawn so as to minimize these deviations, or it can be a line drawn between the end points of the transfer function once the gain and offset errors have been nullified. The second method is called end-point linearity and is the usual definition adopted since it can be verified more directly. For a DAC the deviations are measured at each step. The name integral nonlinearity derives from the fact that the summation of the differential nonlinearities from the bottom up to a particular step, determines the value of the integral nonlinearity at that step [TI 95]. EQ 3 describes the INL error analytically [Wikner 2001]:

\[
INL_k = INL_0 + \sum_{i=1}^{k} DNL_i
\]  

(EQ 3)

INL_k is the INL for a particular code k, equal to the sum of all precedent DNL errors.

INL and DNL specifications are usually given for the largest values of INL_k and DNL_k.

1.1.4 Dynamic specifications

The dynamic DAC performance describes the quality of the converter when transforming dynamic (ac) signals. To characterize dynamic performance, usually a sinewave as an input signal is used and then the DAC’s output is evaluated. The most important dynamic DAC specifications are the signal-to-noise ratio (SNR), the signal-to-noise-and-distortion ratio (SNDR), and the spurious-free-dynamic-range (SFDR). Additional figures of merit are the total-harmonic-distortion (THD), the inter-modulation-distortion (IMD), etc.

1.1.4.1 SNDR, SNR, and THD

The signal-to-noise-and-distortion ratio (SNDR) computes, usually in decibels, the ratio between the powers of the signal’s main harmonic (the signal is a sinewave) and the noise plus distortion harmonics in the bandwidth of interest (EQ 4).
, where $P_s$ is the signal power, $P_n$ is the noise power, and $P_k$ is the $k^{th}$ harmonic.

Signal-to-noise-and-distortion-ratio is the most encompassing frequency domain specification since it includes all of the noise and distortion that falls within the band of interest. A similar figure of merit is the signal-to-noise ratio (SNR), which omits the distortion introduced by non-linear effects. Ideally, the computed noise should only be due to quantization noise. The natural sources of noise, e.g. thermal or 1/f noise, should be buried below the level of the quantization noise. SNR must be specified over half the sampling frequency and should ideally follow the theoretical formula: 

$$SNR = 6.02 \times n + 1.76 \text{ [dB]}$$

, with $n$ - the resolution of the converter. Specifications must be given as a function of the signal frequency with various amplitudes and as a function of amplitude with a constant signal frequency.

The total-harmonic-distortion (THD) is also computed as a ratio. It is the ratio of the harmonic distortion power to the power of the main harmonic. Usually, the total harmonic distortion power is calculated by summing the powers of all the harmonics that fall in the band of interest. The ratio between the latter sum and the main harmonic is usually given in decibels and is considered as the THD specification [Hendriks 97].

$$THD = 10\log_{10} \frac{\sum_{k=2}^{\infty} P_k}{P_s}$$

, where $P_s$ is the signal power, and $P_k$ is the $k^{th}$ harmonic.

### 1.1.4.2 SFDR

Spurious-free-dynamic-range (SFDR), perhaps the most often quoted DAC specification, defines the difference, in decibels, between the rms power of the fundamental and the largest spurious signal within the specified frequency band, see Figure 3. The spur does not have to be harmonically related to the fundamental (although it often is) nor does the frequency band necessarily have to include the DAC’s baseband Nyquist zone [Hendriks 97].
1.1.4.3 Output Frequency Spectrum of a DAC converted Single Sinewave.

The above discussed dynamic specifications are defined for single tone converted sinewave, considered in the frequency spectrum of the DAC output signal, when converting a pure tone (sinewave as an input). An example of such a frequency spectrum is given in Figure 3.

The SFDR is defined as the difference between the levels of the main harmonic and the greatest harmonic distortion component within the frequency band of interest.

The SNDR is defined as the ratio of the main harmonic power to the sum of all the noise and harmonic distortion components within the frequency band of interest.

The THD is defined as the sum of the powers of the first five or six harmonic distortion components to the power of the main harmonic.

1.1.5 Dynamic errors

Dynamic errors comprise all non-idealities caused by the dynamic nature of the DAC normal operation. They include glitches due to switching inaccuracies, output slewing due to capacitive loads, digital feedthroughs due to MOS transistors based switches, etc.

1.1.5.1 Glitch impulse

When the input code word is applied, a brief but often high amplitude transient, called GLITCH, appears due to delay skews associated with the arrival of input-code word digits and with the internal switches of the D/A. [Tewsbury78]. The glitch impulse is a measure of the size of the earliest part of the transient generated when a DAC switches between two output levels. Glitch impulses are commonly associated with various time skew errors within the DAC - non simultaneous action of the current switches - and is usually measured as the area under the transient. Its code dependency, as opposed to its mere existence, is just one of several sources of frequency domain distortion [Hendriks 97].

1.1.5.2 Output slewing

Output slewing is associated with the output rise and fall times. When there are code-dependent rise and fall times, these are also a major contributor to distortion. In fact, the code dependency of a DAC’s settling time has far greater impact upon its frequency domain performance than the settling time itself [Hendriks 97]. For example, the code-dependent output capacitance, e.g. generated by the parallel connected current sources in the current steering DACs, causes unequal delays, which leads to code-dependent settling time.

1.1.5.3 Digital feedthrough

Digital feedthrough, both internal and external to the monolithic IC, is a form of dynamic correlated noise that tends to increase the overall DAC noise floor. Clock feedthrough, on the other hand, is not
a source of additional noise or distortion since it typically does not exhibit any code dependency. Its effects are easily removed by a reconstruction filter [Hendriks 97].

1.1.6 References


1.2 DACs in comparative perspective

1.2.1 DAC Architectures

1.2.1.1 Binary-weighted architecture

Binary-weighted architectures realize the DAC transfer function given in Eq 1 in a straightforward way, graphically shown in Figure 4.

Each input digital bit controls a particular amount of analog binary weight, which is added/subtracted to/from the output. Sometimes, these converters are referred to as binary-scaled or binary-encoded. To implement binary weights, either current sources, capacitors, or resistors can be used.

The most important advantage of the binary converters is their compact, area-saving architecture. However, the accuracy requirements of the analog values generating the converter's output become more and more stringent with every successive bit in resolution. This property becomes a problem if the standard DAC specification of DNL < 0.5LSB has to be achieved. The maximal DNL, in binary converters, is directly dependent on the resolution of the converter. It is set by the mid-scale transition, when the two most-significant bits, generated by two different analog values, are switched. Subsequently, this transition also generates major glitches, which deteriorate the dynamic performance.

A detailed discussion about binary Current-Steering DAC is offered further in this thesis.

1.2.1.2 Thermometer Encoded architecture

The thermometer-encoded DAC architecture utilizes a number of equal-size independent elements to generate the output analog signal. The binary input code, comprising N bits, is converted into a thermometer code, comprising M=2^N-1 bits, by a decoder. The output analog value is given by:

\[ A(nT) = A_0 \sum_{m=1}^{M} c_m(nT) \]  

(EQ 7)

, where \( c_m(nT) \in \{0, 1\}, 1 \leq m \leq M \) are the thermometer-coded bits.

The most important advantage of the thermometer converters is their inherent monotonicity. This property is a direct consequence of the transfer function, given by (EQ 11): when the input code is incremented by one, the analog values, generating the output are supplemented by an additional analog value. Therefore, for thermometer DAC, every generated output analog value, for a particular input digital code, is greater than the output analog values for minor digital codes, and is smaller than those for major digital codes.
A direct consequence of the monotonic property of the thermometer converters is the relaxed requirements for element matching, in comparison to binary converters, with respect to DNL specification. In fact, as long as the matching error is within a 50% margin, the DNL<0.5LSB specification is guaranteed.

Furthermore, the thermometer converters have equally small glitches at all code-transitions, given the fact that equal analog elements generate every analog value.

However, full thermometer decoded architectures are impractical to implement for high resolution because of enormous complexity [Bugeja 99]. Figure 6 shows a simplified schematic diagram of a thermometer encoded DAC architecture, often also referred to as fully segmented architectures.

1.2.1.3 Segmented architecture

The majority of recent DAC implementations employ the advantages of both the binary and the thermometer architectures, combining them in a hybrid structure, often referred to as a segmented DAC, see Figure 6.

Segmented DACs have their Least-Significant-Bits implemented as a binary converter, allowing compact area and avoiding stringent accuracy requirements. Their Most-Significant-Bits are implemented as a thermometer converter, providing relaxed accuracy requirements and avoiding the exponential silicon area growth at higher resolutions. The DC output of a segmented DAC at time instant \( nT \) is:

\[
A(nT) = A_0 \left( \sum_{m=1}^{N_1} 2^{m-1} b_m(nT) + \sum_{m=1}^{M} c_m(nT) \right)
\]

(EQ 8)

Common approaches are a single segmentation (the LSB part is binary and the MSB part is thermometer) and a double segmentation (the LSB part is binary, the Middle-Significant Bits part is thermometer, and the MSB part is thermometer).
Thus, we say that a \( N \)-bit converter is segmented as \( N = [N_1 - N_2] \) when the \( N_1 \) more significant bits control \( 2^{N_1 - 1} \) equal unit elements of value \( 2^{N_2} I_{\text{unit}} \), and the \( N_2 \) less significant bits control \( N_2 \) binary weighted unit elements, each being a power of 2 multiple of \( I_{\text{unit}} \) [Bastos 98].

### 1.2.2 DAC Families

#### 1.2.2.1 Current-Based DAC

Current-Based (CB) DACs generate current as an output analog value. Additional terminating resistors (25-75\( \Omega \)) may convert this current into voltage. The basic topologies of a CB DAC are shown in Figure 7 [Vital 2002]. The simpler forms of this type of DACs are just digitally programmable current sources/sinks that dump their output current into the load. The resistive part of the load is responsible for the static current-to-voltage conversion function, whereas the capacitive part represents the ultimate limitation for the settling behavior of the resulting output voltage.

The basic uni-polar topologies can be further refined by adding a fixed half scale current sink/source, such that the total output current can assume both positive and negative values, see Figure 7c. Finally, a generic topology employing an additional output block can also be considered, see Figure 7d. This block can represent a transimpedance amplifier for current to voltage conversion, allowing more flexible driving capabilities, and/or an output resampler for more sophisticated output formats other than the zero order hold, which may have benefits from the frequency domain performance point of view [Vital 2002].

As a remark, it is important to notice that most of the implementations use, in fact, two complementary outputs, such that the internal elementary current sources can be steered from one output to the other without the need to be shut-off. These differential architectures have, as well, the advantages of cancelling even harmonics, suppression of common-mode noise, and easy implementation of a signed output.

The Current-Based architecture can be either Current-Division or Current-Steering. The latter is much more popular due to its overwhelming advantages over the Current-Division architecture. With time Current-Steering DACs have become a synonym of Current-Based DACs. More detailed discussion about Current-Steering and Current-Division architectures is provided further in this thesis.
1.2.2.2 Charge redistribution DAC

The charge-redistribution DAC is a switched-capacitor (SC) circuit, implementing DA conversion in Q-domain [Pelgrom 88, Plassche 94 Khanoyan 2002]. Usually, charges stored on a number of capacitors are used to perform the required conversion. Figure 8 shows an example of a differential charge-redistribution DAC. Its output signal is generated by an OTA, the speed and the linearity of which set to a greater extent the performance of the DAC.

Furthermore, the performance of these converters is also constrained in accuracy due to the finite matching of the capacitors.

1.2.2.3 R-2R Ladder DAC

The R-2R ladder is a simple approach to implement DA converters. Its basic principles are outlined on Figure 9 a). When a voltage is applied to node 6 in the circuit, a binary voltage scale builds up along the upper nodes. The impedance between nodes 1, 2..., 6 and ground is equivalent to a single resistance R. Thus, the series combination of all voltages along the upper nodes implement a binary scale. The same applies to the currents flowing in the vertical resistances 2R [Jespers 2001].

The binary weighted currents flowing through the vertical resistances 2R can be combined in a common node and consequently converted to voltage, for example as shown in Figure 9 b). Switches, which are controlled by the input digital word, Bn, pass the binary weighted currents to the summing node or redirect them to ground. The summing node in the example, Figure 9 b), is the virtual ground at the negative OpAmp input.

The R2R ladder approach was mainly used in the past. Today, it is rarely encountered in state-of-the-art DACs, but there are of course always exceptions: [Seo 2000].
1.2.3 References


1.3 Calibration techniques for Current-Steering DACs

DAC Calibration is as a general term describing a process, the objective of which is to increase converter’s accuracy. The results of the calibration are improved performance characteristics, such as INL, DNL, SFDR, etc. However, calibration complicates DACs design. That is why many designers prefer to avoid it and to design intrinsic converters\(^1\). However, they exclusively rely on matching properties of the used process, large silicon areas, and fully optimized circuits & lay-outs. These requirements may make the DAC design-flow more complicated and effort consuming, than the application of calibration. Finally, accuracy of 14 bits and above is practically hardly achievable without the aid of calibration.

The term calibration is used as a general term for various methods of self-tuning, such as calibration, pre-compensation, correction, etc. In particular, calibration implies adjusting the analog values of a certain set of analog elements, generating the converter's analog output, so that they generate together a more accurate analog output. Next, pre-compensation implies adjusting the digital input in a way that the generated analog output is closer to the desired analog output for the original digital input. Finally, correction implies adding particular amount of analog value to the converter's generated analog value, so that their sum becomes more accurate.

Figure 10 offers a classification of the main calibration techniques encountered in literature. The first basic distinction is made between calibration (1A) and correction (1B, 1C). Theoretically, DAC calibration implies changing particular properties of the electric circuit, which is part of the DAC, while correction implies adding/subtracting particular bits/values to DAC’s input/output so that the generated analog output becomes more accurate.

![FIGURE 10. Classification of DACs’ Calibration techniques.](image)

Calibration of current cells (1A) is a technique which makes every individual DAC current cell, under calibration, more accurate. Correction of the DAC output current (1B) is a technique which

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1. See Section 2.1.3 on page 33 for a further discussion about Intrinsic and Calibrated DACs.
adds/subtracts particular amount of current to/from DAC output current, for a particular input digital word. Pre-Correction of the DAC’s input (1C) is a technique which re-maps the input digital word, so that the DAC’s generated output is closer to the desired one. This technique is mostly used to correct non-monotonicity.

Furthermore, there are Start-up Calibration (2A) and On-going Calibration (2B). The former is a process that is executed once when the chip is powered up. The On-going Calibration (2B), is a process that is continuously carried out. It refreshes the DAC’s parameters within a period of time.

Consequently, the On-going Calibration (2B) can be divided into two new sub-categories: Off-line Calibration (2B.A) and On-line Calibration (2B.B). The former technique substitutes an element in DAC’s current cell array, calibrates it, and returns it back. Thus, Off-line Calibration (2B.A) is carried out while the current cell under calibration is not operating. The process of getting out and putting back an analog cell usually influences DAC’s dynamic performance. On-line Calibration or background trimming (2B.B) is a process that fixes some electrical parameters in the analog cells, while they are operating. Therefore, the negative impact on DAC’s dynamic performance is decreased.

1.3.1 Calibration of current cells. 1A.

A widely used approach in CB DAC calibration is to fix the generated by each current cell/current source (CS) (under calibration) current to a common reference value, often called a calibration/reference current source. Thus, these techniques adjust the currents generated by the CS.

For example, it is possible to measure first the output current of a CS, then to compare it to a reference value, and, to fix the former to the latter. This sequence of basic operations can be repeated for every CS that is designed to be calibrated, Figure 11.

The major design challenge of the calibration techniques tuning DACs current cells’ output currents is to design a current cell that can be calibrated with enough precision.

One of the oldest principles in MOS systems is the charge storage calibration principle. In Figure 12, the basic operation of the current calibration system is shown - calibration and operational cycle. During calibration of the MOS current source, the MOS device M1 is connected as a diode by closing the switch S1. The current $I_{ref}$ is applied to the system and because of the diode connection of M1, the gate-source voltage $V_{gs}$ is adjusted in such a way that the drain current is made equal to $I_{ref}$.
After the current has been calibrated to the reference value $I_{ref}$, the switch $S_1$ is opened and the gate-source voltage of the transistor $M_1$ retains the calibration value. The output switch $S_2$ is switched to the output terminal. The current flowing through the output will theoretically be $I_{ref}$, because the $V_{gs}$ is not changed.

However, note that the drain voltages of transistor $M_1$ in phase 1 and phase 2 might be different. In principle, such a difference will cause different drain currents during phase 1 and phase 2 for the same gate-source voltage, because of the channel-modulation effect. On top of that, there are errors from digital feedthrough stored in $C_{gs}$, which could not be neglected. Finally, other source of non-accuracy can be listed: leakage currents associated with $C_{gs}$, finite output resistance of the reference current source, and etc.

Thus, the above-discussed approach influences the gate-to-source voltage $V_{gs}$. However, it is possible to influence other parameters that define the transistor’s drain current. In [Tang 94] an approach is described that effectively alters the transistor’s W/L ratio, to calibrate its drain current. This trimmable MOSFET is shown in Figure 13.

A set of secondary parallel transistors “tune” the W/L ratio of the main transistor. Thus, a digital signal via switches can control the flowing current through the terminals $S$ (source) and $D$ (drain).

1.3.2 Correction of the output current. 1B.

The Correction of the output current is a popular technique to calibrate a DAC. Instead of trimming every current source, this technique measures the output of the DAC, compares it to a desired value, and stores the difference (i.e. the error for the particular code). These three operations are executed for each possible DAC input during the “calibration phase”, usually at the beginning. During the “operation phase”, the already stored differences are added to the DAC’s own output, so that the error is corrected.

Figure 14 shows the high-level concept of this approach, a), and its usual implementation, b). Usually, the correction DAC only compensates for a number of MSB.
As a most recent practical example, the work of [Cong 2003] is recommended. It is a 14-bit current-steering DAC with segmentation 6-8, the error of the 6 MSB of which are compensated by a parallel CALDAC.

FIGURE 14. Correction of the output current: a) high-level concept; b) usual implementation.
1.4 Brief DAC literature overview

This chapter summarizes DAC performance, recently reported in literature and commercial offers. Various designs are ordered in Table 1, as well as their key-features, such as: architecture, resolution, supply voltage, process, power consumption, area, performance for a given input signal frequency and update frequency.

Graphical comparison is provided in Figure 15, Figure 16, Figure 17, and Figure 18. These DACs, the performance of which is situated in the right-upper corner of Figure 16 and Figure 15, represent the very-state-of-the-art in DA converters. These are: [Pirkkalaniemi 2002] with SFDR of 86 dB for input signal frequency of 11.4 MHz; [Bugeja 99] with SFDR of 74 dB for input signal frequency of 44 MHz; [Van der Plas 2000] with SFDR 84 dB for update frequency of 150 MHz; [Hyde 2002] with SFDR of 72 dB for update frequency of 250 MHz, and etc.

Figure 17 and Figure 18 illustrates the same DACs, ordered according to their area and power consumption. The DACs with a higher performance, in terms of SFDR, for minimal costs - area or power consumption, are in the left-upper corner. These are: [Schofield 2003] with SFDR of 90 dB for 0.3 mm² active area; [Tan 97] with 55 dB for 1.5 mW power consumption; [Tenhunen 97] with 60 dB for 6.5 mW power consumption.

TABLE 1. State-of-the-art reported DACs summary

<table>
<thead>
<tr>
<th>No</th>
<th>Reference</th>
<th>Architecture</th>
<th>Supply voltage</th>
<th>Process</th>
<th>Power [mW]</th>
<th>Area [mm²]</th>
<th>Signal freq. [MHz]</th>
<th>Update freq. [MSps]</th>
<th>SFDR [dB]</th>
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<tr>
<td>1</td>
<td>[AD 98]</td>
<td>Current-steering. Interpolation ratio of 4.</td>
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<td>CMOS</td>
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<td>-</td>
<td>5.01</td>
<td>32</td>
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<td>4</td>
<td>0.3</td>
<td>10</td>
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<td>4.43</td>
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<td>CMOS</td>
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<td>0.6</td>
<td>20</td>
<td>250</td>
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<td>5</td>
<td>CMOS</td>
<td>150</td>
<td>1.8</td>
<td>3.9</td>
<td>125</td>
</tr>
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<td>5</td>
<td>BiCMOS</td>
<td>650</td>
<td>4.8</td>
<td>10</td>
<td>100</td>
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<td>[Tesch 97]</td>
<td>Hybrid current-steering and R-2R ladder. Thermometer coded MSBs</td>
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<td>5/5.2</td>
<td>BiCMOS</td>
<td>650</td>
<td>17</td>
<td>2.03</td>
<td>10</td>
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<td>CMOS</td>
<td>1.5</td>
<td>4.8</td>
<td>3</td>
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<td>Supply voltage</td>
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<td>Area [mm²]</td>
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<td>1.23</td>
<td>10</td>
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<td>13</td>
<td>3</td>
<td>150</td>
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<td>±5</td>
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<td>500</td>
<td>8.2</td>
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<td>CMOS</td>
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<td>2</td>
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<td>1</td>
<td>0.1</td>
<td>100</td>
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<td>CMOS</td>
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<td>1.2</td>
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<td>0.44</td>
<td>60</td>
<td>320</td>
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</table>
FIGURE 15. DAC performance, reported in the literature: SFDR versus input signal frequency.

FIGURE 16. DAC performance, reported in the literature: SFDR versus update frequency.
FIGURE 17. DAC performance, reported in the literature: SFDR versus Area.

FIGURE 18. DAC performance, reported in the literature: SFDR versus Power consumption.
1.4.1 References


Introduction


2.0 System Level Design

This chapter discusses the system level choices that determine the general characteristics of the presented DAC. It starts with a basic discourse on Current Based DACs, segmentation, and intrinsic and calibration approaches. Subsequently, the architecture of the presented DAC is outlined. The chapter continues with the requirements for the current-cell output impedance and current source transistor matching. Finally, the elaborated calibration method and the developed calibration algorithm are presented and discussed. To keep the line of argument smooth, throughout this chapter some decisions are taken, the motivation of which is proposed at the end.

2.1 Concepts

2.1.1 Current based DAC

The analog values that can generate the output of the DAC usually are currents, voltages or charges. Last years’ publications and commercial offers show that the preferred type of DA converter is the current based one. This is not surprising given the higher achievable speeds, when currents are used as output analog values. In addition, the summation of currents is a straightforward operation, if compared to a summation of voltages, for example. The current based DACs are usually implemented as Current-Steering and rarely as Current-Division converters [Figure 19].

The Current-Division Converters use a single global current source, the generated current of which is divided according to the converted bits. The appropriate parts are combined at the output of the system. The accuracy of the system depends on the matching of the series resistance of the switches, Figure 19.

Alternatively, the Current-Steering converters use a set of current sources, as basic generators of analog values, which are switched and combined at the output of the system. The accuracy of the system depends on the matching of the current sources.

An important, fundamental disadvantage of the Current-Division converters is the need of enough matched current branches loads. This may be a major bottleneck for higher resolutions. Mainly due to this disadvantage, the Current-Division converters are not popular implementations.

Thus, the Current-Steering architecture is a preferred choice for a current based DAC and with time this architecture has become a synonym of the Current Based DAC. Commonly discussed problems of the Current-Steering implementations are the matching of the current sources and their finite output impedance. A closer look at these two problems is offered in Section 2.3 on page 37.
2.1.2 Current-Steering Binary, Thermometer, and Segmented DACs

An important architectural high-level feature of a Current-Steering (CS) DAC system is the level of segmentation. This characteristic shows what part of the converter is implemented as a binary and what part as a thermometer converter. The choice of the segmentation level is a complicated function dependent on the converter’s architecture, technology (layout issues), and the fundamental advantages of the binary and the thermometer type converters.

The CS binary converters use binary weighted currents to generate the output. The DC output of a binary DAC at time instant $nT$ is:

$$ A(nT) = A_0 \sum_{m=1}^{N} 2^{m-1} b_m(nT) $$

(EQ 9)

where $A_0$ is a common gain reference, $b_m(nT) \in \{0, 1\}$, $1 \leq m \leq N$, are the input bits, and $T$ is the update period of the DAC.

The major advantage of the CS binary converters is their compact, area-saving architecture. However, the accuracy requirements for the current sources become more and more stringent with every successive bit in resolution. This characteristic becomes a problem if the standard DAC specification of DNL<0.5LSB has to be achieved. The maximal DNL is set by the mid-scale transition, when the two most-significant bits, generated by two different currents, are switched. Then, the DNL error will be set by the square sum of the standard deviations of the two switching currents, times the number of the desired $\sigma$ confidence level. In the popular case, when the current sources are built-up by unit elements, the DNL error, for $1 \sigma$ confidence level, is given by [Bastos 98]:

$$ DNL \approx 2 \sigma \sum_{m=1}^{N-1} 2^{m-1} \left( \frac{\sigma_I}{I_{\text{unit}}} \right) [\text{LSB}] $$

(EQ 10)

where $N$ is the resolution of the DAC, $I_{\text{unit}}$ is the analog unit-element constructing the binary analog value, $\sigma_I$ is its standard deviation.

These stringent accuracy requirements, concerning the DNL specifications, are not a bottleneck in the thermometer type of converters. The thermometer-coded CS DAC architecture utilizes a number of equal current sources. The binary input code, comprising $N$ bits, is converted into a thermometer code, comprising $M=2^N-1$ bits, by a decoder. The output analog current is given by:

$$ A(nT) = A_0 \sum_{m=1}^{M} c_m(nT) $$

(EQ 11)

where $c_m(nT) \in \{0, 1\}$, $1 \leq m \leq M$ are the thermometer-coded bits.

As previously shown and as seen from EQ 11, the thermometer converters are monotonic. Hence, the relaxed requirements for currents matching, in comparison to CS binary converters, with respect to DNL specification. In fact, as long as the matching error is within a 50% margin, the DNL<0.5LSB specification is guaranteed. Moreover, compared to the CS binary architecture, the glitches, associated with the process of current switching, are also reduced, since for an increment/decrement of the signal value, bits are only turned on/off.
However, the thermometer converters occupy more area, require more internal connections, and need a binary-to-thermometer decoder. These drawbacks increase exponentially with every additional bit in resolution. Therefore, the CS thermometer DACs are considered impractical for resolutions of more than 8 bits.

The INL figure of merit is identical for both types of converters. It is mathematically the same, if unit-element approach is used. Statistically, the maximal INL error is expected at mid-scale, where most independent unit-currents are switched. Thus, for 1 \( \sigma \) confidence level, the INL error will be the square sum of the variances of the currents generating the output [Bastos 98], i.e.:

\[
INL \cong \sqrt{2^{N-1}} \times \left( \frac{\sigma_I}{I_{unit}} \right) [LSB]
\] (EQ 12)

The majority of recent CS DAC implementations employ segmentation. Segmented DACs have their Least-Significant-Bits implemented as a binary converter, allowing compact area and avoiding stringent accuracy requirements. Their Most-Significant-Bits are implemented as a thermometer converter, that provides relaxed accuracy requirements and avoids the exponential silicon area growth at higher resolutions. An interesting study on the balance of the segmentation level, i.e. how many LSB bits to be implemented binary and how many MSB bits to be implemented thermometer is done by P.C.W. van Beek in 2003 [van Beek 2003]. In the presented project, a segmentation level of 6-6 is chosen, i.e. a single segmentation where the 6 LSB are implemented as a binary converter and the 6 MSB as a thermometer one. Further discussion on this choice is offered in Section 2.5 on page 52.

2.1.3 Intrinsic and Calibrated CS DACs

As stated above, Current-Steering DACs rely on matching of the current sources, to achieve certain accuracy of the generated analog output. In general, the analog resources used to generate the analog output must be accurate enough, so that their combined product meets a certain specified INL figure of merit. Such requirements might be achieved by two approaches: an intrinsic approach and a calibration approach.

The intrinsic approach implies accuracy, thanks to technology. The converters employing this approach are called Intrinsic Converters. The analog elements generating the converter’s output are designed in such a way that they are accurate enough to generate together an output analog value, according to a specification. Such an approach assumes a very stable technology (a process to produce the chip) and a sufficient amount of silicon resources to achieve the required accuracy for the basic analog elements. While the former point is out of the scope of microelectronics designers, the latter is entirely a subject of their choice.

In general, there is always a trade-off between the accuracy of an analog microelectronic element and the area it occupies:

The bigger the element, the more accurate it is!

A first order explanation of that rule-of-thumb is as follows: The random mismatch is mainly dependent on four local physical causes, related to the process: edge effects, implantation and surface-state charges, oxide effects, and mobility effects [Pelgrom 89]. Since these are local and random, shapes of larger areas have better averaging than those of smaller areas.
This first order explanation is very primitive and incomplete of course, because a complete set of various factors and complex inter-correlations influences the analog parameters of microelectronic elements (e.g. $V_{th}$, current factor $\beta$, substrate factor $K$)\(^1\). On top of that the matching of two elements is also highly dependent on the way these elements are actually laid-out on the silicon. For a deeper insight in the subject, the reader is recommended the work of Bastos from 98 and Pelgrom from 89, [Bastos 98] and [Pelgrom 89].

Thus, intrinsic CS DACs give a particular emphasis on the built-in accuracy of the unit-current sources. That is why the latter are usually very large transistors. The relationship between the active area of a CMOS transistor, its operational point, the technology, and its expected accuracy is derived by Pelgrom in 89, see EQ 38. It is observed that to increase the accuracy of a DAC by 1 bit, four times bigger transistors have to be used. Therefore, the current-source transistors of an intrinsic design occupy a large portion of the chip and heavily depend on the random variations of the process parameters, such as $A_{v}$ and $A_{\beta}$ for example.

Any accidental shift of these values, any instability of the process, or inter-shift between layers of the process, would lead to a change of the DAC accuracy, hence the performance of the produced DACs. That is why intrinsic DACs are often over-designed, i.e. they are designed to perform better than specified, leaving a lot of margin to cope with any shift in the process parameters.

The other approach in DACs design employs calibration. The calibration approach implies accuracy, thanks to additional self-adjustment. This approach depends on the process parameters to a far smaller extent. Although not completely self-independent, the calibration approach can be considered technology decoupled, if compared to the intrinsic approach. The concept behind self-calibration is the ability of the DAC to perform certain set of extra operations, which lead to a more accurate analog output. Thus, the specified DAC accuracy is not built-in, but it is additionally reached by the converter, after power-on. Inherently, a calibrated DAC can adapt to shifts in the process parameters.

In all calibration approaches\(^2\), there always exists some additional circuitry to perform the operations of self-tuning. However, it is likely that these additional circuits influence the generated analog output and it is a designer's duty to minimize this drawback, so that only the benefits of calibration are in effect. Furthermore, employing calibration may lead to smaller converters, since intrinsically the analog elements are designed with relaxed accuracy specifications, i.e. smaller in size.

Nevertheless, calibrated DACs always comprise an intrinsic DAC core, which of course has relaxed specifications. Thus, the design of calibrated DACs includes a design of an intrinsic DAC core and a calibration add-on.

\(^1\) These might be: gate oxide, substrate doping, implantations, fixed oxide charge, edge roughness, mobility, lithography, etc.

\(^2\) See “Calibration techniques for Current-Steering DACs” on page 19.
2.2 Architecture

During the presented TWAIO project, a 12-bit Current-Steering DAC, employing 6-6 segmentation, with calibration was implemented. The designed converter has differential LVDS inputs for the input digital word and a differential current output, with a full-scale output current of 20.48mA. The converter's outputs are terminated by two 25Ω resistors. A block diagram of the designed DAC is presented in Figure 20.

The input of the DAC complies with the LVDS standard used by Xilinx, 1.2V DC level and bits amplitude of 200mV, i.e. digital one is 1.3V and digital zero is 1.1V. This input is passed to LVDS buffers, which amplify the signals. Further, the 12-bit differential signal is sampled by a set of flip-flops. The digital signal is split into 6-bits LSB and 6-bits MSB.

The MSB bits are encoded into 63-bits of thermometer code by a binary-to-thermometer decoder and the LSB bits are delayed by buffers in series with an approximately equal delay to that of the decoder. Equalizing the moments when the information appears at the inputs of the 69 Master-Slave latches, positioned just before the switching cell, hence just before the outputs of the DAC, is important, since every bit-switching will directly propagate to the outputs of the DAC via the parasitic capacitances in these flip-flops. The decoder works asynchronously. Thus, the information has to be again synchronized after it. The advantage of such an approach is that the implementation of the decoder is decoupled from the implementation of the flip-flops, e.g. the type of logic (CMOS, Differential-NMOS, Current-Steering, etc.). A disadvantage is that an asynchronous decoder always allows slower speeds than a synchronous one. On the other hand, if the decoder is synchronous, then the following flip-flop block can be reduced to a latch block, saving some silicon area and reducing the path of the signals. However, this is not always a optimal, because the signal path between the...
master/slave latching might be increased. In addition, a synchronized decoder requires a clock. Therefore, it must be of the same logic family as the following latches, so that the same clock is used.

Next, after the binary-to-thermometer decoder, the signals are directed to 69 Master-Slave Latches. These flip-flops are referred to as "analog", because of their sensitivity and importance to the quality of the generated converter's output. Thus, all physical processes, going on in these, are considered at a very low, analog level, hence the electrical signals of the carried information are of significant importance, though the information itself is still digital. The Master-Slave Latches synchronize the data and shape their physical signals in a proper way for the next block - the current switching cells.

The main task of the current switching cells is to combine the appropriate currents, generating the analog current output for the input digital word, being converted. The currents, or the analog elements, which are used to generate the analog current output, are placed in the block "Pool of Current sources". The thermometer currents generated by this block are fine-tuned by currents coming from the Array of CALDACs. The calibrated thermometer currents are passed to the current switching cells to generate the output of the converter.

The thermometer currents are fine-tuned by the CALDACs at the unit-element level: the coarse currents from the Pool of unit-current sources are combined with the fine currents of the Array of CALDACs before the current switching cells. Thus, the calibrated current sources might be considered as an entity. Therefore, the dynamic performance of the DAC does not deteriorate due to calibration.

In parallel with the above described core of the DAC, there are the components needed to perform calibration: a comparator, references, and a set of other sub-blocks.

According to the operation of the DAC, its sub-blocks can be classified as dynamic and static blocks. The circuits classified as dynamic are those which process dynamic signals, i.e. data signals and the converter's main clocks. On the other hand, the circuits classified as static are those which operate with static analog values (currents and voltages) during the normal operation of the converter.

The dynamic group includes: Input LVDS buffers & flip-flops, the decoder and the LSB delay line, the 69 differential flip-flops, and half of the current switch cells. The static group includes: the second half of the current switch cells, Pool of current sources, and Array of CALDACs. The calibration add-ons are neutral blocks, since they will be switched off during the normal operation of the DAC.
2.3 Requirements for the converter core sub-blocks

2.3.1 Finite output impedance

A well known problem in Switched-Current (SI) applications is the finite or limited output impedance of the current sources. Frequently, for the sake of calculations, a single current source is considered to have an infinite output impedance. However, if for example 4096, or $X$ in general, current sources are added in parallel their output impedances are combined also in parallel and the resulting common output impedance might significantly decrease. In addition, the value of the resulting output impedance, seen at the output of the converter, is a function of the combined in parallel current sources, i.e. it is correlated to the converted signal, hence is a source of accuracy problems in the DC domain, and distortion in the AC domain.

A model of the finite output impedance of the unit current sources is shown in Figure 21.

Thus, the output conductance of the used current sources is a function of the code, being converted. It comes in parallel with the load resistance, $R_L$, and causes an error current $I_e$. Therefore, the current going through $R_L$ is no longer the theoretically generated current by the converter, $I_{dac}$, but $I_{load} = I_{dac} - I_e$. If we express the value of the error current $I_e$ as a function of the finite output impedance of the unit current source, the signal current through the load resistor is as shown by (EQ 13).

$$I_{load} = \frac{X \cdot I_u}{1 + X \rho_G}$$  \hspace{1cm} (EQ 13)

where $I_{load}$ is the signal current through the load resistor, $X$ is the code being converted, $I_u$ is the unit-current source, $\rho_G = \frac{R_L}{R_u}$, $R_L$ is the load resistor, and $R_u$ is the finite output impedance of a unit-current source.

As mentioned above, this error current is a source of DC and AC errors. In the DC domain, we consider the INL and DNL specifications. Recalling the basic definition of DNL and INL:

$$DNL_X = \frac{I_{load}(X) - I_{load}(X-1)}{I_u} - 1 \text{ [LSB]}$$  \hspace{1cm} (EQ 14)

$$INL_X = \text{INL}_0 + \sum_{i=1}^{X} DNL_i = \frac{I_{load}(X) - I_{load}(0)}{I_u} - X \text{ [LSB]}$$  \hspace{1cm} (EQ 15)
where \( DNL_X \) is the DNL error for code \( X \), \( INL_X \) is the INL error for code \( X \). If we substitute (EQ 13) in (EQ 14) and (EQ 15), then the expressions for the DNL and INL errors as functions of the finite output impedance of the current-sources are as shown by (EQ 16) and (EQ 17):

\[
DNL_X \approx \frac{1}{(1 + X \rho_G)^2} - 1 \text{ [LSB]} \tag{16}
\]

\[
INL_X \approx \frac{X^2 \rho_G}{1 + X \rho_G} \text{ [LSB]} \tag{17}
\]

, with \( \rho_G = \frac{R_L}{R_u} \).

In the AC domain, the code-dependant output impedance causes distortion, hence deterioration of the SNDR and SFDR figures of merit. In 2001, Wikner showed that SNDR and SFDR can be expressed as functions of the resistance ratio \( \rho_G \). Wikner proposes the following expressions for SNDR and SFDR, given by (EQ 18) and (EQ 19).

\[
SNDR \approx -20 \log_{10} \rho_G - 6(N - 0.4) \text{ [dB]} \tag{18}
\]

\[
SFDR \approx -20 \log_{10} \rho_G - 6(N - 2) \text{ [dB]} \tag{19}
\]

, with \( N \) the resolution of the converter.

---

**FIGURE 22.** a) SNDR as a function of \( \rho_G \) for 10b, 12b, and 14b converters; b) SFDR as a function of \( \rho_G \) for 10b, 12b, and 14b converters; Simulated (solid) and Calculated (dashed) lines. From Wikner 2001.

Figure 22 shows the SNDR and SFDR figures of merit as a function of the conductance ratio \( \rho_G \), for 10b, 12b, and 14b DACs. Thus, the more bits in resolution, the more unit-elements are used, hence a greater value of the unit-element output impedance is required. Figure 22 suggests also a minimum conductance ratio \( \rho_G \) of \( 10^{-8} \), for a 12-bit DAC. With \( R_L = 25 \Omega \), the output impedance, \( R_u \), of a unit-current source should be more than 2.5GΩ. This requirement covers also the DC case, because DNL and INL are primarily determined by the mismatch of the current sources.

These requirements have to be considered carefully in a Calibrated DAC. Normally, the unit-current source transistors are reduced in size, depending on the depth of calibration. Therefore, the length of
their channels is much shorter than the lengths used in the intrinsic approaches. This reduces the output impedance of the whole current sources. To increase the output impedance to the specified value, more than one cascode transistors might be required.

On system level, it is possible to avoid the problem of the finite output impedance, by introducing a virtual ground node at the output of the DAC. Subsequently, the current sources see zero load impedance, hence $\rho_G = 0$. However, another design problem is introduced: the design of enough high-speed and linear buffer.

In order to keep the design of the DAC core simple and to concentrate the effort on the calibration, it was decided not to use the virtual ground node approach. Instead, the output impedance of the current sources is increased by cascode transistors.

---

1. In the intrinsic approaches, the sizes of the current source transistors are huge due to matching requirements. Inherently, the lengths of their channels are enough long to provide high output impedance. Thus, only a single casode transistor is normally used.
2.3.2 Unit-current sources matching

In the presented DAC design, the unit-current sources are implemented with NMOS transistors. These are always a subject of various types of mismatches. According to the definition of Pelgrom from 89, mismatch is the process that causes time-independent variations in physical quantities of identically designed devices. These variations are partly deterministic and partly random.

The deterministic mismatch. The deterministic variations are due to various gradients on the silicon wafer: gradients in ion implantation, doping, oxide thickness, etc. These errors can be compensated to a large extent by applying proper lay-out techniques. For example, a popular layout technique for the array of current sources is the common centroid layout, see Figure 24.

Linear gradients along x and y axes are assumed. All current sources are divided on four parts. Each of these four parts is so laid-out that when combined with the other three, the resulting current source generates a current, as if it was laid-out in the center of the common centroid structure. The example in Figure 24 shows the placements of two current sources, current source 1 and current source 2. These current sources are composed of four parts - a, b, c, and d. Parts a and d compensate the gradients along x axis for parts b and c. Analogically, parts a and b compensate the gradients along y axis for parts d and c. By applying common centroid or similar layout techniques, the effect of the deterministic mismatch can be minimized to a negligible level.

The random mismatch. Unfortunately, random mismatch cannot be compensated by layout techniques. However, it can be minimized to a desired level by increasing the active size of the current source transistor, as previously mentioned. To find out what this area should be, the currents generated by the unit-elements are presented as a sum of the designed current and an error current:

\[ I_u = I + \delta I \]

where \( I_u \) is the actual generated current, \( I \) is the current, set by the design of transistors’ W/L ratio, and \( \delta I \) is the error current due to the random mismatch in the current source transistor.

The error \( \delta I \) is considered a stochastic value with a normal distribution. Thus, the actual current \( I_u \) is also a stochastic value with a normal distribution, as given in EQ 20, mean \( \mu = I \) and standard deviation \( \sigma_u \), see Figure 25.

\[
f_\delta(x) = \frac{1}{\sqrt{2\pi}\sigma_u} e^{-\frac{(x-\mu)^2}{2\sigma_u^2}}
\]

(EQ 20)

where \( x \) is a particular value, \( f_\delta(x) \) is the normal PDF; \( \mu \) is the expected value; \( \sigma \) is the standard deviation.
The standard deviation, $\sigma_u$, is used to describe the stochastical properties of the unit-current source. 99.8% of all actual samples are expected in a region of +/- $3\sigma$ from the mean value. This region, i.e. spread, is often referred to as $3\sigma$ confidence level.

The work of Wikner from 2001 [Wikner 2001], expresses the dynamical figures of merit SNDR and SFDR as functions of the standard deviation $\sigma_u$ of the unit current sources:

$$\text{SNDR} = 6.02N + 1.76 - 10\log(1 + 3\sigma_u^2 2^{N+1})$$  \hspace{1cm} (EQ 21)

$$\text{SFDR} = 3(N + 3) - 10\log\sigma_u^2$$  \hspace{1cm} (EQ 22)

, where $N$ is the resolution of the converter.

In the DC domain, the mismatch of the unit-current sources highly influences the DNL and INL figures of merit. It was shown earlier in this text that DNL is dependent on the architecture of the converter. The accuracy requirements for binary converters are most stringent, followed by segmented architecture, and for the thermometer ones these requirements are most relaxed. Concerning the INL, the accuracy requirements are the same for both binary and thermometer converters.

INL is defined as the deviation of the actual converter's transfer function from the ideal transfer function, after the gain and offset errors are compensated, see Figure 26. Statistically, the maximal INL error is expected at mid-scale. At mid-scale, the output of the DAC is generated by half of all unit-current sources. Therefore, the stochastical variance of the converter's output will be the sum of the variances of the unit-current sources, building up the output current:

$$\sigma_{\text{mid}}^2 = 2^{N-1} \sigma_u^2$$  \hspace{1cm} (EQ 23)

Consequently, the maximal standard deviation of the converter’s output, at mid-scale, is shown by

$$\sigma_{\text{mid}} = \sqrt{2^{N-1}} \sigma_u$$  \hspace{1cm} (EQ 24)
Finally, if EQ 24 is normalized for 1 LSB and multiplied by 3 for 3 $\sigma$ confidence level, the frequently mentioned expression for the INL error is derived:

$$INL = 3\sqrt[2N-1]{\frac{(\sigma_u)}{I_u}} \text{ [LSB]}$$  \hspace{1cm} (EQ 25)

where N is the resolution of the DAC, $\sigma_u$ is the standard deviation of a unit element, $I_u$ is the DAC’s LSB element.

Equation EQ 25 gives an estimate of the accuracy requirement of the unit current source in order to design a N-bit linearity DAC.

Thus, for a 12-bit DAC with 12-bit accuracy and 3$\sigma$ confidence level, the relative matching of the unit element, $\frac{\sigma_{\text{unit}}}{I_{\text{unit}}}$, can be found from EQ 25:

$$\frac{\sigma_{\text{unit}}}{I_{\text{unit}}} = \frac{INL_{0.5\text{LSB}}}{I_{\text{unit}}\sqrt{2^{N-1}}} = \frac{0.5}{3\sqrt{2^{11}}} = 0.37\%$$  \hspace{1cm} (EQ 26)

Consequently, for a 12-bit DAC with 10-bit accuracy (close to the designed intrinsic DAC accuracy) and 3$\sigma$ confidence level, the relative matching of the unit element, $\frac{\sigma_{\text{unit}}}{I_{\text{unit}}}$, can be again found from EQ 25:

$$\frac{\sigma_{\text{unit}}}{I_{\text{unit}}} = \frac{INL_{2\text{LSB}}}{I_{\text{unit}}\sqrt{2^{N-1}}} = \frac{2}{3\sqrt{2^{11}}} = 1.48\%$$  \hspace{1cm} (EQ 27)

These results show that an intrinsic 12-bit DAC requires a minimum relative accuracy of its unit-current sources $\frac{\sigma_{\text{unit}}}{I_{\text{unit}}} = 0.37\%$. However, if calibration is used, then the converter can be designed intrinsically with lower accuracy, e.g. 10-bit, which will be further improved by calibration. 10-bit accuracy corresponds to an INL error of 2 LSB and a requirement for the relative accuracy of the unit-current sources of just 1.48%.
2.4 Calibration Method

One of the most important objectives of all common calibration techniques is to increase the DC accuracy of the DAC. Stated differently, calibration adjusts the actual DAC transfer function closer to the theoretical one, i.e. improves the INL figure of merit.

The calibration approach, applied in this project, aims at adjusting to a higher accuracy the individual contributions of the thermometer bits. In the classification proposed in Chapter 1.3 on page 19, it is of type 2A - Start-up Calibration.

The calibration method improves the DC DAC accuracy to a 12-bit level. It adjusts the currents of all thermometer current sources to a reference current source, constructed by the sum of all binary current sources plus 1 dummy LSB current source. This operation is executed once and the results of it are stored. During the normal operation of the DAC, the thermometer current sources generate fine-tuned currents, based on the results of the calibration.

2.4.1 Calibration requirements

The calibration method can improve DAC’s accuracy to the desired level, providing a minimum level of intrinsic DAC accuracy. Below we will derive: First, what the level of the intrinsic DAC accuracy should be, so that INL<0.5LSB can be achieved after calibration; Next, what the level of the post-calibrated relative accuracy should be, for a given intrinsic accuracy; Finally, what the step of the calibration should be, so that INL<0.5LSB can be achieved after calibration. The derivations are valid for a single segmentation.

From, EQ 25, we can express the INL as a function of the relative matching of the binary and the thermometer unit-elements, with $2^B - 1 \approx 2^B$:

$$INL = 3 \sqrt[4]{2^{N-1} - 2^B \left( \frac{\sigma_u}{I_{u,b}} \right)^2 + 2^B \left( \frac{\sigma_u}{I_{b}} \right)^2} \text{ [LSB]}$$  \hspace{1cm} (EQ 28)

, where $B$ is the level of segmentation, $\left( \frac{\sigma_u}{I_{u,b}} \right)$ is the accuracy of the unit-elements making the thermometer bits, and $\left( \frac{\sigma_u}{I_{b}} \right)$ is the accuracy of the unit-elements making the binary bits. Furthermore, we express the relative matching for the thermometer current source as a whole:

$$\left( \frac{\sigma_u}{I_{u}} \right) = 2^B \left( \frac{\sigma_u}{I_{u,b}} \right) \Rightarrow \left( \frac{\sigma_u}{I_{u,b}} \right)^2 = \left( \frac{\sigma_u}{I_{u}} \right)^2 2^{-B},$$  \hspace{1cm} (EQ 29)

, where $\left( \frac{\sigma_u}{I_{u}} \right)$ is the relative matching of the thermometer current sources.

We substitute EQ 29 in EQ 28, with $2^B - 1 \approx 2^B$:

$$INL = 3 \sqrt[4]{2^{N-1} - 2^B \left( \frac{\sigma_u}{I_{u}} \right)^2 + 2^B \left( \frac{\sigma_u}{I_{b}} \right)^2} \text{ [LSB]}$$  \hspace{1cm} (EQ 30)

EQ 30 also expresses the INL, but as a function of the relative matching of the binary unit-elements and the thermometer elements. For the case of the presented calibration method, EQ 30 expresses
that the INL figure of merit at half scale is related to the square root of the sum of the standard deviations of the binary elements plus the sum of the half of the thermometer elements’ standard deviations (being calibrated), times the level of confidence. When all thermometer elements are calibrated, then this formula can be interpreted in the following way: The maximum possible INL is related to the intrinsic unit-element matching (the elements that will not be calibrated) \( \frac{\sigma_a}{I_u} \), and the calibrated thermometer elements (the elements that will be calibrated) \( \frac{\sigma_t}{I_t} \).

From EQ 30, we can express the minimum intrinsic binary relative accuracy \( \frac{\sigma_a}{I_u} \) as a function of the relative accuracy for the calibrated thermo-current sources \( \frac{\sigma_t}{I_t} \), the level of the segmentation \( B \), for INL<0.5LSB, as:

\[
\frac{\sigma_a}{I_u} < \frac{1}{3} \sqrt{\frac{0.25 - 9 \times 2^B \times (2^{N-1} - 2^B) \times \frac{\sigma_t}{I_t}^2}{2^B}}
\]

(EQ 31)

Thus, the achievable relative post-calibration accuracy, \( \frac{\sigma_t}{I_t} \), determines how much the requirements for the intrinsic matching can be relaxed. That is why we have to find out up-to what accuracy level the thermometer elements should be calibrated. Again from (EQ 30) with \( INL = 0.5LSB \), i.e. accuracy level equal to the resolution:

\[
\frac{\sigma_t}{I_t} = \sqrt{\frac{0.25 - 3^2 \times 2^B \times (2^{N-1} - 2^B) \times \frac{\sigma_a}{I_u}^2}{3^2(2^{N-1} - 2^B)2^B}}
\]

(EQ 32)

(EQ 32) is a general expression for the relative accuracy to which the thermometer bits should be calibrated in a N-bit DAC, so that the overall accuracy after calibration is N-bit, i.e. INL<0.5LSB.

For the particular case of the presented DAC, i.e. \( N=12 \), \( B=6 \), \( \frac{\sigma_a}{I_u} = 0.0148 \), according to (EQ 32), the relative matching of the thermometer current sources should be tuned to a level of: \( \frac{\sigma_t}{I_t} = 330 \times 10^{-6} \).

2.4.2 Calibration algorithm

The proposed calibration algorithm adjusts the value of the element being calibrated by adding or subtracting an appropriate number of extra elements, in an iterative procedure, until the sum of all is equal, within a margin of one element, to that of a given reference element.

The concept of this calibration algorithm is shown in Figure 27, illustrating an example of a calibration. The seventh bit, the thermometer bit, \( I_{thermo} \), with intrinsic accuracy of 10-bit is calibrated to a relative accuracy of \( \frac{\sigma_t}{I_t} = 330 \times 10^{-6} \). The LSB bit for the presented DAC is chosen to be 5\( \mu \)A, hence the mean value of \( I_{thermo} \) is 320\( \mu \)A. Its standard deviation is \( \sigma_{I_t} = \sqrt{2^B \sigma_u} = 592nA \), hence the total area of its spread will be \( S_{99.8\%} = 6\sigma_{I_t} = 3.552\mu A \), (3\( \sigma \) confidence level). This area should be covered by the
device that will provide the additional elements for tuning. Thus, the full-scale output current of the caldac should be at least 3.552\( \mu \)A.

First the actual value (\( A' \)) is compared to a reference, \( I_{\text{ref}} \), equal to the designed value of \( I_{\text{thermo}} \). If the actual value (\( A' \)) is smaller/greater, a calibration LSB element, i.e. \( I_{\text{LSBCAL}} \), is added/subtracted and their common sum, (\( A'' \)) is again evaluated. Repeating this set of basic operations, the desired final value is successively approached and eventually reached (\( A''' \)).

The calibration step, \( I_{\text{LSBCAL}} \), should be chosen in such a way that the resulting standard deviation for the seventh bit becomes \( \sigma_{I_7} = 106nA \) (according to (EQ 32)), which corresponds to a 12-bit accuracy requirement. After calibration, the total spread of \( I_{\text{thermo}} \) will be \( S_{99.8\%} = 2\times I_{\text{LSBCAL}} \).

![FIGURE 27. Calibration of a 10-bit accurate \( I_7 \) into a 12-bit accurate \( I_7 \).](image)

All actual values that are situated on the left side of the reference current will be put, by means of calibration, in a region from \( \mu - I_{\text{LSBCAL}} \) to \( \mu \):

\[
g(x) = f(x) + \sum_{k=1}^{2^M-1} f(x-ki_{\text{LSBCAL}}), \quad x \in [-I_{\text{LSBCAL}}, 0] ,
\]

(\( \text{EQ 33} \))

where \( g(x) \) is the distribution function of the post-calibration; \( \mu \) is the mean value of the thermometer current, \( f \) is a normal distribution function, as given in EQ 20; \( M \) is the resolution of the CALDAC; \( I_{\text{LSBCAL}} \) is the LSB current of the CALDAC; \( k \) is a number of CALDAC LSB steps away from \( \mu \).

Respectively, all values that are situated on the right side of the mean value, \( \mu \), will be put, by means of calibration, in a region from \( \mu \) to \( \mu + I_{\text{LSBCAL}} \):

\[
g(x) = f(x) + \sum_{k=1}^{2^M-1} f(x+ki_{\text{LSBCAL}}), \quad x \in (0, I_{\text{LSBCAL}}] \]

(\( \text{EQ 34} \))
The post-calibration boundaries of the distribution of the calibrated current, shown in Figure 27 in dark, are fixed by the calibration step, \( I_{LSBCAL} \). The standard deviation \( \sigma_7 \) of the post-calibration distribution is a certain function of this calibration step, \( I_{LSBCAL} \). That function is related to the Probability-Density-Function (PDF) of the post-calibration distribution.

Assuming that the PDF of a current source has a normal distribution, after its calibration with the successive algorithm described above, its PDF is described by EQ 33 and EQ 34.

Figure 28 shows the graph of \( g(x) \). The standard deviation for \( g(x) \) has to be computed, in order to find the needed proper value for \( I_{LSBCAL} \) that guarantees a 12-bit DAC accuracy.

The above-given equations and presented calibration method were verified with a MATLAB simulation. 100000 normally distributed samples, with mean value \( I_7 = 320 \mu A \) and standard deviation \( \sigma_7 = 592 nA \) were used. These samples were calibrated by a 4-bit calibration DAC with a LSB step of 250nA. Figure 29 a) shows the histograms of the normally distributed initial 100000 samples. These samples were calibrated, resulting in a distribution as shown in Figure 29 b). Finally, Figure 29 c) shows the distribution of the absolute number of iterations for the calibration of a single sample, i.e. the distribution of the CALDAC words.

Furthermore, to simplify the analysis, we will approximate that the PDF of a calibrated current source, \( g(x) \), has a uniform distribution with a mean value \( I_{\text{thermo}} \) and a standard deviation:

\[
\sigma_{I_{\text{cal}}} = \frac{I_{LSBCAL}}{\sqrt{3}}
\]  

Then, we require that the standard deviation of the calibrated current source is within particular boundaries, so that the sum of all respective variances stays within the necessary accuracy of the converter.

For example, if we require a 12-bit accuracy, as shown above the standard deviation should be \( \sigma_{I_{c}} = 106 nA \). Using it in EQ 35: \( I_{LSBCAL} = \sqrt{3} \sigma_{I_{\text{cal}}} = 184 nA \). For the general case, from EQ 32, the step of the calibrating unit should be:
EQ 36 represents in a general case the requirements for the size of the calibration step $I_{LSBCAL}$, so that $INL_{max}$ is reached, starting from a particular intrinsic relative matching $\left(\frac{\sigma_t}{I_t}\right)$, for segmentation $B$, for a thermometer current $I_t = 2^B I_u$ (being calibrated), and resolution $N$.

As shown, if the post-calibration distribution is assumed to be uniform, then it is easy to calculate its standard deviation. However, the distribution of Figure 27 is not uniform but it has a greater probability towards its center, hence its standard deviation will be smaller than the standard deviation of the uniform distribution. This means that if the $I_{LSBCAL}$ step is designed to be sufficient for a particular DAC accuracy, assuming uniform post-calibration distribution, in reality a higher DAC accuracy will be achieved. Therefore, the error, coming from the assumption that the post-calibration distribution is uniform, can be used as a design margin.

**2.4.3 Calibration implementation**

An implementation of the discussed calibration algorithm is designed. The implementation uses a reference current source, a temporary current source, and a current comparator to sense the difference between a reference current and the current under calibration.

The reference is called also a binary reference, as it is the sum of the binary current sources plus 1 LSB, i.e. its expected current is equal to the thermometer current:

$$I_{binref} = I_{LSB} + \sum_{m=1}^{B / 2^N - 1} 2^{m-1} b_m$$  \hspace{1cm} (EQ 37)

The temporary current source generates a current, $I_{temp}$, the value of which is equal to the thermometer current. This current source is used to record the value of the unavoidable comparator’s input offset current, $I_{offset}$.

This implementation of the calibration algorithm can be considered in two phases, phase $A$ and phase $B$. During the first phase, phase $A$, $I_{temp}$ is calibrated to $I_{binref}$. By doing that $I_{temp}$ not only records the value of $I_{binref}$, but also the comparator’s input offset current. During the second phase, phase $B$, each thermometer current source, $I_{thermo#i}$, is calibrated to $I_{temp}$. By doing that the comparator’s input offset is cancelled, so that $I_{thermo#i}$ is offset free.

The calibration logic is organized in a Finite-State-Machine (FSM), the state diagram of which is shown in Figure 30.
After Reset, the FSM goes to state 0 and waits for the signal Start_cal to move to state 1 and actually start the calibration. Once in state 1, phase A begins. $I_{\text{temp}}$ and $I_{\text{binref}}$ are enabled. In state 2, $I_{\text{temp}}$ and $I_{\text{binref}}$ are compared and the polarity of the calibration current is chosen. State 3 can be repeated several times. In this state, the calibration current, fine-tuning $I_{\text{temp}}$ is successively increased until its value is sensed greater than $I_{\text{binref}}$. Should this happen, the calibration current is decremented and phase A is concluded: $I_{\text{temp}} = I_{\text{binref}}$.

Phase B begins with state 4. $I_{\text{binref}}$ is disabled. The calibration option of $I_{\text{temp}}$ is disabled, too. The first thermometer current source is enabled. States 5, 6, 7 repeat the basic operations descibed in phase A but calibrating a thermometer current to $I_{\text{temp}}$. Once, all the thermometer current sources are calibrated, phase B concludes and the DAC is considered calibrated.

A block diagram of the calibration implementation is shown in Figure 31. A Current Comparator is used to sense the difference between the current being calibrated and its reference. The unavoidable input offset, $I_{\text{offset}}$, of the current comparator is drawn in gray. The purpose of using $I_{\text{temp}}$ is to record this input offset. Subsequently, calibrating the thermometer current sources to $I_{\text{temp}}$ will cancel the offset current. This input offset might be as large as the FS of the CALDAC of the $I_{\text{temp}}$ allows.

The main components used by this implementation of the calibration algorithm, the current sources, the CALDACs, and the current comparator, are with relaxed design requirements.
The use of $I_{\text{temp}}$ alters the derived in Section 2.4.1 on page 43 post-calibration PDF. It is indeed increased by the post-calibration PDF of $I_{\text{temp}}$, see Figure 32. This is a drawback of the chosen approach, in its part of comparator’s offset compensation. A solution is to reduce the calibration steps, shrinking the post-calibration PDFs.

Another approach to compensate for the offset was considered. It is a two step calibration of the thermo current sources. A brief description of it is as follows. First, the thermo current source is calibrated to the binary reference, recording the offset, and the result is stored. Next, the thermo current source is again calibrated to the binary reference, but their places at the inputs of the comparator are swapt, recording the offset with a negative sign. The second result is also stored. The final result will be the mean of both results, hence cancelling the offset. However, such a type of implementation was found complicated. It would increase significantly the silicon area of the calibration logic and introduce complexity in switching the current sources to the comparator. Thus, this approach was not chosen, but it deserves further research.
Another calibration approach, a variation of the implemented one, was also considered. It minimizes the width of the post-calibration PDF. This approach suggests to calibrate all thermometer current sources to the same side (left or right) of the reference current source. This is possible, if the polarity of the calibration current is taken into account, i.e. the side (left or right) in which the actual intrinsic sample is positioned. When the actual sample is found on the chosen calibration side, its last increment is discarded (like in the transition from state 6 to state 7, in Figure 30). When the actual sample is positioned on the other side, its last increment is stored (during the transition from state 6 to 7, there will be no decrement, see Figure 30). Figure 33 illustrates this alternative.

In terms of DNL and INL accuracy, no improvement is expected with regard to the original implementation of the calibration algorithm, since the mean value of the post-calibrated thermo current source is different from the intrinsic one, though the width is smaller. Improvement is expected in the dynamic performance, because the thermometer currents will be more accurate with regard to each other.

This approach was not implemented because, it makes the calibration logic more complicated. It was decided to implement and test the core algorithm first. However, this variation of the algorithm deserves further research.

2.4.4 Calibration algorithm simulations

The above-presented equations were verified by MATLAB simulations, based on the already developed models provided with the book of Jespers [Jespers 2001]. The simulations, shown in Figure 34, present the INL and DNL figure of merit for 100 random sets of the elements’ values of a 12-bit DAC with 6-6 segmentation. Only the elements’ accuracy is simulated, not the calibration algorithm itself. The input of the DAC is normalized to a [-1; 1] scale.

Figure 34 a) shows the INL and DNL of a 12-bit DAC with 10-bit accuracy, before calibration. The matching of the unit-elements is as given by EQ 27. The INL approaches 2LSB limit, i.e. 10bit accuracy, and the DNL stays around 0.5LSB, thanks to the segmentation.
Figure 34 b) shows the INL and DNL of a 12-bit DAC with 10-bit accuracy, after the calibration of the thermometer bits, as given by EQ 32 with the following derived result for the case of the presented DAC. INL stays within the 0.5LSB limits, as calculated. The DNL is also reduced in comparison with a).

Figure 34 c) shows the INL and DNL of a 12-bit DAC with 10-bit accuracy, after the calibration of the thermometer bits, as given by EQ 36. The PDF of the post-calibrated thermometer elements is assumed uniform with width of \( \sqrt{\frac{1}{3}} \times \left( \frac{\sigma_t}{I_t} \right) = \sqrt{3} \times 330 \times 10^{-6} = 572 \times 10^{-6} \). The INL and DNL stay within 0.5LSB boundaries.

Figure 34 d) shows the INL and DNL of a 12-bit DAC with 10-bit accuracy, after the calibration of the thermometer bits, as given by the implementation with offset compensation. The PDF of the post-calibrated thermometer elements is assumed uniform with width of \( \sqrt{\frac{1}{3}} \times \left( \frac{\sigma_t}{I_t} \right) = \sqrt{3} \times 330 \times 10^{-6} = 572 \times 10^{-6} \). The offset due to \( I_{\text{temp}} \) from Figure 32, is simulated with an uniform distribution with half of the width of the thermometer elements one, \( 286 \times 10^{-6} \). Due to the temporary current source the uniform distribution may shift. The uniform distribution of the temporary current source is simulated with half of the width of the thermometer one. The INL and DNL still stay within 0.5LSB boundaries.
2.5 System level decisions

The following text explains some of the previously introduced system-level decisions in this Chapter. These have a major impact on the overall design and performance of the DAC. The most crucial choices to be taken were as follows:

1. What and when to calibrate.

It was decided to calibrate only the thermometer current sources. These are identical, so a common calibration circuitry can be used. The binary currents scale down with the powers of two. The impact that they have on the output of the DAC, scales down with the same pace, too. On the other hand, to calibrate a single binary current, specific circuitry should be used (a reference current source, connections, and a current comparator). Thus, the choice to calibrate only the thermometer current source is motivated by the common calibration resources and the greater impact on the output of the DAC.

It was decided to perform calibration only once and to store the results. Thus, the calibration capabilities remain transparent, during the normal operation of the DAC. They do not influence the dynamic performance.

2. What level of segmentation to be used.

The level of segmentation has a direct impact on the calibration. The greater the segmentation, the more thermometer bits are calibrated, the greater the benefits of the calibration. However, the choice of the segmentation level was mainly influenced by previous experience in the MsM group. Two successful projects with 6-6 segmentation were recently accomplished. It was believed that segmenting more than 6 bits (hence 63 thermometer bits) would increase the complexity of the DAC core and particularly the complexity of the layout. Therefore, a segmentation of 6-6 was assumed as a starting point of that project.

3. What intrinsic accuracy to be designed.

The choice of the intrinsic accuracy of the DAC core is closely related to the segmentation level. There is a practical limit, in the case of the 6-6 segmentation, for the intrinsic accuracy. When the impact on the output of the DAC of the non-calibrated binary part becomes too large, there is no practical thermometer-bits calibration that can keep INL<0.5 LSB, see EQ 36. This practical limit is between 9bit and 10bit accuracy. More precisely, with intrinsic accuracy of a unit element \( \frac{\sigma_{I_u}}{I_u} > 2.1 \% \), the impact of the binary part on the maximal INL for the output of the DAC, with 3\( \sigma \) confidence level, is already more than 0.5 LSB. Therefore, it can be considered that 10bit intrinsic accuracy is the practical minimum for the proposed calibration method, for the case of 6-6 segmentation. In practice, it has been chosen slightly higher intrinsic accuracy level, as it will become clear in Section 3.1.4 on page 57.
3.0 Transistor Level Design

This chapter presents the transistor schematics and simulations of the main DAC's building blocks. It starts with the DAC Core, the discussed components of which are the Binary-to-Thermometer Decoder, the Current-Steering Master-Slave Latches, the Current Switching Cells, and the unit element approach used for the current source transistors. The second part of the chapter presents the circuits comprising the calibration capability of the DAC, including the CALDACS, the Current Comparator, the Calibration Logic, and the Reference Current source. The chapter concludes with discussion on some calibration simulations.

3.1 DAC Core

3.1.1 Thermometer Decoder

The thermometer decoded architecture is designed according to the widely used Row-Column decoder, firstly proposed by Miki in 86 [Miki 86], shown in Figure 35. It converts the 6 MSB bits into a 63bit thermometer code. It is asynchronous and fully differential.

The decoder consists of two identical Column and Row decoders. The former converts bits 7, 8, and 9, and the latter converts bits 10, 11, and 12.

The logic levels used by the decoder are gnd/vdd, as defined by the CVSL logic. The consumed power is dynamical. It depends on the rate with which the inputs are changing and the load capacitance at the outputs of the converter. In addition, due to layout consideration the thermometer bits are decoded in groups of 9, i.e. the decoder is divided on 7. Thus, the column decoder is repeated 7 times and the ROW decoder is implemented in 9 groups of three cells. Further insight is proposed in Section 4.3.6 on page 74.
The basic principle of the CVSL logic, used to implement the gates in the decoder, is shown in Figure 36. It has a crossed coupled PMOS pair, which switches the outputs according to the NMOS and the inverted NMOS logic at the gates’ inputs. A design requirement for this type of logic is that the PMOS transistors are weaker than the NMOS transistors in the NMOS logic. So, the NMOS logic can override the settled output levels by the PMOS pair. Therefore, the sizes of the PMOS transistors are designed equal to those of the NMOS, since the mobility of the holes (for PMOST) is always lower than the mobility of the electrons (for NMOST).

### 3.1.2 Master-Slave Latch

The information coming from the Decoder (63 thermo MSB) and that from the delay line (6 binary LSB) is synchronized by 69 current-steering flip-flops. These are organized in a Master-Slave configuration as shown in Figure 37.

![Master-Slave Latch Configuration](image)

The Master and the Slave latches are identical. So are both buffers $B$ and $D$. The outputs of the latches are directly connected to the current switches of the current switch cell. Thus, the second buffer, buffer $C$, is also a driver for the current switches. Therefore, the shapes of the latch blocks’ output signals, their purity, and synchronization, are very important design objectives. To meet these, even at higher clock rates, the logic of the latches is chosen to be Current-Steering Logic. The transistor schematics of the Buffers and of the Latches are shown in Figure 38.

![Current-Steering Logic: a) a Buffer; b) a Latch](image)

The latches and the buffers are designed similar, i.e. having identical transistors’ sizes and resistor values. Such an approach brings symmetry and a level of regularity in the layout. Furthermore, these blocks operate at the same logic levels: 2.5V and 1.7V. The choice of the lower logic level sets the crossing point of the differential signals controlling the current switching process in the current...
switch cell. As a rule of thumb, the higher this point is, the better for the current switch cell. More discussion about the effects of the logic levels on the current switches will be provided in the Current Cell chapter.

Figure 39 shows the processing of the digital signals inside the Master-Slave Latches. On top, the differential clock signals are given. A design goal is to have clock signals with as sharp rising and falling edges, as possible, so that the transient switching processes in the clocked blocks are kept short. The rising and the falling edges of the clock signals are 700ps.

Furthermore, a CVSL signal coming from the decoder is shown, Figure 39 b). It appears with 900ps asynchronous delay after the clock. Its rising and falling edges are neither equal nor sharp. An important aspect of the Master-Slave Latches is to convert these rough digital bits into smooth and well synchronized signals with short rising and falling edges and a different logic level. The signals first pass through the Master-Latches and the Master-Buffer, see Figure 39 c) and d). The effects of the clock-feedthrough (point A) and signal-feedthrough (point B) appear at the outputs of the Master Latches as disturbances with amplitudes up-to 100 mV. Such glitches propagate through the parasitic transistors’ capacitancies to the output of the DAC. Therefore, a high design priority is to minimize their energy.

Finally, the outputs of the Master Latches are followed by the Slave Latches Figure 39 e) and f). The signal disturbancies due to clock-feedthrough (point C) remain the same, but those due to signal-feedthrough overlap with a clock-feedthrough, resulting in a single glitch with a greater energy (point D). The output signals of the Slave-Latches, with rising and falling signal edges limited to 100ps, are provided as control bits to the current switching cell.

The current consumption of the Master-Slave Latches is constant with regard to the clock frequency. The current needed to sample a single bit of information is \(4 \times 266.66 = 1.07\, mA\) (the constant current
flowing through the Master Latch, the buffer, the Slave Latch, and the driver). Hence, the current needed for all 63 thermometer bits and 6 LSB is 73.6 mA.

### 3.1.3 Current Switching Cell

The current switching cell is the actual place where the bit currents are summed and provided as an output of the DAC. It is designed in way to accommodate the options of calibration, but it can be also used without these. A transistor schematic of the thermometer current switching cell is shown in Figure 40. Its design is largely based on the work of Pieter van Beek on the optimization of the current cell with respect to dynamic performance [van Beek 2003]. The binary current cells scale down with the amount of the binary current. $M1$ is the current source transistor. At its drain the contribution of the CALDAC is added. The output impedance of both the nominal current source ($M1$) and the CALDAC is increased by the cascode transistor $M2$. The second cascode ($M3$ and $M3a$) is used also as a switch to redirect the current either to the current switches or to the current comparator for calibration. $M4$ and $M5$ are the current switches that redirect the signal current either to the positive output or to the negative output of the DAC. $M6$ and $M7$ are cascode transistors that shield the entire current switch cell from the output of the DAC.

The control signals, coming from the Slave Latch are given as data signals in Figure 40. As previously mentioned their crossing point is of interest for the proper operation of the current source transistor $M1$.

If the crossing point is chosen too low, then the switching process will go in the following way: the switch transistor, due to be turned off, say $M4$, will have a decreasing voltage at its gate, starting from $vdd$. Meanwhile, the increasing voltage at the gate of the other switch, $M5$, will be too low to turn it on. This scenario results to an increasing impedance at the common source point of $M4$ and $M5$ ($M4$ increases its impedance and $M5$ is not turned on yet). Subsequently, the voltage at the drain of $M1$ will decrease. If this voltage drops enough, it might even push $M1$ out of saturation!
On the other hand, this scenario cannot be completely avoided, i.e. there will be always some variation at the drain of M1. A design objective is to minimize these fluctuations. Figure 41 shows the effect of current switching on the drain voltage of M1. Although the crossing point of the data signals is chosen high, M5 still needs time to get in a proper ON mode, while M4 decreases its impedance almost immediately. Subsequently, a voltage drop is observed at point A. These voltage variations at the drain of M1 are minimized to a level of 1mV and a saturation margin of 30mV is allocated for the operation point of M1.

3.1.4 Unit-element approach

The current sources are based on unit current source transistors. The standard unit-element approach implies that the LSB bit is the unit-element, the second bit is two unit-elements in parallel, the third - four units, and so forth. Thus, the unit-current source array for a 12b DAC would have 4096\(^1\) unit elements.

To save half of the non-active silicon area, the unit-element is chosen to be the second bit. Thus, the unit-element array consists of 2047 unit elements. The channel of the unit element is designed with \(W=2\mu m, L=4\mu m\), Figure 42.

According to Pelgrom’s formula, EQ 38, the parameters of the UMC25 process, and the transistor’s biasing, the unit-element would have relative matching of \(\frac{\sigma_I}{I} = 7.3 \times 10^{-3}\), hence for the converter’s output and for 3 \(\sigma\) confidence level, the intrinsic accuracy \(INL = 9.9\mu A\), i.e. DC DAC’s accuracy slightly more than 10 bits.

---

1. 4095 signal element plus a dummy LSB element for the binary reference in the calibration.
\[ \frac{(\sigma_I^2)}{I} = \frac{1}{2} \left[ \frac{A_{\beta}^2}{(WL_{\min})} + \frac{4A_{VT}^2}{(V_{gs} - V_{th})^2} \right] \]  

(Eq 38)

where \( A_{\beta} \sim [\mu m \times 10^{-2}] \) and \( A_{VT} \sim [mV \times \mu m] \) are technological constants, which express the deviation of respectively \( \beta \) and \( V_{th} \) as a function of the transistors’ area; \( (V_{gs} - V_{th}) = V_{os} \) is the overdrive voltage of the current source transistor; \( \frac{(\sigma_I^2)}{I} \) is the relative accuracy.

![Figure 42](image.png)

**Figure 42.** Unit-element approach: a) doubling L with 2 unit elements in series; b) increasing W with N elements in parallel.

Table 2 summarizes the sizes of the current sources. Bit 1 is constructed as shown in Figure 42 a), Bit 2 is the unit element, and Bit 3, 4, 5, 6, and 7 (the thermo bit) are constructed as shown in Figure 42 b).

<table>
<thead>
<tr>
<th>BIT</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
</tr>
</thead>
<tbody>
<tr>
<td>W/L</td>
<td>( \frac{2}{4} \times \frac{2}{4} )</td>
<td>( \frac{2}{4} )</td>
<td>( 2 \times \frac{2}{4} )</td>
<td>( 4 \times \frac{2}{4} )</td>
<td>( 8 \times \frac{2}{4} )</td>
<td>( 16 \times \frac{2}{4} )</td>
<td>( 32 \times \frac{2}{4} )</td>
</tr>
</tbody>
</table>

### 3.1.5 DAC Core Dynamic Performance

The dynamic figure of merit, being considered mainly in this project, is SFDR. This is the preferred figure of merit for a DAC dynamic performance, according to the literature survey in Section 1.4 on page 23. The majority of the covered 12-bit DACs show SFDR=65 [dB] for 10MHz input signal at update frequencies of around 200-300MHz. These are measurement results and it is not fair to compare them with the below discussed ideal dynamic simulations of the presented DAC core.

The optimal dynamic performance\(^1\) of the DAC core is up to 20MHz signal frequency at 400MHz update frequency. The output frequency spectrum for these specs is shown in Figure 43. The SFDR is 79[dB] and it is between the main harmonic, point \( A \), and the third harmonic, point \( B \). The power of the even harmonics (between points \( A \) and \( B \)) at 400MHz update frequency is significant, but it is still 20 [dB] less than the third harmonic. A common estimation is to expect in reality around 10[dB] drop of the SFDR, due to current-sources mismatch and layout impact.

The proposed DAC core is based on high-speed DAC designs, which had been previously designed in the MsM group, mainly leaded by Kostas Doris. A property of these high-speed designs is the cur-

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\(^1\) All dynamic simulations are performed with ideal transistors (no mismatch) due to practical difficulties to execute a true Monte-carlo simulation. Therefore, all presented results here concern “best-case” scenario.
rent-steering master-slave latches, which allow faster and purer differential switching signals for the current-switching cell. This is a main difference between the proposed DAC Core and those 12-bit DACs studied from the literature.

For the proposed DAC core, when the update frequency is increased, then energy of the even harmonics increases too, due to non-differential errors in the process of current switching, as it was explained in the previous chapter.

Analogically, if the update frequency is decreased, then these errors become relatively smaller with respect to the update period, so the even harmonics have less power, see Figure 44 a). However, the SFDR remains the same, as it is set by the ratio between the signal and the greatest, usually the third or the fifth, harmonic.

The power of the third harmonic is determined mainly by the input signal frequency. Doubling the input signal frequency causes growth of the power of the third harmonic with 10 [dB], hence a decrease of SFDR to 70 [dB]. The output spectrum of the DAC for 40MHz input signal frequency at 400MHz update frequency is shown in Figure 44 b).
Table 3 summarizes the dynamic performance of the proposed DAC core. All results concern ideally matched transistors. These reported numbers of SFDR represent the “best-case” scenario.

**TABLE 3. SFDR, HD3, and HD5 as a function of the input signal frequency and the update frequency.**

<table>
<thead>
<tr>
<th>Signal Freq.</th>
<th>Update Freq. 50MHz</th>
<th>100MHz</th>
<th>200MHz</th>
<th>400MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>5 MHz</td>
<td>SFDR=77.9</td>
<td>SFDR=78.8</td>
<td>SFDR=81.5</td>
<td>SFDR=85.6</td>
</tr>
<tr>
<td></td>
<td>HD3=77.9</td>
<td>HD3=85.7</td>
<td>HD3=82.9</td>
<td>HD3=85.6</td>
</tr>
<tr>
<td></td>
<td>HD5=82.3</td>
<td>HD5=83.6</td>
<td>HD5=83.7</td>
<td>HD5=93</td>
</tr>
<tr>
<td>10 MHz</td>
<td>SFDR=90.5</td>
<td>SFDR=78.8</td>
<td>SFDR=79.1</td>
<td>SFDR=78.2</td>
</tr>
<tr>
<td></td>
<td>HD3=78.8</td>
<td>HD3=88.5</td>
<td>HD3=84.1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>HD5=81.8</td>
<td>HD5=83.5</td>
<td>HD5=84.2</td>
<td></td>
</tr>
<tr>
<td>20 MHz</td>
<td>SFDR=82.6</td>
<td>SFDR=78</td>
<td></td>
<td>SFDR=79</td>
</tr>
<tr>
<td></td>
<td>HD3=80</td>
<td></td>
<td>HD3=79.1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>HD5=78</td>
<td></td>
<td>HD5=79</td>
<td></td>
</tr>
<tr>
<td>40 MHz</td>
<td>SFDR=77</td>
<td></td>
<td>SFDR=69.1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>HD3=69.1</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>HD5=71.3</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>80 MHz</td>
<td></td>
<td>SFDR=64.5</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

The presented simulation results are for signal input frequency that is an integer number of the update frequency. This means that every simulated signal period in time domain, is constructed by the same simulated points with regard to the output signal period. This helps to easier acquire an integer number of simulated sinewave periods for the FFT, but might hide any non-linearities in-between the simulated points.
3.2 Calibration Add-on

3.2.1 CALDAC

Calibration DACs (CALDACs) provide the fine-tune current to the thermometer current sources. They are binary-encoded DC mini-DACs. The calibration word is set by the calibration logic during the calibration phase. It is stored inside the CALDAC and is used during the normal operation of the DAC.

The resolution of the CALDAC is 5bits and its LSB current, $I_{LSBCAL} = 200nA$. The direction of the current (add or subtract) is set by a polarity switch, see Figure 45. Thus, the effective CALDAC resolution is 6 bit, i.e. its full-range is $12.8\mu A$. The CALDAC FS has to cover the intrinsic spread of the thermometer currents, so that the calibration algorithm can tune the DAC to a 12-bit level. The FS of the CALDACs is designed with a lot of margin. The intention is to investigate the behaviour of the calibration, when smaller calibration steps are applied in the prototype chip.

The accuracy requirements of the CALDAC are relaxed given the fact that its $I_{LSBCAL}$ step is very small with regard to the thermometer current. Therefore, it is only required a monotonicity from the CALDAC:

$$DNL_{CALDAC} < 0.5 \times I_{LSBCAL}$$  \hspace{1cm} (EQ 39)

In binary architectures, the largest DNL appears during switching the MSB bits, hence bit 4 and bit 5. Therefore, the relative matching of the unit-elements of the CALDAC must be smaller than $\frac{\sigma_I}{I_{LSBCAL}} < 20.8 \times 10^{-3}$, according to:

$$DNL_{CAL} = 3 \times 2^{\frac{N-1}{2}} \times \frac{\sigma_I}{I_{LSBCAL}}$$  \hspace{1cm} (EQ 40)

$$\frac{\sigma_I}{I_{LSBCAL}} < \frac{DNL_{CAL}}{3 \times 2^{\frac{N-1}{2}}} < \frac{0.5}{3 \times 2^{\frac{4}{2}}}$$  \hspace{1cm} (EQ 41)

The transistor schematic of the CALDAC is shown in Figure 46. To generate the calibration current, an unit-element approach is used. Furthermore, the implementation of the polarity switch is straightforward. There are no accuracy requirements for the polarity switch.
To set the polarity of the calibration current, a simple current mirror is either used or skipped, see Figure 46. Transistor implementation of the CALDAC.

Figure 47. In addition, the polarity switch effectively increases the resolution of the CALDAC with 1 bit for less silicon resources.

Figure 47. Transistor implementation of the polarity switch.
3.2.2 Temporary Current source & CALDAC

The Calibration algorithm uses a temporary current source to record the value of the sum of the binary current sources plus 1 LSB and the unavoidable input offset of the current comparator. Further, it calibrates all the thermometer current sources to that reference resulting in an offset cancelation, see Section 2.4.1 on page 43.

The temporary current source is built-up exactly in the same manner as the thermometer current sources. It is always connected to one of the comparator’s inputs. The reference current source is calibrated by a 6 bit of thermometer CALDAC plus a Polarity switch. The LSB current of the reference CALDAC is 100nA. It is desired that the error in the calibration of the reference current source is minimized, because all the thermometer current sources are calibrated to it. Any error in its calibration will appear as a DNL error during every transition of the code at bit 6 to bit 7 (binary boundary). This error will also influence the dynamic performance of the DAC.

The presented calibrated DAC uses a 6-bit thermometer CALDAC of the I_temp with 1LSB step of 100nA. The FS of this CALDAC is 6.4µA, which is multiplied by 2 by a Polarity switch. 3.6µA of these are reserved for the mismatch between I_temp and I_binref. Thus, the comparator input offset is allowed to be 9.2µA for an operation current of 320µA.

3.2.3 Current Comparator

A current comparator is implemented to compare the current being calibrated with a reference current. Its 1-bit output is used by the calibration logic to increment/decrement the CALDAC word or to proceed to a new state.

The specifications of the current comparator are relaxed to an offset current of I_{offset}=9.2 [µA]. These come from Full-Scale (FS) of the CALDAC of the temporary current source used in the calibration, see Section 3.2.2 on page 63.

The speed of the current comparator is not important, because the calibration phase is executed once after the chip is powered-up, hence its clock might be as slow as necessary.

The simplest current comparator is the current mirror comparator, shown in Figure 48.

It has low impedance inputs and a high impedance output. This structure is not convinient for the presented calibration algorithm, because for the case of the presented DAC, both input currents, I_a and I_b, are coming from the current source, i.e. from NMOS transistors. Therefore, an additional current-mirror structure, in front of the current mirror comparator, has to be used.

A more compact solution is proposed by Traff in 92, [Traff 92] which was also used in a calibration DAC [Tiilikainen 2001]. Based on their approach, a current comparator is designed. Its transistor schematic is shown in Figure 49.
The current comparator is composed by the components given in black. Those drawn in gray are the actual current sources being compared.

The designed current comparator has low impedance inputs and a low impedance output (at point S).

It is composed of a current mirror (M5-M8), a push-pull stage (M1-M2), and a gain stage (M3-M4). The current mirror subtracts the compared currents at point S.

For big current differences $|I_a - I_b| > I_s$, either M1 or M2 is on, and the impedance level at point S is low. Therefore, the voltage at point S changes slowly with the current difference. The output of the inverter M3-M4 keeps the push-pull stage on and provides the logic level for the following inverter, which shape the output of the comparator.

For small current differences $|I_a - I_b| < I_s$, both M1 and M2 are off, and the impedance level at point S is high. This operation region is referred to as “dead zone”. Given the high impedance at point S, the voltage there changes sharply. This change is additionally multiplied by the inverter M4-M3 and fed to the push-pull stage M1-M2.

The input offset current of the current comparator is due to mismatches between M7 and M8, hence $I_a \neq I'_a$, and due to different potentials at their drains. However, the requirements addressed to it are relaxed to a great extent, as the comparator’s offset is compensated at a system level, which is part of the proposed calibration algorithm. Transistors M7 and M8 are inherently large (small random mismatch) to meet the requirements for a higher output impedance.

Finally, as a remark, the purpose of the push-pull stage M1-M2 and the feedback through the inverter M3-M4 is to provide a low-impedance input for $I_b$. 
3.2.4 Calibration simulations

The transistor functionality of the calibration algorithm, explained in Section 2.4.3 on page 47, is demonstrated by transient transistor simulations. Some of the results of these simulations are commented here. Figure 50 shows transistor simulations, illustrating the states and the operations of the proposed DAC calibration. There are two plots. On top, the states of the FSM, as defined in Figure 30, are given. Below, the comparator’s currents are shown. The calibration process contains two phases: phase A (states 0, 1, 2, 3) and phase B (states 4, 5, 6, 7). In parallel, the “PDF domain” equivalent of this transient simulation is given in Figure 51. Gray dashed lines on the both sides of the binary reference, $I_{binref}$, show the required boundaries of the post-calibration distribution, in both Figure 50 and Figure 51.

1. All the currents are given with a negative sign. This inconvenience was realized at a very late moment of the thesis preparation. We beg for the apologies of the reader.
During phase A, the temporary current is calibrated to the sum of the binary currents plus 1 LSB and the input comparator offset is recorded, see Figure 51 a). The calibration step is 100nA, to comply with the high level simulation results of Figure 34. By the end of this phase, the temporary current is equal to the binary reference plus the input offset of the current comparator, see point A, see Figure 50. When the temporary current becomes greater than the current, it is compared to, the temporary current’s CALDAC is decremented by one and the calibration algorithm proceeds to the next state 4. The last current decrement is done to comply with the post-calibration PDF given in Figure 28, hence the resulting PDF can be approximated to uniform.

During phase B, all the thermometer current sources are calibrated to the temporary current source. The calibration step is 200nA. Each calibration loop takes different number of cycles, depending on the deviation of the actual intrinsic current from the temporary current. Each thermo-current calibration ends with a decrement, which is done to comply with the post-calibration PDF given in Figure 28, hence the resulting PDF can be approximated to uniform. At the end of each calibration loop, the calibrated current does not deviate from the binary reference, $I_{binref}$, more than 200nA plus/minus the offset (100nA) due to the calibration of the temporary current $I_{temp}$.

At the end of each calibration loop, the calibrated currents are positioned at the same side of their intrinsic value, thanks to the last decrement. Therefore, their post-calibration PDF will have greater probability towards its center and can be approximated as uniform distribution1. If the last increment is not discarded, than the actual intrinsic samples will be calibrated to the opposite side of the reference, i.e. the smaller currents will become greater, and vice versa. This will result in a post-calibration PDF, the greater probability of which will be towards its edges. Therefore, its approximation with an uniform distribution will introduce an error2.

Figure 51 e) shows the behaviour of the proposed calibration towards intrinsic samples that fall within the calibration boundaries. These are incremented and decremented, resulting in a post-calibration values which coincide with the intrinsic values.

---
1. The actual standard deviation will be smaller than the approximated one.
2. The actual standard deviation will be greater than the approximated one.
3.3 Transistor level decisions

The Decoder

The binary-to-thermometer decoder was realized with CVSL logic. Two other alternatives were considered: uni-polar CMOS implementation and differential current-steering implementation. The uni-polar implementation was found not convenient because to interface it to the following differential latches, an unary-to-differential conversion is needed. The other alternative was current-steering logic. This is perhaps the best choice, from performance point of view. A current-steering decoder would be in unison with the following master/slave latches. However, current/steering logic occupies significant silicon space. That is why CVSL logic was chosen, since it is differential and occupies less area in comparison with current-steering logic.

The unit-element approach

The unit-element approach offers a high degree of matching. The cost is silicon area and interconnection complexity. The area cost comes from the fact that independent elements are used in parallel. Thus, the total silicon area is increased by the non-active area of all unit-element transistors. A decision was taken to reduce this area loss by half, choosing the second bit as the unit-element transistor. Therefore, the matching between bits from 2 to 12 still apply the advantages of the unit-element approach, while bit 1 is implemented as shown in Figure 42 and as proposed by Bastos [Bastos 98]. In such a way, the effective length of the current source transistor is increased by 2, without introducing a different size element in the array. Because further research was not devoted on the structure of connected transistors in series, hence its exact effect was not precisely modelled, it was decided to limit its implementation only to the first bit.

The CALDAC of $I_{\text{temp}}$

The CALDAC of the temporary current $I_{\text{temp}}$, used to store the comparator’s offset is designed as thermometer type. Its LSB current is 100 nA. These decisions were taken, to minimize the effect of the calibration error $I_{\text{binref}}-I_{\text{temp}}$ on the calibration of the thermometer current sources, see Figure 32. A thermometer CALDAC is always monotonic, regardless the size of the LSB step.

The approach concerning the simulations

The nature of the project involves a variety of aspects, such as stochastics, transistor level time and frequency optimization. Therefore, the perfect simulation which would fairly prove and show the DAC system transistor level design will be a transient Monte-Carlo simulation of at least 100 tries covering the performance of the DAC from its initial phase of calibration of the 63 thermometer currents till its normal operation afterwards (converting a sinewave). Such a simulation is impossible, given the software and the computational power of the design machines that were available for the project. Therefore, transistor-level Monte-Carlo simulation was never done. Instead, the design only relied on combinations of system-level and time-based transistor level simulations and the performance of the DAC in the frequency domain was evaluated with mismatch-free transistors.
4.0 Layout Design

4.1 Layout considerations

The layout is the actual physical implementation of the DAC. The DAC layout cannot improve its performance but introduces many problems, which may deteriorate it. Some of these problems are: signal interference, non-balanced signal propagation, parasitic wire resistances and capacitances, and mismatch.

When components or metal wires are physically placed close to each other, their electrical signals directly interfere with each other through the parasitic capacitances or via the bulk connection between them. To limit and isolate the negative effects of this interference, special care has to be taken for the sources of major interference and for the sensitive components and wires. These two groups have to be kept well separated from each other. For example in DACs, the clock and data signals are sources of major interference and due to their high impedance the current sources and the output current lines are sensitive components and wires.

The electrical signals are delayed, depending on the length (hence the resistance) and the environment (hence the capacitance) of the path. The wires that are not equally long and not equally surrounded have different delay times. If parallel signals propagate these lines, by the end of the lines, these signals are no longer synchronized. CS DAC systems are very sensitive to that respect, since all the digital signals propagate to the current switches in parallel. Therefore, their paths have to be designed as balanced as possible.

The signal paths are implemented by physical metals. Depending on the material, these paths have a particular sheet resistance. Therefore, any current flowing through a wire will cause a voltage drop along it. In that respect, sensitive wires in CS DACs are those in the current cell. A bigger than designed voltage drop may push the cascodes or the current source transistors out of saturation. In addition, the parasitic capacitances along the metal wires may influence the settling times of the DAC. Sensitive connections in the current cell are between the cascodes and the switches, for example.

Finally, the absolute matching of the applied CMOS process is very poor. An actual component may have up to 20% deviation of its designed parameters. Luckily, the relative matching is reliable. That is why any matched elements have to be laid-out in exactly the same manner and surrounded by exactly the same environment. CS DAC systems comprise many matched components, such as the Master and Slave Latches, the current switches, the current cascodes, the current sources, etc.

These considerations have to be taken into account when designing the floorplan of the DAC layout. The top-level layout planning highly determines the performance of the DAC. Moreover, there are publications, [O’Sullivan 2003], which present layout driven DAC design, where the requirements in the layout phase dictate to a great extent the transistor level design.
4.2 Chip floorplan

The DAC layout floorplan not only determines to a great extent its performance, but also guides the layout design of its building blocks. The layout floorplan of the presented DAC is shown in Figure 52. The DAC is divided on an dynamic part and a static part, as given in Section 2.2 on page 35. The dynamic part includes the blocks which operate with dynamic signals, such as the Decoder, the Master and Slave Latches, the Clock and the Data buffers, and the current switches. The static part includes the blocks which operate with static voltages, such as the current sources, the cascoded transistors, and the CALDACs.

The dynamic and the static part are separated by the calibration components, which will be turned-off during normal DAC operation.

The static part is organized in stacks. On the bottom is the array of unit-current sources, where the bit currents are generated. These currents are fine-tuned by the CALDAC currents. Therefore, the Array of the CALDACs is just above the unit-current sources. Next, these currents pass through the cascoded transistors, the array of which is above the CALDACs stack.
The *dynamic* part is organized in a symmetrical manner, so that the paths of parallel signals are kept equally long. The symmetry lies along the $y$ axis. Thus, the paths of the signals go from the decoders through the Master and Slave Latches, to the output of the DAC. For the sake of symmetry, the Decoder has to be split. Therefore, its area will be larger.

Furthermore, the sensitive output wires are kept away from the major sources of dynamic influence: the data and clock signals. To avoid inter-crossings with these, the output is fed out of the chip through the *static* part.
4.3 DAC components

4.3.1 Array of unit current sources

The array of unit-current sources contains the signal unit-current sources, their biasing transistors built-up with the same unit-elements, and dummy unit-elements used as gate-oxide capacitors to protect the biasing line. To compensate for the deterministic matching errors, the signal unit-current sources are organized in 4 arrays. Each array is a common-centroid structure, as described in “Unit-current sources matching” on page 40 and shown in Figure 24. Every thermometer current source has two transistors in each of the quadrants of the arrays. The binary current sources are composed by transistors equally spaced from the $y$ (mirror) axis of the layout.

A region of the Array of unit-current sources is shown in Figure 53. A couple of two unit current sources is laid-out along a ground line. These two unit-current sources belong to a single thermometer current source. For the binary current sources, this couple is separated. A mesh of vertical and horizontal metal lines provides the interconnections between the unit-elements of a single current source. To minimize any interference between the mesh and the channel of the underlying unit-current source transistor, the latter is shielded by a metal layer on the transistor’s gate potential.

The entire array of unit current sources (including the associated biasing and dummy structures, and the interconnections) occupies 420x980$\mu$m$^2$ silicon area.

FIGURE 53. A layout region of the array of unit-current sources.
4.3.2 Array of CALDACs

A single CALDAC cell of the Array of CALDACs contains the CALDAC unit-current source transistors, a *Polarity switch*, and 6 flip-flops. It is shown in Figure 54. On the right, the 6 flip-flops are placed. 5 of them control the CALDAC currents, generated by the array of unit-elements on the left-down. The 6th flip-flop controls the *Polarity Switch* on the left-top.

The unit-current sources, which generate the calibration current have to be matched, as specified in Chapter 3.2.1 on page 61. That is why each active transistor is surrounded by the same environment. On the boarders of the array, dummy transistors are added. The array is guarded by a ring to ground, to minimize bulk related disturbancies.

The *Polarity Switch* effectively increases the resolution of the CALDAC by 1-bit, while occupying less than 50% of the current source transistors.

A single CALDAC cell occupies 36x67μm² silicon area and the entire array (including the associated biasing structures) is placed on 180x980μm², which less than a half of the unit-current sources array.

4.3.3 Array of cascodes

The the three cascode transistors of the current switching cell are separated from the current switches in an independent block. The cascodes operate with static currents and they are laid-out in the bottom half of the total DAC area, above the Array of CALDACs. Their layout is shown in Figure 55.
On the right, as a 10-folded transistor is laid-out the first cascode, M2 from Figure 40. The second cascode is next on its left side, M3. The switches, controlling the phase of operation (either calibration or normal operation) and the inverter for the Enable signal are on the left side of M3. Finally, M3a is placed on the right side of Figure 55.

The gates of the cascode transistors are shielded by a metal layer on the gate potential. This is meant to protect the gates from disturbancies coming from the metal layers crossing above.

This cell occupies 10x67µm². The entire array of the cascodes occupies 55x970µm².

4.3.4 Current comparator

The layout shape of the current comparator is forced by the layout floorplan of the DAC. It is a very long structure, see Figure 56, so that it can fit on the pitch dictated by the stacked layers of the static bottom part. To minimize its input offset, the current mirror transistors M7 and M8 and their cascodes M5 and M6 from Figure 49, are designed unit elements.

Each of M7 and M8 are divided on 8 identical unit transistors of W/L size 9/2. These unit elements are electrically connected in parallel on the layout. Physically, they are ordered in two rows. The top row alters a unit of M7 with an unit of M8, while the bottom row alters a unit of M8 with a unit of M7. Thus, both transistors M7 and M8 are positioned in an exactly the same environment. Therefore, the expected mismatch between them is only random. M8 and M7 can be found on the left side of Figure 56. Next to them are M5 and M6. On the right of Figure 56, the push-pull stage and the three inverters are placed.

The occupied area by the current comparator is 21x567µm².

4.3.5 Master-Slave latches and Current Switches

The Master-Latches and the following buffer are designed as a single sub-cell. The Slave latches and the current switches, associated with a particular bit, are designed as another single sub-cell, to minimize and equalize the signal paths from the latches to the current switching transistors. Both cells are combined as the Master-Slave latches and current switches cell.

Figure 57 shows the layout of the this cell. The Master Latches are on the left side and the Slave Latches are on the right side, together with the current switches. The layout structure is regular,
thanks to the equally sized transistors and resistors in the Master/Slave latches, Figure 38. Regular structures provide better elements matching - a very important requirement for the Master/Slave latches. The numbers on the layout snapshot show the particular sub-blocks.

The bit-signal paths are indicated by number 1. Under this interconnection matrix, the 3K resistors are placed, see also Figure 38. The current source transistors of the Latches are given by number 3. The top transistors are those of the buffers (close to the output) and the bottom transistors are those of the latches. The output of the current switches, i.e. the currents that will contribute to the overall output of the DAC, pass through the top metal layer lines, indicated by 4. It is positioned as far as possible from the clock lines, indicated by number 5. The equally sized transistors of the Master and the Slave Latches are given as number 6. Finally, number 7 indicates the biasing transistor for the current sources (number 3).

The area occupied by a single cell, containing 9 Master/Slave Latches and current switches is 97x330µm\(^2\). The whole array of Master/Slave latches is organized in 8 such cells: 7 cells for the thermometer bits (63 Master/Slave Latches) and 1 cell for the binary bits (6 Master/Slave Latches). The whole array occupies 405x960µm\(^2\).

![FIGURE 57. Layout of a cell containing Master/Slave latches and current switches.](image)

### 4.3.6 DAC layout

According to the layout floor-plan, given in Figure 52, the sub-blocks of the DAC were designed and integrated in a common layout structure, shown in Figure 58. The current-source transistors array is at the bottom (1). The array of CALDAs (3) and the cascodes (4) are as a stacked structure above. As seen, the array of the CALDAs occupies half the array of the current source transistors, while in theory, the array of the current source transistors should be 16 times bigger, if designed for 12bit intrinsic accuracy. Number 4 shows the necessary circuitry for calibration: the current comparator and digital logic. Part of it is designed as a stack on top of the cascodes and another part is placed between the mirrored arrays of Master/Slave latches (5). On the outer side of the Master/Slave Latches (5) are positioned the parts of the Binary-to-Thermometer Decoder (6). The clock, (7), for the Master/Slave latches propagates through the outer side, in order to stay further from the output of the DAC (8).

The presented DAC occupies 1.3x1.2 mm\(^2\).
By January 2004, there is still integration effort going-on. The layout sub-blocks have to be interconnected, some of the biasing networks and the clock and data buffers are not laid-out yet. Furthermore, the layout core has to be connected to PADs and internal test-PADs have to be introduced.

FIGURE 58. The current state of the presented DAC layout.
Conclusions

The Calibration relaxes the design requirements. It wisely combines components, with reduced design specifications, into a single entity having higher performance specifications. The presented converter is designed for 10-bit intrinsic accuracy and thanks to additional circuits and operations, its DC accuracy is improved to 12-bit level.

The Calibration can detach to some extent the system from the technology, thanks to the additional calibration operations, the higher allowable design margins, and the design requirements relaxation.

The Calibration, itself, does not directly lead to smaller designs. To achieve smaller designs, it is necessary a devoted “design for layout”, see [O’Sullivan] for an example. Such an approach was not applied in the presented DAC design. Therefore, the size of the chip is comparable to the big DAC designs known from the literature, see Figure 17.

The presented Calibration algorithm is applicable for various types of a single segmentation. It is designed for current-steering DACs, but can also be implemented in other DAC families, such as Switched-Capacitor DACs.

A 12-bit current steering DAC with the presented calibration algorithm is designed. A balanced layout floorplan is proposed and realized. The layout design phase is at a very advanced stage: the individual laid-out blocks are being integrated, by January 2004. The tape-out of the chip is planned for May 2005. The expected specifications of the designed DAC are given in Table 4.

<table>
<thead>
<tr>
<th>TABLE 4. Expected final specification of the presented DAC.</th>
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</thead>
<tbody>
<tr>
<td><strong>Resolution</strong></td>
</tr>
<tr>
<td>DNL</td>
</tr>
<tr>
<td>Intrinsic INL</td>
</tr>
<tr>
<td>Calibrated INL</td>
</tr>
<tr>
<td>SFDR at 400MSps,</td>
</tr>
<tr>
<td>for f_{signal} = 20MHz (estimation)</td>
</tr>
<tr>
<td>FS Output current</td>
</tr>
<tr>
<td>Supply Voltage</td>
</tr>
<tr>
<td>Analog Supply Current</td>
</tr>
<tr>
<td>Digital Supply Current at 400MSps (estimation)</td>
</tr>
<tr>
<td>Technology</td>
</tr>
<tr>
<td>Area</td>
</tr>
</tbody>
</table>
Recommendations

The presented implementation of the Calibration algorithm is only one of the implementations, given in Section 2.4.3 on page 47. Two other implementations, which deserve further attention, were outlined. These may lead to more accurate results, because of the narrower post-calibration distribution of the thermometer current sources.

The presented DAC has a 6-6 segmentation. This architecture was a starting point for the presented work. However, it was shown that calibrating more thermometer bits increases the benefits of calibration. Therefore, a promising subject for further research would be the trade-offs between segmentation and calibration.

An interesting application in calibrated DACs may find the approach introducing a virtual ground node at the output of the DAC, solving the code-dependent output impedance problem, see Figure 23. In future technologies, the supply voltage will drop and circuits relying on cascode transistors will become problematic. The inherent small size of the current source transistors in calibrated DACs will require a new solution, different than cascodes. Therefore, the above recommended approach deserves attention, particularly with respect to DACs with higher resolutions (above 14 bits) and calibration.

In Section 3.3 on page 67, a practical simulation problem was mentioned, which constrained our verification capabilities to quasi-ideal transistor level simulations. Such a problem can be reduced to a great extent, if a simulation software is used, which allows to set different transistor-model precision levels to the design’s sub-blocks, and which allows to change the simulation step, during a simulation. In this way, for the DAC transient simulation, a large time step will be set during the calibration phase and a small one during DA converting phase. Analogically, the precision of the transistor models can be controlled for the different parts of the design, during these two simulated phases.

The layout of the presented DAC was designed fully manually. However, if more complicated digital calibration logic has to be designed, the use of automated layout synthesis tools, such as Silicon Ensamble, is strongly recommended.
Bibliography


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Lastly, my gratitude and love go to Eli. Thank you for letting me love you.