An optimal CMOS structure for the design of a cell library

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An Optimal CMOS Structure for the Design of a Cell Library

by
M. Dielen
and
J.F.M. Theeuwen

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Eindhoven
January 1987
Deliverable

Report on activity 5.2.C: Cell generation schemes. Developing or studying cell architectures for various CMOS families.

Abstract:
A study of the literature provided the basis of this report. The articles were used to give an overall picture of possible CMOS design structures and to extract theoretical models for these structures.

First the general properties of CMOS are examined, also the CMOS inverter is dealt with, because this is the basic building block. Next the various structures of CMOS are examined. CMOS provides several structures that are suitable for poly cell design. These structures are:

1. And or invert circuits
2. pass transistor circuits
3. domino CMOS

For every structure a theoretical model is formed and a SPICE simulation is performed.

Domino CMOS was found to have the most advantageous properties with respect to the cell library design.

deliverable code: WP 5, task: 5.2, activity: 5.2.C.
date: 19 - 01 - 1987
partner: Eindhoven University of Technology

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With increasing complexity and size of integrated circuits, computer aids for layout and simulation have begun to play an ever-increasing role. The development of new technologies, searching for better performances, has also become an important part of the progress in the circuit design. In September 1986, the Automatic System Design group (ES) will have the possibility to use CMOS for integrated circuits. Because of its promise of high switching speeds and low power consumption, CMOS is rapidly becoming the technology of choice for digital system design. Until now, only NMOS has been used. Since CMOS hasn't the same properties as NMOS, the software packages will have to be adjusted.

The library, in which cells are stored, is a part of the software packages. These cells contain elementary building blocks by which complex circuits can be built fast and efficient with the assistance of the computer. Because of the fast changing in the integrated circuit design, e.g. decreasing design rules, or new technologies, the demand for standard logic cells, also called polycells, increases. These polycells can perform small boolean functions, but although each polycell performs a different function, the circuit structure for each polycell is the same. Although known to have some chip area penalty the polycell-based design approach allows significant savings in design effort and time. With availability of a polycell library that provides information on propagation delay time and layout of each polycell, logic designers can come up with timing specifications by estimating delay times in critical paths.

Because CMOS circuits have other properties than NMOS circuits, research has to be done into the CMOS circuit structure, which circuit structure has the most advantageous properties. The current library contains static NMOS cells. In CMOS (as well as in NMOS) exists besides the static realization also the possibility of building dynamic cells.

In this report will be investigated which cell structure gives the optimal use of CMOS. This is done by theoretical calculation and SPICE simulation. SPICE is a circuit simulation program. Also a thorough study of published articles about CMOS has been carried out, through this an overall picture is given of possible CMOS design structure.
There has been a renewed interest in CMOS technology, judging by the large number of articles published. CMOS has emerged as the most important technology for VLSI, this because of the low power consumption of CMOS. The low power consumption arises from the series connection of NMOS and PMOS transistors. In the operation of the CMOS circuit, at least one type of transistor in the series connection is off, so that steady-state power dissipation is insignificant. Since the total power dissipation allowed for a chip limits the number of transistors on a chip and the gate speeds, higher chip performance is obtained with CMOS.

The design of CMOS polycells requires optimization of multiple criteria. Usually design objectives specified in terms of power dissipation, chip area, propagation delay and noise margins are conflicting and some trade-offs need to be made among them. Another design objective that is becoming more and more important, although less measurable, is the possibility of using computer aids. Designable parameters for the optimization were identified to be channel width and channel length in PMOS and NMOS transistors.

The most important performance measures are:

- the product of power dissipation and propagation delay. This product is regarded important since it represents the dissipated energy per switching operation.
- the chip area, since it denotes the number of cells that can be placed on a chip. In CMOS circuits, power dissipation is small and so far has not been a limiting factor. Therefore for polycell design, we will concentrate on propagation delay and chip area.
- the noise margins. Without sufficient noise margins, cross coupling between adjacent metal or polysilicon lines on the chip may cause erroneous outputs. Decreasing design rules tend to increase such cross couplings and the consideration of noise margins becomes an important factor.
- The use of computer aids. This because the circuit technology is moving from LSI to VLSI geometries. Although the circuits are growing the customer wants short design times. On the other hand the design must be economical, to be competitive with alternate approaches.

The following assumptions are made for polycell design:

- The power supply is equal to 5V.
- 5μm design rules.
- Power dissipation is not a limiting factor
- The gate, source and drain length of PMOS and NMOS transistors are equal to 5μm
2.2. The SPICE program

SPICE is a circuit simulation program for DC and transient analyses. SPICE [36,37] uses models for the transistors, and the user needs to specify the model parameters. These parameters are mentioned in appendix 1. In SPICE, three MOSFET models are implemented, MOS1 is described by square law I-V characteristic, MOS2 is an analytical model, while MOS3 is a semi empirical model. Although MOS3 gives a more accurate computation, it is decided to work with MOS2, because the parameter specification of MOS3 is very complex and a complete survey of the CMOS process that will be used at the EFFIC, i.e. the semiconductor laboratory of the Eindhoven University of Technology, is not yet available.

Because the exact values of the parameters are not yet available, they probably have to be adjusted afterwards. The CMOS parameters of the process used by the EFFIC will be identical to the parameters used by PHILIPS [34]. However the parameters used by PHILIPS don't correspond with the SPICE parameters. It was only possible to track nine parameters, which are shown in table 1.

Table 1: The SPICE parameters, the corresponding PHILIPS parameters and their values.

<table>
<thead>
<tr>
<th>SPICE parameters</th>
<th>PHILIPS PARAMETERS</th>
<th>value</th>
</tr>
</thead>
<tbody>
<tr>
<td>VTO</td>
<td>VTE0</td>
<td>1.6</td>
</tr>
<tr>
<td>KP</td>
<td>β</td>
<td>2.2</td>
</tr>
<tr>
<td>GAMMA</td>
<td>K</td>
<td>0.72</td>
</tr>
<tr>
<td>PHI</td>
<td>2Φ</td>
<td>0.006</td>
</tr>
<tr>
<td>LAMBDA</td>
<td>θ</td>
<td>0.006</td>
</tr>
<tr>
<td>RSH</td>
<td>RSH+/&gt;RSH-</td>
<td>15</td>
</tr>
<tr>
<td>TOX</td>
<td>TOX</td>
<td>0.1</td>
</tr>
<tr>
<td>NSUB</td>
<td>NSUB</td>
<td>1.74 E16</td>
</tr>
<tr>
<td>LD</td>
<td>LD</td>
<td>1.1</td>
</tr>
</tbody>
</table>

The remaining parameters are set to values of an NMOS model composed by the electronic circuit group (EEB). This group uses four different models, each with different properties for the parameters KP, GAMMA and LAMBDA, see appendix 3. It is decided to work with model 1 because in this model the PHILIPS parameters cover the greatest number of parameters, see table 2.
Table 2: The composed SPICE parameters.

<table>
<thead>
<tr>
<th>SPICE PARAMETERS</th>
<th>ENHANCEMENT FET PARAMETERS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>NMOS</td>
</tr>
<tr>
<td>VTO</td>
<td>1.6</td>
</tr>
<tr>
<td>KP</td>
<td>20U</td>
</tr>
<tr>
<td>GAMMA</td>
<td>2.2</td>
</tr>
<tr>
<td>PHI</td>
<td>0.72</td>
</tr>
<tr>
<td>LAMBDA</td>
<td>0.006</td>
</tr>
<tr>
<td>PB</td>
<td>0.75</td>
</tr>
<tr>
<td>CGSO</td>
<td>370P</td>
</tr>
<tr>
<td>CGDO</td>
<td>370P</td>
</tr>
<tr>
<td>CGBO</td>
<td>395P</td>
</tr>
<tr>
<td>RSH</td>
<td>15</td>
</tr>
<tr>
<td>CJSW</td>
<td>80U</td>
</tr>
<tr>
<td>MJSW</td>
<td>0.5</td>
</tr>
<tr>
<td>CJSW</td>
<td>330P</td>
</tr>
<tr>
<td>MJSW</td>
<td>0.25</td>
</tr>
<tr>
<td>JS</td>
<td>6.2U</td>
</tr>
<tr>
<td>TOX</td>
<td>0.1U</td>
</tr>
<tr>
<td>XJ</td>
<td>0.7U</td>
</tr>
<tr>
<td>LD</td>
<td>1.1U</td>
</tr>
</tbody>
</table>

2.3. The product of area and propagation delay

One of the most important design objectives in CMOS design is the product of area and propagation delay. For this purpose the objective function \( H \) is defined. \( H \) depends on the channel width of the PMOS and NMOS transistor (\( W_p \) and \( W_n \)), if the aspect ratio is fixed then \( H \) depends only on one of them.

The function \( H \) consists of two parts, one part is the chip area and the other the propagation delays.

\[ H = (\text{chip area}) \cdot (\text{propagation delays}) \]

The propagation delays are well-defined either by the theoretical model or SPICE simulation. An important fact is that the function \( H \), concerning the minimum, is not sensitive to constants, because the derivative is set to zero. That is why the average propagation delay may be used, \( \bar{\tau} = 0.5(\tau_f + \tau_r) \). The average propagation delay of an inverter can be generally represented as follows, where \( a \) and \( b \) denote two constants:

\[ \bar{\tau} = a + b/W \]

(1)

The chip area of a general circuit is not fixed, because the layout of a circuit can be realized in a lot of different ways. One of the possibilities has been drawn in figure 1. This structure is often used for A01 polycells.
Because this structure is very regular, it can be easily used for polycell design. But a lot of other structures are possible, e.g. a layout of 3 or 4 rows of transistors, or the NMOS and PMOS transistors could be mixed up.

In this report the layout is restricted to the layout given in figure 6. In this way the different CMOS structures can fairly be compared. This structure also provides a regular structure, so automatic tools can easily be applied.

The length of this layout is variable and depends on the function that has to be performed. When restricting to several functions and therefore several polycells, an average polycell with a fixed length can be defined. Hence, this fixed length can be eliminated from the objective function $H$, during optimization of one CMOS structure.

Yet, when several CMOS structures are compared, the length has to be taken into account because the length is not the same. This length is determined by the product of half the number of transistors. The length of one transistor is equal to the summation of the length of the gate, drain and source and a spacing of $5\mu m$ that separates the transistors of each other. So, the length of a transistor is equal to $20\mu m$.

The width of the layout for a polycell is equal to the summation of the width of the PFET, the width of the NFET and an interjacent spacing. The average chip area can now be represented as follows, where $c$ and $d$ denote two constants:

$$A = c.W + d$$

(2)

From equation (1) and (2) the following general representation can be derived for the objective function:

$$H = a.c.W + (b.c + a.d) + \frac{b.d}{W}$$

(3)
the derivative: $H' = \frac{a \cdot c - b \cdot d}{W^2}$

with $H' = 0$ \[ W = \sqrt{\frac{b \cdot d}{a \cdot c}} \]

The variables $a$, $b$, and $c$ are all well defined, however $d$ is defined by the interjacent spacing of the PMOS and NMOS transistor. This spacing is fixed at $15\mu m$, but it is seen that the optimum for $W$ is proportional to the square root of $d$. So, the minimum depends for a great part on the choice of $d$. Here it is assumed that the interjacent spacing is determined by the thinox regions between the PMOS and NMOS transistors and also some space is reserved for one wire.

Another important fact, indirectly related with the objective function, is the relationship between transistor count, cell count and area consumption for the realization of a large circuit, see [5]. It is found that the total macro area, including wiring, plotted as a function of cell count shows a minimum for a particular logic realization.

On the one extreme, with relatively few, quite complex cells, and thus a high transistor count, there are many transistors to be connected to some net, and there is not much freedom for reducing the wiring space by a good placement, because each circuit has connections to many nets. The other extreme, using many small cells with a relative low transistor count, has a larger overhead percentage and also a relatively large wiring space. The smallest area is obtained somewhere in between these two extremes.

In this report we will restrict ourselves to small cells with a relative low transistor count. The maximum function that is allowed is equal to: $f = a \cdot b \cdot c + d \cdot e \cdot f + g \cdot h \cdot i$. Allowing larger functions would degrade the propagation delays to much, only domino CMOS permits the use of large NMOS trees, and therefore domino CMOS can perform larger functions.

2.4. The CMOS inverter

2.4.1. Theory

The smallest building block for CMOS cells is the inverter. For the equations of the current of the PMOS and NMOS transistor can be formed complex formulae. By this it is often impossible to form a theoretical model for large circuits. However due to the small number of transistors in the inverter, namely two, a theoretical model can be formed [28]. Subsequently it appears that this model also is
applicable to multi-input gates.

In the following part first a general formula for the rise and fall time will be derived, after that the aspect ratio \( K = W_p / W_n \) will be calculated and subsequently the objective function \( H \) will be optimized.

-rise and fall time

The propagation delays \( t_f \) (fall time) and \( t_r \) (rise time) decrease as current-driving capability of the driver (proportional to gate channel width \( W_n \) and \( W_p \)) increase, whereas they increase with capacitive loading which consists of the drain capacitance in the driver (\( C_o \)), the interconnection-wire capacitance (\( C_w \)) and the total input capacitance of fanout gates (\( C_i \)). Propagation delay times also depend on input waveforms. Usually input waveforms with shorter rise and fall time yield less propagation delay. Therefore the functional relationship between propagation delays and important circuit parameters can be described by:

\[
\begin{align*}
    t_f &= f \left[ W_n + W_p, C_o + C_w + C_i, V_{\text{in}}(\cdot) \right] \\
    t_r &= f \left[ W_n + W_p, C_o + C_w + C_i, V_{\text{in}}(\cdot) \right]
\end{align*}
\]

where \( V_{\text{in}}(\cdot) = \text{input waveform} \)

The rise and fall time of a CMOS inverter shall be calculated. The inverter is schematically drawn in figure 2.

![CMOS inverter](image)

**Figure 2:** The CMOS inverter.

The input voltage \( V_{\text{in}}(t) \) has an "ideal" pulse waveform for simplicity. The propagation delay of the inverter is determined by averaging 50 percent point delay times in the NMOS and the PMOS transistor.

An analytical expression for \( t_f \) can be derived from the following state equations, where \( C_i \) denotes the total load capacitance:
NFET in saturation: \( V_{g}-V_{out} \leq V_{th(n)} \)

\[
\frac{dV_{out}}{dt} = \beta_n (V_{g}-V_{th(n)})^2
\]  

(5a)

NFET in linear region: \( V_{g}-V_{out} > V_{th(n)} \)

\[
\frac{dV_{out}}{dt} = \beta_n \left[ 2(V_{g}-V_{th(n)})V_{out} - V_{out}^2 \right]
\]  

(5b)

where

\[
\beta_n = \frac{u_n W_n C_{ox}}{2 L_n}
\]

\[
C_{ox} = \frac{K_{ox} \varepsilon_{ox}}{t_{ox}}
\]

The time interval for the NMOS transistor to remain in saturation denoted by \( t_k \) can be obtained from (5b):

\[
V_{dd} - V_{th(n)}
\]

\[
C_{l} \int_{0}^{t_k} dV_{out} = \beta_n (V_{dd} - V_{th(n)})^2 \int_{0}^{t_k} dt
\]

\[
t_k = \frac{V_{th(n)}}{\beta_n (V_{dd} - V_{th(n)})^2} C_{l}
\]  

(6)

The time interval for the NMOS transistor to stay in the linear region until it reaches one half of \( V_{dd} \) is obtained from (5b):

\[
0.5V_{dd}
\]

\[
C_{l} \int_{V_{dd} - V_{th(n)}}^{1} \frac{1}{2(V_{dd} - V_{th(n)})V_{out} - V_{out}^2} dV_{out} = -\beta_n \int_{V_{dd} - V_{th(n)}}^{t_k} dt
\]

(7)

By filling in \( t_k \) from (6), \( t_f \) is solved from (7)

\[
t_f = \frac{2C_{l}ln t_{ox}}{u_n W_n K_{ox}} \left[ \frac{V_{th(n)}}{(V_{dd} - V_{th(n)})^2} + \frac{1}{2(V_{dd} - V_{th(n)})} \ln \left( \frac{1.5V_{dd} - 2V_{th(n)}}{0.5V_{dd}} \right) \right]
\]  

(8)

Similarly \( t_f \) can be expressed by (8) with subscript \( n \) replaced by \( p \). In this case the absolute value has to be taken for \( V_{th(p)} \).
For m-input NAND en NOR gates, ordered in an AND-OR-INVERT fashion, the maximum propagation delays in PMOS and NMOS can be approximated by [33]:

\[
\begin{align*}
\text{tr} \text{(NANDm)} &= \text{tr} \\
\text{tr} \text{(NORm)} &= m \text{tr} \\
\text{tf} \text{(NANDm)} &= m \text{tf} \\
\text{tf} \text{(NORm)} &= \text{tf}
\end{align*}
\]

The SPICE parameters which can be used in equation (8) are:

\[
\beta = \frac{W}{2L}
\]

\[
V_{th} = V_{TO}
\]

( This is true when \( V = 0 \) for an NFET and \( V = V_{dd} \) for a PFET )

<table>
<thead>
<tr>
<th></th>
<th>NMOS</th>
<th>PMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>KP</td>
<td>20µA/V²</td>
<td>7.4µA/V²</td>
</tr>
<tr>
<td>VTO</td>
<td>1.6V</td>
<td>-1.65V</td>
</tr>
</tbody>
</table>

The load capacitance \( C_l \) can be calculated from the following equations. It is assumed that the interconnection-wire capacitance remains constant, therefore this capacitance is counted for in the total input capacitance \( C_i \) of the fanout gates.

\[
C_l = C_0 + C_1
\]

1) \( C_1 \) is estimated by 0.2pF

2) \( C_0 = C(\text{area contribution}) + C(\text{periphery contribution}) \)

\[
\begin{align*}
\text{area:} & \quad C_{A(n)} = C_{A(p)} = 0.5 \times 10^{-4} \text{ pF/µm}^2 \\
\text{periphery:} & \quad C_{P(n)} = C_{P(p)} = 5 \times 10^{-4} \text{ pF/µm}
\end{align*}
\]

\[
\text{area} = W \times L \quad \text{periphery} = 2L + W
\]

We can derive now for \( C_1 \) the following equation:

\[
C_1 = 7.5 \times 10^{-4}(W_n + W_p) + 0.21 \quad \text{(in pF)} \quad (W_n \text{ en } W_p \text{ en µm})
\]

By filling in (10) and (11) in equation (8), the rise and fall time can be expressed by:

\[
\begin{align*}
\text{tf} &= \frac{L_n}{W_n} \left[ 7.5 \times 10^{-4}(W_n + W_p) + 0.21 \right] 2.1816 \times 10^{-8} \\
\text{tr} &= \frac{L_p}{W_p} \left[ 7.5 \times 10^{-4}(W_n + W_p) + 0.21 \right] 6.0664 \times 10^{-8}
\end{align*}
\]
In [28] one of the design goals is to maximize the noise margins. The noise margins of a logic gate are defined as the input voltage differences between the DC operating points and their nearest unity gain points. In other words the gate switching point ($V_i$) has to be centered at $0.5V_{dd}$ to allow larger noise margins. Both NMOS and PMOS transistors operate in saturation in this case:

$$\beta_n(V_i-V_{th(n)})^2 = \beta_p(V_i-(V_{dd}-V_{th(p)})^2$$

$$V_i = \frac{\beta_r(V_{dd}-V_{th(p)})+V_{th(n)}}{1+\beta_r}$$

Assuming that $V_{th(p)} = V_{th(n)}$, the switching point will be centered at $0.5V_{dd}$ by setting:

$$\beta_r = 1$$

or:

$$\frac{u_pW_p}{u_nW_n} = 1$$

As is well known $u_n = 3u_p$. So, for maximum noise margins, $W_p$ should be about three times of $W_n$.

The noise margins are not the only criteria by which the aspect ratio $K = W_p/W_n$ is defined. Another important criteria are the propagation delay times. Figure 3 shows the relation between the aspect ratio and the average propagation delay [$\tau = 0.5(t_f+t_r)$], achieved by SPICE simulation.

![Figure 3: The average propagation delay of an inverter and the voltage $V_i$, for different values of $R$ with $W_p + W_n = 60\mu m$.](image)
The aspect ratio $R=3$ was found for maximum noise margins, such a choice is not desirable for the minimum propagation delay because the minimum occurs for $R$ between 1 and 2. The aspect ratio $R=2$ is chosen to avoid degrading the switching speed.

- the objective function $H$

For the optimization of the product of propagation delay times and chip area, the following objective function is defined:

$$H(W_p, W_n) = \text{area} \cdot \bar{t}$$

(15)

The width of the inverter is determined by the width of the NMOS and PMOS transistor and an interjacent spacing ($S=15\mu m$) between the PMOS and NMOS thinox regions imposed by design rules, see figure 4.

![Figure 4: Layout of the inverter.](image)

Because the length of each transistor is fixed, comparing the chip area of each inverter can be done by setting $A$ to:

$$A = W_n + W_p + S$$

So, the objective function can be written as:

$$H(W_n, W_p) = (W_n + W_p + S)0.5(t_f + t_r)$$

(16)

Note that $H$ depends only on one variable ($W_p$ or $W_n$), when the aspect ratio is fixed. By replacing $W_n$ by $0.5W_p$ the objective function gets the form:

$$H(W_p) = (1.5W_p + 15)[7.5 \times 10^{-4}(1.5W_p + 0.21)(2.5)(2.1816 + 6.0664)(10^{-14})]$$

$\frac{2}{W_p}$
The minimum can be calculated by setting the derivative of \( H \) equal to zero.

\[ H'(W_p) = 0 \]

minimum:

\[ W_p = 43.2 \mu m \]
\[ W_n = 21.6 \mu m \]

\[ H(W_p) = 124.55 \times 10^{-15} \]

Table 3 shows the propagation delays and the objective function \( H \), for different values of \( W_p \) and \( W_n \), calculated with the theoretical model.

Table 3: Propagation delays and the function \( H \) for \( R=2 \), calculated with the theoretical model.

<table>
<thead>
<tr>
<th>( W_p ) (( W_n ))</th>
<th>( W_p=10 )</th>
<th>( W_p=20 )</th>
<th>( W_p=30 )</th>
<th>( W_p=40 )</th>
<th>( W_p=50 )</th>
<th>( W_p=60 )</th>
</tr>
</thead>
<tbody>
<tr>
<td>( W_n=5 )</td>
<td>4.83</td>
<td>2.54</td>
<td>1.77</td>
<td>1.39</td>
<td>1.16</td>
<td>1.01</td>
</tr>
<tr>
<td>( W_n=10 )</td>
<td>6.71</td>
<td>3.53</td>
<td>2.47</td>
<td>1.93</td>
<td>1.61</td>
<td>1.40</td>
</tr>
<tr>
<td>( W_n=15 )</td>
<td>173.1</td>
<td>136.6</td>
<td>127.2</td>
<td>124.5</td>
<td>124.7</td>
<td>126.5</td>
</tr>
</tbody>
</table>

2.4.2. SPICE simulation

The inverter has been implemented in SPICE, as follow. The circuit diagram of the inverter has been drawn in figure 5.

![Circuit Diagram of CMOS Inverter](image)

Figure 5: The CMOS inverter.

* CIRCUIT INVERTER
M1 2 1 0 0 MOD1 W=5U AS=25P AD=25P PS=15U PD=15U
M2 2 1 3 3 MOD2 W=10U AS=50P AD=50P PS=20U PD=20U
COUT 2 0 0.2P
The propagation delay times computed with SPICE are reported in table 4.

Table 4: Propagation delay times and the objective function $H$ for $K=2$ computed with SPICE.

<table>
<thead>
<tr>
<th>$W_{p}$ (μm)</th>
<th>$W_{p}=10$</th>
<th>$W_{p}=20$</th>
<th>$W_{p}=30$</th>
<th>$W_{p}=40$</th>
<th>$W_{p}=50$</th>
<th>$W_{p}=60$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$W_{n}$ (μm)</td>
<td>$W_{n}=5$</td>
<td>$W_{n}=10$</td>
<td>$W_{n}=15$</td>
<td>$W_{n}=20$</td>
<td>$W_{n}=25$</td>
<td>$W_{n}=30$</td>
</tr>
<tr>
<td>$t_{f}$ (ns)</td>
<td>5.9</td>
<td>3.7</td>
<td>2.9</td>
<td>2.5</td>
<td>2.3</td>
<td>2.1</td>
</tr>
<tr>
<td>$t_{r}$ (ns)</td>
<td>5.7</td>
<td>3.6</td>
<td>2.9</td>
<td>2.5</td>
<td>2.3</td>
<td>2.2</td>
</tr>
<tr>
<td>$H(W_{p})$ ($10^{-15}$)</td>
<td>174</td>
<td>164.3</td>
<td>174</td>
<td>187.5</td>
<td>207</td>
<td>225.8</td>
</tr>
</tbody>
</table>

It follows from table 4 that the minimum of the objective function appears for:

$$W_{p} = 20 \mu m$$
$$W_{n} = 10 \mu m$$
$$H = 164.3 \times 10^{-15} \text{ms}$$

2.4.3. Conclusions

Comparing the results of the theoretical model of the inverter to the results of SPICE simulation, it is observed that the difference grows with increasing transistor sizes. The difference is mainly caused by the fact that SPICE simulation has been performed with input waveforms with rise and fall times equal to 2ns, otherwise the simulation is aborted. Because of the small propagation delays of the inverter, about 4ns, this fact cannot be neglected. Another important fact is the incompleteness of the theoretical model. Not all the parasitic capacitances are included. However by calculating this effect, the equations will not be easy to handle. Figure 6 shows the average delay times against the width of the transistors, as well for the theoretical model as the SPICE simulation.

It follows from equation (17) that $H$ is concave in $W_{p}$ and $W_{n}$, this can also be seen in figure 5. Physically, it is indeed necessary to increase transistor sizes beyond the minimum size to overcome capacitive loadings from interconnection wires. On the other extreme, if the transistor sizes become excessively large, the gate loading from fanout gates would be dominant over routing capacitance and the propagation delay would remain almost constant leaving the increase in chip area unjustified.
Figure 6: The average propagation delay for R=2 with variable W.
And-Or-Invert (AOI) circuits are characterized by complementary symmetry about a gate's output node. In other words, if the NMOS transistors between the output and ground are connected in series then the PMOS transistors between the output and Vdd will be connected parallel and vice versa. In this configuration with the inputs high or low, there is no DC path between Vdd and ground: thus the power dissipation is very nearly zero.

The theory of the inverter can be applied to the AOI-circuits, see equations (9). Maximal eighteen transistors are allowed for the AOI polycell, nine PFETs and nine NFETs. Of these nine PFETS or NFETs are connected maximal 3 NFETs or 3 PFETs in series respectively. Hereby the maximum possible function that can be performed by a polycell is equal to:

\[ f = a \cdot b \cdot c + d \cdot e \cdot f + g \cdot h \cdot i \]

**Figure 7** shows the 3-input NAND.

![3-input NAND circuit diagram](image)

**Figure 7: The 3-input NAND.**

In the operation of the circuit, when all inputs are high, the three NMOS transistors are on and the output will be connected to the ground. If one or more inputs are low, surely one of the NMOS transistors turns off. In that case one or more PMOS transistors are on and the output will be connected to Vdd.
For the optimization of the polycell design the following set of logic is selected: inverter, 2-input and, 3-input NAND and NOR gates, because these five circuits determine the performance of an AOI cell. The cells are denoted by:

INV, 2NAND, 3NAND, 2NOR and 3NOR

The propagation delay can be calculated by using equations (9), (12), (13). Let \( t_{f}^{(j)} \) en \( t_{r}^{(j)} \) denote the propagation delays in the \( j \)-th polycell among the five as ordered aforementioned, the mean delay time in an "average" polycell can be expressed by:

\[
\bar{t} = \frac{1}{N} \sum_{j=1}^{N} 0.5 \left( t_{f}^{(j)} + t_{r}^{(j)} \right) 
\]

\[
\bar{t} = 0.25(2t_{f} + t_{r} + 3t_{f} + t_{r} + 2t_{f} + t_{r} + 2t_{f} + t_{r} + 3t_{f} + t_{r}) 
\]

\[
\bar{t} = 0.8(t_{f} + t_{r}) 
\]

Because of the optimization of the noise margins and the propagation delays, see page 7, the aspect ratio \( R \) of the NMOS and PMOS transistors is 2. The area \( A \) is determined by the width of the NMOS and PMOS transistors and an interjacent spacing \( S=15\mu m \).

\[
A = W_{n} + W_{p} + S 
\]

Now the objective function \( H \) can be formed:

\[
H(W_{p}, W_{n}) = (W_{p} + W_{n} + 15)0.8(t_{f} + t_{r}) 
\]

Comparing this result with equation (16) it follows that:

\[
H_{AOI}(W_{p}, W_{n}) = 1.6H_{INV}(W_{p}, W_{n}) 
\]

Because constants don't affect the form of a derivative, the minimum of the average AOI polycell is equal to the minimum of the inverter.

minimum AOI polycell: \( W_{p} = 43.2\mu m \)

\[
W_{n} = 21.6\mu m 
\]

\[
H(W_{p}, W_{n}) = 199.28 \times 10^{-15} 
\]

In table 5 the propagation delay times and the objective function are stated.
Table 5: The propagation delays and the objective function $H$ for $R=2$, calculated with the aid of the theoretical model.

<table>
<thead>
<tr>
<th></th>
<th>$(\mu m)$</th>
<th>$W_P=10$</th>
<th>$W_P=20$</th>
<th>$W_P=30$</th>
<th>$W_P=40$</th>
<th>$W_P=50$</th>
<th>$W_P=60$</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>(ns)</td>
<td>$W=5$</td>
<td>$W=10$</td>
<td>$W=15$</td>
<td>$W=20$</td>
<td>$W=25$</td>
<td>$W=30$</td>
</tr>
<tr>
<td>3NOR</td>
<td>$t_f$</td>
<td>4.8</td>
<td>2.5</td>
<td>1.8</td>
<td>1.4</td>
<td>1.2</td>
<td>1.0</td>
</tr>
<tr>
<td></td>
<td>$t_r$</td>
<td>20.1</td>
<td>10.6</td>
<td>7.4</td>
<td>5.2</td>
<td>4.8</td>
<td>4.2</td>
</tr>
<tr>
<td>2NOR</td>
<td>$t_f$</td>
<td>4.8</td>
<td>2.5</td>
<td>1.8</td>
<td>1.4</td>
<td>1.2</td>
<td>1.0</td>
</tr>
<tr>
<td></td>
<td>$t_r$</td>
<td>13.4</td>
<td>7.1</td>
<td>4.9</td>
<td>3.5</td>
<td>3.2</td>
<td>2.8</td>
</tr>
<tr>
<td>3NAND</td>
<td>$t_f$</td>
<td>14.5</td>
<td>7.6</td>
<td>5.3</td>
<td>4.2</td>
<td>3.5</td>
<td>3.0</td>
</tr>
<tr>
<td></td>
<td>$t_r$</td>
<td>6.7</td>
<td>3.5</td>
<td>2.5</td>
<td>1.7</td>
<td>1.6</td>
<td>1.4</td>
</tr>
<tr>
<td>2NAND</td>
<td>$t_f$</td>
<td>9.7</td>
<td>5.1</td>
<td>3.5</td>
<td>2.8</td>
<td>2.3</td>
<td>2.0</td>
</tr>
<tr>
<td></td>
<td>$t_r$</td>
<td>6.7</td>
<td>3.5</td>
<td>2.5</td>
<td>1.7</td>
<td>1.6</td>
<td>1.4</td>
</tr>
<tr>
<td>INV</td>
<td>$t_f$</td>
<td>4.8</td>
<td>2.5</td>
<td>1.8</td>
<td>1.4</td>
<td>1.2</td>
<td>1.0</td>
</tr>
<tr>
<td></td>
<td>$t_r$</td>
<td>6.7</td>
<td>3.5</td>
<td>2.5</td>
<td>1.7</td>
<td>1.6</td>
<td>1.4</td>
</tr>
<tr>
<td>COUT</td>
<td></td>
<td>9.23</td>
<td>4.86</td>
<td>3.39</td>
<td>2.52</td>
<td>2.22</td>
<td>1.93</td>
</tr>
<tr>
<td>$H$</td>
<td></td>
<td>276.9</td>
<td>218.7</td>
<td>203.4</td>
<td>189</td>
<td>199.8</td>
<td>202.7</td>
</tr>
</tbody>
</table>

3.2. SPICE simulation

The AOI circuits are implemented in SPICE, as follow. For the implementation of the inverter, see page 9. The AOI circuits are drawn in figure 8.

* CIRCUIT 2NAND

M1 1 4 0 0 MOD1 W=5U AS=25P AD=25P PS=15U PD=15U
M2 2 4 1 0 MOD1 W=5U AS=25P AD=25P PS=15U PD=15U
M3 2 4 3 3 MOD2 W=10U AS=50P AD=50P PS=20U PD=20U
M4 2 4 3 3 MOD2 W=10U AS=50P AD=50P PS=20U PD=20U
COUT 2 0 0.2P

* CIRCUIT 3NAND

M1 1 5 0 0 MOD1 W=5U AS=25P AD=25P PS=15U PD=15U
M2 2 5 1 0 MOD1 W=5U AS=25P AD=25P PS=15U PD=15U
M3 3 5 2 0 MOD1 W=5U AS=25P AD=25P PS=15U PD=15U
M4 3 5 4 4 MOD2 W=10U AS=50P AD=50P PS=20U PD=20U
M5 3 5 4 4 MOD2 W=10U AS=50P AD=50P PS=20U PD=20U
M6 3 5 4 4 MOD2 W=10U AS=50P AD=50P PS=20U PD=20U
COUT 3 0 0.2P
Figure 8: The four AOI circuits (a) 2NAND (b) 3NAND (c) 2NOR (d) 3NOR

* CIRCUIT 2NOR

M1 1 4 0 0 MOD1 W=5U AS=25P AD=25P PS=15U PD=15U
M2 1 4 0 0 MOD1 W=5U AS=25P AD=25P PS=15U PD=15U
M3 1 4 2 3 MOD2 W=10U AS=50P AD=50P PU=20U PS=20U
M4 1 4 3 3 MOD2 W=10U AS=50P AD=50P PD=20U PS=20U
COUT 1 0 0.2P

* CIRCUIT 3NOR

M1 1 5 0 0 MOD1 W=5U AS=25P AD=25P PS=15U PD=15U
M2 1 5 0 0 MOD1 W=5U AS=25P AD=25P PS=15U PD=15U
M3 1 5 0 0 MOD1 W=5U AS=25P AD=25P PS=15U PD=15U
M4 1 5 2 4 MOD2 W=10U AS=50P AD=50P PS=20U PD=20U
The results of the SPICE simulation are stated in table 6.

Table 6: The propagation delays and the objective function $H$ for $R=2$, computed with SPICE.

<table>
<thead>
<tr>
<th>Cell</th>
<th>$W_p$</th>
<th>$W_n$</th>
<th>$W_p$</th>
<th>$W_n$</th>
<th>$W_p$</th>
<th>$W_n$</th>
<th>$W_p$</th>
<th>$W_n$</th>
<th>$W_p$</th>
<th>$W_n$</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>(μm)</td>
<td>5</td>
<td>10</td>
<td>15</td>
<td>20</td>
<td>25</td>
<td>30</td>
<td>35</td>
<td>40</td>
<td>45</td>
</tr>
<tr>
<td>3NOR</td>
<td>$t_f$</td>
<td>2.5</td>
<td>1.5</td>
<td>1.4</td>
<td>1.3</td>
<td>1.2</td>
<td>1.2</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$t_r$</td>
<td>23</td>
<td>13.5</td>
<td>10.8</td>
<td>9.3</td>
<td>8.5</td>
<td>7.8</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2NOR</td>
<td>$t_f$</td>
<td>3</td>
<td>1.6</td>
<td>1.6</td>
<td>1.6</td>
<td>1.4</td>
<td>1.4</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$t_r$</td>
<td>13.5</td>
<td>8.4</td>
<td>6.6</td>
<td>5.8</td>
<td>5.2</td>
<td>5</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3NAND</td>
<td>$t_f$</td>
<td>22</td>
<td>14</td>
<td>10.6</td>
<td>9</td>
<td>7.8</td>
<td>7.3</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$t_r$</td>
<td>2.5</td>
<td>1.5</td>
<td>1.5</td>
<td>1.5</td>
<td>1.5</td>
<td>1.4</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2NAND</td>
<td>$t_f$</td>
<td>13.5</td>
<td>8.4</td>
<td>6.6</td>
<td>5.6</td>
<td>5</td>
<td>4.6</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$t_r$</td>
<td>3.5</td>
<td>2.3</td>
<td>1.8</td>
<td>1.8</td>
<td>1.6</td>
<td>1.6</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>INV</td>
<td>$t_f$</td>
<td>5.9</td>
<td>3.7</td>
<td>2.9</td>
<td>2.5</td>
<td>2.3</td>
<td>2.1</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$t_r$</td>
<td>5.7</td>
<td>3.6</td>
<td>2.9</td>
<td>2.5</td>
<td>2.3</td>
<td>2.2</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$\bar{t}$</td>
<td>9.51</td>
<td>5.85</td>
<td>4.67</td>
<td>3.41</td>
<td>3.07</td>
<td>2.81</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$H$</td>
<td></td>
<td>285.3</td>
<td>263.3</td>
<td>280.2</td>
<td>255.6</td>
<td>276</td>
<td>302.8</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

It follows from table 6 that the minimum of the objective function occurs for:

\[
W_p = 20\mu m \\
W_n = 10\mu m \\
H = 263.3 \times 10^{-15} ms
\]

3.3. Layout

Usually a uniform height is used for all polycells. This uniform height allows easy routing of power bus lines internal to polycells and helps to fully utilize the routing domain[22,28]. Figure 9 shows a typical polycell layout of a 2-input NAND gate for illustration.
Another layout style of AOI circuits is denoted in [11,12]. The disadvantage of this layout style is that it doesn't use a uniform height for all polycells. For example, figure 10 shows a CMOS AOI circuit extendible in the AND direction.

3.4. Conclusions

The AOI circuits are fast. According to the theoretical model, the minimum for $H$ of the AOI polycell is situated for the width of the NMOS and PMOS transistor respectively at $W_p=40\mu m$ and $W_n=20\mu m$. In this case the average polycell applies to a propagation delay of $2.52\text{ ns}$. The minimum found with SPICE simulation is situated at $W_p=20\mu m$ and $W_n=10\mu m$ with a propagation delay of $5.85\text{ ns}$.

The differences of the theoretical model and the SPICE simulation are mainly caused by the rise and fall time of the input waveform used in the SPICE simulation.

A drawback of the AOI circuit, compared with NMOS, is the required chip area. The function is twice implemented, one time in NMOS and one time in PMOS. Therefore the layout is complex. Also because of this the capacitive load on gates is very high.

Another drawback is the large difference in rise and fall times. Especially in the 3NAND and the 3NOR circuit, this causes the degradation of the noise margins.
Figure 10: CMOS AOI circuit extendible in the AND direction.
CHAPTER 4 - PASS TRANSISTOR CIRCUITS

4.1. Properties

The properties of pass transistor circuits used for boolean functions, have not been studied thoroughly. When designing with pass transistors, three special properties have to be considered:

1) Parasitic capacitance associated with the pass transistor network can form unexpected memory elements.

2) A "sneak pass" between \( V_{dd} \) and ground can arise if the pass transistor circuit has been designed incorrectly.

3) The signals can propagate through both directions of a pass transistor chain.

When designing a pass transistor network these three problems have to be taken into account. In [27,30] two different design methods are proposed. In the first article the methodology is divided in two parts. For small circuits it is based on the Karnaugh Map and for large circuits (more than six variables) it is based on the Quine McCluskey tabular approach. In the second article the methodology is based on expanding the function into minterms first, and after that a binary tree is constructed. In this article is also mentioned a dynamic CMOS circuit, because of the great resemblance with domino CMOS. This network is dealt with in section 5.5.

The basic elements of a CMOS pass network are the NMOS and PMOS transistor. The gates of the NMOS and PMOS transistor are driven by the true and complement control signal, respectively. If the control signal is high, the input signal will be passed to the output, see figure 11.

![CMOS pass transistor representation](image)

<table>
<thead>
<tr>
<th>( P_i )</th>
<th>( V_{in} )</th>
<th>( V_{out} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>high imp.</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>high imp.</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Figure 11: CMOS pass transistor representation.

The theory of the inverter cannot be applied to calculate the propagation delay times of pass transistor networks. In figure 12 has been drawn a pass transistor chain with equivalent circuit.
Figure 12: (a) pass transistor chain
(b) equivalent circuit

A voltage along the chain divides into $V_{ds}$ of the transistors. So, $V_{ds}$ is usually low, and the pass transistors work mainly in saturation. By this a transistor can be replaced by a series resistance and a capacitance to ground. The capacitive load times the equivalent output resistance of the driving stage forms the delay time constant. The delay of a given stage can be decreased by increasing the area of the first element, thus decreasing its output resistance but this in turn increases the capacitance seen by the previous stage.

The response at node $V_2$ with respect to time is given by equation (21):

$$\frac{dV_2}{dt} = \frac{1}{C} \left[ (v_1 - v_2) - (v_2 - v_3) \right] / R$$  \hspace{1cm} (21)

By taking a large number of networks, the limit of equation 21 may be taken:

$$\frac{dV}{dt} = \frac{d^2V}{dx^2}$$  \hspace{1cm} (22)

$R$ and $C$ are the resistance and capacitance per unit length, respectively.

Equation (22) is the diffusion equation, although its solutions are complex, in general the time required for a signal to propagate a distance $x$ is proportional to $x^2$. Comparing this with figure 10 it is seen that if the number of pass transistors is doubled, both the resistance and the capacity are doubled. Therefore causing the response time to increase by a factor of approximately four.
If one transistor is added in a path of N transistors, then the added delay is small if N is small but very large if N is large. Therefore it is necessary to group the transistors into small sections and each section has to be separated of one another by an inverter. For this partition exists an optimum, the summation of the delay of the pass transistor chain and the delay of the inverter has a minimum for a particular length of the chain, depending on the transistor sizes of the pass transistors and the delay of the inverter.

4.2. - SPICE simulation

The pass transistor circuits have been implemented in SPICE as follow. The circuits have been drawn in figure 13.

![Diagram of the three pass transistor circuits, (a) 1NAND, (b) 2NAND, (c) 3NAND.]

* CIRCUIT 1NAND

M1 1 6 0 0 MOD1
M2 1 6 2 2 MOD2
M3 6 4 5 0 MOD1
M4 6 3 5 2 MOD2
COUT 1 0 0.2F
For the optimization of the noise margins and the propagation delays, the aspect ratio is determined. This can be done by comparing the values of the rise and fall times of the pass transistor cells. A function for the average deviation of the rise and fall time is defined. By this the largest noise margins can be determined:

\[ D = \frac{1}{3} \sum_{j=1}^{3} \frac{\Delta t_j}{t} \times 100\% \]

Where \( \Delta t_j \) is the difference of the fall and rise time of the \( j \)-th pass transistor circuit as ordered in table 7.

Table 7: The propagation delay times for the aspect ratio \( R=1, R=2, R=3 \).

<table>
<thead>
<tr>
<th>( K )</th>
<th>width (( \mu )m)</th>
<th>( t ) (ns)</th>
<th>3-input NAND</th>
<th>2-input NAND</th>
<th>1-input NAND</th>
<th>( \tau ) (ns)</th>
<th>D</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>( W_p=30 ) ( W_n=30 )</td>
<td>( t_f )</td>
<td>9.7</td>
<td>7.1</td>
<td>5.6</td>
<td>6.5</td>
<td>23%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( t_r )</td>
<td>7.1</td>
<td>5.6</td>
<td>4.6</td>
<td>6.5</td>
<td>23%</td>
</tr>
<tr>
<td>2</td>
<td>( W_p=40 ) ( W_n=20 )</td>
<td>( t_f )</td>
<td>8.8</td>
<td>8.6</td>
<td>7.6</td>
<td>4.4</td>
<td>10.6%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( t_r )</td>
<td>8.6</td>
<td>6.2</td>
<td>3.9</td>
<td>6.6</td>
<td>10.6%</td>
</tr>
<tr>
<td>3</td>
<td>( W_p=45 ) ( W_n=15 )</td>
<td>( t_f )</td>
<td>10.8</td>
<td>10.4</td>
<td>8</td>
<td>6</td>
<td>14.7%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( t_r )</td>
<td>10.4</td>
<td>6.8</td>
<td>4.2</td>
<td>7.7</td>
<td>14.7%</td>
</tr>
</tbody>
</table>

From table 7 it follows that the the average delay time \( t \) is minimal for \( R=1 \) and that the average deviation \( D \) is minimal for \( R=2 \). Because the average delay time for \( R=1 \) and \( R=2 \) is almost equal and the average deviation for \( R=2 \) is half the average deviation for \( R=1 \), it is decided to work with \( R=2 \).
In table 8, the propagation delay times and the object function for R=2 are stated.

Table 8: The propagation delay times and the objective function H for R=2, computed with SPICE.

<table>
<thead>
<tr>
<th>Function</th>
<th>(um)</th>
<th>(W_p=10)</th>
<th>(W_p=20)</th>
<th>(W_p=30)</th>
<th>(W_p=40)</th>
<th>(W_p=50)</th>
<th>(W_p=60)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>(W_n=5)</td>
<td>(W_n=10)</td>
<td>(W_n=15)</td>
<td>(W_n=20)</td>
<td>(W_n=25)</td>
<td>(W_n=30)</td>
</tr>
<tr>
<td>3NAND</td>
<td>(t_f)</td>
<td>12.6</td>
<td>10.6</td>
<td>10.3</td>
<td>8.8</td>
<td>9.8</td>
<td>9.6</td>
</tr>
<tr>
<td></td>
<td>(t_r)</td>
<td>18</td>
<td>10</td>
<td>8.4</td>
<td>8.6</td>
<td>7.9</td>
<td>7.8</td>
</tr>
<tr>
<td>2NAND</td>
<td>(t_f)</td>
<td>11.2</td>
<td>8.6</td>
<td>8</td>
<td>7.6</td>
<td>7.4</td>
<td>7.2</td>
</tr>
<tr>
<td></td>
<td>(t_r)</td>
<td>10</td>
<td>7.6</td>
<td>6.6</td>
<td>6.2</td>
<td>6</td>
<td>5.8</td>
</tr>
<tr>
<td>1NAND</td>
<td>(t_f)</td>
<td>8.2</td>
<td>6.6</td>
<td>5.8</td>
<td>5.4</td>
<td>5</td>
<td>4.9</td>
</tr>
<tr>
<td></td>
<td>(t_r)</td>
<td>7.6</td>
<td>4.7</td>
<td>4.2</td>
<td>3.9</td>
<td>3.8</td>
<td>3.7</td>
</tr>
<tr>
<td>(T)</td>
<td></td>
<td>8.4</td>
<td>8.0</td>
<td>7.2</td>
<td>6.6</td>
<td>6.7</td>
<td>6.5</td>
</tr>
<tr>
<td>(H)</td>
<td></td>
<td>252</td>
<td>361</td>
<td>432</td>
<td>494</td>
<td>599</td>
<td>683</td>
</tr>
</tbody>
</table>

It follows from table 8 that the minimum of the objective function occurs for:

\[
\begin{align*}
W_p &= 10 \mu m \\
W_n &= 5 \mu m \\
H &= 252 \times 10^{-15} \text{ms}
\end{align*}
\]

This is only true for 5\mu m design rules, the optimum of the objective function \(H\) lies in the region between 0 and 10\mu m for the width of the pMOS transistor.

4.3. - Conclusions

Pass transistor circuits show a great regularity in layout design, this because of the connection into chains and therefore an array of pass transistors can be formed. However, for the realization of a boolean function the 'normal' function and the complement function have to be realized, to ensure that no high impedance state is produced at the output.

The pass transistor circuit can be realized with fewer then the basic number of pass transistors required. A design procedure to find the minimum set of transistors is hard and cumbersome, especially because of the three special properties of pass transistor chains.
Another drawback of pass transistor circuits is that the propagation delays are quadratic proportional to the number of transistors in the chain. Thus longer chains of pass transistors must be partitioned into small groups with buffer stages interposed, to overcome this quadratic delay characteristic.

Pass transistors are widely used for building analog circuitry. Using pass transistors for the realization of boolean functions is a new application. More attention has to be directed to the special properties of pass transistor chains and their behaviour in boolean logic.
CMOS design can also benefit from NMOS techniques. That the number of NMOS and PMOS transistors in a circuit should be the same is not cast in either reality nor in silicon. Precharging a technique used in NMOS to increase speed and reduce power consumption can be applied to CMOS, as can other techniques. Probably the most published alternative CMOS design style is "domino CMOS".

A basic domino CMOS gate is by nature non-inverting. An AND gate consists of a precharged NAND gate followed by a standard inverter, see figure 14.

![Diagram of a standard domino CMOS cell.](image)

Figure 14: Standard domino CMOS cell.

During precharge, the PMOS transistor connected to the clock is on, while the NMOS transistor is off. Therefore, the intermediate (NAND) output is precharged high, while the buffer holds the output low. The key to the glitch-free nature of domino CMOS is the fact that all outputs, and therefore inputs are driven low during precharge. At the beginning of an evaluation phase, the precharged signal is removed. Because all of the inputs are initially low, the gate remains in the precharged condition. Thus, each stage of logic will hold each subsequent stage in the precharged condition until the circuit can evaluate its own inputs. This way, logic signals propagate from stage to stage much like a series of dominos, each toppling the next. Because each gate cannot change until enough inputs have been evaluated, glitches and race conditions are eliminated.

Another important property of domino CMOS is the possibility to use the wired OR and AND function [14]. Standard CMOS
circuits have to use additional (N)OR and (N)AND circuits. In domino CMOS the wired OR and AND function provide two-way or wider AND and OR functions, with no additional transistors, see figure 15.

Figure 15: The wired OR and AND function in domino CMOS.

Domino CMOS can be realized in four different ways:

1) Single-ended cascode voltage switch logic, see section 5.2.
2) Differential cascode voltage switch logic, see section 5.3.
3) Latched domino CMOS, see section 5.4.
4) Domino CMOS without a buffer, see section 5.5.
5.2. Single-ended cascode voltage switch logic

5.2.1. Theory

The structure of single-ended cascode voltage switch (SCVS) logic is equal to the standard domino cell described on page 22. For the NMOS network are permitted maximal three transistors in series and three transistors parallel. So, the maximal logic function that can be performed by an SCVS circuit is equal to:

\[ f = a \cdot b \cdot c + d \cdot e \cdot f + g \cdot h \cdot l \]

Only the series connection of the transistors in the NMOS network will be investigated for the optimization of the SCVS circuit, because the parallel branches hardly influence the propagation delay. Since the capacitive load of the intermediate (NAND) output is mainly determined by the gate capacitances of the inverter. So, the 3-input AND, the 2-input AND and the 1-input AND will be further investigated. The latter is necessary for taking into account the OR function with singular literals.

-Propagation delay times

The SCVS circuit will be partitioned into two parts for the calculation of the propagation delay times, namely the variable NAND and the inverter. One NMOS transistor in the series connection is connected to the clock in the SCVS circuit, so the variable NAND will consist of the 4-input NAND, the 3-input NAND and the 2-input NAND.

For the calculation of \( t_f \) and \( t_c \) of the NAND and the inverter can be used equations 9 and 10. However the load capacitance of the NAND has to be adjusted. The load capacitance of the NAND consists of a contribution of the drains of the PMOS and NMOS transistor of the NAND, connected to the intermediate output, and a contribution of the gates of the PMOS and NMOS transistor of the inverter.

\[ C_1 = C_o + C_i \]  \hspace{1cm} (23)
\[ C_o = \text{drain capacitance} \]
\[ C_i = \text{gate capacitance} \]
\[ C_o = C(\text{area contribution}) + C(\text{periphery contribution}) \]

area: \[ C_{A(n)} = C_{A(p)} = 0.5 \times 10^{-4} \text{ pF/µm}^2 \]
periphery: \[ C_{P(n)} = C_{P(p)} = 5 \times 10^{-4} \text{ pF/µm}^2 \]
area = \( W \cdot L \) periphery = \( 2L + W \)
\[ C_o = 7.5 \times 10^{-4}(W_n + W_p) + 100 \times 10^{-4} \]  \hspace{1cm} (in pF)  \hspace{1cm} (24a)  \hspace{1cm} (W_n en W_p in µm)
\[ C_L = 27.5 \times 10^{-4} (W_n + W_p) + 100 \times 10^{-4} \] (25)

The propagation delay times of the NAND can now be formed with equations (12), (13) by replacing \( C_l \) of the inverter by \( C_l \) of the NAND.

\[
\tau_f = \frac{L_n}{W_n} [27.5 \times 10^{-4} (W_n + W_p) + 100 \times 10^{-4}] \times 2.1816 \times 10^{-8} \] (26)

\[
\tau_r = \frac{L_p}{W_p} [27.5 \times 10^{-4} (W_n + W_p) + 100 \times 10^{-4}] \times 6.0664 \times 10^{-8} \] (27)

Now, the aspect ratio \( R \) of the PMOS and NMOS transistor will be calculated. In section 2.3. is determined which \( R \) yields the maximum noise margins. In this case it was assumed that the noise margins are maximal when \( V_i = 0.5V_{dd} \) at the midtransition point. Another way to achieve this is to equalize the fall and rise time of the SCVS circuit. The propagation delay of the average SCVS circuit can be calculated as follow:

\[
\tau = \frac{1}{N} \sum_{j=1}^{N} 0.5(\tau_{f,j} + \tau_{r,j})
\]

\[
\tau = 1.5\tau_f + 0.5\tau_r
\]

For the total domino cell the rise and fall time have to be equal:

\[ 1.5\tau_{d,NAND} + 0.5\tau_{s,INV} = 0.5\tau_{s,NAND} + 0.5\tau_{d,INV} \]

Together with equations (12), (13), (26), (27), also substituting \( W_n = W_p / R \), we get the form:

\[
W_p = \frac{(-1.21 + 0.39R)R}{1.64 \times 10^{-2}R^2 + 0.42 \times 10^{-2}R - 1.21 \times 10^{-2}}
\] (28)
\( W_p \) is positive for 
\[ 0 < K < 0.74 \quad K > 3.1 \]

\( W_p \) is negative for 
\[ 0.74 < K < 3.1 \]

The area for which \( W_p \) is negative is not useless for the optimization. In this area \( W_p \) is negative if it is desired that the rise and fall time is equal. However in practice a negative size is impossible. If \( R \) is chosen in \([0.74,3.1]\) and \( W_p \) is positive, then the rise and fall time are not equal. Furthermore it can be seen that each \( W_p \) (for some \( W_p \) twice) applies to another aspect ratio.

For the optimization of the domino cell the area \( R > 3.1 \) is useless because of the small values of \( W_p \) and even smaller values of \( W_n \). Through which designable parameters of \( W_p \) and \( W_n \) would cause \( R \) grow to large.

\[ R = 3.5 \quad W_p = 2.6 \]
\[ R = 4 \quad W_p = 5 \]
\[ R = 10 \quad W_p = 10 \]

For \( R = 1 \) and \( R = 2 \) has been investigated which one has the largest similarity between the rise and fall time. In table 9 the results obtained with SPICE are stated.

Table 9: Rise and fall time of the domino cell for \( R = 1 \) and \( R = 2 \)

<table>
<thead>
<tr>
<th>( R )</th>
<th>width ((\mu\text{m}))</th>
<th>( t_r ) ((\text{ns}))</th>
<th>( t_f ) ((\text{ns}))</th>
<th>( t ) ((\text{ns}))</th>
<th>( \bar{t} ) ((\text{ns}))</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>( W_p = 30 ) ( W_n = 30 )</td>
<td>9.4</td>
<td>6.3</td>
<td>5.9</td>
<td>5.9</td>
</tr>
<tr>
<td>2</td>
<td>( W_p = 40 ) ( W_n = 20 )</td>
<td>10.2</td>
<td>6.2</td>
<td>8.6</td>
<td>6.9</td>
</tr>
</tbody>
</table>

For the average deviation the function \( D \) is used, see page 25:

\[ D = \frac{1}{3} \sum_{i=1}^{3} \frac{|\Delta t_i|}{t_i} \times 100\% \]

The average deviation of the domino cell is:

\[ D_{R=1} = 26\% \]
\[ D_{R=2} = 35\% \]

It follows that the SCVS cell with \( R = 1 \) has the smallest difference in fall and rise time. Another important measure is the propagation delay. It can be seen that for \( R = 1 \) the average propagation delay of the average domino cell is smaller then the propagation delay for \( R = 2 \).

So, for \( R = 1 \) the noise margins are larger and the average propagation delay is smaller, therefore it is decided to
work with this aspect ratio to optimize the product of chip area and propagation delay.

-The objective function $H$

A layout of the SCVS cell was not found, in spite of the large number of articles about domino CMOS that were found. Therefore is choosen to use the same formula for the area as was used for the AOI circuit. This does not imply that the internal structure of the AOI circuit is the same as the that of the domino circuit. The PMOS transistors for the AOI circuit were placed in the top row of the layout, in domino circuits only two PMOS transistors are used. The solution for this problem is placing the two PMOS transistors in the first column. In this way the output and inputs of the domino cell can be easily connected to other cells. No area is wasted because the size of the PMOS transistors is equal to the size of the NMOS transistor.

Thus:

$$A = W_p + W_n + S$$

By keeping the aspect ratio $R$ fixed ($R=1$), $H$ and the propagation delay depend only on one variable. By replacing $W_n$ by $W_p$ the propagation delay times can be written as:

$$E_{NAND} = (5.5 \times 10^{-3} W_p + 10^{-2}) \cdot 5 \cdot \frac{1}{W_p} \cdot 10^{-8}$$

$$E_{INV} = (15 \times 10^{-4} W_p + 0.21) \cdot 5 \cdot \frac{1}{W_p} \cdot 10^{-8}$$

The objective function $H$ gets the form:

$$H(W_p) = A \cdot (E_{NAND} + E_{INV})$$

$$H(W_p) = 40.867 W_p + 12.356 + \frac{W_p}{W_p}$$

The minimum can be calculated by setting the derivative of $H$ equal to zero:

$$H'(W_p) = 40.867 - \frac{6968.22}{W_p^2}$$

minimum:

$$W_p = 13.1 \mu m$$

$$W_n = 13.1 \mu m$$

$$H(W_p) = 108.0 \times 10^{-15}$$

The propagation delay times and the objective function for $R=1$ are stated in table 10.
- 34 -

Table 10: The propagation delay times and the objective function $H$ for $N=1$ calculated with the theoretical model.

<table>
<thead>
<tr>
<th>$W_p=W_n$</th>
<th>5</th>
<th>10</th>
<th>15</th>
<th>20</th>
<th>25</th>
<th>30</th>
</tr>
</thead>
<tbody>
<tr>
<td>1AND</td>
<td>$t_f$</td>
<td>7.03</td>
<td>4.42</td>
<td>3.56</td>
<td>3.13</td>
<td>2.87</td>
</tr>
<tr>
<td></td>
<td>$t_r$</td>
<td>14.84</td>
<td>8.25</td>
<td>6.04</td>
<td>4.96</td>
<td>4.28</td>
</tr>
<tr>
<td>2AND</td>
<td>$t_f$</td>
<td>7.03</td>
<td>4.42</td>
<td>3.56</td>
<td>3.13</td>
<td>2.87</td>
</tr>
<tr>
<td></td>
<td>$t_r$</td>
<td>15.66</td>
<td>8.96</td>
<td>6.71</td>
<td>5.62</td>
<td>4.92</td>
</tr>
<tr>
<td>3AND</td>
<td>$t_f$</td>
<td>7.03</td>
<td>4.42</td>
<td>3.56</td>
<td>3.13</td>
<td>2.87</td>
</tr>
<tr>
<td></td>
<td>$t_r$</td>
<td>16.48</td>
<td>9.67</td>
<td>7.38</td>
<td>6.28</td>
<td>5.56</td>
</tr>
<tr>
<td>$H$</td>
<td>5.67</td>
<td>3.35</td>
<td>2.57</td>
<td>2.19</td>
<td>1.95</td>
<td>1.80</td>
</tr>
</tbody>
</table>

- Charge redistribution

The charge redistribution that appears for some input sequences can influence the logic levels of the circuit [5,6,21]. Referring to the 3-input AND gate in figure 16.

![Figure 16: charge redistribution in 3-AND domino CMOS.](image)

During precharge the capacitance $C_1$ will be charged. If the inputs $A$ and $B$ go high and $C$ stays low, the charge stored in $C_1$ is redistributed between $C_1$, $C_2$ and $C_3$. By this redistribution the precharged level is degraded, the output level can go high and influence fanout gates.
A static variation of domino CMOS can solve the charge-sharing problem. This can be obtained by the addition of a PMOS transistor as shown in figure 17a. The transistor functions as a means of removing charge which accumulates on the output node as the result of leakage or noise. Another way of solving this problem is to add a feedback PMOS transistor, see figure 17b.

![Figure 17: Two ways to eliminate the charge-sharing problem.](image)

Although the second solution adds an additional capacitance at the output, this solution is more well-considered. If the output goes high (and the intermediate output low) the feedback transistor stops conducting. Therefore the additional power needed is minimal.

Another variant of CMOS uses only the pull up transistor with the gate connected to the ground. This can be used for cases in which the precharged cycle can be very long.

### 5.2.2. SPICE simulation

The SCVS circuits are implemented in SPICE as follows. The three SCVS circuits are drawn in figure 18.

* CIRCUIT 'LAND'

```
M1 1 4 0 0 MOD1 PD=15U PS=15U
M2 2 5 1 0 MOD1 PD=15U PS=15U
M3 2 4 3 3 MOD2 PD=15U PS=15U
M4 6 2 0 0 MOD1 PD=15U PS=15U
M5 6 2 3 3 MOD2 PD=15U PS=15U
COUT 6 0 0.2P
```
Figure 18: The three SCVS circuits.

* CIRCUIT 2 AND

M1 1 5 0 0 MOD1 PD=15U PS=15U  
M2 2 6 1 0 MOD1 PD=15U PS=15U  
M3 3 6 2 0 MOD1 PD=15U PS=15U  
M4 3 5 4 4 MOD2 PD=15U PS=15U  
M5 7 3 0 0 MOD1 PD=15U PS=15U  
M6 7 3 4 4 MOD2 PD=15U PS=15U  
COUT 7 0 0.2P

* CIRCUIT 3 AND

M1 1 6 0 0 MOD1 PD=15U PS=15U  
M2 2 7 1 0 MOD1 PD=15U PS=15U  
M3 3 7 2 0 MOD1 PD=15U PS=15U  
M4 4 7 3 0 MOD1 PD=15U PS=15U  
M5 4 6 5 5 MOD2 PD=15U PS=15U  
M6 8 4 0 0 MOD1 PD=15U PS=15U  
M7 8 4 5 5 MOD2 PD=15U PS=15U  
COUT 8 0 0.2P

The results of the SPICE simulation have been noted in table 11.
Table 11: The propagation delay times and the objective function $H$ for $R=1$, computed with SPICE.

<table>
<thead>
<tr>
<th>$W_p = W_n$</th>
<th>5</th>
<th>10</th>
<th>15</th>
<th>20</th>
<th>25</th>
<th>30</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_f$</td>
<td>10</td>
<td>7.1</td>
<td>6.4</td>
<td>6</td>
<td>5.7</td>
<td>5.5</td>
</tr>
<tr>
<td>$t_r$</td>
<td>15</td>
<td>9.4</td>
<td>7.7</td>
<td>6.8</td>
<td>6.2</td>
<td>5.9</td>
</tr>
<tr>
<td>$t_f$</td>
<td>10.5</td>
<td>7.3</td>
<td>6.9</td>
<td>6.5</td>
<td>6.1</td>
<td>5.9</td>
</tr>
<tr>
<td>$t_r$</td>
<td>17</td>
<td>11.3</td>
<td>9.5</td>
<td>8.7</td>
<td>8.1</td>
<td>7.1</td>
</tr>
<tr>
<td>$t_f$</td>
<td>10.5</td>
<td>8.5</td>
<td>7.1</td>
<td>6.7</td>
<td>6.5</td>
<td>6.3</td>
</tr>
<tr>
<td>$t_r$</td>
<td>19</td>
<td>13</td>
<td>11.3</td>
<td>10.3</td>
<td>9.7</td>
<td>9.4</td>
</tr>
<tr>
<td>$H$</td>
<td>341.8</td>
<td>330.1</td>
<td>366.8</td>
<td>412.5</td>
<td>458.3</td>
<td>508.5</td>
</tr>
</tbody>
</table>

It follows from table 11 that the minimum of the objective function occurs for:

$$W_p = 10\mu m$$

$$W_n = 10\mu m$$

$$H = 330.1 \times 10^{-15}$$

5.2.3. Conclusions

SCVS logic offers great possibilities. Especially the reduction of the number of PMOS transistors is an important factor, that's why domino CMOS is often referred to as pseudo NMOS.

The SCVS circuit consists of a standard part, i.e. the inverter and the transistors connected to the clock. This part contains two PMOS and two NMOS transistors. The second part is a variable NMOS network, the number of NMOS transistors is equal to the number of inputs, to a maximum of 9 transistors. This circuit structure reduces the chip area considerably.

In general, dynamic logic is not considered suitable for the design of standard cells due to the sensitivity to changing load conditions. Because SCVS logic is fully buffered by an inverter, the dynamic nodes are isolated of the load capacitance. Thus domino CMOS is not sensitive to changing load conditions.

Since the input capacitance of SCVS cells consists of the gate capacitance of one NMOS transistor, large fanouts can
be applied.

The dynamic part of the SCVS cell is built in such a way that one single clock pulse turns on all the gates. Thereby a complex clock circuit is not needed and the full speed of the dynamic part can be used.

According to the theoretical model, the object function is optimal for $W_p = W_n = 13.1 \mu m$. In this case the average propagation delay of the three SCVS circuits is equal to 5.5ns. Through SPICE simulation an optimum was found for $W_p = W_n = 10 \mu m$ with an average propagation delay time of 9.4ns. Comparing the results of the theoretical with the results of SPICE simulation, it can be seen that large differences occur in the propagation delay times. This is mainly caused by the fact that the theoretical model doesn't take into account the "non ideal" input waveform of the inverter. Because the output of the variable NAND has not an "ideal" pulse waveform, the delay of the inverter is much larger than calculated.

A drawback of the SCVS circuits is that inverted logic signals cannot be used. As a result the construction in an SCVS circuit of an exclusive or function is very complex.

Charge-sharing is another problem of domino CMOS. At the expense of chip area and extra delay, an additional PMOS transistor connected to the internal node can solve this problem.

5.3. Differential cascode voltage switch logic

5.3.1 Properties

Differential cascode voltage switch (DCVS) logic can be formed by adding another set of NMOS transistors in the NMOS network [5,8,9,19]. More specific, DCVS logic can be composed by joining two standard domino circuits. One of them performing the "true" function and the other the complement function. DCVS logic can be designed as a static or dynamic circuit, see figure 19.

The layout of this circuit is very regular as it forms into a rectangular array to provide improved density, see figure 20.
For the reduction of charge-sharing and noise within the tree a feedback transistor can be added see figure 21.
Figure 21: DCVS logic with reduced charge sharing and noise.

Other implementations of DCVS logic have been published \{7,13\}, see figure 22. In figure 22a, the DCVS circuit includes a trigger circuit, for decreasing logic rise and fall times. Figure 22b shows a DCVS circuit with two depletion NMOS transistors, a higher tree of NMOS transistors may be used in the combinational network.

(a) With a trigger circuit  (b) With two depletion NMOS transistors

Figure 22: Two additional implementations of DCVS logic.

For the realization of a DCVS circuit both the true and complement function have to be realized in the NMOS network. Beside of that, a standard part has to be realized,
containing six PMOS transistors and two NMOS transistors, see figure 18b. So, the chip area per cell is large.

On the other hand, all signals are present in DCVS logic, non-inverted as well as inverted. Therefore logic functions like exclusive ors can easily be implemented. A drawback of the presence of the true and complement signal, is the high wiring complexity.

DCVS logic seems to need a large chip area but some advantages have not yet been mentioned.

1) The true and complement function are totally realized with NMOS transistors, so the drawback of using PMOS transistors is avoided.

2) The two cross coupled PMOS transistors can be made very small, because they don't have to charge load capacitances.

3) As mentioned in section 2.4., it is preferable to use cells which can perform medium functions, e.g. with 24 input signals. In articles [15,17,18,19] a DCVS masterslice implementation is discussed. Logic trees with \( N \)-high cascading of differential pairs of NMOS devices are capable of processing boolean functions with up to \( (2^N-1) \) input variables. By this the area used for the standard part per function reduces, while the variable part is larger.

5.3.2. SPICE simulation

It is assumed that the aspect ratio \( R \) of the DCVS circuit is equal to the aspect ratio of the SCVS circuit, so \( R=1 \). During the optimization of the object function \( H \), the width of the two latch transistors is kept at 5\( \mu \)m, because they don't have to charge load capacitances.

The DCVS circuits have been implemented in SPICE, as follow. The 3-input AND/NAND has been drawn in figure 23. The 1-input and 2-input AND/NAND can be derived from the latter.

*CIRCUIT 3AND/NAND*

```
M1 1 8 0 0 MOD1
M2 2 8 1 0 MOD1
M3 3 8 2 0 MOD1
M4 4 9 0 0 MOD1
M5 4 9 0 0 MOD1
M6 4 9 0 0 MOD1
M7 3 4 5 5 MOD2
M8 4 3 5 5 MOD2
M9 6 3 0 0 MOD1
```
Figure 23: 3-input AND/NAND in DCVS-logic.

The results of the SPICE simulation are stated in table 12.

The SPICE program did only simulate the DCVS circuit for W is equal to 20, 25 and 30µm, for smaller values of W the simulation was aborted. It can be seen from table 12 that the average delay time t is minimal for the smallest value of W. Thus the objective function is minimal for W=20µm. Also the average deviation is minimal for W=20µm. However, this doesn't imply that the objective function and the average deviation are optimal for W=20µm. More investigation has to be done into smaller values of the width of the NMOS and PMOS transistors.
Table 12: The objective function $H$ and the average delay time of the DCVS circuit for different values of $W$

<table>
<thead>
<tr>
<th>$W_p=W_n$</th>
<th>20</th>
<th>25</th>
<th>30</th>
</tr>
</thead>
<tbody>
<tr>
<td>**1AND/  **</td>
<td>$\tau_f$</td>
<td>23</td>
<td>23.5</td>
</tr>
<tr>
<td><strong>NAND</strong></td>
<td>$\tau_r$</td>
<td>16.5</td>
<td>17.5</td>
</tr>
<tr>
<td>**2AND/  **</td>
<td>$\tau_f$</td>
<td>19</td>
<td>25</td>
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<tr>
<td><strong>NAND</strong></td>
<td>$\tau_r$</td>
<td>18</td>
<td>23</td>
</tr>
<tr>
<td>**3AND/  **</td>
<td>$\tau_f$</td>
<td>22</td>
<td>21.5</td>
</tr>
<tr>
<td><strong>NAND</strong></td>
<td>$\tau_r$</td>
<td>12</td>
<td>11</td>
</tr>
<tr>
<td>$E$</td>
<td></td>
<td>15.3</td>
<td>15.3</td>
</tr>
<tr>
<td>$D$</td>
<td></td>
<td>65%</td>
<td>83%</td>
</tr>
<tr>
<td>$H$</td>
<td></td>
<td>841.0</td>
<td>996.5</td>
</tr>
</tbody>
</table>

5.3.3. Conclusions

Because most of the advantages and disadvantages of DCVS logic have been dealt with in section 5.3.1., the several items will only be recapitulated.

**Advantages DCVS logic:**
- low power dissipation
- simple realization of XOR functions
- possibility of masterslice implementation
- simple clock realization
- same speed as standard domino CMOS
- high fanout
- glitch free

**Disadvantages DCVS logic:**
- the need for large chip area
- high wiring complexity
- charge sharing, however this can be solved at the expense of extra chip area and extra delay.
5.4. Latched domino CMOS

5.4.1. Properties

In [25] a new domino CMOS structure is proposed. SCVS logic suffers from the disadvantage that inverting logic cannot be implemented in standard domino logic. This limits the logic functions that can be implemented and the complement of a function has to be done at the input or output of a domino circuit. DCVS logic has been proposed to overcome this problem. Another circuit structure that solves this problem too, is called "latched domino CMOS".

A circuit diagram of a basic latched domino circuit is shown in figure 24.

![Figure 24: Basic domino AND/NAND gate.](image)

It can be seen that the gate is precharged when the clock is low. Evaluation starts when the clock goes high. If the combinational network doesn't discharge the node n2, the node n1 will always be discharged, because M1 turns on and M2 will stay off. Complement output Q will then go high and Q will stay low. If the combinational network discharges node n2, M1 will stay off and M2 turns on, therefore node 1 remains high. Output Q stays low and Q will go high.

Also an improved latched domino gate is proposed see figure 25. A pull up device M_p added between node n3 and V_{dd}, the clocking transistor M_{ck} is split in two. By the pull up transistor M_p, node 3 is precharged high. This improves the reliability of operation, because it enables the single-ended logic block to apply a larger voltage imbalance to the sense amplifier, on the rising edge of the clock signal. This can be done at the expense of a small delay in the latching operation.
Figure 25: Improved latched domino gate.

However, this technique can only be applied to the first stage of logic in a series of domino gates, if the glitch-free property of domino logic is to be preserved. Latched domino logic can drive standard domino gates, but they cannot be driven by standard domino gates, because the glitch-free operation requires that the inputs to a gate stabilize during the precharge clock phase. In spite of this drawback, any logic function can be performed in two stages. The fact that latched domino gates create complement functions increases the logic flexibility of domino CMOS.

Another advantage is the reduction in wiring overhead. Latched domino logic doesn't require the complementation of input signals, which in worst cases can double the area.

5.4.2. Conclusions

The advantages and disadvantages of latched domino CMOS are:

advantages:
- improvement in logic flexibility by the possibility of complement functions
- reduction of wiring overhead
- the same speed as standard domino CMOS

disadvantage:
- the glitch-free property of standard domino CMOS is lost.
5.5. Domino CMOS without a buffer

In [10,30] a novel structure of domino CMOS is reported. In [30] it is proposed as a dynamic pass transistor network, because the great resemblance with the operation of a chain of pass transistors. Here the new design is seen as sort off domino CMOS. This because of the fact that it consists of the first part of a standard domino circuit, see figure 26.

![Diagram of Domino CMOS without a buffer]

Figure 26: Domino CMOS without a buffer.

In the operation of the circuit in figure 22a, when the clock goes high, the complement clock goes low, turning on the clocked PMOS transistor, and the the output is precharged to $V_{dd}$. If the clock goes low, the complement of the clock goes high, turning on the clocked NMOS transistor, and the NMOS network may discharge the output to ground. Its complementary circuit is shown in figure 22b. It can be seen that the output goes low during precharge and that the PMOS network may charge the output to $V_{dd}$ during the evaluation phase.

The design structure is based on the fact that a p-load gate can directly drive an n-load gate and vice versa. The circuit consists of alternating the two types of CMOS dynamic logic gates.

A drawback of the novel structure is that charge-sharing appears at the output and that the input is sensitive to spikes. This because of the precharging at the output node. Charge-sharing can be avoided by carefully examining the internal nodes in the NMOS or PMOS network and selectively precharge this nodes as well as the output, figure 27 gives an example.
Figure 27: Domino CMOS without a buffer implementation of a one-bit adder.

An additional NMOS transistor $Q_5$ was added to node 2 to eliminate the charge redistribution between this node and the output node 3. In this case however, an easier solution consists. By interchanging the transistors $Q_2$, $Q_3$ and $Q_4$ with $Q_1$, charge redistribution is also avoided. In general, when only one input in each of the serial structures, comes from a preceding stage, no additional transistor is needed. In the NMOS network this input goes to the bottom of the device and in the PMOS network it goes to the top.

The new domino CMOS structure is very fast because of the lower capacitance and lower threshold, though at the expense of reduction in noise margins. Also the additional delay of the buffer is avoided.

The chip area is very small because of the fact that only two additional transistors are needed besides the NMOS network.

Another advantage of this design structure is that the logic function can be generated using only one polarity of the input variables.

A disadvantage of this circuit is that with more than two levels of gates, may cause the possibility of driving an input with gates from the same type. By this the device will stay turned on during the precharge and some time afterward, depending on the input combination, and charge redistribution is possible. This may be avoided by separation through inverters as in standard domino CMOS.
Before dealing with the CMOS structures, some attention will be directed to the theoretical model and the SPICE simulation. The differences of the theoretical model and the SPICE simulation are large, in some cases a difference of more than 50% occurs. The largest part of the discrepancy between the theoretical model and the SPICE simulation can be ascribed to the difference of the rise and fall time of the input signal. In the theoretical model an 'ideal' pulse is used and in the SPICE simulation a pulse with rise and fall time equal to 2ns is applied, this was necessary because in some cases the simulation was aborted when smaller values than 2ns were applied.

Besides the aforementioned aspect, the SPICE simulation yields a more accurate result than the theoretical model. Especially because of the small transistor sizes that are used, therefore a precise calculation of the parasitic capacitances is important, e.g. the drain and source-junction sidewall capacitance. This calculations would be theoretically very time expensive, and complex.

Although the SPICE simulation using level 2 models is very accurate, it would be better using SPICE with level 3 models because this model takes accurately into account the charging and discharging of parasitic capacitances, especially for small transistor sizes.

The area of the CMOS structures has to be adjusted before they can be compared equally. So far, only the width has been taken into account. Assuming that an average boolean function contains 6 literals, and knowing that the length of a PMOS or NMOS transistor is equal to 20µm, we can derive for the length of the three CMOS structures:

- **AOI cell**
  \[ L = 6 \times 20 = 120\mu m \]
  (one row of 6 NMOS transistors and one row of 6 PMOS transistors)

- **pass transistor cell**
  \[ L = 6 \times 20 + 1 \times 20 = 140\mu m \]
  (one row of 6 NMOS transistors, one row of PMOS transistors and one inverter)

- **SCVS cell**
  \[ L = 3 \times 20 + 1 \times 20 + 1 \times 20 = 100\mu m \]
  (two rows of 3 NMOS transistors, the clock transistors and one inverter)

Taking into account the length yields the following results for the optimized cell structures according to the SPICE simulation:

- **AOI cell**
  \[ W_p = 20\mu m \quad W_n = 10\mu m \quad H = 316.0 \times 10^{-19} \]

- **pass transistor cell**
  \[ W_p = 10\mu m \quad W_n = 5\mu m \quad H = 352.8 \times 10^{-19} \]

- **SCVS cell**
  \[ W_p = 10\mu m \quad W_n = 10\mu m \quad H = 330.1 \times 10^{-19} \]
The object function is minimal for the AOI circuit. Let us now look closer at the two parts that determinate the function $H$, the area and the propagation times of a cell.

- The average delay times are:
  
  AOI cell : $\bar{\tau} = 5.9$ns
  
  pass transistor cell : $\bar{\tau} = 8.4$ns
  
  SCVS cell : $\bar{\tau} = 9.4$ns

It can be seen that the SCVS cell is about one and a half times slower then the AOI cell. However, three items have not yet been mentioned:

1) The clock of the SCVS cell. In the operation of the cell, the clock needs a full period. The precharge phase of the cell, can be spread over several cells connected in series. Thus only a small part of the precharge phase contributes to the average delay. (e.g. ten cells in series adds 1ns delay to one cell).

2) The input capacitance of AOI cells is two to three times larger then the input capacitance of AOI cells. Because of this the average delay of a SCVS cell will decrease by half the value mentioned.

3) The interconnection wires of AOI cells are more complex and large then that of SCVS cells (the output capacitance, and thus the propagation delay, depends on interconnection wire capacitance). Because of this the average delay of an AOI cell will increase.

It follows from this three properties that in practice SCVS cells and AOI cells will have about equal propagation delays.

- The average areas of the cells are:
  
  AOI cell : $A = 5400\mu m^2$
  
  pass transistor cell : $A = 4200\mu m^2$
  
  SCVS cell : $A = 3500\mu m^2$

The SCVS cell occupies the least area. Beside of that also in this calculation the difference of the interconnection wires is not taken into account, this is especially a drawback of the AOI circuit.
The average deviation is used to compare the noise margins of the CMOS structures:

- **AOI cell**: $D = 128\%$
- **pass transistor cell**: $D = 89\%$
- **SCVS cell**: $D = 38\%$

It follows that the SCVS cell yields the greatest noise margins. The average deviation of the AOI cell is large, this is a result of the large difference of the rise and fall time of the 3-input NOR and NAND. It is advisable to avoid using many 3-input NOR or NAND cells (AOI) because it degrades the noise margins and it also degrades the propagation delays.

It is difficult to say which CMOS structure yields the most advantageous properties for using computer aids. The interconnection wiring of AOI cells is complex, the difference of the width of the NMOS and PMOS transistor is also a drawback. It is hard to layout the corresponding NMOS and PMOS transistor in the same column. The pass transistor chains will be easy to layout, because they can easily be fit into an array. The SCVS cell consists of a standard part, namely the inverter and the two clocking transistors, the layout of this part is the same for every cell. The other part consists of the NMOS network, wherein every variable correspondents with one transistor. Another advantage of SCVS logic is the glitch-free nature of SCVS logic. This implies that during the design of a circuit no time is wasted searching undefined states. One other possibility to store SCVS cells logic is, using pluricell layout style. Whereas polycell layouts find their cells in a master library that is built and maintained independently from the individual applications, pluricells are constructed ad hoc. This is feasible because the transistors in the NMOS network can easily be interchanged. With the pluricell layout style it is also possible to use SCVS cells with larger trees of NMOS transistors, thus SCVS cells executing larger functions.

So far no attention has been paid to the power dissipation of the CMOS structures. Because of the lower transistor count, the smaller transistor sizes and the smaller output capacitances the power dissipation of the SCVS cell will be about half the power dissipation of the AOI cell.

It is hard to tell what are the disadvantages and the advantages of the pass transistor cells. Mostly they intervene between the advantages and disadvantages of the SCVS cells and the AOI cells. Obviously more research has to be done after the properties of pass transistor cells, todays knowledge is not sufficient.
Looking back, it is seen that the SCVS cell has the most advantageous properties. Therefore it is decided that domino CMOS provides the best features building a CMOS library.

More research has to be done into the special domino CMOS structures:

1) DCVS logic
2) latched domino CMOS
3) domino CMOS without a buffer

For convenience the properties of SCVS logic will shortly be recapitulated:

advantages:

- small area
- large noise margins
- fast
- low power dissipation
- suitable for computer aided design
- glitch-free
- suitable for pluricell design
- wired OR and AND function
- no complex clocking scheme
- high fanout
- high fanin

disadvantages:

- charge-sharing:
  this can be solved by using a static pull up transistor

- complement variables are not available:
  this can be solved by using:
  - DCVS logic
  - latched domino CMOS
  - domino CMOS without a buffer
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### Appendix 1. - SPICE parameters

<table>
<thead>
<tr>
<th>Variable</th>
<th>Definition</th>
<th>Unit</th>
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<tr>
<td>LEVEL</td>
<td>model index</td>
<td>-</td>
</tr>
<tr>
<td>VTO</td>
<td>zero-bias threshold voltage</td>
<td>V</td>
</tr>
<tr>
<td>KP</td>
<td>transconductance parameter</td>
<td>A/V²</td>
</tr>
<tr>
<td>GAMMA</td>
<td>bulk threshold parameter</td>
<td>V⁰.⁵</td>
</tr>
<tr>
<td>PHI</td>
<td>surface potential</td>
<td>V</td>
</tr>
<tr>
<td>LAMBDA</td>
<td>channel length modulation</td>
<td>1/V</td>
</tr>
<tr>
<td>RD</td>
<td>drain ohmic resistance</td>
<td>Ohm</td>
</tr>
<tr>
<td>RS</td>
<td>source ohmic resistance</td>
<td>Ohm</td>
</tr>
<tr>
<td>CBSD</td>
<td>zero-bias B-D junction cap.</td>
<td>F</td>
</tr>
<tr>
<td>CBS</td>
<td>zero-bias B-S junction cap.</td>
<td>F</td>
</tr>
<tr>
<td>IS</td>
<td>bulk junction saturation current</td>
<td>A</td>
</tr>
<tr>
<td>PB</td>
<td>bulk junction potential</td>
<td>V</td>
</tr>
<tr>
<td>CGSO</td>
<td>gate-source overlap capacitance per meter channel width</td>
<td>F/m</td>
</tr>
<tr>
<td>CGDO</td>
<td>gate-drain overlap capacitance per meter channel width</td>
<td>F/m</td>
</tr>
<tr>
<td>CGBO</td>
<td>gate-bulk overlap capacitance per meter channel length</td>
<td>F/m</td>
</tr>
<tr>
<td>KSH</td>
<td>drain and source diffusion sheet resistance</td>
<td>Ohm/m²</td>
</tr>
<tr>
<td>CJ</td>
<td>zero-bias bulk junction bottom cap. per sq-meter of junction area</td>
<td>F/m²</td>
</tr>
<tr>
<td>MJ</td>
<td>bulk junction bottom grading coef.</td>
<td>-</td>
</tr>
<tr>
<td>CJSW</td>
<td>zero-bias bulk junction sidewall cap. per meter of junction perimeter</td>
<td>F/m</td>
</tr>
<tr>
<td>MJSW</td>
<td>bulk-junction sidewall grading coef.</td>
<td>-</td>
</tr>
<tr>
<td>JS</td>
<td>bulk-junction saturation current per sq.-meter of junction area</td>
<td>A/m²</td>
</tr>
<tr>
<td>TOX</td>
<td>oxide thickness</td>
<td>m</td>
</tr>
<tr>
<td>NSUB</td>
<td>substrate doping</td>
<td>1/cm³</td>
</tr>
<tr>
<td>NSS</td>
<td>surface state density</td>
<td>1/cm²</td>
</tr>
<tr>
<td>Symbol</td>
<td>Description</td>
<td>Unit</td>
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<tr>
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<tr>
<td>NFS</td>
<td>fast surface state density</td>
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</tr>
<tr>
<td>TPG</td>
<td>type of gate material</td>
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<tr>
<td></td>
<td>+1 opp. to substrate</td>
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</tr>
<tr>
<td></td>
<td>-1 same as substrate</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>0 Al gate</td>
<td>-</td>
</tr>
<tr>
<td>XJ</td>
<td>metallurgical junction depth</td>
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<td>LD</td>
<td>lateral diffusion</td>
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<td>UO</td>
<td>surface mobility</td>
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<td>UCRIT</td>
<td>critical field for mobility degradation</td>
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</tr>
<tr>
<td>UEXP</td>
<td>critical field exponent in mobility degradation</td>
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</tr>
<tr>
<td>UTRA</td>
<td>transverse field coef. (mobility)</td>
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</tr>
<tr>
<td>VMAX</td>
<td>maximum drift velocity of carriers</td>
<td>m/s</td>
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<tr>
<td>NEFF</td>
<td>total channel charge coefficient</td>
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<tr>
<td>XQC</td>
<td>thin-oxide capacitance model flag and coefficient of channel charge share</td>
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</tr>
<tr>
<td></td>
<td>attribute to drain</td>
<td>-</td>
</tr>
<tr>
<td>KF</td>
<td>flicker noise coefficient</td>
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</tr>
<tr>
<td>AF</td>
<td>flicker noise exponent</td>
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<tr>
<td>FC</td>
<td>coefficient for forward-bias depletion capacitance formula</td>
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<td>KAPPA</td>
<td>saturation field factor</td>
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Appendix 2. Symbols and abbreviations

\( A(w_p, w_n) \) chip area

\( p', n \) transistor gain factor of PMOS and NMOS transistors

\( C_A(p), C_A(n) \) capacitance per unit area in PMOS and NMOS transistors

\( C_G(p), C_G(n) \) gate channel capacitance

\( C_i \) input capacitance of fanout

\( C_l \) load capacitance

\( C_d \) drain capacitance in the driver

\( C_P(p), C_P(n) \) capacitance per unit perimeter in PMOS and NMOS transistors

\( C_w \) interconnection-wire capacitance

\( \Delta \) average deviation of fall and rise times

\( \varepsilon \) permittivity of free space

\( H(w_p, w_n) \) objective function, product of propagation delay and chip area

\( K_{ox} \) relative permittivity of the silicon dioxide

\( p', n \) mobility of minority carriers in PMOS and NMOS transistors

\( R \) aspect ratio \( w_p/w_n \)

\( t_f \) fall time

\( t_r \) rise time

\( V_{dd} \) power supply voltage

\( V_{ds} \) drain source voltage

\( V_g \) gate voltage

\( V_{th(p)}, V_{th(n)} \) threshold voltage

\( V_i \) midtransition voltage

\( V_{in}(\cdot) \) input waveform

\( w_p, w_n \) gate channel width in NMOS and PMOS transistors
Appendix 3. - Four NMOS SPICE models

HERZIENE VERSIE 29-01-1985

1) MODEL THE EEN 3-02-1984
   KP CONSTANT
   GAMMA CONSTANT
   LAMBDA CONSTANT
   .MODEL DEP NMOS(LEVEL=2 VTO=-3.75 KP=22.5U GAMMA=0.5 PHI=0.58
   +LAMBDA=0.02 PB=0.75 CGSO=370P CGDO=370P CGBO=395P RSH=20
   +CJ=80U MJ=0.5 CJSW=330P MJSW=0.25 JS=6.2U TOX=70N
   +XJ=0.7U LD=0.7U
   )
   .MODEL ENH NMOS(LEVEL=2 VTO=0.85 KP=34U GAMMA=0.35 PHI=0.58
   +LAMBDA=0.02 PB=0.75 CGSO=370P CGDO=370P CGBO=395P RSH=20
   +CJ=80U MJ=0.5 CJSW=330P MJSW=0.25 JS=6.2U TOX=70N
   +XJ=0.7U LD=0.7U
   )

2) MODEL THE TWEE 3-02-1984
   KP VARIABEL
   GAMMA VARIABEL
   LAMBDA CONSTANT
   .MODEL DEP NMOS(LEVEL=2 VTO=-3.605
   +LAMBDA=0.02 PB=0.75 CGSO=370P CGDO=370P CGBO=395P RSH=20
   +CJ=80U MJ=0.5 CJSW=330P MJSW=0.25 JS=6.2U TOX=70N NSUB=1.66E15
   +XJ=0.7U LD=0.7U UO=581 UCRIT=37E4 UEXP=0.24)
   .MODEL ENH NMOS(LEVEL=2 VTO=0.847
   +LAMBDA=0.02 PB=0.75 CGSO=370P CGDO=370P CGBO=395P RSH=20
   +CJ=80U MJ=0.5 CJSW=330P MJSW=0.25 JS=6.2U TOX=70N NSUB=8.7E14
   +XJ=0.7U LD=0.7U UO=738 UCRIT=4.25E4 UEXP=0.06)

3) MODEL THE DRIE 14-03-1984
   KP VARIABEL
   GAMMA VARIABEL
   LAMBDA VARIABEL
   .MODEL DEP NMOS(LEVEL=2 VTO=-3.605
   +LAMBDA=0.02 PB=0.75 CGSO=370P CGDO=370P CGBO=395P RSH=20
   +CJ=80U MJ=0.5 CJSW=330P MJSW=0.25 JS=6.2U TOX=70N NSUB=1.66E15
   +XJ=0.7U LD=0.7U UO=581 UCRIT=37E4 UEXP=0.24)
   .MODEL ENH NMOS(LEVEL=2 VTO=0.847
   +LAMBDA=0.02 PB=0.75 CGSO=370P CGDO=370P CGBO=395P RSH=20
   +CJ=80U MJ=0.5 CJSW=330P MJSW=0.25 JS=6.2U TOX=70N NSUB=8.7E14
   +XJ=0.7U LD=0.7U UO=738 UCRIT=4.25E4 UEXP=0.06)

4) MODEL THE VIER 17-10-1984
   KP VARIABEL
   GAMMA CONSTANT
   LAMBDA CONSTANT
   .MODEL DEP NMOS(LEVEL=2 VTO=-3.75 GAMMA=0.5 PHI=0.58
   +LAMBDA=0.02 PB=0.75 CGSO=370P CGDO=370P CGBO=395P RSH=20
   +CJ=80U MJ=0.5 CJSW=330P MJSW=0.25 JS=6.2U TOX=70N NSUB=1.66E15
   +XJ=0.7U LD=0.7U UO=581 UCRIT=37E4 UEXP=0.24)
   .MODEL ENH NMOS(LEVEL=2 VTO=0.85 GAMMA=0.35 PHI=0.58
   +LAMBDA=0.02 PB=0.75 CGSO=370P CGDO=370P CGBO=395P RSH=20
   +CJ=80U MJ=0.5 CJSW=330P MJSW=0.25 JS=6.2U TOX=70N NSUB=8.7E14
   +XJ=0.7U LD=0.7U UO=738 UCRIT=4.25E4 UEXP=0.06)
DE REALISATIE VAN EEN MULTIFUNCTIONELE I/O-CONTROLLER MET BEHULP VAN EEN GATE-ARRAY.


A COURSE ON FIELD PROGRAMMABLE LOGIC.


MILLIMETER-WAVE ANTENNA MEASUREMENTS WITH THE HP8510 NETWORK ANALYZER.


SHORT-CIRCUIT CURRENT INTERRUPTION IN A LOW-VOLTAGE FUSE WITH ABLATING WALLS.


DEVIATION FROM LOCAL THERMODYNAMIC EQUILIBRIUM IN A CESIUM-SEEDED ARGON PLASMA.


SOME ASYMPTOTIC PROPERTIES OF MULTIVARIABLE MODELS IDENTIFIED BY EQUATION ERROR TECHNIQUES.


THE INFLUENCE OF A HIGH-INDEX MICRO-LENS IN A LASER-TAPER COUPLING.


A THEORETICAL STUDY OF THE ELECTROMAGNETIC FIELD IN A LIMB, EXCITED BY ARTIFICIAL SOURCES.


A PROGRAM FOR OPTIMAL STATE ASSIGNMENT.


DEVELOPMENT OF TRANSMISSION FACILITIES FOR ELECTRONIC MEDIA IN THE NETHERLANDS.


HARMONIC AND RECTANGULAR PULSE REPRODUCTION THROUGH CURRENT TRANSFORMERS.


PARTIAL DISCHARGES AND THE ELECTRICAL AGING OF XLPE CABLE INSULATION.


DIRECT LAYOUTS FOR RANDOM LOGIC: Cell generation schemes.


HIGHER LEVELS OF A SILICON COMPILER.


GAAL: A Gate Array Description Language.


GAAL: A Gate Array Description Language.


AN OPTIMAL CMOS STRUCTURE FOR THE DESIGN OF A CELL LIBRARY.


ESKISS: A program for optimal state assignment.