MASTER

Design of a dimmable 2-lamp ballast based on the unequal LC-principle

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DESIGN OF A DIMMABLE
2-LAMP BALLAST
BASED ON THE
UNEQUAL LC-PRINCIPLE

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De Faculteit der Elektrotechniek van de Technische Universiteit Eindhoven aanvaardt geen
verantwoordelijkheid voor de inhoud van stage- en afstudeerverslagen.
SUMMARY

This report describes the efforts to develop an electronic ballast for fluorescent lamps. This ballast must be suitable for 2 TLD 58 W lamps and must regulate the light level between 1% of nominal power and full power. The ballast will make use of a special arrangement called ‘unequal LC topology’. This type of ballast will not use a current balancing transformer, but will actively regulate the power balance of the two lamps.

The ballast consists of a half bridge converter, followed by a resonant circuit for each lamp. The power balancing is done using frequency modulation. The total power setting is done via pulse width modulation of the half bridge converter. The power-frequency and power-duty-cycle characteristics have been analyzed to determine the values for the resonance frequencies. The best choice has appeared to be equal resonance frequencies, and any difference caused by component tolerances or lamp-characteristics can be compensated for. The allowed tolerance in the resonance circuit components is 5%.

The ballast is controlled by a microcontroller. This microcontroller measures the lamp voltage and the lamp current for both lamps, and uses a fuzzy-logic technique to regulate the power balance and the total power level. Accurate measurement circuits are developed for the lamp current to be able to detect a power unbalance even at low light levels. Unfortunately the power measurement is not insensitive for parasitic capacitances. Extensive research is done on phase angle detection, but it has been found that the position of the zero-crossings of current and voltage cannot be used to correct the lamp power. Lamp power is calculated by multiplying the average voltage and current value. Parasitic currents will lead to a higher power representation than the real lamp power. Because of the PWM-control and the difference in resonance frequencies, a differential current will flow from one branch to the other.

The ballast is able to operate with only one lamp connected or with a defect lamp. The open voltage across the defect lamp is kept lower than 230 V. A lamp exchange will result in a re-ignition procedure. The electrode heating is still a separate circuit.

The losses in the power circuit can be estimated at 5 Watt at full power and consist of conduction losses (40%), switching losses (20%) and snubber losses (40%). Other losses can be found in: resonance inductor, gate-source capacitance and power supply for the total circuit. The losses at 1% dimming level are not considerable lower because the inductor current will remain almost the same. The snubbers are necessary because the converter is duty-cycle controlled.

The control program is optimized for a minimum ignition light-flash. It uses fuzzy-logic techniques to adjust the duty-cycle and the operating frequency.
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1. Introduction.

Fluorescent lamps are commonly used because of their advantages over incandescent lamps. Some of these advantages are: high efficiency, high luminous output, less heat production and long lifetime. To operate the discharge lamp, a special circuit called a ballast is required. This ballast combined with the igniter, must be able to create the high ignition voltage and the ballast must adapt the power source (mains) to the lamp characteristic.

Since the invention of the fluorescent discharge tube, a large inductor is used as lamp ballast when operated from the mains. These inductors are very large and heavy, because they are designed to operate at the mains frequency of 50 or 60 Hz. They have also a considerable series-resistance which causes dissipation.

The use of an electronic ballast has several advantages over the conventional copper-iron ballast.

- It can be made lightweight and more effective
- It operates the lamp at a high frequency, and it appears that the fluorescent lamps at high frequency produce about 10% more light at the same lamp power.
- It can perform flicker free ignition and proper preheating of the electrodes to extend the lifetime of the lamp.
- It is able to regulate the light output.

Nowadays however the electronic ballasts are still much more expensive than the conventional ballasts. A way to overcome this problem is to connect two or more lamps to one ballast to reduce overall costs. This will require a ballast with special arrangements.

A problem in operating more than one lamp is to limit or control the light unbalance in the lamps. The unbalance can be caused by differences in characteristics of the lamps (lifetime, temperature) or by differences in wiring (cable length, parasitic capacitances). The light unbalance usually becomes greater when the light level of the lamps is decreased, because the operating frequency of the ballast will increase to dim the lamps. At these high frequencies the effect of the capacitances is also higher.

At present this problem is more or less solved by a balancing transformer to ensure the same current will flow through the lamps. But this does not solve the problem caused by the parasitic capacitances, and is not able to drive only one lamp.

In this project we aim at using a special electronic ballast arrangement called the 'unequal LC' topology. This type of ballast has also only one lamp power converter, but has two control parameters. The total lamp power will not be controlled by the operating frequency, but by varying the duty-cycle for the switching elements. The operating frequency will be used to balance the two
lamp powers. This frequency variation is very small compared to a conventional
dimming electronic ballast.
The two branches will have the maximum power at different frequencies.
Between those frequencies will be a point where the two lamps have the same
power. The ballast must find this point and set its control parameters to the
correct values. In the figure below this principle is visualized.

![Figure 1 Lamp power for Unequal LC topology.](image)

We want to focus first on digital techniques to realize the control quickly.
The starting points for this project are the current prototypes of the Digital
Ballast and the Satarius gear. These are single lamp ballasts that use duty-cycle
variation to control the lamp power. These ballast use a microcontroller to
control the ballast. The prototype must be modified in both hardware and
software.

The resulting circuit must have the following characteristics:

- The circuit must be suitable for at least the TLD 58 W lamp
- Dimlevel range from 1..100%.
- Light flux unbalance less than 20% at any lightlevel.
- Measurement circuit for low lamp currents, insensitive for wiring
capacitances.
- Single lamp operation must be possible, while avoiding a high voltage
  across the defect lamp.
- The ignition procedure must be optimized to reduce the ignition lightflash.
- Pulse Width Modulation for total lamp power control.
- Frequency variation for current balancing.

A tolerance investigation has to be done for the critical components:

- Inductor and Capacitor for the resonant circuit.
- Component values for the measurement circuits.
First the unequal LC principle has to be analyzed further to determine the required spacing between the two resonance frequencies. Simulations can be done to predict the lamp power for several combinations of duty-cycle and operating frequency.

To adapt the prototypes’ hardware for two lamp operation with the unequal LC topology several circuits must be designed or re-designed:

- The circuit must be able to deliver twice the amount of lamp power compared to single lamp operation.
- An accurate operating frequency generator must be designed.
- The measurement circuits for the lamp current must be re-designed, to be able to get an accurate representation for the difference in lamp power. Preferably these circuits must be able to compensate for currents through parasitic capacitances.

The software must regulate the control parameters until the desired total power level is reached and the power balance is within the limits. It must also be able to detect defect lamps, switch over to single lamp operation if necessary and perform a re-ignition after a lamp change.

The report will start with the analysis of the performance of a duty-cycle controlled half bridge converter to be able to set the boundary conditions for the unequal LC-topology. Then the hardware and the software adaptations will be discussed. Finally the tolerance investigations and the conclusions will be presented.
2. Analysis of the Unequal LC-topology.

2.1 Introduction.

In this project we try to develop a dimmable electronic ballast for TL lamps. This ballast must be designed for two TLD 58 Watt lamps. Electronic ballasts for fluorescent lamps usually have this topology:

- AC-DC converter, to convert to mains voltage to a DC voltage.
  310 Volt DC for a bridge rectifier or 380 to 400 Volt for an electronic up-converter to ensure a sinusoidal mains current and a constant DC levels with small ripple voltage.

- Half-Bridge converter to regulate the current through the lamp.

We will not examine the AC to DC converter, but only the half-bridge converter. This type of converter in lamp circuits is usually regulated by controlling the half-bridge frequency. The lamp is connected to the half-bridge converter via a resonant circuit consisting of an inductor and a capacitor. In figure 2 this topology is shown.

![Figure 2 Universal half-bridge converter for TL-lamps](image)

The capacitor with reference Cdc will be very large compared to the resonance capacitor C. Across this capacitor a DC voltage will occur of approximately half the supply voltage of the half-bridge converter. This ensures an AC current flowing through the lamp.

To be able to compare different results, we will assume that the light level of a fluorescent lamp is proportional to the electrical power that is dissipated.

The lamp power can be regulated by several modulation methods: Frequency Modulation (FM), Supply Voltage Modulation (SVM) or Pulse Width Modulation (PWM). Usually adjusting the half bridge switching frequency (FM) is used. Because normally the resonance frequency of the LC combination is chosen below the operating frequency, the lamp power will decrease when the operating frequency is increased.

To reduce the costs for lighting installations often two lamps are connected to one ballast. The lamps can be connected in series or parallel. This scheme works well when the two lamps are operated at full power, but when the lamp power
is reduced by increasing the frequency it is very susceptible to differences in lamp power. These differences are caused by inequalities in lamp characteristics (lamp voltage at a certain power level), of which the effects are greater when the lamp current decreases. The differences in lamp power are also caused by the different wiring capacitances, of which the effects become greater when the operating frequency is increased.

When the two lamps are connected via a current balancing transformer, it will largely block differential mode current, so the current through the two lamps must be equal. Also the open voltage for the two lamps will be equal, which will help to ignite both lamps simultaneously. This is shown in figure 3.

![Figure 3 Two lamp half-bridge converter with balancing transformer](image)

This balancing transformer is a rather large and an expensive part in the ballast, so we want to find a way to ensure the current balancing without using this transformer. The main idea for this new type of ballast is using frequency control for the current balancing. This may be possible by using LC combinations for each lamp with different resonance frequencies. The basic topology for this type of ballast is shown in figure 4.

![Figure 4 Unequal LC topology half bridge converter](image)

For the total power control two options are available: Controlling the DC supply voltage of the half bridge or controlling the duty-cycle of the converter. For this project duty-cycle control is chosen.
2.2 Experimental board.

The 2-lamp gear will be operated with only one half-bridge converter, driving two branches consisting of an inductor and a capacitor. For the total lamp power regulation, duty-cycle control will be applied. By choosing different resonance frequencies for the two branches, the operation frequency of the half-bridge gives the possibility to control the power difference in the two branches. In this way it must be possible to set the light level of the two lamps at a fixed difference, but we are most interested in equal power in the two branches.

An experimental board was available to get started. It was equipped for driving two PL-L 36 Watt lamps. The board consists of a half-bridge converter as explained above, and a control circuit to adjust the half-bridge frequency and the ratio of the conducting times of the two FETs (=duty cycle).

The duty cycle is defined as $t_1/T$ or $(t_2 - \frac{1}{2}T)/T$. The duty cycle is the relative ‘on’ time of a FET compared to the full oscillator period. It must lie between 0 and 0.5 (0% to 50%). These parameters can be seen in figure 5.

![Figure 5: Fet gate-source voltage for duty cycle control](image)

With the aid of this board, some qualitative experiments have been carried out, to get an idea of the control parameters.

Some conclusions from these tests are:

- At high power levels, the operating frequency has little effect on the power difference.
- At low power levels, the operating frequency has great effect on the power difference; one of the lamps can stop burning.
- The frequency at which the power levels in the two branches are equal, is not constant throughout the dimming range.

2.3 Simulations.

To get a good understanding of the principle of the unequal LC topology, simulations have been made for different LC-combinations. In the analysis we assume that the two branches do not interact.
The program AHBO [1] can find LC-combinations suitable to drive a lamp as load. Input parameters are:

- The lamp model.
- The desired power at a certain frequency.
- The search range for the inductor and capacitor.

The lamp model has to be characterized by three points in the Voltage - Power plane, or by three other parameters:

- $A_1$ = the slope of the voltage-power characteristic (V/W).
- $A_0$ = the intersection with the voltage axis of the linear approximation (V).
- $R_{lim}$ = the limiting resistance parallel to the lamp.

These parameters are explained in figure 6.

![Figure 6 Explanation of lamp model parameters](image)

The lamp model for the TLD 58W Kr has been taken for $T_{ambient} = 25 \degree C$ [2].

$(A_0 = 184.0 \, V \quad A_1 = -1.575 \, V/W \quad R_{lim} = 125.3 \, k\Omega)$

We want to get some LC-combinations which give 50 Watt power at a frequency of 28 kHz. The supply voltage is 320 V and the capacitor range is from 10 nF to 22 nF. AHBO gives the following results:
We have taken nr. 3, 6 and 9 to evaluate with the program NHBO [3]. This choice is only based on the resonance frequencies of these LC-combinations. The power efficiency is not taken into account. The larger the capacitor is chosen, the larger the reactive current that flows through the inductor, the capacitor and the switching elements. Any resistive part in this current path will lead to dissipation. It is advisable to choose a capacitor between 12 nF and 18 nF.

In the NHBO program a half-bridge circuit can be simulated with a TL lamp as load. This program computes lamp power, lamp currents and lamp voltages (as well as some other results) for a known LC-combination. The program iterates until a stable situation is found. The program starts with a initial lampresistance, calculates the lamp power delivered by the circuits, adapts the lampresistance and so on.

We can find the dimming characteristics for the specified LC-combinations by varying the working frequency of the half-bridge while keeping the duty cycle constant. In this way a frequency-power plot can be made for the whole dimming region from 100% to 1% of the nominal power. The results of these simulations are in Appendix 1.

2.4 Interpretations.

If we look at the various plots some properties become apparent:

- The maximum power is delivered at a frequency which is lower than the resonance frequency of the circuit.
- When the duty-cycle is decreased the frequency at which the maximum power is delivered will increase first and then decrease.
To explain these properties we have to look at the figure in appendix 2c. The plot shows the lamppowers if the duty-cycle is kept at 50% (maximum power transfer) and the supply voltage of the half-bridge converter is decreased. We see now that the frequency at which the maximum power is delivered remains constant throughout the dimming region.

The explanation is found in the harmonic contents of the half-bridge voltage. For supply voltage control this harmonic distribution remains constant, but when using duty-cycle control, the fundamental harmonic of the half-bridge voltage will strongly increase when decreasing the operating frequency. When the amplitude of the fundamental is multiplied with the band-pass characteristic of the resonant circuit, the resulting characteristic will have a maximum power transfer at a lower frequency than would be expected from the resonant circuit. The resonant circuit will be loaded with the lamp-impedance and in an article of Kazimierczuk [4] we find that even for sinusoidal signals the maximum power transfer to a load parallel to the capacitor will occur at a frequency lower than

\[ f_c = \frac{1}{2\pi \sqrt{LC}} \]

This difference is caused by the relatively poor quality factor \(Q\) of the resonant circuit with load.

If we combine two of the three plots as in figure 7, we can find the points in the frequency-power plane at which the two branches deliver the same power. The intersection of two characteristics with the same duty-cycle gives the required operating frequency. The control circuit must adjust the duty-cycle and the frequency until the desired power level is reached and the lamp powers are equal.

The angle at which the two characteristics do intersect gives a measure for the accuracy at which the operating frequency must be set. A steep angle will give a relatively large unbalance for a small frequency deviation. If the desired power level is decreased, the angle of intersection will increase.

There are some considerations for choosing the resonance frequencies for the LC-combinations:

- Tolerances in \(L\) and \(C\) are inevitable, and with these tolerances the resonance frequencies must be distinguishable in order to get unequal \(L\)\(C\). So the resonance frequencies have to be chosen far enough from each other.
- In order to maintain a stable operation at low dimlevels, the resonance frequencies must not lie too far apart, because there could be a ‘gap’ between them. If this happens only one lamp can be driven correctly.
- At low dimlevels the frequency-power plots have a very steep slope. At the setpoint for equal power a slight frequency variation will cause a high unbalance in power. This effect becomes less when the resonance frequencies are chosen near to each other.
- For single lamp operation it is necessary to set the frequency at such level, that the open voltage in the branch with the defect lamp will be as
Tests have been carried out with LC-combinations 3 and 9 (26 kHz and 35 kHz) on the experimental board.

As expected from the simulations, at high dimlevels the operation frequency does not have much effect on the power difference, the power difference is mainly caused by the difference in burning voltage of the lamps.

At moderate dimlevels (40% - 10 %) the power difference becomes more and more dependent on the operation frequency, it seems to be necessary to have a frequency accuracy of about 10 Hz.

At low dimlevels (< 8%) the power balancing control is very critical, when the operation frequency varies too abruptly one of the lamps will extinguish.
If we sum all the tolerances and parasitic effects, it might be possible that the resonance frequencies of the two branches will become equal. This would be a boundary condition for the circuit to be developed. To examine the performance of this condition, two equal LC-combinations have been ‘matched’ and tested on the experimental board.

The qualitative results are:

- There is still an optimal frequency, which gives no unbalance in power!
- When this frequency is determined at low dimlevels, then no further frequency adjustment is necessary.
- At high power levels, the power unbalance cannot be controlled via the operation frequency. The unbalance is caused by different burning voltages.
- The power unbalance depends only slightly on the operation frequency. The difference in resonance frequency is caused by parasitic capacitances (wiring). The higher the parasitic capacitance, the lower the resonance frequency.

With these results a new way can be turned into. If we try to keep the resonance frequencies equal then two options are possible:

1. The resonance frequencies are indeed the same. Now the operation frequency cannot influence the power balance. The possible unbalance is caused by the different burning voltages of the lamps. Simulations with AHBO have proved that the power unbalance will always be within 6% over an A0 range from 181 V to 190 V.

2. The resonance frequencies are unequal. The (digital) control circuit will be able to identify the branch with the highest resonance frequency and the branch with the lowest resonance frequency. By varying the operation frequency it is possible to adjust the power unbalance. The resonance frequencies will not be more apart than the allowed tolerances in L an C and additional parasitic capacitances.

Using equal LC-combinations has some more advantages:

- Equal L and C means that there can be made no mistake in placement of the components.
- The inductor currents will be the same in both branches so it offers the possibility to use the capacitor as electrode-heating capacitor. Both lamps will have the same electrode current, which will not be possible with unequal LC-combinations.

These arguments have led to the decision to choose the equal LC-combinations. It offers a good option for driving two lamps at the same power level. The control circuit will take advantage of the normally parasitic effects. The topology
may still be called Unequal LC-topology, because the (frequency) control action can only take place when the resonance frequencies are unequal.

2.5 Behaviour of the half bridge converter when driving two LC-combinations.

In the analysis we assumed that the two branches do not interact. This is true when the two LC-combinations are exactly equal. If however the energy storage in the LC-combinations differ and the duty-cycle is less than 50% there will be interaction. This interaction can be explained if we divide one HF period into different states. In figure 8 are the half-bridge voltage, the two inductor currents (current towards the lamp is positive), and the gate-source voltage of the upper Fet plotted. In this case the LC combination associated with I₁ (dotted line) has the lowest resonance frequency.
Figure 8 Inductor currents during one switching period

Figure 9 Current through the two branches and switching elements
In the following explanation left and right refers to the left and right branch in figure 9. The left branch can be identified with \( l_1 \) in figure 8.

1: The upper FET is turned on, but the current through the left inductor is still negative and thus supplying current to the right inductor. This current decreases rapidly and become zero.

2: Both inductors are supplied through the upper FET until it is switched off.

3: The current is immediately taken over by the lower diode. The current in the right branch decreases more quickly because due to the higher resonance frequency the lamp voltage in this branch will have a leading phase with respect to the other branch.

4: The current in the right branch becomes negative and thus flows into the left inductor.

5: The lower diode current has become zero, and the upper diode is conducting now. A very small current flows through this diode, most current is exchanged between the two branches.

6: The lower FET is turned on and in this state, the current flowing out off the right branch flows into the left inductor and the FET.

7: Both inductor currents are negative and are sunk by the lower FET.

8: The lower FET is turned off and the current is taken over by the upper diode.

9: The right inductor current has become positive and drains current from the left inductor.

10: The total current has become positive and the upper diode is conducting. Again only a small current is flowing through the diode.

Another way to visualize the interaction between the two branches is looking at the sum and difference of the two currents. The sum of the currents represents the current supplied by the half-bridge converter. The difference of the currents can be regarded at as twice the current which is flowing from one branch to the other. In figure 10 these sum and difference signals are plotted. The sum signal looks very alike the normal half-bridge current for single LC operation. The difference signal however is a sinusoidal current which is constantly flowing from one branch to the other.

The actual inductor current is formed by:

\[
\begin{align*}
I_1 &= \frac{1}{2}(I_1 + I_2) + \frac{1}{2}(I_1 - I_2) \\
I_2 &= \frac{1}{2}(I_1 + I_2) - \frac{1}{2}(I_1 - I_2)
\end{align*}
\]

Experiments have shown the dependency of the differential current:

The amplitude is dependent on the difference in resonance frequencies, the larger the frequency difference, the higher the amplitude. This can be made obvious by looking at state 3, 4 and 8, 9 where the current difference increases due to difference in resonance frequencies (or energy storage). The resonance frequency of the two branches is determined by the inductor and the capacitor value and also by all the parasitic capacitances.
The half-bridge frequency influences the amplitude and the phase angle of the difference signal. The maximum amplitude is reached approximately half-way the two resonance frequencies. In first order approximation the amplitude is inversely proportional to the norm of the difference of the operating frequency to the two resonance frequencies, and is proportional to the difference of the resonance frequencies.

The amplitude and phase are also determined by the duty-cycle. The amplitude decreases with increasing duty-cycle because the effect of different capacitor values is damped by the lamp impedance. Of course the phase of the differential current is dependent on which branch has the highest resonance frequency.

2.6 Conclusions.

With analyzing and simulating the unequal LC topology we have found that the best way to ensure equal power in the two lamps, is choosing the LC combinations equal. The differences are then only caused by tolerances and parasitic effects.

The control circuit will have to set the operating frequency with an accuracy of about 10 Hz for LC combinations with the resonance frequencies 10% from each other. Duty cycle control of the converter will be used to set the total
power level. The exact determination of the setting point will be controlled in the software.
In the analysis we assumed no interaction between the two branches, but due to the duty cycle control there will be exchange of energy between the two branches. This will probably even out partly the differences between the two branches.
3. Hardware.

3.1 Introduction.

The prototype of the digital ballast controls the lamp power with a duty cycle controlled half bridge converter. This converter is regulated with a microcontroller. The operating frequency is fixed at 27.7 kHz. The measurement circuits for lamp voltage and lamp current can calculate lamp power with a 0.25 Watt accuracy. For the heating of the electrodes an extra converter is used, which can be controlled to give the correct extra electrode current when dimming the lamp.

For the unequal LC topology this prototype must be modified. The operating frequency has to be adjustable between 24 kHz and 32 kHz with a 10 Hz accuracy.

The electrode heating must be reviewed to be able to heat the electrodes for two lamps. One option is using the resonance capacitor current, another is using a separate circuit to be able to regulate the extra current.

The measurement circuit will be extended for two lamp measurements, and has to be accurate to determine the difference between the lamp currents at low power levels. Preferably these are insensitive to wiring capacitances, which means the circuits will have to measure only the lamp current and not the capacitive currents.

Lamp detection is necessary to detect exchange of lamps after lamp failure. Finally the pulse width modulator has to be examined. This circuit is designed for fixed frequency operation only. If the operating frequency is changed while the duty cycle control signal is kept the same, the duty cycle of the converter will change. This effect will be examined and compared to real duty cycle control.

The individual circuit adaptations have been carried out, and except from the phase sensitive power measurement, they worked as expected. Voltage and current must be multiplied without phase angle information, because the detected phase angle information has no relation with cos φ.

The losses created in the power circuit are identified and the total losses in the power circuit are estimated at 5 Watt. These losses involve conduction and switching losses in the FETs and snubber losses. Inductor losses and gate-charging losses are not calculated.

3.2 Voltage Controlled Oscillator.

The unequal LC-topology is based on a duty-cycle controlled half-bridge converter with an adjustable operating frequency. In the original design of the digital ballast the operating frequency can only be chosen in steps of 600 Hz. This resolution is insufficient for regulating the light balance. As stated in chapter 2.2 a frequency accuracy of about 10 Hz. will be needed. A circuit that
can control the operating frequency is built with a voltage controlled oscillator (VCO). This VCO is controlled by the microcontroller.

A study for various VCO’s gives the VCO part of a HEF4046 as best option. This IC is a PLL circuit, consisting of a VCO, phase comparators and control logic. Only the VCO is used. The lower and upper boundary frequency can be set, and the frequency can be controlled between these boundaries with a DC input signal from 1.2 V to Vcc (= 5 V). The DC input signal is constructed with a periodic signal from Timer2. This signal has a varying duty cycle from 0% to 100% in 1024 steps. This signal is first averaged to an analog DC signal with an amplitude of 0..5V. The time constant of 10 ms is chosen well above the cycle time of the input signal, which is 768 \mu s.
For exact details on the Timer2 signal see the section about the software in chapter 4.3.4.

With R1, R2 and C1 the lower and the upper frequency are set from 24 kHz to 32 kHz. This frequency range can be controlled in about 800 steps, which gives a resolution of about 10 Hz.
Care should be taken with using this VCO for further developments, it has high tolerances in frequency output between individual parts. A qualitative test with some different IC’s showed a difference in output frequency of +/- 750 Hz. The output frequency has also a temperature dependency, a temperature rise of 50 degrees can increase the frequency with 700 Hz.
This however does not affect the control strategy, because an absolute value for the operating frequency is not necessary. Only the minimum and maximum frequency can shift due to the tolerances.

![Schematic Voltage Controlled Oscillator](image)

**Figure 11** Schematic Voltage Controlled Oscillator

The DC input signal for the VCO will contain a small ripple voltage due to the filtering with the first order low pass filter (R3/C2). This ripple will cause a frequency modulation at the output. The modulation frequency is 1302 Hz.
3.3 Electrode heating.

Under certain circumstances it is possible to use the current flowing through the inductor and capacitor to heat the electrodes. To ensure a good emission of electrons the electrodes must have the correct temperature. If the electrodes are too cold, electrons are not easily emitted, which gives poor luminous output and may damage the emitter material, if the electrodes are too hot, the emitter material will vaporize which will shorten the lamp life-time. The electrons are heated by the current through the electrodes. This current must lie between strict limits, so if the lamp current decreases an extra current must flow through the electrodes.

In the design process we have used several different LC-combinations. These combinations are calculated with AHBO and are dependent on: resonance frequency, nominal power and supply voltage. Not all combinations are able of delivering the correct electrode current. The final LC combination would be able to heat the electrodes, but in choosing this option, one must keep in mind that the current sensing transformer would require two primary windings to separate the lamp current from the electrode current. Also the lamp detection would be somewhat more complicated. For these reasons a separate electrode heating is chosen. This ensures that the regulating process cannot be disturbed by cold electrodes. This choice is made because the type of electrode heating does not affect the results for the unequal LC-topology.

![Figure 12 Separate electrode heating and heating with resonance capacitor](image)

3.4 Measurement circuits.

To be able to control the half-bridge converter it is necessary to obtain a representation for the electrical power in each lamp. Several methods can be used, e.g. a real-time multiplier for lamp voltage and lamp current, but the costs for the measurement circuits must not be too high. When no parasitic effects are taken into account, a multiplication of average current and average voltage gives a good representation.
3.4.1 Current sensor.

The current sensor must give an output voltage that is suitable for the AD-converter. The input range for the converter is 0..5 V. The mean lamp current at full power is about 0.5 A. A direct conversion from current to voltage using a resistor would require a resistor of 10 Ohm. Such a resistor would dissipate 2.5 Watt. This is of course unacceptable.

A way to limit the dissipation is to use a very small resistor, e.g. 0.5 Ohm and amplify the signal across the resistor 20 times. This will work well at high lamp current, but at a lamp current of 5 mA only 2.5 mV will be present across the resistor. This would require an OpAmp with a very low input offset voltage.

Another way to measure accurately and limit the dissipation in the sensing resistor is using a transformer.

![Figure 13 Current sensor with transformer](image)

The current transformer has a transfer ratio of 1:20. This implies that the secondary current will be a factor of 20 less than the primary current. To obtain the same voltage output, the resistor must now be 200 Ohm. The power dissipation is reduced to 125 mW. The secondary current is rectified in stead of the output voltage, because in this way the voltage drop across the diodes has no influence.

This sensor is a good option for single lamp operation, but with the unequal LC-topology the difference in lamp current must be measured accurately, especially at low dim levels. At 1% dim level the lamp current is about 5 mA and with a 10 bit AD-converter, the output value of the converter will be 10 (1% of full scale). The sampling error at this level can be as large as 10 % of the measured value, so little can be said with regard to the difference in lamp current.

A good solution is the circuit in figure 14. The current is now fed through two resistors, and the output voltage is connected to two ADC inputs. The output voltage of the high output is limited by the 2 V stabistor. At low current the high output is used to measure the lamp current. As the current increases, the voltage across the zener diode increases and at a certain
current, a non-negligible current will flow through the zener diode. This will cause an error in the high output. When the lamp current increases above this point, only the low output can be used. Measurements show the distortion of the high output. In figure 15 the measured output voltages on the high and the low output are shown. At 1.7 V across the zener diode the high output starts to deteriorate and the differential voltage between the high and the low output settles at 2 V. When the voltage at the high output rises above 5 V then the diode to the 5 V supply will start to conduct to prevent excessive dissipation in the internal clamping diode in the microcontroller.

To determine the exact current at which to switch from using the high output to using the low output and vice versa, some calculations have been made with MATLAB. The high voltage has to be 8 times the low voltage, because the total resistor value for the high output is 8 times the low resistor value. At 28 mA the error for the high output is about 2.5% of the expected value. At 25 mA the AD converter value for the low output is 40. This means a quantisation error of 1.25% can be expected. Switching over at this point (converter value 40 for the low output) results in an almost continuous sensing with little distortion from 4 mA to 500 mA. The current sensing circuit behaves as a converter with 13 bit accuracy at current below 25 mA and 10 bit resolution at current up to 500 mA.

Averaging is done with a simple first order RC-filter with a time-constant of 220 μs. This is about 12 times the period time of the signal at the resistor (the rectifier doubles the frequency).

Using a transformer for the current sensing means that the DC-component of the current will be filtered out, so it is not possible to measure the DC power. Since we want to multiply the average value for current and voltage as a power representation, only the AC components must be averaged and multiplied. So the disadvantage of having no DC component can turn into an advantage.

Some design considerations for the transformer:

The secondary inductance must not be too low. At 27 kHz the impedance must be high compared to the sensing resistors.
Figure 15 Characteristics for the two stage current sensor

The transformer used in the circuit has a secondary inductance of 58 mH, which gives the following current distribution:

\[ I = I_1 + I_2 \]
\[ U = ZI = j\omega LI_1 + RI_2 \]
\[ I_1 = (\frac{-R}{j\omega L} + 1) I_2 \]
\[ I_2 = \frac{j\omega L}{R + j\omega L} I \]
\[ |I_2| = \frac{\sqrt{\omega^2 L^2}}{\sqrt{R^2 + \omega^2 L^2}} |I| \]

Figure 16 Current distribution transformer
With \( L = 58 \text{ mH} \) and \( R = 1260 \Omega \):

- @24 kHz. \( I_2 = 0.990 \text{ l} \)
- @27 kHz. \( I_2 = 0.992 \text{ l} \)
- @30 kHz. \( I_2 = 0.993 \text{ l} \)

This shows that the secondary inductance has little influence on the current through the resistor, and the frequency dependence is negligible.

A lamp current of 1 mA (RMS AC) makes a secondary current of 0.05 mA, this gives 8 mV (RMS) across the 160 \( \Omega \) resistor. The averaging circuit reduces this value for sinusoidal signals to:

\[
8 \text{ mV} \times 1.414 \times 2/\pi = 7.20 \text{ mV/mA}
\]

Experiments show an output voltage of 7.38 mV/mA, which is about 2.5% higher than expected. This is caused by tolerances in resistor values and because the waveform is not exactly sinusoidal. The accuracy of the measurement equipment can also influence the result.

The DC resistance of the primary winding is about 80 m\( \Omega \), this gives a maximum dissipation of 20 mW.

The DC resistance of the secondary winding is 5.5 \( \Omega \), this gives a maximum dissipation of 3 mW.

The magnetising current due to the secondary inductance is:

\[
i = \frac{U_{\text{sec}}}{J \omega L_{\text{sec}}} = \frac{6.5}{8746} \approx 0.745 \mu\text{A}
\]

Using these parameters in CONV, a computer program to calculate magnetic components for power converters, it becomes clear that the core- and HF-losses are zero.

\( B_{\text{max}} = 20 \text{ mT} \), so this forms no problem.

3.4.2 Voltage sensor.

The voltage sensor must also block any DC component to keep the multiplication of current and voltage usable.

The first order high-pass filter formed by the capacitor and the total resistance has a time constant \( \tau = R_1 \times C_1 = 150 \times 10^3 \times 470 \times 10^{-12} = 70.5 \mu\text{s} \) \( (F_c = 2.26 \text{ kHz}) \). This ensures a high DC rejection. 100 Hz frequencies are attenuated 27 dB \( (\approx 0.044) \). The remaining AC signal is divided by the resistive divider. Only the positive half-wave is passed through the diode, because under normal conditions
Figure 17 Measurement circuit lamp voltage

The lamp voltage is symmetrical and full wave rectifying would require more components. A first order low-pass filter takes the average of this rectified signal. Its time constant is 1 ms, ensuring a high ripple rejection. The dividing ratio for the voltage sensor is:

$$\frac{R_2}{R_1+R_2+\frac{1}{j\omega C_1}} \approx 0.0163$$

A lamp voltage of 100 V (RMS AC) gives a peak value across the 2k5 resistor of 1.63 V * 1.414 = 2.30 V. The averaging circuit (first order low-pass) converts this to a DC value of: 2.30 * 2/2π = 0.734 V/100V.

In experiments a conversion factor of 0.845 is found. The difference is caused by some reasons:

- during the negative half wave the voltage at R₂ is 200 mV in stead of 0 V. This voltage originates from C₃ divided by R₂ and R₁. If the voltage at the anode of D₁ drops below this value, the diode stops conducting. The extra voltage created during the second half wave is $\frac{2k5}{2k5+10k} \cdot 0.5 \cdot V_3 = 0.1 \cdot V_3$. This means the conversion factor will be increased 10%.
- The waveform is not exactly sinusoidal, but contains higher harmonics. The mean value will become closer to the RMS value, and thus the conversion factor will also increase.

We have found conversion factors for current and voltage that are independent of the operating frequency, but are dependent on the waveform. This forms a (little) problem for the absolute value of the lamp power, but for balancing the two lamps this forms not a problem, because the waveform, the voltage and the current will be almost equal, so the difference in error is negligible.
3.4.3 Phase-angle detection.

The method to measure the power described above, takes no parasitic effects into account. Such an effect is the wiring capacitance. These capacitances can cause a phase-shift between lamp current and lamp voltage. If we only measure the absolute values, the result from these measurements will be too high. One way to overcome this problem is a measurement circuit for the phase angle. The power will be represented by \( \text{av}(U) \times \text{av}(I) \times \cos \phi \).

The phase angle is represented by the time-difference of the zero-crossing of current and voltage. To be able to measure this time-difference accurately, this signal must be measured with an AD converter, so the time difference signal must be converted to a DC value. With the circuit in figure 18 it is possible to determine whether or not the current and voltage have the same polarity. This digital signal has a varying duty-cycle, 0% for complete in phase, 50% for 90 degrees phase angle and 100% for 180 degrees phase angle. With a first order low pass filter this signal can be averaged and fed to the AD converter.

![Figure 18 Phase angle detection](image)

In the upper half of the schematic, the lamp voltage is compared with the zero-level. The voltage is AC-coupled, because the opamps have only a single supply voltage. The lamp voltage is divided by 48 and superimposed on a DC voltage of 6 V. The impedance of the capacitor is about 86 \( \Omega \) at 27 kHz, so this effect can be neglected. This voltage is compared to 6 V, and if the lamp voltage is positive, the output of the opamp will be +12 V, else 0 V.

The lower half of the circuit evaluates the lamp current. The output voltage of the transformer will reflect the current direction. If the voltage is positive, the current is positive and vice versa. The secondary side of the transformer in not directly connected to ground, so both ends must be AC coupled to the opamp. The resistors to set the DC offset, must be high-ohmic to prevent too much
current flowing through these resistors instead of the current sensing resistors. 1 MΩ is high enough compared to the current sensing resistors. Again, the output of the opamp is +12 V if the current is positive.

The two signals are fed to an EXCLUSIVE-OR gate, this device has the following truth table:

<table>
<thead>
<tr>
<th>Voltage</th>
<th>Current</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

If the voltage and the current have the same polarity, then the output is '0' else the output is '1'. This output limited to 5 V and averaged with a first order low pass filter with a time constant $t$ of 220 $\mu$s.

The exact characteristic for the $\cos \phi$ is measured and calculated into 8 bit values. These values are implemented in software in a table.
3.5 Parasitic capacitances and phase angle detection.

The phase angle detection circuit must be able to measure the effects of parasitic capacitances between the connection wires of the two lamps. If this is not the case, the measurement circuit will still measure lamp power even when the lamp is off. Several capacitances can be identified. In figure 19 the capacitances across the electrodes are omitted because their impedance will be high compared to the electrode impedance.

![Figure 19 Parasitic capacitances in two lamp ballast](image)

All the parasitic capacitances will alter the resonance frequency of one or both branches. This results in a change in the differential current.

The capacitances $C_{1,++}, C_{1,+-,gnd}$ and $C_{2,+-,gnd}$ will not cause an error in the current sensor because the current through these capacitances will not be measured by the current sensor.

The other capacitances will influence the current sensor, because the current transformer adds the capacitor current to the lamp current. For the capacitances $C_{1,++}$ and $C_{2,+-}$, this extra current will be a fraction of the inductor current. $C_{1,+-}$ and $C_{2,++}$ give an extra current which is a fraction of the inductor current in the other branch.
The magnitude of the capacitor currents is proportional to the ratio of the lamp capacitor \( C_1 \) and the parasitic capacitor. Only at low dim levels these small currents become important. They will alter the zero-crossings of the current, but this will not necessarily be a good representation of the phase-angle. A parasitic capacitance must give a leading current with respect to the voltage, the zero-crossings must come earlier. Especially the lamp current in state 5 and state 10 in figure 8 are very susceptible to changes in zero-crossing. With practically no change in current amplitude, the 'phase angle' can change 60 degrees, depending on whether the differential current in figure 8 is positive or negative.

In practice this means that when the same amount of parasitic capacitance from the hot electrode to the cold electrode \((C_{1+},_1 = C_{2+},_2)\) is connected to both lamps, the measured phase angle will not be the same. This gives a power value that is not the same for both lamps, while the real lamp power is equal.

Moreover the capacitances from the hot electrode of one lamp to the cold electrode of the other lamp, will add currents that can have phase angles over 90 degrees. The \( \text{av}(U) \times \text{av}(I) \times \cos \phi = P \) theorem cannot hold here, because this will give negative lamp power (\( \cos \phi \) is negative).

The effects of the parasitic currents tend to be greater if the resonance frequencies of the two branches are further apart, due to the amplitude of the differential current and the resulting phase angle between the two inductor currents.

These results lead to the conclusion that the phase angle measurement in this way will not give a more accurate result in lamp power, because the sign of the correction factor cannot be determined. This is a direct result from using a duty-cycle controlled half bridge converter. In a 50% duty-cycle half bridge converter with supply voltage control, state 5 and state 10 will not occur and because of the full-cycle driving of the FET's the two inductor currents will be in phase. When using this method the phase angle correction will give improvement.

In our measurement circuit we will not use the phase angle detector. The total effect of parasitic capacitances which is mainly caused by long wires must be further investigated. \( C_{1+},_1 \) and \( C_{2+},_2 \) can be reduced by using a grounded luminaire and wires that are not closely fit to each other. The effects at 28 kHz are probably small.

3.6 Lamp detection.

The ballast must be able to detect an exchange of lamps. This is done using the lamp electrode as a switch. In figure 20 this circuit is shown. If the lamp is removed, the input of the low-pass filter (R2 and C1) goes to +5 V. As a result the detection output will also rise to +5 V, with a time constant of 20 ms. This rejects any AC component caused by the lamp current. If a new lamp is inserted, the output drops to almost 0 V with a time constant of 10 ms. The electrode-heating transformer must be connected via a capacitor to prevent a DC current flowing through the transformer to ground. If this precaution is not
taken, a lamp exchange cannot be detected. This capacitor must have a low impedance at the operating frequency of the electrode heating.

![Figure 20 Lamp detection circuit](image)

The output of the lamp-detection is connected to a digital input.

3.7 PWM generators

The Pulse-Width-Modulators which are originally placed in the digital ballast, are not true duty-cycle generators. In stead of controlling the ratio of the conducting time to the total period time, the absolute conducting time is controlled (T_on control). For fixed frequency operation, there is principally no difference duty-cycle control and T_on control, but with frequency variation the frequency vs. power characteristic is completely different.

Since \( \text{duty-cycle} = \delta = \frac{T_{on}}{T_{total}} = T_{on} \cdot F \), the duty-cycle will change if we take the T_on constant and change the operating frequency.

With duty-cycle control, the conduction time for the FETs is a constant percentage of the period time. If the frequency is increased, the conduction time decreases. If we on the other hand use T_on control, the conduction time remains the same, for all frequencies. So if we increase the frequency, more power will be delivered than with duty-cycle control, and if we decrease the frequency, less power will be delivered. This results in the following frequency vs. power characteristics in figure 21.

The measurements for figure 21 are performed with \( F_{res1} = 27.0 \) kHz and \( F_{res2} = 27.4 \) kHz. The T_on and the duty-cycle are adjusted to give the same lamp power at the intersection point. The difference between the two types of control is most significant at low power levels. The Lamp1-Lamp2 characteristic will be referred to in chapter 4.2.5.
Figure 21 Power-frequency plots for $T_{on}$ & duty-cycle control

Note that the declining power in the duty-cycle plot means that the operating frequency is above the resonance frequency, or at least above the frequency with the maximum power transfer.

The constant $T_{on}$ control is achieved by a sawtooth signal generator, consisting of a current-source and a capacitor. The sawtooth signal is compared with the $U_{duty}$ signal, and if the sawtooth signal is greater, the FET is turned off.

Figure 22 $T_{on}$ control and duty-cycle control

Duty-cycle control can be achieved by adjusting the current-source. The circuit of figure 22 on the right side increases the current into the capacitor as the frequency increases, resulting in a shorter 'on' time for the FETs. The input for the circuit is the same input voltage as is used for the VCO. To compensate for
the 'dead-zone' in the VCO below 1.2 volt, the diode is placed in the emitterpath. A high input voltage increases the current through R2, resulting in an increase of the capacitor current. The circuit will generate the same duty-cycle and T_on at 28 kHz. as the original circuit does.

By varying R6 it is possible to make a linear combination of T_on & duty-cycle control. In this way it must be possible to minimise the dependency of the lamp power on the operating frequency and this will help the control loop. Experimenting with R6 resulted in figure 23. In fact we alter the duty cycle at the high frequency to get the same total power level as at the low frequency. The total power at the lowest and the highest frequency are the same, but now there are two crossings. This forms a complication in the control of the current balancing. The control software determines by the sign of Power1-Power2 whether to increase or decrease the frequency. Note that this sign at high and at low frequencies is the same, but a frequency control action in the other direction is necessary. The occurrence of this double settling point would require more sophisticated software.

This experiment is carried out at only one power level and to get the same result at higher power levels R6 has to be adjusted again. This arrangement can give only a solution for one power level and not throughout the whole dimming region.

![Linear combination of T_on & duty-cycle control](image)

**Figure 23** Power-frequency plot for linear combination

The final conclusion is that T_on control offers better performance than duty cycle control because the power varies less with T_on control than with duty cycle control for the same frequency deviation. This makes the need for the very accurate frequency generator somewhat less strict. In appendix 2 there are
several plots which give the frequency accuracy for a certain dimming level. This is done for different types of control.

3.8 Snubber design.

Varying the duty-cycle of a half bridge converter implies that at a certain setting the FETs can be turned on, while the opposite diode is (still) conducting. If this state occurs, the reverse recovery phenomenon will occur in the diode. While the diode is conducting, a depletion zone is present in the diode with excess-minority carriers. At the desired switch-off time of the diode \( t_0 \) these minority carriers must be recombined. At \( t_1 \) not all the excess carriers have recombined, so the diode remains conducting, and the reverse current increases with a constant \( \frac{di}{dt} \). At \( t_2 \) all the excess carriers have recombined and the resistance of the diode increases and the diode voltage increases also. Now the reverse current will decrease rapidly and a barrier layer will be built inside the diode. Now the diode is off \( (t_3) \). The reverse current through the diode together with the relatively high reverse voltage, will give an excessive power dissipation in the diode. The maximum reverse current will add up to the inductor current, which gives the total FET current.

\[
\begin{align*}
& i_d \quad \frac{di_F}{dt} \\
& t_0 \quad t_1 \quad t_2 \quad t_3 \quad t
\end{align*}
\]

If we place an inductor in series with the diode, the forward current will decrease more slowly, which gives the excess minority carriers more time to recombine. The maximum reverse current \( I_{rr} \) will decrease, and also the stress on diode and FET.

The energy stored in the inductor must be released, this will be done via the diode and the resistor and also via the resonant circuit.

The best way to reduce the losses due to reverse recovery and parasitic capacitance at the half bridge point, is using two snubbers.

The value for the inductor can be found by comparing the extra switch-off losses \( \frac{1}{2} L i^2 \) with the losses introduced at the switch-on point. The turn-off losses are fairly high and give the suggestion to lower the inductor value. However this will increase the switch-on losses and the switch-on peak current. This peak current will cause EMI problems and must be kept as low as possible. The resistor must be able to dissipate the inductor energy in a short time compared to the half-bridge period time.

A good snubber design will always be a compromise between the arguments mentioned above.

- 32 -
3.9 Losses.

The losses in the power circuit can be divided in some groups:

Losses in the FETs
Losses in the snubbers

3.9.1 Losses in the FETs.

The FETs are responsible for two types of losses; Conduction losses and Switching losses. The conduction losses are dependent on the duty cycle and will be maximal when the duty cycle is 50%. The $R_{\text{on}}$ for the IRF830 is 1.5 Ohm. At maximum power and duty-cycle the RMS current through the FETs is 0.85 A. This gives a power dissipation for each FET of: $0.85^2 \times 1.5 = 1.08$ Watt.

The switching losses are somewhat more complicated to measure. At the switch-on point the current through the FET will not increase rapidly, but during the off-switching of the FET there will be power dissipation. The switch-off characteristic is displayed in figure 26. Using the mathematical functions of the Tektronix TDS460A it is possible to multiply real-time the voltage and the current input. With the measurement function the mean value between the two cursors is obtained.

Care must be taken with the exact calculation of the power dissipation. The scaling factors must be taken into account.
Figure 26 Switch-off losses in the FETs

Voltage input: 1 V = 100 V Drain-Source voltage
Current input: 1 V = 2 A Fet current
Power (Math1) channel: 1VV = 200 Watt

A mean value of 210 mVV in 300 ns gives a power dissipation of:

\[
P = f_s \cdot P_{\text{mean}} \cdot \Delta t = 28 \times 10^3 \times (0.210 \times 200) \times 300 \times 10^{-9} = 0.353 \text{ Watt}
\]

3.9.2 Losses in the snubbers.

The snubber losses can be calculated in different ways. First we can calculate the energy stored in the snubber inductor at switch-on and switch-off points. This gives 4 energy storage points. However not all the stored energy will be dissipated, this can be seen in figure 27 in the lower current plot.

- The peak just after the trigger point will not decrease completely to zero, because the total FET current is increasing.
- The energy in the snubber inductor at the switch-off point will not completely be dissipated, but will be released also during the off-switching of the FET.

A more accurate way to measure the losses in the snubber is looking at the current through the snubber resistor. Here also 4 peaks can be identified and all
the power will be dissipated. The RMS current through the resistor in one oscillator period is: 4.20 mV * 0.05 A/mV = 0.21 A. This gives a total dissipation of: 0.21^2 * 22 Ohm = 0.97 Watt.

In this calculation dissipative effects within the inductor are not taken into account, as core losses, HF losses and RMS losses. Since the inductors do not become very warm, we expect that these effects can be neglected.

![Resistor current and Inductor current](image)

**Figure 27 Snubber currents**

The total losses in the power circuit can be added up:

- 2 * $R_{DSON}$ losses = 2.16 Watt
- 2 * switching losses = 0.71 Watt
- 2 * snubber losses = 1.94 Watt

**Total losses:** 4.81 Watt

These losses are necessary to produce a 100 Watt PWM regulated half bridge converter.

The losses for the total circuit are not calculated, because no optimisation is done here. Other losses can be found in:

- supply for the microcontroller and additional circuits
- energy for the gate-source capacitance in the FETs
4. Software.

4.1 Introduction.

The program to start with is the program for the Digital Ballast. This ballast is a part of the Local Digital Lighting (LDL) system. In this system various peripherals as ballasts, lighting controllers, light sensors and presence detectors communicate via the InfraRed medium.

For this project these features are not necessary. The object is to develop a control program to set total lamp power at a desired level between 1% and 100%. This must be done with an accuracy of 6% of the desired power level. The light flux unbalance must be less than 20% but in experiments has been observed that such an unbalance is visible. We will try to set the maximum unbalance at 6% also.

The program must perform proper ignition procedures to extend lamp lifetime and minimize ignition lightflash. If one of the lamps is defect, this must be detected and the ballast must continue to operate in single lamp operation. Objective is to keep the lightlevel in this mode as desired with the open voltage across the defect lamp as limiting condition. An exchange of lamps must also been detected and in this case a re-ignition procedure must be started.

The program for the ballast must be written for the 80C552 microcontroller. A high level programming language PLM51 is used, to keep the program readable and to make future adaptations easy to implement. For reasons of execution speed, some routines are written in ASM51, the machine language for the 8051 family.

The detailed comment to the program is placed in the program list. This is easy to read and handy when making changes to the program.

The resulting program can perform the functions as required. Via a datalink to a PC the various dimming commands can be transmitted to the ballast.

4.2 Program structure.

The program execution can be seen as a sort of state machine. The various lamp and burning conditions have been analyzed and can be visualised as in figure 28. The functions of the various parts will be discussed briefly. The preheat phase which will normally be present can be ommitted because a separate circuit is used for the prototype. This circuit will allways deliver power to the electrodes.

4.2.1 Off.

This state is entered first when the ballast is switched on and also when a new ignition procedure has to be started. The half bridge converter is switched off for 2 seconds to ensure both lamps are off. Also the lamp present states will be initialized. This procedure will be
4.2.2 Check LC.

This procedure tries to determine the resonance frequencies for the two branches. This is done by sweeping through the frequency range at a low duty-cycle. The open voltage over the capacitor (= lamp voltage) when the lamp is not burning will show a peak at the resonance frequency. For resonance frequencies not too close to each other, this is certainly true, and will give a characteristic like figure 29.

The two curves at the bottom of the plot are the open voltages. The two resonance points are easily identified. The sum of these two signals has one maximum at which the two voltages are almost equal. This is easier to detect than the zero-point in the difference. The frequency at which the voltages are equal will be used for the ignition procedure because in this way the lamps will
Figure 29 Open voltage vs. frequency characteristics

ignite most probably at the same time. This will minimize the ignition lightflash, because otherwise one lamp will be burning at a high power level, while the other still has to be ignited. The two maxima in the open voltages are stored and can be used together with the voltages at the lowest and the highest frequency for the single lamp operation mode. These voltages determine how to get the lowest voltage across the defect lamp.

As stated above this algorithm does not always work. If the two resonance frequencies are almost equal, there will be no peak $V_1 + V_2$. One of the voltages shows a maximum and the other a minimum. This effect is probably caused by the very small duty cycle of the half-bridge converter. When the half-bridge converter is operated at small duty-cycle values, it will perform like a current source. This current source will give no resonance peak in the circuit. The small duty-cycle is necessary because the voltage across the lamps must be much lower than the ignition voltage. The half bridge voltage will contain many higher harmonics which do not contribute significantly to the open voltage. The differences in the open voltage characteristics can be explained with the differential current as introduced in 2.5. The differential current will introduce an extra voltage across the inductor. When the resonance frequencies are almost equal, the differential current is small, and also the voltage at the capacitor originating from the differential current. The exact determination of the resonance frequencies is difficult and needs further investigation. The voltages seem also to be influenced by magnetic coupling of the two inductors. On the other hand, when the resonance frequencies are almost equal, the operating
frequency is less important. Figure 30 shows the characteristic for almost equal LC.

![Figure 30 Open voltage for equal LC](image)

4.2.3 Ignition.

Every time the ignition procedure is invoked (every 4 ms) the duty-cycle is increased one step of 10 Hz. The frequency is set according to the preceding CheckLC routine. Several checks are done during this ignition procedure:

- If one lamp burns and the other lamp is not present, the single lamp operation mode is entered (BURN1 or BURN2).

- If both lamps are burning the SET mode is entered. Before the SET mode is entered, a ‘first guess’ for the duty cycle is done to minimise the ignition lightflash. An exact duty cycle value is not possible due to the tolerances in L and C.

- If none or only lamp is burning and the maximum ignition voltage is reached for both lamps, ignition_2 mode is entered.
4.2.4 Ignition2.

This mode is entered when a lamp is present but has not ignited at the maximum ignition voltage. This voltage will be applied for a maximum extra time of 200ms. If both lamps are on, the SET mode is entered, if not, one of the single lamp operation modes is entered or the standby mode.

4.2.5 Set.

The SET procedure tries in a fast way to find a setting point for the frequency and the duty-cycle. This is done by a technique called fuzzy-logic [5]. In this scheme the possible lamp-power values are compared with the desired power (P_desired) and the result is divided in 5 areas. If a result is contained in one area, the actions belonging to that area are executed. This can be visualised in so called management functions. In fuzzy-logic not only the actual values are contained in management functions, but also the derivatives of these values may be contained. If we take another look at figure 19 we see that the power difference for t_on control is not a monotonous function. If the frequency is far from the setting point, the difference will first become greater before going to zero. So the derivative can only be applied in a small frequency region. In which region this is, is very hard to determine. It is dependent on dimming level, resonance frequencies, temperature and possibly more parameters. For this reason only the actual value will be used, together with the parameters from the check_lc routine.

The management functions for the power control are in the table below.

The internal representation for power values is $6.13 \times 10^{-3}$ Watt/unit (or 0.613 W/100 units).

<table>
<thead>
<tr>
<th>P_total criterium 1</th>
<th>criterium 2</th>
<th>action</th>
</tr>
</thead>
<tbody>
<tr>
<td>P_desired</td>
<td>ABSDIF &gt; 200</td>
<td>decrease2</td>
</tr>
<tr>
<td></td>
<td>ABSDIF &lt; 200</td>
<td>decrease</td>
</tr>
<tr>
<td></td>
<td>ABS(POWER1) &gt; 400 and ABS(POWER2) &gt; 400</td>
<td>adjust_freq</td>
</tr>
<tr>
<td></td>
<td>ABS(POWER1) &gt; 50 and ABS(POWER2) &gt; 50</td>
<td>decrease</td>
</tr>
<tr>
<td></td>
<td>ELSE</td>
<td>adjust_freq</td>
</tr>
<tr>
<td>+12%</td>
<td>ABS(POWER1) &gt; 50 and ABS(POWER2) &gt; 50</td>
<td>adjust_freq</td>
</tr>
<tr>
<td></td>
<td>ELSE</td>
<td>TRACE</td>
</tr>
<tr>
<td>+6%</td>
<td>powermove = true or freqmove = false</td>
<td>adjust_freq</td>
</tr>
<tr>
<td></td>
<td>powermove = false and freqmove = true</td>
<td>TRACE</td>
</tr>
<tr>
<td>-6%</td>
<td></td>
<td>increase</td>
</tr>
<tr>
<td>-12%</td>
<td></td>
<td>increase2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>increase</td>
</tr>
<tr>
<td></td>
<td></td>
<td>increase2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>increase</td>
</tr>
</tbody>
</table>

- 40 -
The abbreviations used in the table above are:

**ABS(.):** The absolute power value for a lamp.

**ABSDIF(.):** The absolute difference between the total lamp power and the desired power.

**POWERMOVE:** Indicates whether a power adjustment has been done.

**FREQMOVE:** Indicates whether the frequency has been adjusted to a correct value.

**INCREASE:** Increase the power 1 step.

**INCREASE2:** Increase the power 5 steps.

**DECREASE:** Decrease the power 1 step.

**DECREASE2:** Decrease the power 5 steps.

**ADJUSTFREQ:** Adjust the operating frequency until the power balance of the two lamps is within the given limits.

If the total power is between the 6% of P_desired, and the frequency has been adjusted to ensure the power balancing, the TRACE mode is entered.

The total T_on range is divided in 1023 equal steps of 15.6 ns. The T_on can be adjusted from 0..16 μs.

### 4.2.6 Adjust_frequency.

This routine is used in combination with the SET procedure. Each time it is invoked, the operating frequency will be adjusted. The speed of adjustment is dependent on the result of the previous action. This method will probably cause some overshoot because the settling point will be approached in large steps. If such a large step crosses the tolerance zone, small steps will be used to regulate within the 6% limits (see figure 31).

In this way a fast response can be obtained, but at low dim-levels, the overshoot could be greater than the original error in power balance. At lamp power levels below 1 Watt only small frequency steps are applied.

This procedure will be quit only if this power balance is within the 6% range.

Figure 31 Frequency steps according to the power difference
4.2.7 Trace.

The trace mode is first entered when both power level and power balance are within the tolerance boundaries. It only has to compensate for effects which are caused by changing temperature of the lamps or the circuit. These effects will be very small in the time between two measurements, so only small frequency or power steps are necessary. This will be done alternating, this means a frequency step followed by a power step and again a frequency step. Even dimming from one level to another is possible but it will take more time than the SET and ADJUST_FREQUENCY routines.

4.2.8 Single lamp operation.

The single lamp operation mode will be executed in either BURN1 or BURN2, depending on whether the lamp in branch 1 is still burning, or the lamp in branch 2.

Every program cycle of 4 ms. the lamp-present detectors are checked. If one lamp is absent (or the ‘cold’ electrode is defect), the single lamp operation mode is entered. In this mode the frequency is increased or decreased until the upper or lower limit is reached. The choice whether to increase or decrease the frequency is made upon the results from the check_Ic routine. The open voltage across the defect lamp must be as low as possible and this is determined in the check_Ic routine. Furthermore the duty-cycle is decreased until the open voltage is below 230 Volt. This voltage is allowed across the lampholder. If possible, the lamp power of the remaining lamp is increased to give the same light output as with two lamps.

If the defect lamp is replaced, the program flow chart will be restarted at the top, to try to ignite both lamps. If however the remaining lamp is removed, the standby phase is entered in which the half bridge converter is switched off.
4.3 Assembly language procedures

Some of the softwareroutines are written in assembly language ASM51 in stead of PLM51. This has been done because the execution time for these routines in PLM51 would be much higher than when written in ASM51.

These routines are:
- MULT\_IU
- AVERAGE
- COMPARE\_0
- COMPARE\_1

4.3.1 Interfacing between PLM51 and ASM51.

The interfacing between the assembly routines and the other parts of the program must be done in a specific syntax.

First the procedure must be declared in PLM to be able to invoke the procedure (the declaration must be done prior to the use of the procedure): e.g.

```plaintext
procedurename: PROCEDURE (x,y) WORD EXTERNAL;
DECLARE (x,y) WORD;
END procedurename;
```

In the first line the name of the procedure is declared. The (x, y) part gives the names and number of input parameters. If the input parameters are placed within parentheses the parameters will be transferred via subsequent memory locations.

The keyword WORD means that the return variable is of the WORD type and PLM51 assumes that the machinecode places the return variables for the WORD type in internal registers R6 and R7 (high, low). If other types are used for the return variable then the machinecode must use the accumulator for a BYTE value, and the carry register for BIT values.

The keyword EXTERNAL means that this procedure is written in another module, in this case an extra module which contains only ASM51 routines.

The DECLARE part in the second line must contain the same input parameters as in the first line, and it defines the type of the input variables (BYTE, WORD or BIT).

In the assembly module (which must be compiled by ASM51), the procedure must also be declared. Now it must be declared PUBLIC, because other modules must be able to acces it. The procedure name must have the underscore character ( _ ) as prefix because this is the way PLM51 tries to acces it. When the procedure is invoked, PLM51 puts the input parameters in on-chip ram at location labeled by: _procedurename\_byte and _procedurename\_bit. Words are placed in the byte data space (high, low). For these dataspaces and the code space separate segments can be declared. These segments keep the program structured.
The most common way to declare an ASM51 routine is:

PUBLIC _procedurename
segmentnamebytes RSEG DATA
segmentnameproc RSEG CODE

    RSEG segmentnamebytes
    _procedurename_BYTE:
       x: DS 2
       y: DS 2

    RSEG segmentnameproc
    _procedurename:
       ---
       ---
       RET

4.3.2 MULT_I_U.

The MULT_I_U routine is able to multiply a 13 bit current value and a 10 bit voltage value, into a 16 bit word which is a representation for the lamp power. The exact result is: (I*U)/128. For the intermediate result a 24 bit representation is used to prevent data loss. The routine uses the standard assembly operator MULT AB, which multiplies two 8 bit values into a 16 bit value. The multiplication itself for the current and voltage is done in the very same way as is done in a written multiplication:

```
\begin{align*}
\text{MULT}_I_U & \quad \text{MSB} \quad \text{LSB} \\
\text{R6} & \quad \text{R7} \quad \text{TEMP} \\
I_max & = 8191 = \$1FFF \\
U_max & = 1023 = \$03FF \\
I_L & \times U_L \\
I_H & \times U_L \\
I_L & \times U_H \\
I_H & \times U_H \\
/ 128
\end{align*}
```
The routine uses approximately 62 machinecycles for the multiplication and the division by 128.

4.3.3 AVERAGE

The average routine is used to calculate the average power value. A mathematical first order low pass filter is made by taking 7/8 of the previous power value and add 1/8 of the actual power value. The time constant for this filter is 8 * 4ms = 32 ms. The data loss is reduced by first multiplying the previous power value by 7 and then adding the actual power value. This result is then divided by 8.

\[ P(k) = \frac{7 \times P(k-1) + P_{new}}{8} \]

Because the result of the multiplication cannot be fit into word, a machinelanguage routine is used for this purpose. This gives a very fast averaging routine. The duration of the averaging routine is 28 + 26 = 54 machinecycles.

4.3.4 COMPARE_0 and COMPARE_1

COMPARE_0 and COMPARE_1 are two interrupt routines. They are used to make Timer2 a 10 bit PWM generator. Timer2 is a 16 bit timer/counter which will be incremented each machinecycle (= \( f_{osc} / 12 \)). This timer has 3 timer_compare registers, which can initiate different actions at a programmed timer_value. We set timer compare register_0 to 1024, at which counter value outputport bit P4.0 will be set. This portpin is the inputsignal for the VCO. At the same moment outputport bit P4.1 will also be set. This portpin is connected to the RT2 pin, which will reset Timer2 at the rising edge. Finally the timer compare register_0 will start the interrupt procedure COMPARE_0. This routine is very short and uses no registers, so there is no need to store the accumulator, the datapointer, the B register or other registers. The routine resets outputport bit P4.1 to ensure that at timer value 1024 a rising edge will occur at RT2. It must also clear the Timer2 compare_0 interrupt register (CMIO). Each period of Timer2 will have a duration of:

\[ T = \frac{1024}{12} \times \frac{1024 \times 12}{16MHz} = \frac{768 \mu s}{=1302Hz} \]

Timer2 compare register_1 is used to reset outputport P4.0 at the desired duty cycle. This is done via the STE register. This ensures an automatic reset of P4.0 on a match between Timer2 and compare register_1. The interrupt routine reloads immediately after this reset of P4.0 the timer compare register_1 with the (new) frequency value. This must be done within an interrupt routine because the frequency is a word value, and the microcontroller can transfer only one byte at a time. If the bytetransfer is not synchronized with Timer2, the
compare register can be triggered at an intermediate value. This routine must clear the interrupt flag CMI1.

The two interrupt procedures have high priority, so they cannot be interrupted by the I2C routines and other low level interrupt routines.
5. Results & Tolerance investigations.

5.1 Introduction

During the design process several tests are performed to determine the quality of the regulation. The circuit must be able to work with components which have tolerances. The tolerances can be found in the resonant circuit and the measurement circuits. Furthermore the regulation speed of the control loop is checked.

5.2 Tolerances in the resonant circuit (L and C).

The circuit has been tested with several different LC combinations. The main problem is to determine the branch with the highest and the lowest resonance frequency. If this determination is correct, the whole circuit will work properly. In the control loop precautions are taken to prevent the lamps from extinguishing. Measurements are taken when using different resonance frequencies.

In figure 33 the results are plotted. The resonance frequencies are indicated with dots, the theoretical settling frequency is also plotted. The measured settling frequency lies always somewhat lower than the theoretical and this may be caused by parasitic capacitances, which will lower the resonance frequency.

![Figure 33 Settling frequencies for different resonance frequencies]

The control program always identified the correct branch with the lowest resonance frequency.
5.3 Tolerances in the measurement circuits.

The critical components in the measurement circuits are the sensing resistors. The components have a 1% tolerance. The coupling factor of the current transformer will be very high, so we estimate a maximum error of 1% will be introduced. This gives a maximum error in the analog part of 2%. The supply voltage for the analog to digital converter will influence directly the sampling values. A standard voltage stabilizer will have a tolerance of at least 5%. The errors within the ADC can be estimated at maximum 2 LSB.

5.4 Switching characteristics

The speed of control can be measured by switching from the 100% level to the 1% level and vice versa. In figure 34 the light output is measured during the change of power level. The circuit settles the power level and the balance between the two lamps within 500 ms for both directions. Further experiments showed that little frequency adjustment is necessary for power balancing at 100% and at 1%.

![Figure 34: Light level switching time](image)

**Figure 34** Light level switching time
6. Conclusions.

The circuit has proved that it is possible to eliminate the current balancing transformer. Two branches with the same resonance frequencies give the best result for dimming at low levels, but care must be taken with identifying the branch with the highest and lowest resonance frequency. The need for a very accurate frequency generator is with \( T_{on} \) control somewhat less than with duty-cycle control, because the dependency of the power on the frequency is less.

The accuracy for inductors and capacitors is set at 5%, this gives a maximum deviation of the resonance frequencies of 10%.

The minimum dimming level at which the control loop remains stable is 0.3%. Below this level errors in the mathematical routines are introduced which will cause erroneous power values.

The light-flash measurements at ignition of the lamps at 1% dimming level show the following properties:

- duration of light-flash: 16 ms. This means that in 4 program cycles the control loop is able to detect the ignition and to give a good first guess.
- the height of the light-flash is about 20% of the nominal light output.

The program is able to switch from the 100% level to the 1% level within 500 ms.

Single lamp operation is possible. If the open voltage across the defect lamp is to be kept below 230 V, the lamp power in the other branch will be at least 20% of nominal power. The remaining power is dependent on the difference in resonance frequencies.

The price we have to pay for this achievement is a half-bridge converter which must contain snubber circuits. These snubber circuits are necessary to prevent excessive dissipation in the FET's and diodes. The total dissipation in the power circuit (including snubbers) is estimated at 5 Watt.

The control circuit is now implemented with a microcontroller. This microcontroller is very flexible to identify whether to increase or decrease the operating frequency for current balancing. If an analog circuit has to be designed for the unequal LC topology, it must be necessary to choose the resonance frequencies far enough apart to ensure distinctive resonance frequencies with component tolerances. Because the large difference in resonance frequencies, the minimum dimming level shall be higher than with the digital circuit. On the other hand, an analog circuit will not suffer from quantisation problems.
Frequency characteristics $C=12\text{nF}$ $L=1.697\text{mH}$ $F_{res}=35.27\text{kHz}$.
Frequency characteristics $C=16\text{ nF} \ L=1.733\text{ mH} \ F_{res}=30.23\text{ kHz}$.
Frequency characteristics $C=22\text{nF}$ $L=1.703\text{mH}$ $F_{\text{res}}=26.00\text{kHz}$.

- $d=0.4$
- $d=0.35$
- $d=0.30$
- $d=0.25$
- $d=0.225$
- $d=0.21$
- $d=0.20$
- $d=0.19$
- $d=0.18$
- $d=0.175$
- $d=0.17$

Lamp power (W)

Frequency (Hz) Parameter = duty-cycle

Appendix 1. NHBO simulations for different LC combinations, real duty-cycle control.
Appendix 2a. Dimming characteristics and frequency requirements.

Duty cycle control.

Dimming characteristics $F_{res} = 27.048$ kHz $F_{res II} = 30.120$ kHz

Graph showing the relationship between lamp power (W) and frequency (kHz) with the parameter being the duty cycle.
Appendix 2a. Dimming characteristics and frequency requirements.
Duty cycle control.

Mutual difference in power with duty cycle control

Frequency (kHz) parameter = dimlevel

Lamppower difference (%)
Appendix 2b. Dimming characteristics and frequency requirements. 
T\textsubscript{on} control.

![Graph showing lamp power with T\textsubscript{on} control vs. frequency (kHz)]
Appendix 2b. Dimming characteristics and frequency requirements.

T\textsubscript{on} control.

**Mutual difference in lamppower with T\textsubscript{on} control**

![Graph showing mutual difference in lamppower with T\textsubscript{on} control vs frequency (kHz). The x-axis represents frequency in kHz, ranging from 28 to 29. The y-axis represents lamppower difference in percentages, ranging from -25% to 25%. Various lines indicate different dimming levels (1%, 2.5%, 3%, 8%).](image)
Appendix 2c. Dimming characteristics and frequency requirements.
Supply voltage control.
Appendix 2c. Dimming characteristics and frequency requirements.
Supply voltage control.

![Graph showing mutual difference in power with supply-voltage control](image)
References:

[1]  AHBO - a computer program to calculate resonant components for half-bridge lamp converters. see [3]

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