MASTER

Experimental determination of contact resistance and the density of states in field-effect transistors

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Experimental determination of contact resistance and the density of states in field-effect transistors

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Abstract

The goal of this thesis is to obtain more information about charge transport processes in disordered transistors via the determination of contact resistances and the density of states. Scanning Kelvin Probe Microscopy is used to obtain information about the surface potential above thin film field-effect transistors. The detected surface potential corresponds to the potential within the accumulation channel and therefore enables investigation of the potential profile in lateral direction, indicating local obstructions (resistances) in the channel. Furthermore, the dependence of the surface potential on the gate bias can be used to determine the shape of the density of states.

For different device geometries and varying dimensions of a transistor with zinc oxide as the active material, quantitative contact resistance measurements are obtained via electrical characterization and Scanning Kelvin Probe Microscopy (SKPM). The nature of the contact is further studied using SEM. Contact resistances in zinc oxide thin film transistors arise predominantly due to a complicated non-ideal morphology and non-ideal energy level alignment between the contacts and the active material. The latter appears to be of minor importance in the used transistor structures. Quantitative values of $(10 \pm 5) \, \text{M}\Omega$ at an applied gate voltage of 10 V for the contact resistance could be determined. Contact resistances decrease with increasing gate voltage and appear to be independent of channel length and applied source and drain voltages.

For both the zinc oxide thin film field effect transistor as well as for a transistor consisting of a self-assembled monolayer of an oligothiophene, density of states profiles are obtained via Scanning Kelvin Probe Microscopy. The slope of the density of states, represented by a temperature $T_0$, could also be obtained from electrical characterization. The $T_0$ values calculated from SKPM measurements are similar to the $T_0$ values extracted from electrical measurements. ZnO transistors are found to have $T_0 = 800\pm200$ K. For the monolayer of oligo thiophene a somewhat lower value of $T_0 = 350\pm200$ K is found.
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Introduction

The transistor is probably one of the most important inventions of the last century. Enabling the downsizing of computers and thereby the development of personal computers, mobile phones, smart phones and gaming computers, the transistor forms a vital element of today’s society. The switching speed of integrated circuits can be estimated when considering the performance of individual transistors. High switching speeds, resulting in fast computers, are obtained with high mobility silicon transistors. Processing of these transistors is however time consuming and production costs are high. Since the 1980’s the interest for research into organic electronics has largely increased since organic, carbon-based, materials have the potential to be easily manufactured, low in cost and create flexible electronic circuitry. In addition, more research towards this topic also improved mobilities in these devices. To further increase device mobilities, a better understanding of the transport physics is desirable.

In this thesis, research is done on thin film field effect transistors. Zinc oxide (ZnO), an inorganic compound, is chosen as the active material because of its high mobility of 1 cm²/Vs, easy processing for which no vacuum environment is needed, and its potential use as transparent material in flat panel displays. In a transistor, charges are injected from the source contact, travel along the gate dielectric interface and are extracted from the drain contact. In that process they encounter 3 interfaces. A more detailed description of the effect and existence of contact resistance on device performance enables a clear distinction between charge injection and extraction and the local charge transport within the conducting channel. Therewith better insight in transport near the interface can be obtained.

Charge transport in disordered materials is determined by the density of states (DOS); it determines the amount of charge carriers available for conduction. Direct determination of the DOS will form an important step towards a better understanding of charge transport in transistors. The shape of the DOS is usually modeled by a Gaussian or exponential distribution but experimental information on its specific shape is seldom investigated. In this thesis research is done on the DOS of an organic self-assembled monolayer field-effect transistor of oligothiophene and on the inorganic ZnO transistor.

The goal of this thesis is to obtain more insight in charge transport near transistor interfaces through the detection of contact resistances and density of states profiles. Electrical characterization as well as the SPM techniques will be used to obtain potential profiles throughout the transistor. The DOS is investigated through the use of Scanning Kelvin Probe Microscopy (SKPM) on a very thin layer of active material. In addition to that information about the DOS is gathered through current-voltage measurements as a function of temperature.
Chapter 1: Physics and properties of transistors

How does the transistor work?
Although the field effect transistor was invented as early as 1925 it was only in 1952 that the first working devices were made. These devices consisted of inorganic materials. Mid 1980’s organic transistors that were composed of carbon-based materials, came up. Here we study a specific transistor, the field-effect transistor (FET). In figure 1 a schematic representation of a thin-film field-effect transistor is shown. TFT’s are composed of a source, drain and gate electrode as well as a gate dielectric and a semiconducting layer.

![Schematic representation of a TFT with bottom gate contact and the semiconducting layer applied on top of source and drain contacts](image)

Figure 1. Schematic structures of a TFT with bottom gate contact and the semiconducting layer applied on top of source and drain contacts [1].

When a voltage is applied on the gate electrode, charges are accumulated at the semiconductor-dielectric interface, creating a conducting path between source and drain electrode. The role of the source and drain contacts is to inject and extract charge carriers into and out of the semiconducting material. The semiconducting layer is often called the active layer since this is where the charge transport takes place. The charge distribution in the bulk of the semiconductor is not uniform; it decreases from the semiconductor/dielectric interface towards the bulk. The accumulation layer in which charges are moving has a thickness of a few nm [2]. Increasing the thickness of the active layer will increase the amount of bulk material but does not increase the amount of charges being transported.

Semiconductors can be p-type, n-type or ambipolar meaning that the transport is carried by holes, electrons or both, respectively. For n-type transistors a positive gate voltage needs to be applied to create a conducting channel consisting of negative charge carriers. For a p-type material a negative gate voltage is needed to create a conducting channel of positive charge carriers. Figure 2 shows the IV characteristic of an n-type thin film transistor; such a characteristic is called a transfer curve. When a negative gate voltage is applied on the gate, positive charges are attracted to the channel. Since these have limited or zero mobility in an n-type material, no current can flow. Here the transistor is in the so-called ‘OFF-state’, or depletion region of the IV curve. For positive gate voltages electrons are accumulated in the channel and a current can flow between source and drain. It is not necessary that the onset of the accumulation regime starts at exactly zero gate voltage.
The deviation from zero gate voltage as the onset of accumulation is called the threshold voltage. $V_{T}$ needs to be overcome in order to turn the transistor on. The offset can be either positive or negative which makes the effective applied gate voltage equal to $V_{\text{GATE}} - V_{T}$. Depending on the voltage differences applied from gate to source and from source to drain, different regimes in the transfer curve corresponding to different field distributions, can be found as stated in figure 3.

For $V_{\text{GATE}} - V_{T}$ values much larger than the value of $V_{SD}$, the current increases with the gate voltage. In this case the voltage drop over the channel from drain towards source contact is linear, as shown in figure 3b in the two highest lying curves. For $V_{\text{GATE}} - V_{T} \leq V_{SD}$, a non-linear spreading of the charge carriers is found in the conduction channel (the two lowest lying curves in figure 3b). Close to the drain the potential within the channel drops below the threshold and the charge carrier concentration drops to zero. Figure 3c shows how the charge carrier concentration is varied over the channel for the different
field distributions. Because of the non-linear spreading of the charge carriers for $V_{GATE} - V_T \leq V_{SD}$, this so called saturation regime corresponds to an increase of the source-drain current that is saturating with increasing source-drain voltage.

### Charge transport models

Despite the fact that charge transport in organic and disordered inorganic materials is not yet fully understood, simple transport models are often used to extract device parameters such as threshold voltage and mobility. For a better understanding of these models a short introduction in the physics of charge transport in organic materials is given first.

### The physics of charge transport in organic materials

Zooming in on an organic material and its chemical structure throws light on charge transport processes. In an organic material, the covalent bonds between atoms in one molecule are very strong while in between different molecules only small $vdW$ bonds exist and electrons are hardly shared between molecules. This is to a large extent due to limited overlap between orbitals on different molecules. For this reason the electrical current flowing through organic materials can be seen as electrons hopping from one molecule to the next.

Charge transport within a semiconducting material is thus described by a certain energy level at which a charge can be situated and by energy spots that are available to move to. The Fermi level, $E_f$, is the term used to describe the top of the collection of electron energy levels at absolute zero. For $T > 0K$ electrons energy levels are spread out as described by the Fermi-Dirac distribution given in equation (1.1).

$$f_{FD}(E, E_f) = \frac{1}{1 + e^{\frac{E - E_f}{k_B T}}}$$

In this equation $T$ represents temperature and $k_B$ is Boltzmann's constant. The available energies for conduction electrons are situated somewhat above the Fermi level into the conduction band. In contrast to crystalline inorganic materials, thin films of disordered semiconductors do not have two delocalized energy HOMO and LUMO (or valence and conduction) bands separated by an energy gap. Instead, because of disorder, a distribution of energies for all different sites in which an electron can be situated is present. The distribution in energy of the charge transport sites is called the density of states, $g(E)$.

The product of the Fermi-Dirac distribution and the density of states gives the total density of charges that is present at a given temperature for a particular piece of material.

$$n = \int_{-\infty}^{\infty} g(E)f_{FD}(E - E_f)dE$$

In equation (1.2) the electron occupation is shown with $g(E)$ the density of states (DOS) and $f_{FD}$ the Fermi-Dirac distribution. The energetic position of the valence and
Chapter 1: Physics and properties of transistors

Conduction band levels around which the DOS is situated, are material specific. The shape of the Fermi function is a general function that applies to any solid material in thermal equilibrium. The DOS-shape is specific to a particular type of material. In disordered semiconductors the density of states is often approximated in shape by a Gaussian density of states.

Idealized MOSFET model

The most common model for the description of charge transport is the idealized Metal Oxide Semiconductor Field-Effect Transistor model, MOSFET model, which is based on the assumption of constant field-effect mobility. Furthermore in the idealized model, it is assumed that the transverse field \( E_x \) in the channel is much larger than the longitudinal field \( E_y \). This is the so-called gradual channel approximation [3]. In the linear regime the current can be approximated by equation (1.3).

\[
I_{SD} = \frac{\mu_{FE} C_D W}{L} \left( V_G - V_T - \frac{V_{SD}}{2} \right) V_{SD}
\]

\[V_{SD} \ll V_G - V_T\]

In which \( \mu_{FE} \) is the field effect mobility, \( C_D \) the capacitance per unit area of the dielectric layer, \( W \) and \( L \) channel width and channel length respectively and \( V_T \) the threshold voltage. The mobility is derived from this equation:

\[
\mu_{FE} = \frac{L}{C_D W V_D} \frac{dI_{SD}}{dV_G}
\]

To allow for equation (1.4) to be valid, it is assumed that \( \mu \) is not gate voltage dependent. When the transistor is operating in the saturation regime, equation (1.3) with \( V_{SD} = V_G - V_T \), gives:

\[
I_{SD,SAT} = \frac{\mu C_D W}{2L} (V_G - V_T)^2
\]

\[V_G - V_T \leq V_{SD}\]

The mobility in the saturation regime is found using equation (1.6).

\[
\sqrt{I_{SD,SAT}} = \sqrt{\frac{W}{2L}} C_D \mu (V_G - V_T)
\]

Plotting the square root of \( I_{SD,SAT} \) versus gate voltage results in a straight line. The mobility can be obtained from the slope of this line and the threshold voltage corresponds to the extrapolation of the line to zero current.
Research indicated that the mobility in disordered materials depends on both charge density and temperature\[4\]. Within the saturation regime charges are non-linearly spread through the channel implying a not constant mobility and therefore no calculations of saturation mobility are performed in this thesis.

Depending on the structural and chemical properties, several models have been proposed to describe the mobility of charge carriers in the semiconducting layer of both organic and inorganic TFTs.

**Variable range hopping as described by Vissenberg & Matters (VRH)**

For organic amorphous materials an often used model is that of Vissenberg &Matters suggesting variable range hopping (VRH). In the VRH model charge transport is considered to be governed by hopping; the thermally activated tunneling of carriers between localized states. The name variable range hopping means that the rate-limiting hop is determined by a trade-off between hops over a small distance with a high activation energy, and hops over a long distance with a low activation energy. Hops between nearby states with a small energy difference are not rate limiting. Vissenberg & Matters suggest that for low enough temperatures and carrier densities, the transport properties are determined mostly by the tail of the DOS distribution; the DOS can be approximated by an exponent as shown in equation (1.7).

\[
g(E) = \frac{N_t}{k_B T_0} \exp \left( \frac{E}{k_B T_0} \right) \quad \text{(1.7)}
\]

In this equation $k_B$ represents Boltzmann’s constant, $N_t$ is the number of states per unit volume and $T_0$ represents the width of the exponential density of states distribution.

With this exponential density of states and the assumption of variable range hopping, expressions for a temperature and gate voltage dependent field-effect current and linear mobility can be obtained, stated in equations(1.8) and (1.9) \[4-6\].

\[
I_{SD} = \frac{WV_{SD} \varepsilon_{layer} \varepsilon_0 \sigma_0}{Lq} \left( \frac{T}{2T_0 - T} \right)^{2k_B T_0 \varepsilon_{layer} \varepsilon_0} \left( \frac{T_0}{T} \right)^4 \sin(\pi T / T_0) \left( \frac{2\alpha}{B_C} \right)^T \pi \frac{C_D (V_G - V_T)}{2k_B T_0 \varepsilon_{layer} \varepsilon_0} \left( \frac{C_D V_G}{2k_B T_0 \varepsilon_{layer}} \right)^{T/T_0} \quad \text{(1.8)}
\]

\[
\mu_{FE} = \frac{\sigma_0}{q} \left( \frac{\pi (T_0 / T)^4 \sin(\pi T / T_0)}{(2\alpha)^3 B_C} \right)^{T/T_0} \left( \frac{C_D V_G}{2k_B T_0 \varepsilon_{layer}} \right)^{2T_0 / T - 1} \quad \text{(1.9)}
\]
In these equations $\sigma_0$ is the conductivity pre factor, $\varepsilon_0$ the dielectric constant, $\alpha$ the effective overlap parameter, $q$ the elementary charge and $\varepsilon_{\text{layer}}$ the relative permittivity of the semiconducting layer. $B_C$ is a constant describing the onset of percolation. $B_C \approx 2.8$ in amorphous 3 dimensional systems[4, 7].

Within the VM formalism, a field effect mobility that is both temperature and gate voltage dependent is found. In a field-effect transistor, an applied gate voltage gives rise to the accumulation of charge in the region of the semiconducting layer that is close to the insulator. As these accumulated charge carriers fill the lower-lying energy states of the organic semiconductor, additional charges in the accumulation layer will occupy states at higher energies. Consequently, these additional charges will require less activation energy to hop away to a neighboring site. This results in a higher mobility with increasing temperature and gate voltage[4].

Multiple trapping and release model (MTR)

For organic materials with a high ordering or slightly disordered inorganic materials, the multiple trapping and release model is often used. This model, first proposed by Horowitz and Delannoy [8] is a transport model combining both hopping and band-like transport. In this model an exponential distribution of traps with characteristic temperature $T_0$ and density $g_0$ is assumed near grain boundaries combined with a band in which charge carriers move with mobility $\mu_0$. The effective mobility in the channel than becomes:

$$\mu = \mu_0 \frac{N_{\text{mob}}}{N_{\text{tot}}}$$

With $N_{\text{mob}}$ the number of mobile charge carriers:

$$N_{\text{mob}} = \int_{-\infty}^{0} g(E) f_{FD}(E, E_f) dE$$

and $N_{\text{tot}}$ the total amount of charge carriers is given by:

$$N_{\text{tot}} = \int_{-\infty}^{\infty} g(E) f_{FD}(E, E_f) dE$$

States below $E=0$ are mobile, states above $E=0$ have negligible mobility and are therefore called trapped charges with $N_t$ the amount of trapped carriers. The onset in energy of the band is called the mobility edge (ME). In this model the amount of temporarily released charge carriers to an extended-state transport level, the conduction band for classical n-type semiconductors, depends on the energy level of the localized states, the temperature, and the gate voltage. The model is able to account for both the thermally activated conductivity and the gate bias dependent activation energy of the field-effect mobility.
Chapter 2: Scanning Kelvin Probe Microscopy

The technique used in this research to obtain information about charge transport and the density of states in particular, is Scanning Kelvin Probe Microscopy (SKPM). The technique originates from the macroscopic Kelvin Probe, which is a non-contact, non-destructive measurement device used to investigate the work function of materials. It is based on a vibrating capacitor and measures the surface potential between a conducting specimen and a vibrating tip. The work function is the energy needed to move an electron from the Fermi level into vacuum.

When two conducting materials with different work functions are brought together, for example via an external wire contact, electrons in the material with the lower work function flow to the one with the higher work function. These materials together form a capacitor. The flow of electrons towards the material with higher work function induces surface charges which result in a voltage difference over the capacitor. This voltage difference can be translated to a non-zero electric field or a force which can be measured. An external potential can now be applied to the capacitor until the surface charges disappear and zero force is experienced; at this point the external potential equals the contact potential difference. However, this produces a once only measurement, as the surfaces become charged, and the charge must dissipate before another measurement can be made. By using a vibrating probe, a varying capacitance is produced. The vibrating probe or tip is a reference electrode that forms a capacitor with the surface, over which it is scanned laterally at a constant separation. An alternating current ($V_{AC}\cos\omega t$) voltage is applied at the tip resonance frequency to reduce the force between tip and transistor surface to zero.

When using the SKPM technique, a surface is scanned twice. On the first pass, the sample topography is measured by tapping mode: in tapping mode the cantilever to which the tip is attached is physically vibrated near its resonance frequency by a small piezo electric element. A laser beam is focused on the cantilever position above the tip. When the cantilever is moving freely, the reflected laser beam generates a sinusoidal, electronic signal from the four-quadrant detector on which it is focused. Placed above a surface, the tip deflects when it is in contact with a surface.

On the second pass, the piezo that vibrates the cantilever is turned off and an oscillating voltage, $V_{AC}\cos\omega t$ is applied directly to the cantilever tip creating an oscillating electrostatic force at frequency $\omega$. The resulting force between tip and the surface is given in equation (2.1) [9].

$$F = \frac{dC}{dz} V_{CPD} V_{AC} \cos \omega t$$  \hspace{1cm} (2.1)

In this equation $\omega$ gives the resonance frequency of the tip, $dC/dz$ is the vertical derivative of the tip/sample capacitance and $V_{CPD}$ is the contact potential difference between tip and sample. The force experienced by the cantilever depends on the product.
of contact potential difference and the ac drive force. When there is no contact potential
difference, no force will thus be detected. \( V_{\text{CPD}} \) is determined by adjusting the voltage on
the tip \( V_{\text{tip}} \) until the oscillating amplitude becomes zero. This \( V_{\text{tip}} \) is recorded to construct
a potential map of the surface.

![Figure 4. Overview of the Scanning Kelvin Probe technique. Vibrations of the metalized cantilever are detected with the use of a laser by a four quadrant detector. Due to this output signal, vibrations of the cantilever are adjusted while scanning the cantilever over the transistor surface; a lateral image of the surface potential is created[10].](image)

Scanning Kelvin probe microscopy measurements are done with a Veeco Dimension 3100 AFM connected to a Nanoscope IIIa controller equipped with an extender module, operating in the dark in ambient air. Ti/Pt-coated Si tips (NSC36/Ti-Pt, MikroMasch) with force constant of \(~1\ N/m\), resonance frequency of \(~100\ kHz\) and apex radius of \(~40\ nm\) were used. Topographic images are taken in tapping mode, potentials were measured by SKPM in lift mode with a typical lift height of \(25\ \text{nm}\), using an AC voltage modulation of \(3\ \text{V}\) superimposed on the CPD tip potential. With this system lateral resolutions in the order of \(100\ \text{nm}\) and an energy resolution of a few milli-electronvolts are obtained.

With the use of SKPM, information about the shape of the DOS can be gathered. Therefore a more detailed description of the density of states and Fermi level in the active layer is needed. When a positive voltage is applied on the gate, electrons are accumulated in the channel (negative gate voltage in case of a p-type transistor). This accumulation requires a downward shift of the DOS level towards the Fermi level as shown in figure 5. The Fermi level is fixed due to grounded source and drain contacts. A further increase of the gate voltage will increase the electron concentration within the active channel and the DOS level shifts further down (figure 5 picture on the right). A Gaussian DOS distribution is assumed that has a small density of tail states and an increasing density of states available towards the middle of the DOS distribution. Therefore at the onset of electron accumulation a large energy shift is required to accommodate the additional
energy levels, whereas further increase of the gate voltage only invokes a small decrease in energy of the DOS. The electron affinity (EA) shown in figure 5, gives the energy needed to free an electron from the LUMO towards the vacuum and is assumed to remain constant. A Gaussian DOS is not required; the effect described here, holds for any DOS shape.

Source and drain contact are grounded during the SKPM measurement in order to keep the Fermi level constant during the experiment. A slowly increasing gate voltage is now applied to induce a gradual increase in charge carrier concentration.

Figure 5. Scheme of electron occupation within a Gaussian density of states at different positions with respect to the Fermi level. For $V_G = 0$, no charges are accumulated in the active layer hence no overlap between DOS and Fermi level is shown. For positive gate values, electrons are accumulated and the DOS will shift in energy towards the Fermi level. The energy shift is directly correlated with the contact potential difference measured with SKPM.

Both the Fermi level and the electron affinity remain constant while gate voltage increases. A DOS with a given shape is shifted as compared to a constant Fermi level; the measured energy shift, $qV_L$, can therefore be directly correlated to the charge concentration, and accordingly to the shape of the DOS[11].

Applying a positive voltage at the gate electrode, the LUMO-DOS distribution will bend down as explained previously. When moving away from the interface, level bending will occur, shown in figure 6. At a position within the semiconductor very close to an interface, which is the case for thin layers, it is shown through numerical calculations that level bending is negligible[11].

Figure 6. The energy of lowest unoccupied molecular orbital (LUMO), is shown plotted against the distance where $x=0$ is at the gate dielectric/active layer interface. The dashed LUMO level is valid for
zero applied gate voltage. Applying a positive voltage at the gate electrode the LUMO will bend down closer to the Fermi level. \( \lambda \) gives the distance \( x \) at which a flat band is reached. The energy level near \( x=0 \) is \( qV_L \). In case of negligible band bending, \( V_{CPD} \) is equal to \( V_L \).

In case of negligible level bending, the measured CPD corresponds directly to the potential sensed in the conducting channel.

\[
V_L = V_{CPD} \tag{2.2}
\]

The detected surface potential relates to the charge concentration and the rate of change of this charge concentration relates to the shape of the DOS. If \( E_{fT} \) is defined as the Fermi energy level position for \( V_{GS}=V_T \) and \( V_{SD}=0 \) V, then the shift of the DOS with respect to the Fermi level, \( qV_L=qV_{CPD} \), can be seen as the shift of the Fermi level \( E_f \) with respect to \( E_{fT} \) [12].

\[
E_f = E_{fT} + qV_{CPD} \rightarrow dE_f = qdV_{CPD} \tag{2.3}
\]

The gate is isolated from the active material forming a capacitor with the charges in the accumulation layer. The charge concentration in the accumulation layer can thus be described by equation (2.4).

\[
n(x) = \frac{C_D}{qd} (V_{GS} - V_T - V_{CPD}(x)) \tag{2.4}
\]

In this equation \( d \) is the thickness of the active layer and the three potentials form the net potential difference over the capacitor. Since it is assumed that charge concentration does not dependent on height, \( n \neq n(x, y) \), this equation is only valid in case charge is distributed homogeneously through the organic film depth. Another expression for the electron concentration in the channel is given by that part of the DOS that overlaps with the Fermi level:

\[
n = \int_{-\infty}^{\infty} g(E) f_{FD}(E, E_f) dE \tag{2.5}
\]

The distribution around the Fermi level is given by the Fermi-dirac distribution, equation (2.6).

\[
f_{FD}(E, E_f) = \frac{1}{1 + e^{\frac{E-E_f}{k_BT}}} = \frac{1}{1 + e^{\frac{E-(E_f+qV_{CPD})}{k_BT}}} \tag{2.6}
\]
The rate of change of the charge concentration relates to the density of states and can be found when taking the derivative of the charge concentration with respect to $V_{CPD}$, shown in equation (2.7).

$$\frac{dn}{dV_{CPD}} = \frac{d}{dV_{CPD}} \int_{-\infty}^{\infty} g(E) f_{FD}(E,V_{CPD}) dE = \int_{-\infty}^{\infty} g(E) \frac{d}{dV_{CPD}} f_{FD}(E,V_{CPD}) dE$$  \hspace{1cm} (2.7)

To solve equation (2.7), two assumptions can be made. When the width of $df_{FD}/dV_{L}$ is much narrower relative to that of $g(E)$, valid for very low temperatures, it can be approximated by a $\delta$ function.

$$\frac{dn}{dV_{CPD}} = \frac{q}{k_B T} \int_{-\infty}^{\infty} g(E) \delta \left( E - E^f_j - qV_{CPD} \right) dE$$  \hspace{1cm} (2.8)

This can be reduced further:

$$\delta \left( \frac{x}{a} \right) = a \delta (x) \rightarrow \frac{dn}{dV_{CPD}} = q \int_{-\infty}^{\infty} g(E) \delta \left( E - E^f_j - qV_{CPD} \right) dE$$  \hspace{1cm} (2.9)

$$\int f(x) \delta (x-a) dx = f(a) \rightarrow \frac{dn}{dV_{CPD}} = q g \left( E^T_j + qV_{CPD} \right)$$  \hspace{1cm} (2.10)

The following relation is obtained

$$\frac{dn}{dV_{CPD}} = q g \left( E^f_j + qV_{CPD} \right)$$  \hspace{1cm} (2.11)

The density of states can now be expressed as a function of $qV_{CPD}$ by applying equation (2.11) to equation (2.4).

$$g(qV_{CPD}(x)) = \frac{C_D}{dq^2} \left( \frac{d(V_{GS} - V_T)}{dV_{CPD}} - 1 \right)$$  \hspace{1cm} (2.12)

This equation is valid only for $T=0K$ and very low temperatures, and is therefore referred to as the T-zero approximation. Another approach towards solving equation (2.7) would be to assume a certain shape for the density of states. When an exponential DOS is assumed as shown in equation (2.13), equation (2.5) can be written as stated in equation (2.14)[4].

$$g(E) = \frac{N_f}{k_B T_0} \exp \left( \frac{E}{k_B T_0} \right)$$  \hspace{1cm} (2.13)
\[ n = \int_{-\infty}^{\infty} g(E) f_{FD}(E, E_f) dE = N_0 \exp \left( \frac{E_f}{k_B T_0} \right) \Gamma \left( 1 - \frac{T}{T_0} \right) \Gamma \left( 1 + \frac{T}{T_0} \right) \]  

(2.14)

This approximation is only valid at low temperatures, \( T < T_0 \) and low charge carrier densities. The gamma function stands for:

\[ \Gamma(z) = \int_{0}^{\infty} e^{-y} y^{z-1} dy \]  

(2.15)

The gamma function can be rewritten which results in equation (2.16) [13].

\[ n = N_e \exp \left( \frac{E_f}{k_B T_0} \right) \frac{T}{T_0 \sin(\pi T / T_0)} \]  

(2.16)

With the use of equation (2.4), and \( \frac{dn}{dV_{CPD}} = q \frac{dn}{dE_f} \), an equation for the DOS is found that is similar to the one obtained previously apart from a pre factor.

\[ g(q_{CPD}(x)) = \frac{C_D}{dq} \left( \frac{dV_{GS}}{dV_{CPD}(x)} - 1 \right) T_0 \sin(\pi T / T_0) \]  

(2.17)

The equation can be further simplified; combining (2.4), (2.13) and (2.16) yields:

\[ g(q_{CPD}(x)) = \frac{C_D}{dq} (V_G - V_T - V_{CPD}) \frac{\sin(\pi T / T_0)}{\pi k_B T} \]  

(2.18)

For the second approach where an exponential DOS is chosen, a constant factor difference is found as compared to the T-zero approximation. For p-type materials where a HOMO level shifts towards the DOS, the sign of the net potential changes:

\[ p\text{-type}: V_G - V_T - V_{CPD} < 0 \]
\[ n\text{-type}: V_G - V_T - V_{CPD} > 0 \]  

(2.19)

For this reason equation (2.18) needs to be rewritten:

\[ g(q_{CPD}(x)) = \frac{C_D}{dq} \pm (V_G - V_T - V_{CPD}) \frac{\sin(\pi T / T_0)}{\pi k_B T} \]  

(2.20)

In this equation the + sign is used for n-type transistors, the – sign for p-type transistors. Data obtained by Scanning Kelvin Probe Microscopy is processed with Matlab as depicted in Appendix B.
Chapter 3: Thin layered Zinc oxide MOSFET

To avoid band bending during determination of the shape of the DOS via SKPM, a thin active layer is needed. Therefore a thin metal-oxide-field effect transistor (MOSFET) with zinc oxide as the active layer is investigated. Zinc oxide is an inorganic compound that has a polycrystalline structure. For this research, gold contacts are used for which literature values of device mobilities around 1 cm²/Vs were found[14-15]. Zinc oxide transistors are unipolar and charge is carried by electrons.

Material info and sample preparation

The used substrates consist of a heavily doped Silicon (Si++) gate electrode with 200 nm thermally grown SiO₂ acting as a gate dielectric on top. The capacitance per unit area amounts to 17nF/cm². Contacts are 100 nm thick, made of gold (Au) and 10 nm of titanium (Ti) is used as adhesion layer. The substrate is passivated with hexamethyldisilazane (HMDS).

The resulting transistor structure is shown in figure 7. Source and drain contacts are connected at the contact pads situated above (drain) and below (source). The source fingers are surrounding the drain electrodes. The channel width of the transistor is 10.000 µm and transistors with five different channel lengths are made: 5, 10, 20, 30 and 40 µm.

![Figure 7. Transistor configuration viewed from above. The finger-like structure in light green shows the pre-patterned source and drain electrodes. Contact pads are situated above (drain) and below (source). Zooming in on the source contact shows how the source fingers are surrounding the drain fingers. In dark green the gate dielectric is shown.](image)

Thin film transistors were fabricated by depositing ZnO films on top of pre-patterned source and drain electrodes by spray pyrolysis at a substrate temperature of 673 K in ambient air. The substrates were placed on a hotplate. An aerosol of a methanol solution of zinc acetate dehydrate 0.1 M, was vaporized to create a zinc oxide (ZnO) layer on the surface. The grow rate can be adapted by changing preparative conditions such as
substrate temperature and spray solution concentration. The best transistors were fabricated using a deposition rate of 0.4 nm/s.

Figure 8. Spray pyrolysis of Zinc acetate dehydrate 0.1 M on top of the substrate. The substrate is placed on a 673 K hotplate and a mask is placed above the sample. Distance between mask and sample is exaggerated for clarity.

Zinc oxide films with layer thicknesses ranging from 4 till 30 nm are fabricated. During the spray pyrolysis the contacts of the transistors are covered with the use of a shadow mask to prevent leakage current towards the edges of the substrate.

**Electrical characterization**

After the ZnO deposition, transistors were annealed in vacuum at 425 K. The samples are cooled down to 313 K after which a transfer curve and a drain sweep are measured. Transfer curves of transistors with ZnO layer thicknesses of 8 (green) and 25 nm (black) are shown in figure 9a; the source drain current is measured while the gate bias is swept from -10 till +30V and back at a source drain bias of 2V.

![Graph of transfer curve](image)

Figure 9. Transfer curve and graph of the linear mobility of ZnO for a source drain voltage of 2 V, a channel length of 5 µm and layer thicknesses of 8 (green) and 24 nm (black).
ZnO is an n-type semiconductor. For positive gate bias, charges are accumulated between the source and drain electrodes and therefore a current can flow. For negative gate biases, no current can flow since the transistor is depleted of charge carriers. The threshold voltage is around zero gate bias. The device mobility, calculated using the ideal MOSFET model, is presented in figure 9b. An increase of the mobility with increasing gate voltage is obtained. The maximum extracted device mobility of 0.7 cm$^2$/Vs is comparable to literature values [14]. The mobility is found to increase with layer thickness.

Charges are transported in the first few nanometers of the semiconductor. The remaining layer of the semiconductor does not take part in the charge transport. Therefore for layer thicknesses of 8 and 24 nanometers no significant differences in device mobility are expected. However, differences of about a factor of five are obtained. Deviations of the mobility with layer thickness could be caused by morphological differences or differences in charge injection.

Besides the dependence on layer thickness, the influence of channel length is also investigated. In figure 10 the mobility is plotted versus channel length for an 8 nm thick ZnO transistor at $V_{SD} = 2$V and for different applied gate voltages. An increase in the mobility with increasing channel length is shown while device mobility is expected to be channel length independent[3].

![Figure 10. Field-effect mobility as a function of channel length for a source drain voltage of 2V.](image)

To further investigate the layer thickness and channel length dependence of the mobility, drain sweeps were taken for different layer thicknesses as presented in figure 11. The current flowing from source to drain is measured at a gate voltage of 18 V while sweeping the drain bias from 0V till +10 V. For small source drain voltages charges are equally spread through the accumulation layer and a linear increase of current with drain voltage is expected and obtained for the thick ZnO layer of 24 nm. For high source drain potentials, a non-homogeneous charge distribution is obtained since charges close to the drain experience a different field as compared to charges close to the source. The source drain current is saturating at higher applied source drain potential. For layer thicknesses
of 8 and 16 nm the increase of $I_{SD}$ is not linear with the source drain voltage. The typical s-shaped curve is indicative for a contact resistance. The resulting s-shaped graphs become more pronounced at thinner layers; the contact resistance increases with decreasing layer thickness.

![Graph showing the relationship between drain voltage and normalized $I_{SD}$ for layers of 8, 16, and 24 nm at a gate voltage of +18V.](image)

**Figure 11.** Drain sweep of transistors with layer thicknesses of 8, 16 and 24 nm and a channel length of 5 µm measured at a gate voltage of +18V. Current values are normalized.

Drain sweeps on other ZnO transistors with layer thicknesses of 16 and 24 nanometer have been performed as well. In some cases a distinguished ‘s-shape’ indicating a significant contact resistance was also found for layers of 16 nm and even layers of 24 nm sometimes gave small contact resistances. Layers with a thickness of 24 nm never showed large contact resistances. In general contact resistance increases for decreasing layer thickness. When no strong contact resistance was shown, the mobility was independent of channel length. We attribute the variations to spray conditions.

To be able to perform density of states measurements with SKPM, as thin as possible layers are needed. More information about the DOS is obtained by electrical characterization for which the existence of a contact resistance is of an influence. Unfortunately, ZnO transistors with the thinnest layers of 8 nm suffered most from contact resistance. To further enhance our understanding of charge transport in thin layers, more research into the contact resistance in these thin active layers is performed.

**4-point probe transistor**

To quantitatively determine the contact resistance, measurements are performed on a transistor with a device architecture that is especially designed to detect the voltage drop at the contacts, for known values of $I_{SD}$, of which the contact resistance can be determined. A schematic representation of the layout of this 4-point probe transistor is shown in figure 12.

Voltage sensing probes are positioned in between the source-drain electrodes a distance of 2 µm away from source as well as drain contact. When a source drain voltage is applied, the voltage in the channel at the position of the sensing probes can be detected. The device consists of four transistors with channel lengths of 5, 10, 20 and 30 µm. These are the lengths in between the voltage sensing probes; total channel lengths are an
additional 4 µm longer (9, 14, 24 and 34 µm). The channel width of the transistors is 2000 µm.

![Figure 12. Schematic representation of a sensing probe transistor with sensing probes situated at a distance of 2µm from the contacts. Detection of the voltage at the sensing probe position will get around the contact resistance and enables determination of the voltage drop over the conducting channel.](image)

To study the influence of the voltage sensing probes on the charge transport, we take regular transfer curves of the 4-point probe transistor with floating voltage sensing probes.

![Figure 13. Transfer curve (left) and device mobility (right) of a 4-point probe transistor with a layer thickness of 8 nm measured at a source drain voltage of 2V.](image)

Figure 13 shows the transfer curve and mobility for transistors with a thickness of 8 nm measured at a source drain bias of 2V. The transfer curves show threshold voltages around zero. Apart from an increased leakage current, indicated by the relatively high current for the transistor in depletion, the transfer curve is similar to the earlier measured curve in figure 9. From the transfer curve it is observed that for shorter channel lengths more current is flowing through the transistor, but the extracted device mobility, presented in figure 13b increases with increasing channel length. Similar to what was shown in figure 10 a decrease in device mobility with decreasing channel length is shown. A mobility of almost 1 cm²/Vs is reached indicating that the 4-point probe device architecture does not significantly influence device performance.

In figure 14 the voltage on the sensing probes are given for the ZnO sensing probe transistor for channel lengths of 5 and 30 µm. A schematic representation of the transistor is shown. Below this, the plot in black, top left, shows the detected voltage at the sensing probe situated closest to the source contact for drain voltages of 2, 6 and 10 V. At zero
gate bias no charges are accumulated between source and drain. For gate potentials above zero volts, current flows through the ZnO semiconducting layer. For $V_{\text{GATE}} < V_{\text{SD}}$ the conducting channel of the transistor is pinched off near the drain electrode. The pinched off channel results in high resistance close to the drain. Therefore most of the voltage will drop over the drain contact and only a small potential drop is expected close to the source contact. This is reflected in a small contact drop close to the source contact for low gate voltages. For gate values much higher than the applied source-drain voltage, the curves are saturating, indicating that the linear regime is reached in which charges are equally spread through the conducting channel. In this linear regime no changes in voltage drops are expected and detected.

![Figure 14](image.jpg)

**Figure 14.** A schematic picture of the sensing probe transistor. Graphs with information about source contact area, channel area and drain contact area are given below this picture. Graphs of sensing probe potentials close to the source as well as to the drain contact for source-drain biases of 2, 6 and 10V (pictures a,c,d and f). In the middle, in figures b and e graphs of the difference between sensing probes are shown both for a channel length of 5 and 30 µm. The transistor used here has a thickness of 8 nm.

Figure 14c shows the detected voltage at the sensing probe situated closest to the drain contact for a channel length of 5 µm. This figure is very comparable with Figure 14a. An important difference however is that the value of voltage drop is found when subtracting the detected value from the applied source drain voltage. The small voltage for low gate voltages detected here thus indicates a large potential drop over the drain voltage for $V_{\text{GATE}} < V_{\text{SOURCE DRAIN}}$. The difference in detected potential between sensing probe near source and sensing probe near drain is shown in Figure 14 b. For gate voltages lower than
the applied source drain voltage the potential drop close to the drain is large due to the pinched off conducting channel in this voltage range. As a result of this the voltage drop over the conducting channel is small. In the linear regime at high gate values, relatively constant voltage differences of 0.7, 2 and 3.3 V are detected at $V_{\text{GATE}}=30$ V for applied source drain voltages of 2, 6 and 10V respectively.

Figure 14 d, e and f give similar characteristics but now for a sensing probe ZnO transistor with a channel length of 30 µm.

Table 1 shows the voltage drops over the different channel areas for an channel length of 5 µm and applied source-drain voltages of 2, 6 and 10 V.

<table>
<thead>
<tr>
<th>$V_{\text{GATE}} = +30$ V</th>
<th>Applied voltage</th>
<th>Detected voltage</th>
<th>$\Delta V_{\text{SOURCE}}$</th>
<th>$\Delta V_{\text{DRAIN}}$</th>
<th>$\Delta V_{\text{SENS}} = \Delta V_{\text{CHANNEL}}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Source</td>
<td>0 V</td>
<td>0.7V</td>
<td>0.7V</td>
<td>-</td>
<td>0.6V</td>
</tr>
<tr>
<td>Drain</td>
<td>2V</td>
<td>1.3V</td>
<td>-</td>
<td>0.7V</td>
<td>0.6V</td>
</tr>
<tr>
<td>Source</td>
<td>0 V</td>
<td>2.1V</td>
<td>0.7V</td>
<td>-</td>
<td>1.9V</td>
</tr>
<tr>
<td>Drain</td>
<td>6 V</td>
<td>4V</td>
<td>-</td>
<td>2V</td>
<td>1.9V</td>
</tr>
<tr>
<td>Source</td>
<td>0 V</td>
<td>3.3V</td>
<td>2.1V</td>
<td>-</td>
<td>3.2V</td>
</tr>
<tr>
<td>Drain</td>
<td>10 V</td>
<td>6.5V</td>
<td>3.3V</td>
<td>-</td>
<td>3.2V</td>
</tr>
</tbody>
</table>

Table 1. Overview of the voltage drops over different areas of the ZnO semiconducting channel of a 4-point probe transistor. $L= 5$ µm and applied source drain voltages are 2V, 6V and 10V. Information is gathered from figure 14a, b and c.

From Table 1 it is found that the voltage drops near source and drain contact are comparable. Between gold contacts and ZnO a bad energy alignment is present. A contact resistance arising from this non-ideal energy alignment between ZnO and the gold contact would create a large resistance on the injection side (source) of the conduction channel and a small resistance near the drain. This effect is not observed here and therefore it is assumed that the energy alignment is not the dominant cause for contact resistance in ZnO transistors.

In figure 15 the difference in potential between the two sensing probes for the long (green) and short (black) channel are compared by merging figure 14b and e.
From these data points an increasing potential difference with increasing channel length is demonstrated, caused by the channel length dependence of the voltage drop over the channel. For gate values lower than zero volt, $\Delta V$ increases fast. In this area the device is in depletion and the potential applied on the gate is detected by the sensing probes; this is not a relevant range for measurements on contact resistance.

A contact resistance near the source $R_{CS}$, contact resistance near the drain $R_{CD}$, and a channel resistance $R_{CH}$ can be obtained from table 1 by dividing the respective voltage drops by the source drain current. A similar set of values can be gathered from figure 15 for the transistor with $L=30 \mu m$. The resistances are calculated for the two transistors and given in Table 2.

<table>
<thead>
<tr>
<th>Resistance, $V_{SD}=2V,V_{G}=30V$</th>
<th>$L=5 \mu m$</th>
<th>$L=30 \mu m$</th>
</tr>
</thead>
<tbody>
<tr>
<td>near source, $R_{CS}$</td>
<td>0.016 M$\Omega$</td>
<td>0.033 M$\Omega$</td>
</tr>
<tr>
<td>near drain, $R_{CD}$</td>
<td>0.015 M$\Omega$</td>
<td>0.033 M$\Omega$</td>
</tr>
<tr>
<td>in channel, $R_{CH}$</td>
<td>0.015 M$\Omega$</td>
<td>0.045 M$\Omega$</td>
</tr>
</tbody>
</table>

Table 2. Resistance in the channel, near source and near drain, for ZnO transistors with channel lengths of 5 and 30 $\mu$m is given.

In figure 16 a graph of contact resistance versus gate voltage for the sensing probe transistor with layer thickness of 8 nm and channel length of 30 $\mu$m is given. Both the contact resistance of source and drain contact are shown for applied source-drain voltage of 2V, 6V and 10V.
Figure 16. Contact resistance versus applied gate voltage for a 4-point probe transistor with layer thickness of 8 nm and channel length of 30 µm. Both source and drain contact resistance are shown in MΩ at applied source-drain voltages of 2V, 6V and 10V.

Contact resistance decreases when higher gate voltages are applied. This makes sense since higher gate voltages create higher energy paths for the electrons. The higher the electron energy the easier energy barriers close to the contact or within the accumulation channel are overcome. The contact resistance is independent of channel length and applied source drain voltage in this, and other measured devices.

The current depends on contact- as well as channel resistance. Therefore figure 17a shows both the contact resistance and the resistance within the channel as a function of the applied gate voltage for a channel length of 30 µm and $V_{SD} = 2V$.

Figure 17. A comparison between channel resistance and contact resistance as a function of gate voltage (left). The channel length of the ZnO transistor on which measurements are performed is 30 µm and a source drain voltage of 2V is applied. The figure on the right shows the device mobility corrected for the contact resistances.

Channel resistance and the resistance near the contacts decrease as a function of gate voltage. However, the channel resistance has a slightly higher value. Now that a
quantitative value of channel resistance is obtained, the device mobility corrected for the effect of contact resistance can be calculated[3].

\[ R = \frac{\rho L}{Wd} \]  

\[ R = \frac{\rho L}{Wd} \]  \hspace{1cm} (3.1)

With \( \rho \) the resistivity a measure of how strong a material opposes current, \( L \) and \( W \) the length and width of the accumulation channel respectively, and \( d \) the thickness of the accumulation layer. Mobility can now be found using:

\[ \frac{1}{\rho} = \sigma = qn\mu \]  \hspace{1cm} (3.2)

With \( \sigma \) the conductivity, and:

\[ n = \frac{C_D(V_G - V_T)}{q} \]  \hspace{1cm} (3.3)

\[ \mu = \frac{L}{RC_D(V_G - V_T)W} \]  \hspace{1cm} (3.4)

This mobility is shown in figure 17b and is about 1.5 times larger as the uncorrected mobility shown in figure 13.

**A view on device performance with the use of SKPM**

The 4-point probe transistor gives a quantitative value of contact resistance. For a closer look towards charge transport in the ZnO transistor, SKPM is used.

With Scanning Kelvin Probe Microscopy in tapping mode, the potential above the surface can be detected. Samples are therefore placed in the SKPM setup where a tip scans the transistor surface. The height fluctuations of the tip result in a high resolution height profile picture of the ZnO transistor surface. Figure 18 shows an SKPM/AFM picture of the surface topography. The scanned surface is 15x15 \( \mu \text{m}^2 \). The scan height ranges from zero (brown) till 150 nm high (white). The brown area in the middle shows a transistor channel of 10 \( \mu \text{m} \) long which is surrounded by two gold contacts. The gold contacts are 100 nm high and shown in white.
A view on device performance with the use of SKPM

A second scan with SKPM measures the contact potential difference (CPD) between active layer and tip directly above the transistor surface while biases are applied. Surface potentials of a transistor with a channel length of 20 µm are detected by sweeping the gate voltage from -10V till +10 V at applied source-drain biases of 2V and 10V. Typical profiles are shown in figure 19.

![Figure 19](image)

**Figure 19. Graphs of the potential profile of the ZnO transistor measured over a 20 µm channel from source to drain. The potential profiles are obtained by SKPM technique. Potential profiles for gate voltages of -10, -7, -4, -3, 0, +4 and +10V are measured. The samples have a layer thickness of 24 nm and are measured for a source drain voltage difference of 2V (left) and 10 V (right). A schematic overview of the different resistance areas is shown top left.**

Figure 19a shows potential profiles that were taken at gate voltages of -10 V, -7V, -4V, -3V, 0V, +4 V and +10 V and are corrected for the work function difference between the ZnO active layer and the SKPM tip. On the drain contact a voltage of +2V is applied (left). The source contact is grounded (right). The potential drops in the active area of the ZnO field effect transistor. At gate voltages of +10 V, +4V and 0V, the transistor operates in the linear regime; accumulated charges are homogeneously distributed across the active channel and screen the gate potential. The step in potential close to the source
and the step in potential close to the drain are due to contact resistances. Electrons are injected into the source and are moving towards the drain. The existence of a potential drop near the contacts that is large as compared to the potential drop in the channel indicates injection limited charge transport.

At negative gate biases the ZnO transistor is in depletion and no charges are accumulated in the channel. The voltage measured with the SKPM tip thus reflects the voltage applied on the gate. As can be seen in figure 19, zero voltage is detected for an applied gate voltage of -4 volts. For this applied gate voltage no $V_{CPD}$ voltage drop can be shown within the channel indicating that no current is flowing through the channel; this is the threshold voltage of the device where charges are just accumulated in the channel. A threshold voltage of -4 V indicates the presence of positively trapped charges; the effective potential in the semiconductor for this gate voltage will be just below zero. This threshold value is confirmed by the $V_{CPD}$ voltage detected at $V_{GATE}$ = -10V; instead of a $V_{CPD}$ voltage of -10V, approximately -5 V is detected which confirms that an additional +4V of trapped charges is present.

Figure 19b shows the same ZnO transistor for a source drain voltage of +10 V. The potential profiles +10V, +4V, 0V and -3V are all measured in the saturation regime of the operating ZnO transistor. The potential drop over the channel is not linear but shows an increasing slope towards the drain due to the pinched off conduction channel. Above figure 19 the different resistances within the transistor are shown schematically. Contact resistance near the drain, $R_{CD}$, can be calculated when dividing the voltage step close to the drain by the device current. The potential drop over the channel can be divided by the transistor current to find $R_{CHANNEL}$ and $R_{CS}$ is the contact resistance due to the voltage drop near the source contact.

At the contacts, the $V_{CPD}$ potential that is measured at $V_{GATE}$ = -10V has a lower value as compared to the source and drain potentials for the other curves both in figure 19a and b. The reason for this behavior can be found in the tip of the AFM. The tip is positioned on top of the cantilever that will also be influenced by the field that is detected above the sample surface. The field detected by the cantilever will influence the potential of the tip; an offset is already present resulting in a value lower than +2V needed when measuring above the drain contact. When the potential is detected at the source, the metal plate feels the influence of the gate in an adjacent channel since our devices have a common gate. Therefore the same effect is shown at the source contact.

Several potential profiles have been measured on ZnO transistors with active layer thicknesses ranging from 6 nm up to 24 nm. Also several source drain potential differences have been used to be able to measure both in linear and saturation regime. All show an increase in potential drop near the drain and a decrease in the potential drop near the source in the saturation regime.

Measurements in the SKPM setup are performed in an ambient, dark environment and had a time span of 30 minutes up till a full day. During the determination of potential profiles, the transistors are thus exposed to oxygen and humidity which could influence
the charge transport. To determine whether or not the ZnO transistors remains stable, transfer curves are taken before, after and during SKPM measurements as is shown in figure 20.

![Figure 20](image)

**Figure 20.** Transfer curves taken for a ZnO transistor with channel length of 40 µm and layer thickness of 16 nm. Source-drain voltage is set to 2V while measuring these transfer curves. Different gate sweep ranges are used.

The ZnO transistor has a layer thickness of 16 nm and channel length of 20 µm. A source drain bias of 2V is applied. In green the transfer curve is shown that was obtained in air directly after the transistor was created. The curve has a threshold voltage around zero gate bias and a source drain current that is comparable with graphs shown earlier. After half a day in ambient environment (thus exposure to humidity as well as oxygen), device performance remained stable as shown with the black curve. The device is annealed and a gaseous nitrogen flow is blown into the SKPM setup. Then the last transfer curve of this series is measured during an SKPM measurement; this curve is shown in pink in figure 20.

During SKPM measurements stable device performance was obtained. In figure 21 four graphs are shown; device mobility, a transfer curve and the contact resistances at both source and drain for a sample with active layer thickness of 16 nm. These characteristics are obtained during an SKPM measurement, from which the detected surface potentials are shown in figure 21c, and channel lengths of 10, 20 and 40 µm are investigated. Since the contact resistance appeared to be channel length independent, one channel length, 40 µm is shown here.
Figure 21. Transfer curve (figure a), mobility (figure b) and contact resistances (figure d) for a Zinc oxide transistor with layer thickness of 16 nm are shown. The data for these curves is gathered during an SKPM measurement. Detected surface potentials are shown in figure c. A source drain voltage of 2V is applied.

Figure 21a (top left) shows a transfer curve that is obtained by sweeping the gate from -10 till +10V. The threshold voltage is zero volt. Figure 21b shows the mobility versus gate voltage. The overall mobility as well as the source drain current remained stable during the measurements; no significant decrease of transistor performance is shown. Source drain current and device mobility are similar to measurements performed earlier. Simultaneously created transistors with layer thicknesses of 8 and 24 nm give device mobilities of approximately 0.01 cm$^2$/Vs at gate voltages of +10 V which is again similar to transistor mobilities measured earlier.

Figure 21d shows the curves of contact resistance versus gate voltage for both the source and the drain contact. For the drain contact resistance at $L = 40 \mu m$, a decrease of contact resistance with increasing gate voltage is shown similar to the contact resistance detected for the voltage sensing device in figure 16. The simultaneously created transistors with layer thicknesses of 8 and 24 nm showed a similar decreasing slope for $R_{CD}$ versus gate voltage for all channel lengths. A decreasing curve of which the slope flattens more gradually represents the contact resistance near the source. The drain contact resistance falls off a little faster as compared to source contact resistance for $V_G$ between 0-2V; here the pinch off region close to the drain results in a relatively high resistance. At $V_G = 10V$
an $R_{CD}$ is found that is somewhat lower than $R_{CS}$. Some other transistors also show a lower contact resistance for drain as compared to the contact resistance near the source. Other transistors do not indicate a difference between the two contact resistances. Non-ideal energy alignment of the ZnO and gold electrodes induces an $R_{CD}$ smaller than $R_{CS}$. However, due to batch to batch differences of the ZnO no net difference between $R_{CD}$ and $R_{CS}$ is obtained indicating that this non-ideal energy alignment is not a major cause of contact resistance. No relation between contact resistance and channel length is found. Contact resistance values for a gate bias higher than 0V are ranging from 10 till 10.000 MΩ at $V_G=+10\text{V}$. The transistors with layer thicknesses of 8 nm and 24 transistors, nm give contact resistances ranging from 10.000 and 1000 MΩ at $V_G=0\text{V}$ respectively, till 10 MΩ at $V_G=+10\text{V}$ for both. The detected values are similar as compared to ZnO contact resistances in the sensing probe transistors and literature values[14].

The origin of contact resistance

Sensing probe transistor measurements as well as Scanning Kelvin Probe Microscopy indicated the presence of contact resistance within ZnO transistors. The origin of this contact resistance could be found in two features of the zinc oxide material.

To be able to perform electrical characterizations and SKPM measurements in ambient environment, air stable gold contacts are used. Bad energy alignment between the LUMO level of zinc oxide (-4.3 eV) and gold (-5 eV) is a factor that plays its part in contact resistance [14]. An energy barrier of 0.7 eV needs to be overcome to inject charges from the source contact into the conducting channel. On the other hand the enlarged gap facilitates easy charge extraction. It is expected that the contact resistance near the drain will be smaller than the contact resistance near the source in this situation. Furthermore layer thickness would not be of an influence to this effect. Layer thickness dependence is shown as well as generally symmetric contact resistances; therefore it is assumed that the non-ideal energy alignment is not the dominant factor in ZnO transistors.

Another possible reason for contact resistance can be found in the morphology of the active layer. To obtain information about the morphology of zinc oxide, figure 22 shows pictures obtained with Scanning Electron Microscopy (SEM). Figure 22a shows the transistor surface. In order to perform SEM measurements samples are diced; the edge where the gate dielectric SiO$_2$ is shown, is situated beneath the surface area (darkest grey). In the black bar information about this specific measurement is given with the white bar indicating the scale of this figure. The length of the white bar is 1 µm. The edges of the contact electrodes are rather rough. The SiO$_2$ gate dielectric is atomically flat which means that surface roughness is caused by the ZnO active layer.

A close up of the morphology in the vicinity of a contact is shown in figure 22b. The lowest layer of this cross section again shows the SiO$_2$ gate dielectric with on top of that the gold electrodes. Because of the cleaning treatments that were used when the transistor finger structures were made, the titanium adhesion layer is dissolved at the edges and an under etch is created under the gold electrodes [16].
Chapter 3: Thin layered Zinc oxide MOSFET

Figure 22. SEM picture of the ZnO transistor channels and contacts (left) and a close up near a transistor finger contact (right). The white line centered under the pictures gives the scale. In the left figure the length of the white line is 1 µm. In the right figure the length of the white line is 100 nm. In the inset in figure 36b a cross section of the contact layout is shown with the gate dielectric (dark grey) at the bottom, followed by an adhesion layer of titanium (light grey), an under etched gold electrode (light green) and the ZnO active layer (dark green).

The under etch results in the appearance of some cavities under the gold that is ‘hanging’ over and touching the SiO$_2$ at some point as is schematically depicted in the inset of figure 22b. There in light green the gold contact is shown with an exaggerated thickness of the titanium layer (light grey) and therefore an exaggerated deformation of the gold contact. The gold electrode might not be touching the SiO$_2$ everywhere. When a very thin layer of ZnO (dark green) is sprayed on top, a bad contact could easily be created.

Determination of the density of states in ZnO transistors

After research on the behavior and origin of contact resistance, research towards understanding charge transport in ZnO transistors can be extended further by extraction of the density of states. Figure 23a shows the surface potential detected with SKPM above the active channel when source and drain are grounded and the gate is swept from -37V till +17V continuously with a frequency of 1 mHz. These surface potential values are measured above one point in the active ZnO channel. Top right the starting point of the sweep is indicated. For a gate voltage of +17 V the ZnO transistor is in accumulation. Electrons in the conducting channel are screening the gate voltage and despite an offset caused by the work function difference between tip and active layer, zero voltage is detected with the SKPM tip. When gate values are swept downward, fewer charges can be accumulated within the channel and below the threshold voltage at ~22V the conducting channel is depleted of charges. The Fermi level throughout the conducting channel is kept constant by the grounded source and drain.
Figure 23. DOS measurement performed by SKPM on a 16 nm thick ZnO transistor. On the left a graph of the obtained data is shown; applied gate voltage versus voltage measured just above the surface with SKPM. On the right, the calculated density of states obtained from the data gathered in figure 23 a is shown [11]. Both the DOS calculated with equation (3.5) as well as the DOS calculated with equation (3.6) are shown. Exponential fits are applied with $T_0 = 870$ K, an offset of 0 and a number of states $N_t$ of $1E17$. The dashed lines give fits with $T_0$ values of $650$ K (lowest) and $1100$ K to indicate that an uncertainty of ± 200 K is present. Measurements are performed in a nitrogen rich ambient environment. The gate voltage is swept from -37 V till +17V continuously while scanning at 1 location with a frequency of 1 mHz.

When no charges are accumulated in the channel, the energy level of the tail of the density of states lies below the Fermi level. At a slight increase of the gate voltage the onset of charge accumulation starts which implies an upward shift of the molecular energy level. Sweeping the gate from +17V towards the threshold induces a shift of the DOS away from the Fermi level resulting in a decrease in surface potential. For gate values below the threshold the ZnO transistor is in depletion, the gate is not screened anymore and the detected surface potential drops down towards the applied gate bias.

Figure 23b shows the density of states as a function of the SKPM potential, that is obtained from the gathered data in figure 23a.. The rate with which this energy level is shifted with respect to a changing gate bias is proportional to the density of states. Two formulas have been derived in chapter 2 to calculate the DOS from obtained surface potentials. The curve in black is calculated following:

$$g(qV_{cpd}(x)) = \frac{C_D}{d_{zno} q^2} \left( \frac{dV_G}{dV_{cpd}(x)} - 1 \right) T_0 \sin(\pi T / T_0) \frac{\pi T}{\pi T}$$

(3.5)

The curve in green is calculated using:

$$g(qV_{cpd}(x)) = \frac{C_D}{dq} (V_G - V_t - V_{cpd}) \frac{\sin(\pi T / T_0)}{\pi k_B T}$$

(3.6)

In the black curve of figure 23b two regimes can be observed: In between $V_{cpd}$ values of 0 and 0.2 V the transistor is just switching on, in between 0.2 and 0.35 V more and more charges are accumulated into the semiconducting ZnO layer and an energy level shift
occurs. The green curve shows the DOS calculated using equation (3.6). Exponential fits are applied to both the black and green curve. A $T_0$ value of $870 \pm 200$ K gives the best fit for both the black and green curve.

While scanning the potential above the ZnO transistor, 250,000 data points are collected that have been averaged into 500 DOS data points. Several gate sweep frequencies have been tried. Sweep frequencies up to 50 mHz gave results comparable with the ones given above. Higher frequencies resulted in detection of a lot of noise.

Information about the density of states, about $T_0$ representing the slope of the DOS, can also be extracted out of electrical characterizations. Figure 24 shows a transfer curve measured at a temperature of 313 K. The curve is fitted with the Vissenberg & Matters model given in chapter 1. The Vissenberg & Matters (VM) model describes variable range hopping in an exponential band tail [4]. The transfer curves are plotted as a function of applied gate bias and fitted with the VM model. A $T_0$ value of $815\pm50$ K gives a proper overlap between measured and fitted values.

![Figure 24. ZnO device current in a thick (24nm) layered transistor for a source drain voltage of +2V. The gate is swept from -10V till +30 V and the measurement is performed at a temperature of 313 K. The curve is fitted with the Vissenberg & Matters model. $T_0$ is 820 K, $\alpha$ is 4.66 Å and $\sigma_0$ is $8.5\times10^7$ S/m.](image)

Two approaches towards determination of the DOS have been shown. The resulting $T_0$ values are comparable to one another. The reliability of the direct determination of the DOS through surface potential detection is therefore assumed to be accurate.

So far, benchmark measurements have been performed on a ZnO transistor; a high mobility material that can be applied as a thin film layer. Research towards a transistor with the thinnest possible active layer can now be performed. Self assembled monolayers of oligo thiophene form a self assembled layer of 3 nm thick while maintaining proper charge transport properties.
Chapter 4: DOS measurements on a SAMFET

In order to perform reliable SKPM DOS measurements, very thin active layers are needed. In chapter 3 it was shown that Zinc oxide as an active layer can be deposited on to the gate dielectric with layer thicknesses as thin as 8 nm. In these devices however, batch to batch differences were shown due to the production process, influencing reproducibility. In this chapter DOS measurements on self assembled monolayer field effect transistors (SAMFET’s) will be performed. The self assembled monolayers are grown on top of the gate dielectric with layer thicknesses of only 3 nm; a layer thickness that is comparable with the height of the accumulation layer. As such this forms the thinnest possible active layer.

Material info and sample preparation

The substrates on which SAMs are grown consist of a heavily doped Silicon gate electrode (common gate) with 200 nm thermally grown SiO₂ gate dielectric. Gold contacts of 100 nm high were mounted on top using conventional photolithographic methods and a 10 nm titanium is used as an adhesion layer. The same substrates were used in the previous chapter. There it was shown that the titanium adhesion layer at the edge of the gold electrode is dissolved. The Au electrode collapses onto the silicon dioxide surface and charge injection occurs through the gold contacts.

The core of the liquid crystalline molecules that will form the active layer is formed by quinquethiophene. The molecule is end capped with an ethyl group to enhance stability and solubility and a monochlorosilane anchoring group was attached via an undecane spacer in order to bind the molecule to the gate dielectric surface. This is shown in figure 25 middle right. The chemical structure of the self-assembling molecule, chloro[11-(5''-ethyl-2,2':5',2':5',2'-quinquethien-5-yl)-undecyl]-dimethylsilane is shown on the right of figure 25.
To induce self assembly of the molecules, the SiO$_2$ gate dielectric was activated by an oxygen plasma treatment followed by acid hydrolysis. The SAM was then formed by submerging the substrate in a dry toluene solution of the semiconducting molecule (figure 25 on the left). Full coverage of the SAM on the gate dielectric was reached after an immersion time in the solution of 15 hours. [17].

**Electrical characterization**

After full coverage of the SAM layer is reached, the transistors are brought in a $10^{-6}$ mbar vacuum environment. Electrical characterization on the SAMFET’s is then performed at room temperature, shown in figure 26. Transfer curves of transistors with channel lengths of 5, 10, 20 and 40 µm are measured while a source drain voltage of -2 V is applied. The gate voltage is swept from -25 till +5V.

Figure 26. A transfer curve for SAMFETs with different channel lengths is measured for which the gate voltage is swept from -25 till +5V and the source drain bias is -2V (left). Linear mobilities for these SAMFET’s with $V_{sd}$= -2V are given on the right.
The SAM is a hole conducting material; for positive applied gate voltages the transistor is in depletion while negative applied gate voltages induce a conducting channel. The source-drain current in the transfer curves (left) is comparable to earlier measurements[16] and threshold voltages around zero volt are found. On the right of figure 26, the mobility of the SAM transistors is shown for a source drain voltage of -2V. Mobility shows no channel length dependence.

Drain sweeps of the SAMFET for a transistor with a channel length of 5 µm at gate voltages of -20, -25 and -30 V are given in figure 27. In contrast to the ZnO transistor, no ‘s-shape’ as in figure 11 is observed. Due to the self assembling process, the active layer is in good contact with the gold electrodes; no significant contact resistance is present.

![Figure 27. The drain sweep of a SAMFET with a channel lengths of 5 µm is given. The drain voltage is swept from 0V till -20V and gate biases of -20, -25 and -30V are applied.](image)

Functional transistors are obtained with channel length independent, high mobilities. Charge transport takes place only through one layer of molecules and therefore intrinsic information about this conducting channel could be obtained from electrical characteristics.

The SAMFET is annealed at 383 K after which transfer curves are taken at temperatures ranging from 83 K up to 280 K. A source drain voltage of -2V is applied and the gate voltage is swept from +5V till 30 V and back. The transistor has a channel length of 5 µm and the transfer curves are shown in figure 28.
Chapter 4: DOS measurements on a SAMFET

Figure 28. Transfer curves of an oligothiophene SAMFET with $L = 5 \, \mu m$ at a source drain voltage of 2V. Transfer curves at temperatures ranging from 83 K till 280 K have been measured.

For decreasing temperatures the mobility of the charge carriers decreases and thus the amount of current flowing through the SAM decreases. The linear field-effect mobility versus one over temperature is calculated using the ideal MOSFET model and is shown in figure 29.

Figure 29. Mobility of an oligothiophene SAMFET as a function of 1/T. Mobility is determined at gate voltages of -15, -20, -25, -30 and -35 V.

The mobility for the SAMFET is $0.02 \, cm^2/Vs$ at room temperature which is similar to earlier measurements [16]. For lower temperatures the hole mobility decreases indicating that a hopping model can be applied to fit the transfer curves. The Vissenberg & Matters (VM) model describes variable range hopping in an exponential band tail [4]. The transfer curves are plotted as a function of applied gate bias and fitted with the VM model, shown in figure 30.
According to the VM model, the field effect current is related to $T$, $V_{\text{GATE}}$ and $T_0$, $\alpha$ and $\sigma_0$ as was shown in chapter 1.

![Graph showing the field effect current for a source drain voltage of -2V. The gate voltage is swept from +5V till -30V and measurements are done at temperatures ranging from 83 K up to 280 K. The red lines are VM fit values with $T_0$ is 500 K and $V_T$ is 2V, $\alpha$ is 1.45Å and $\sigma_0$ is $2 \times 10^8$ S/m.](image)

The best fits were obtained with a $T_0$ value of 500 K, a value that is comparable to other organic materials used in field effect transistors[6]. These fits accurately overlap with the performed transfer curves on the thiophene SAMFET for temperatures of 240K and higher. At lower temperatures a mismatch is shown especially at low gate bias.

Another well known model for the description of current voltage characteristics in thin film organic transistors is the mobility edge (ME) model. Charges in low energy states are trapped while above a certain threshold charges become delocalized. Application of this model on to the transfer curves is shown in figure 31.
Figure 31. SAMFET device current for a source drain voltage of -2V. The gate voltage is swept from +5V till -30V and measurements were done at temperatures ranging from 83 K up to 280 K. The blue lines are ME fit values with $T_0$ is 535 K and $V_T$ is -2V. Furthermore a $\mu_0$ value of 0.4 and a number of trap states of 1.45E26 are used to fit the data.

Application of the mobility edge model on the SAMFET shows fits that have a shape that is in accordance with the measured transfer curves but that do not overlap the measured current characteristics very well. Both the ME and VM model cannot satisfactorily describe the transfer curves in the SAMFET for low temperatures. More information about the density of states is needed which is obtained with the use of Scanning Kelvin Probe Microscopy.

**Determination of the DOS in a oligothiophene SAMFET with the use of SKPM**

Scanning Kelvin Probe Microscopy measurements are done to obtain information about the density of states and its shape. In chapter 2 it was shown how a DOS profile can be extracted from the contact potential difference measured between SKPM tip and semiconductor surface. Furthermore, measurements of the DOS of ZnO in chapter 3 indicated that $T_0$ values could be obtained with SKPM that are similar to $T_0$ values extracted from electrical characterization.

**Determination of the DOS in ambient environment**

The potential above the SAM surface is obtained with the use of SKPM potential measurements in dark, ambient environment. To check stability of the SAM, transfer curves have been taken before and after the SKPM measurement, shown in figure 32a.
Determination of the DOS in a oligothiophene SAMFET with the use of SKPM

Before SKPM measurements are performed in the ambient, the transfer curve shown in black is obtained. Several SKPM measurements are performed after which a second transfer curve is obtained shown in blue. Five hours of potential measurements in a dark, ambient environment, result in a small decrease in device current. The field-effect mobility is shown in figure 32b for which a decrease in device mobility of about a factor of 2 is observed. It is reasonable to assume that the performance of the device remained constant during the process of a SKPM DOS measurement which in general lasts for 10 minutes.

During the SKPM measurement, source and drain contact of the SAMFET are grounded and an oscillating sine-shaped gate voltage is applied sweeping from +11V till – 31V at different frequencies. The detected contact potential difference (CPD) as a function of applied gate voltage is shown in figure 33 for two gate voltage sweep frequencies of 50 mHz and 5 Hz. The tip is placed above the SAMFET active surface and multiple gate sweeps are performed while detecting the surface potential.

Figure 32. Transfer curves and mobilities of a thiophene SAMFET with a channel length of 10 µm and at applied source drain current of -2 V. The gate is swept from -25 till +5V.

Before SKPM measurements are performed in the ambient, the transfer curve shown in black is obtained. Several SKPM measurements are performed after which a second transfer curve is obtained shown in blue. Five hours of potential measurements in a dark, ambient environment, result in a small decrease in device current. The field-effect mobility is shown in figure 32b for which a decrease in device mobility of about a factor of 2 is observed. It is reasonable to assume that the performance of the device remained constant during the process of a SKPM DOS measurement which in general lasts for 10 minutes.

During the SKPM measurement, source and drain contact of the SAMFET are grounded and an oscillating sine-shaped gate voltage is applied sweeping from +11V till – 31V at different frequencies. The detected contact potential difference (CPD) as a function of applied gate voltage is shown in figure 33 for two gate voltage sweep frequencies of 50 mHz and 5 Hz. The tip is placed above the SAMFET active surface and multiple gate sweeps are performed while detecting the surface potential.

Figure 33. The surface potential as a function of applied gate voltage is shown for a SAMFET with a channel length of 10 µm. The gate voltage is swept oscillating from +11 V till -31 V with frequencies of 5 Hz and 50 mHz and an amplitude of 21 V. Each dot in the figure represents an averaged value of 30 subsequent data points. Figure b shows a zoom in on the surface potential.
The green curve shown in figure 33a consists of two regimes. On the right a steep upward slope is shown: in this area the transistor is in depletion. The onset of this regime indicates the threshold voltage of the SAMFET. In depletion no screening of the gate potential by charges takes place; the SKPM tip detects the applied gate voltage and a slope of 1 is expected and measured. For gate voltage values lower than +10 V, holes are accumulated in the conducting channel and screen the gate. Up from -30V to +10V a slightly increasing slope is observed indicating that the SAMFET is operating in accumulation and charges are screening the applied gate potential.

The surface potential in black was taken at a frequency of 5 Hz. For this curve, the measured slope is around 1 at +10V but slightly lower (~0.6) for \( V_{\text{GATE}} \) values in between +5 and +10V. This is assumed to be caused by a slow reaction of the transistor. Because of the high frequency of the applied gate voltage, charges just start to accumulate the channel while the gate sweep has already proceeded with its downward sweep. As a result screening is not started immediately at \( V_{\text{GATE}} = +10V \) but somewhat later around +5V. Several transistors have been investigated that showed this transition area due to the charge accumulation being slower than the gate sweep rate. Close to a gate voltage of -31V, over a small area of about 1 V a relatively high increase in surface potential with gate voltage is observed. The lowest point of the sine-shaped gate sweep is reached: the slope of the decreasing gate signal decreases but it takes a while before the accumulation rate of the transistor slows down hence an increased slope.

Figure 33b gives the same data but now zoomed in on smaller values of the detected surface potential. An increase in surface potential of which the slope decreases for higher gate voltages is observed.

![Figure 34. Calculated DOS values for SKPM measurements with oscillating gate sweeps with frequencies of 5 Hz (black) and 50 mHz (green). The DOS is calculated using equation(2.17).](image)

Figure 34 shows the density of states, calculated using equation(2.17), as a function of the detected surface potential. In black a DOS profile is shown that was calculated for a gate sweep with a frequency of 5 Hz. In green the DOS calculated for a gate sweep with a
frequency of 5 mHz is shown. Electrical characterization earlier in this chapter as well as DOS measurements on the ZnO transistor could successfully be fitted with the VM model. Therefore a monotonous exponential DOS that increases towards lower surface potential biases is expected. Figure 34 however, shows a DOS consisting of three regimes. In the green curve at $V_{CPD}<0.31$ V, for large negative gate biases (figure 33b), a decreasing DOS is shown. An exponential regime is found between 0.31 and 0.34 V while for higher surface potential values a tail is observed.

For the black curve a peak is observed around 0.36V. Surface potential values in between 0.36 and 0.39 Volts correspond to an exponential regime where gate voltages lie between -10V and +5V as can be seen in figure 33b. Similar behavior for the green curve as compared to the black curve is shown except for a shift of the peak of about 0.1 V towards the left which is assumed to be caused by a small change in the work function of the SKPM tip.

The tail that is observed in both green and black curve for $V_{CPD}>0.34$ V and 0.39 V respectively, could be caused by trapped charges. For the decreasing DOS shown at surface potentials lower than 0.31V and 0.36 V for green and black curve respectively, an explanation could be found in a slow reaction of the transistor in comparison with the rate of the gate sweep. For the gate sweep with a 10 mHz sweep frequency it takes around 100 seconds to sweep the gate from +11V till -31V; for 2 seconds one particular voltage is applied. It is unlikely that the transistor’s reaction far in accumulation is slower than this sweep rate[18]. Another explanation could be that a larger part of the DOS, instead of the tail states only, is detected when sweeping far in accumulation. This will imply a tremendous decrease in mobility since the DOS would fill up, an effect that is not observed (figure 32). More research on the DOS in far accumulation is needed.

Several surface potential measurements in ambient environment have been performed. At different frequencies and on different positions in one transistor, surface potential measurements have been performed. For high sweep frequencies the start of charge accumulation is slow compared to the sweep velocity of the gate voltage resulting in a large difference in $V_{CPD}$ between fast and slow sweeping at the onset of accumulation( as shown by the difference between the black and the green curves in figure 33a). Given the non-exponential shape of the DOS, no $T_0$ is determined.

**Determination of the density of states in vacuum**

The DOS has been calculated out of electrical characterization as well as through surface potential detection with SKPM. Electrical characterizations were performed in vacuum and SKPM surface potentials were detected in an ambient environment. To investigate the possible influence of the ambient, simultaneously to the DOS measurements in ambient environment, a start was made to perform DOS measurements on SAMFET’s in an ultra high vacuum of $p=10^{-9}$ mbar (UHV).

To be able to perform UHV DOS measurements, the transistor is placed in a sample holder and no reduction in device performance is shown when the transistor and sample holder are brought in good contact. A gate voltage is applied that is swept from +1 till -8
V. One sweep is performed per position; 25 positions within the transistor channel are probed.

Figure 35. On the left the obtained surface potential as a function of applied gate voltage is shown. In the figure on the right, the density of states in UHV is shown as obtained with (2.18)[19].

Figure 35a shows the surface potential that is detected when a gate sweep from -8 till +2V and back is performed. In green the ‘on-sweep’ from +2V towards -8 V gate voltage is shown. The blue curve represents the ‘off-sweep’. The figure is similar to figure 33a except for the ‘bump’ shown in the green curve at an effective gate voltage of 3V. The origin of this bump can be caused by a slow reaction of the transistor; charges are just accumulating the channel and mobilities are low while the gate sweep continues. Within this short ‘non equilibrium state’ charges are not able to fully screen the gate potential causing a bump. The non-zero temperature DOS approximation is used to calculate the density of states of both on and off sweeps, given in figure 35b. A fit is applied to the relevant area of this plot; in between surface potentials of -0.5 and -0.56 V the transistor goes from the onset of accumulation towards far in accumulation. The curvature towards lower surface potentials is due to the bump detected at a gate voltage of -3V and is not a relevant area for DOS determination. T_0 values of 392 K and 453 K are obtained which are in good comparison with literature values and similar to the T_0 values detected with electrical characterization[6].
Discussion and conclusions

Transistors with a ZnO active layer were produced. It was possible to perform stable measurements, both electrical as well as surface potential measurements, which showed decent transistor behavior. However, the extracted device mobility decreased with decreasing ZnO layer thickness due to the presence of a contact resistance. The contact resistance appeared to be independent of applied source and drain voltages as well as channel length. The origin of the contact resistance was found in the contact between gold electrodes and ZnO. The deformed gold contacts as a result of the under etch, combined with a spray pyrolysis application technique of the active layer resulted in improper physical contact of zinc oxide with the gold contacts. Furthermore the energy alignment between the air stable gold electrodes and ZnO is not ideal resulting in an additional injection barrier. The latter however, appears to be of minor importance in the ZnO transistors. Quantitative values of the contact resistance could be determined of $(10 \pm 5) \, \text{M}\Omega$ at an applied gate voltage of 10 V. Device mobilities, corrected for contact resistance, could be obtained that were about 1.5 times higher than uncorrected mobilities. Information about the DOS was gathered through both electrical characterization and SKPM technique. The $T_0$ values that were obtained out of the two approaches, showed very good resemblance and are comparable to literature values[6]. Due to the spray pyrolysis being performed in the ambient, spray rates fluctuated and batch to batch differences of the ZnO transistors were created. Reproducibility and device performance can be enhanced when the ZnO application technique is changed or spray pyrolysis is performed in a controlled environment. Furthermore the use of a top contact transistor structure will enlarge the contact area between ZnO and gold electrodes and therefore reduce the contact resistance.

Research towards the density of states of self assembling oligo thiophene field effect transistors gave more insight into the onset of charge accumulation. Charges were not able to speed up with the gate sweep velocity both in the area around the threshold voltage as well as at the point where the gate sweep changed in direction. Calculated DOS values look promising and applied fits point towards an exponential DOS shape. Values of the width of the DOS that were determined in vacuum, described by $T_0$, range from 135 K till 535 K, very similar values taking into account there different extraction methods and environments. More research is needed towards DOS measurements in the ambient.

More verification towards the DOS detection method as proposed by Tal et al [11] is needed. The assumption of negligible level bending for layer thicknesses smaller than 10 nm is only supported by unpublished work while other literature contradicts this[6]. Furthermore, more research needs to be done towards a possible improvement in detection of the surface potential when measurements are performed in dry nitrogen or vacuum instead of the ambient[20]. A final remark on the DOS detection method is about the calculation of the DOS from the detected surface potential. For this calculation it is assumed that the Fermi-Dirac distribution is smaller than the DOS and that the transistor operates with low charge carrier concentrations and low temperatures. Temperature dependent DOS measurements could provide us with more insight on this topic.
References

19. Roelofs, W.S.C.
Appendix A

Research towards device stability of the ZnO transistor

For ZnO transistors with different channel lengths and layer thicknesses, transfer curves have been measured before, after and during SKPM measurements. The threshold voltage of these transistors shifted towards the left after exposure to oxygen and water while annealing the devices caused a shift of threshold voltage towards the right. Performing measurements caused shifts of the threshold voltage, in general towards the right. Samples that were not annealed but placed in a nitrogen rich environment experienced a threshold voltage shift towards the right. The combined effects of nitrogen exposure and annealing created ZnO transistors that remained stable during SKPM measurements in an ambient environment.

To further investigate the device stability, figure 36a shows transfer curves of a ZnO transistor before (green) and two weeks after exposure to the ambient environment (black), with a layer thickness of 16 nm and channel lengths of 5 and 40 µm. During the measurements before a source drain voltage of 2 V is applied and the gate is swept from -30 V till +10 V and back. Measurements after exposure also have an applied source drain voltage of 2 V but here the gate was swept from -10 V till +10 V. The green curves give a current strength that is comparable with earlier measurements (see figure 9 and figure 13) with a threshold voltage around -15 V and a current value that is increasing with decreasing channel length. At gate biases below -15 V the transistor is switched off. The black curves however show lower current values and no ‘off’ region is detected. Apparently the threshold voltage is shifted towards the left by a significant amount.

Figure 36b gives the mobility of this same device before (green) and after two weeks of exposure (black). An exponential scale is used to be able to place both curves in one graph. The mobility of the green line is as expected [14] while a mobility of almost 500 times smaller is detected after the transistor has been exposed to ambient environment.

Figure 36. A transfer curve of the ZnO transistor measured before (green curves) and after exposure to light and humidity during SKPM measurements (black curves) are shown on the left. The layer thickness of this sample is 16 nm and channel lengths of 5 and 40 µm are measured. Vsd= 2V. Figure b shows the mobility of the device before and after exposure to the ambient.
As can be noted, a long period in ambient environment appears to influence the performance of the devices quit drastically. Mobilities that are measured directly after the devices are made, agree with those measured by Adamopoulos et al[14]. After exposure to a humid environment and air the mobility is reduced by a factor that depends on the time that samples are exposed to ambient environment.

Problems with decreasing device performance occurred for samples that were exposed to the ambient environment for longer than several days. Samples that were measured directly after they were produced and that were measured in a nitrogen rich environment did not show degradation problems.
Appendix B
Matlab m-files that are used to process the data obtained with SKPM are given in the two paragraphs below.

Evaluating potential profiles and determination of contact resistance

function y=plotheightandpotential()

% Measurement ZnO
% Height, potential and resistance

% User settings
nr_rij = 57;          % specify the nr of rows in the matrix it has to read in
nr_kolom = 512;        % specify the nr of columns in the matrix it has to read in
plot_crossections = true; % if ’true’ then plot crossections, if ’false’ full 2D plot
ruis=1
locatiecontact=410
close all;

%==============Generate arbitrary potentials and currents=================
Height = dlmread(file1_height.txt','',[1 1 nr_rij nr_kolom]); % read height data
Potential = dlmread(file1_potential.txt','',[1 1 nr_rij nr_kolom]); % read potential data
GateBias = dlmread('09073160sl5vdsd2.001_aux3.txt','',[1 1 nr_rij nr_kolom]);
GateBias = round(GateBias);
GateBias_eersterij = GateBias(:,1);

sdcurrent=dlmread('file2.txt','','i3..i23')
Vg_for_sdcurrent=dlmread('file2.txt','','A3..A23')
Vg_for_sdcurrent=round(Vg_for_sdcurrent);
Vg_and_Isd=[Vg_for_sdcurrent sdcurrent]

%================================Find the contacts================================
size(Potential)
Offset=[] % Potential(1,:)
if ruis==0
    for i=1:nr_rij
        Potential(i,:)=Potential(i,:)-Offset;
        smoothPotential(i,:)=smooth(smooth(Potential(i,:)));
        location_of_contact(i)=find(diff(smoothPotential(i,10:490))==max(diff(smoothPotential(i,50:80))),1, ’last’); % location_of_contact contains the indices where the derivative drop in potential is maximum in each row
    end
else
    for i=1:nr_rij
        Potential(i,:)=Potential(i,:)%-Offset;
    end
end
location_of_contact(i)=locatiecontact;
end
end
contactpunt=transpose(location_of_contact)
x0=10;
x_average=10;
x_average=2*round(x_average/2); %to assure even numbers 5->6
if x_average>=2*x0
    'You are integrating over the contact!'
end
for i=1:nr_rij
    V_left(i,1)=mean(Potential(i,(location_of_contact(i)-x0-0.5*x_average):(location_of_contact(i)-x0+0.5*x_average)));
    V_right(i,1)=mean(Potential(i,(location_of_contact(i)+x0-0.5*x_average):(location_of_contact(i)+x0+0.5*x_average)));
end
V_delta=V_left-V_right;
for i=1:nr_rij
    current(i,1) = Vg_and_Isd(find(Vg_and_Isd(:,1) == GateBias_eersterij(i)),2);
end
%now current contains a row of currents belonging to each line
contact_resistance = V_delta./current
figure(2)
plot(GateBias_eersterij,contact_resistance) %in our artificial potentials should be a 1/x (V_delta is constant, current is linear in x)
dlmwrite('contactresistance.txt',[GateBias_eersterij,contact_resistance,transpose(location_of_contact)]);

%======potential value is averaged for a particular gatevoltage======
count=1;
Potential_output=[];
GateBias_enkel=[];
for i=1:nr_rij-1
    if(count==1)
        Potential_average=Potential(i,:);
    end
    if(GateBias_eersterij(i)-GateBias_eersterij(i+1)==0 && i<nr_rij-1)
        Potential_average=Potential_average + Potential(i+1,:);
        count = count+1;
    else
        Potential_average=Potential_average/count;
        Potential_output = [Potential_output; Potential_average];
    end
Evaluating potential profiles and determination of contact resistance

Potential_average = zeros(1,nr_kolom); % returns an 1 by 'nr_kolom' matrix of zeros
count = 1;
GateBias_enkel = [GateBias_enkel GateBias_eersterij(i)];
dlmwrite('Potential_vs_Vg.txt', [GateBias_enkel; transpose(Potential_output)]);
end
end

figure('Position', [scrsz(3)/2 scrsz(4)/3 scrsz(3)/2.05 scrsz(4)/2.05])
plot(transpose(Potential_output))
set(gca,'xtick',[0:20:nr_kolom])
hold on
plot(transpose(Potential(1,:)),'LineWidth',4)
end

Processing measured surface potential and calculation of the DOS

function y=DOS()

clear all;
close all;
scrsz = get(0,'ScreenSize')

nr_rij = 50;
.nr_kolom = 500;

Potential = dlmread('fileA_potential.txt', '', [1 1 nr_rij nr_kolom]); % read potential data
GateBias = dlmread('fileA_aux3.txt', '', [1 1 nr_rij nr_kolom])

max(GateBias(1,:))

% find location first max Gatebias, find location first max potential if % equal than offset 0 if not...than determine offset
versterking = 3;
GateBias = versterking*GateBias;

Vskpm_Vg_increase=[];
Vskpm_Vg_decrease=[];
sizeGateBias=size(GateBias)
sizeGateBias(1)
sizeGateBias(2)
for i=1:(sizeGateBias(1)-1)
    for j=1:sizeGateBias(2)-1
        if GateBias(i,j)>=GateBias(i,j+1)
            Vskpm_Vg_increase=[Vskpm_Vg_increase;GateBias(i,j) Potential(i,j)];
        else
            Vskpm_Vg_decrease=[Vskpm_Vg_decrease;GateBias(i,j) Potential(i,j)];
        end
    end
end
Vskpm_Vg_decrease=[Vskpm_Vg_decrease;GateBias(i,j) Potential(i,j)];
end
end
end

%sorteren op Vg, Vg(i) bij Vskpm(i) blijven wel bij elkaar staan
Vskpm_Vg_increase_sort=sort(Vskpm_Vg_increase',2);
Vskpm_Vg_increase_sort=transpose(Vskpm_Vg_increase_sort);
Vskpm_Vg_decrease_sort=sort(Vskpm_Vg_decrease',2);
Vskpm_Vg_decrease_sort=transpose(Vskpm_Vg_decrease_sort);

sizeVskpm_Vg_increase_sort=size(Vskpm_Vg_increase_sort)
sizeVskpm_Vg_decrease_sort=size(Vskpm_Vg_decrease_sort)

%averageing over N points (N-points become 1)

N=100;
VG_dec=Vskpm_Vg_decrease_sort(:,1);
VSKPM_dec=Vskpm_Vg_decrease_sort(:,2);

averagedecVG=[]
averagedecVSKPM=[]
for i=N+1:N:sizeVskpm_Vg_decrease_sort(1)
    averagedecVG=[averagedecVG; mean(VG_dec((i-N):i))];
    averagedecVSKPM=[averagedecVSKPM; mean(VSKPM_dec((i-N):i))];
end
DOS_dec=[diff(averagedecVG)./diff(averagedecVSKPM)];
sizedecDOS=size(DOS_dec)

%same averaging for increasing gatebias
VG_inc=Vskpm_Vg_increase_sort(:,1);
VSKPM_inc=Vskpm_Vg_increase_sort(:,2);

averageincVG=[]
averageincVSKPM=[]
for i=N+1:N:sizeVskpm_Vg_decrease_sort(1)
    averageincVG=[averageincVG; mean(VG_inc((i-N):i))];
    averageincVSKPM=[averageincVSKPM; mean(VSKPM_inc((i-N):i))];
end
DOS_inc=[diff(averageincVG)./diff(averageincVSKPM)];

plot(VG_inc,VSKPM_inc)
hold on
plot(averageincVG,averageincVSKPM,'og')
hold on
plot(VG_dec,VSKPM_dec)
hold on
plot(averagedecVG,averagedecVSKPM,'ob')

sizeincDOS=size(DOS_inc)
figure('Position',[scrsz(3)/2 scrsz(4)/3 scrsz(3)/2.05 scrsz(4)/2.05])
semilogy(averagedecVSKPM(1:sizedecDOS), DOS_dec,'ob')% semilogy creates semi
logarithmic function
hold on
semilogy(averageincVSKPM(1:sizeincDOS), DOS_inc,'og')

dlmwrite('DOS_inc.txt', [averageincVSKPM(1:sizeincDOS),DOS_inc]);
dlmwrite('DOS_dec.txt', [averagedecVSKPM(1:sizedecDOS),DOS_dec]);
dlmwrite('VgVskpm_inc.txt', [averageincVG,averageincVSKPM]);
dlmwrite('VgVskpm_dec.txt', [averagedecVG,averagedecVSKPM]);
end