MASTER

Characterisation of wafer fused InP/GaAs heterojunctions

Wennekes, F.J.M.

Award date:
1997
Characterisation of Wafer Fused InP/GaAs Heterojunctions

Frank Wennekes

STOCKHOLM, NOVEMBER 1997
EEA-541

Diploma work performed at the Laboratory of Semiconductor Materials, KTH, as the graduation project for the study of Electrical Engineering at TUE.

Supervisors: Prof. dr. L.M.F. Kaufmann TUE
Dr. K. Streubel KTH
Dr. M. Hammar KTH

The Faculty of Electrical Engineering of the Eindhoven University of Technology is not responsible for the content of this report.
Acknowledgements

The work presented here concludes my studies of Electrical Engineering at the Eindhoven University of Technology (TUE), the Netherlands. This work has been carried out at the Laboratory of Semiconductor Materials, Department of Electronics, Royal Institute of Technology (KTH), Sweden.

At the first place, I would like to thank Prof. Kaufmann in Eindhoven and Prof. Gunnar Landgren in Stockholm for giving me the opportunity to realise the work in this laboratory.

The main part of this work has been concentrated in the clean room. As a new-comer, I would have been lost there without the help and patience of Janos André, Dan Haga, Lena Bäckborn, Tiina Klinga and Stefan Nilsson. Thank you for all your help and availability.

Special thanks to the "fusion guys" Jonas Bentell and Fredrik Salomonsson for introducing me in the world of fusion and for learning me the secrets of this job. Your help and our discussions were immense valuable for me.

I would like to thank my supervisors at KTH, Dr. Klaus Streubel and Dr. Mattias Hammar. Their encouragement and enthusiasm during the project were inexhaustible and it supported me during difficult phases.

Many people has been involved in performing the analysis, which complete this study. I want to thank Dietmar Keiper for determining the doping level by C-V-profiling, Stefan Rapp and Nikolae Chitica for performing the PL analysis, Dr. Joachim Piprek for analysing the I-V measurements, Dr. Margareta Linnarsson and Dr. Niclas Keskitalo for performing the SIMS analysis and Dr. Laurant Sagalowicz for performing the TEM analysis.

Frank Wennekes

Stockholm, November 1997
Abstract

The aim of this study is to investigate the suitability of InP to GaAs Wafer Fusion in optoelectronic devices. Wafer Fusion is a new technology employed in the integration of lattice mismatched materials. InP to GaAs wafer fusion has mainly been developed for the use in long wavelength (1.3 or 1.55 μm) Vertical Cavity Surface Emitting Lasers (VCSELs). At these wavelengths it is difficult to find high reflecting mirrors lattice matched to the InP based active region. To solve this problem lattice mismatched GaAs Distributed Bragg Reflectors (DBRs) are wafer fused to the active region.

The effect of the n-doping concentration on the junction resistance has been studied. Complementary measurements with Secondary Mass Spectroscopy (SIMS) to analyse the dopant distribution has been performed. SIMS has also been used to search for contaminants at the interface. The electrical measurements are fitted by a theoretical model developed by Dr. Joachim Piprek at the University of California in Santa Barbara. The effect on the electrical properties is investigated for three doping concentrations in the GaAs side, i.e. $2\times10^{17}$, $1.5\times10^{18}$ and $6\times10^{18}$ cm$^{-3}$, and two in the InP side, i.e. $9\times10^{17}$ and $6\times10^{18}$ cm$^{-3}$. No significant influence of the InP doping concentration can be observed. The electrical conductivity improves for higher doping levels in the GaAs side.

It is assumed that the optical losses of a fused interface has a minor importance in the VCSEL device. On the other hand, the heat treatment in combination with the high pressure can give a disordering in the fused structures, which can degrade the optical properties. In the second part of the study the electrical conductivity of the junction has been investigated in fusion experiments at different temperatures, in order to find a minimum fusion temperature with good electrical properties. Above 550 °C the electrical conductivity shows no significant changes. Below this temperature the conductivity degrades progressively.
The effect of fusion on the quality of the quantum wells in an active layer, designed for a double fused VCSEL, was investigated by Photoluminescence (PL) analysis. The PL intensity fluctuates over the same sample after fusion. Probably due to the fusion process or substrate etching, the quantum wells are damaged. A disordering of the quantum wells during the fusion process would give a broadening of the PL signal. This can not be noticed. Finally, a pilot process of a bottom emitting single fused VCSELs was performed.
# Table of Contents

1. INTRODUCTION .............................................................................................................................. 1
   1.1 WAFER FUSION ............................................................................................................................... 1
   1.2 LONG WAVELENGTH VCSELs ....................................................................................................... 2
   1.3 OUTLINE OF THE REPORT ........................................................................................................ 4

2. SAMPLE PREPARATION .................................................................................................................. 5
   2.1 EPITAXY ......................................................................................................................................... 5
   2.2 CHANNELS .................................................................................................................................... 6
   2.3 CLEANING AND MOUNTING ...................................................................................................... 7
   2.4 HEAT TREATMENT ...................................................................................................................... 9
   2.5 SUBSTRATE REMOVAL .................................................................................................................. 10
   2.6 MESA ETCHING ............................................................................................................................ 11
   2.7 CONTACTS .................................................................................................................................... 12

3. ANALYSIS EQUIPMENT .................................................................................................................. 15
   3.1 CURRENT VOLTAGE (I-V) ANALYSIS ............................................................................................ 15
   3.2 CAPACITANCE-VOLTAGE (C-V) PROFILING ............................................................................. 17
   3.3 SECONDARY ION MASS SPECTROSCOPY (SIMS) ...................................................................... 18
   3.4 SCANNING ELECTRON MICROSCOPY (SEM) ........................................................................... 19
   3.5 TRANSMISSION ELECTRON MICROSCOPY (TEM) ................................................................... 19
   3.6 PHOTOLUMINESCENCE (PL) ANALYSIS ..................................................................................... 19

4. EFFECT OF DOPING CONCENTRATIONS ON JUNCTION RESISTANCE .............................. 21
   4.1 INTRODUCTION ............................................................................................................................. 21
   4.2 SIMS ANALYSIS ............................................................................................................................ 22
      4.2.1 Dopant distribution after fusion ............................................................................................... 22
      4.2.2 Detection of oxides at the interface ....................................................................................... 23
      4.2.3 Detection of other contaminations at the interface ................................................................. 24
   4.3 I-V MEASUREMENTS .................................................................................................................... 27
   4.4 MODELLING .................................................................................................................................. 28
      4.4.1 Band structure and carrier transport ..................................................................................... 28
      4.4.2 Thermionic Emission Theory ................................................................................................. 30
      4.4.3 Temperature Dependence ..................................................................................................... 34
4.4.4 Interface States and Tunneling ................................................................. 36
4.5 SUMMARY ................................................................................................. 38

5. EFFECT OF THE FUSION TEMPERATURE ON JUNCTION RESISTANCE .......... 41

5.1 INTRODUCTION ......................................................................................... 41
5.2 PHYSICS OF BONDING .............................................................................. 41
5.3 PROCESS PARAMETERS ............................................................................. 42
5.4 I-V MEASUREMENTS ............................................................................... 43
5.5 TEM ANALYSIS .......................................................................................... 44
5.6 SUMMARY ................................................................................................. 46

6. WAFER FUSION FOR VCSEL DEVICES ....................................................... 47

6.1 INTRODUCTION ......................................................................................... 47
6.2 EFFECT OF FUSION ON THE QUANTUM WELLS ..................................... 47
  6.2.1 Sample Preparation ............................................................................... 47
  6.2.2 PL Results ............................................................................................ 48
6.3 VCSEL PROCESS WITH ONE FUSION STEP ONLY .................................... 52
  6.3.1 Structure ............................................................................................... 52
  6.3.2 Cleaning ................................................................................................ 53
  6.3.3 Fusion .................................................................................................... 54
  6.3.4 Mesa etching .......................................................................................... 54
6.4 RESULTS ..................................................................................................... 55
6.5 SUMMARY ................................................................................................. 56

7. CONCLUSIONS AND RECOMMENDATIONS ............................................... 59

7.1 EFFECT OF DOPING CONCENTRATION .................................................... 59
7.2 EFFECT OF FUSION TEMPERATURE ......................................................... 59
7.3 EFFECT OF FUSION ON QUANTUM WELLS ............................................. 60

APPENDIX A WAFER FUSION RUNS ................................................................. 63

APPENDIX B REFERENCES ............................................................................... 65
1. Introduction

1.1 Wafer Fusion

Heterojunctions between different semiconductor materials play an important role in optoelectronics. For semiconductors with the same lattice constant, i.e. lattice-matched systems, such junctions can be readily fabricated by epitaxial growth techniques such as Metal Organic Vapour Phase Epitaxy (MOVPE) and Molecular Beam Epitaxy (MBE). However, for semiconductors of different lattice parameters the situation is more difficult. The problem is that the strained overlayer beyond a critical thickness, as predicted by interface thermodynamic [1], will relax by the introduction of misfit dislocations and result in a high density of threading arms propagating through the epitaxial film. These threading dislocations adversely affect the electrical and optical properties, making the material unsuitable for device purposes.

Mating mismatched epilayers that are already in the solid phase, provides a promising alternative to epitaxial growth. This is called wafer bonding. In wafer bonding, epitaxial layers are grown on a lattice-matched substrate and then grafted onto a mismatched substrate. The field of wafer bonding can be divided into five techniques: Silicon direct bonding, low temperature Si₃N₄ bonding, interfacial metal bonding, epitaxial lift-off and wafer fusion [2].

Wafer fusion, or Bonding by Atomic Rearrangement (BAR), is the most suitable technique for making optoelectronic devices with lattice mismatched materials [3,4]. In contrast to the other bonding techniques, no foreign materials at the interface are required for bonding to occur. The wafers are joined by stable covalent bonds between the atoms on either side of the interface. Except for a square net of edge type misfit dislocations, the fused interface is most similar to a conventionally grown lattice-matched heterointerface and therefore the electrical and optical quality will be high.
compared to other bonding techniques. Wafer fusion enables the fabrication of novel devices such as wafer fused Vertical Cavity Surface Emitting lasers (VCSELs) [5], silicon heterointerface photodetectors [6], resonant cavity photodetectors [7] or transparent substrate light emitting diodes [8].

1.2 Long Wavelength VCSELs

InP to GaAs wafer fusion has been developed mainly for the use in long wavelength Vertical Cavity Surface Emitting Lasers (VCSELs). These VCSELs can be applied in the telecommunications industry as it provide lasers emitting at the wavelengths of 1.3 or 1.55 µm, which correspond to zero dispersion and minimum absorption in monomode silica fibres respectively. For long wavelength applications the current choice of active material is InP based Quantum Wells (QWs). These wells are made by growing \( \text{In}_x\text{Ga}_{1-x}\text{As}_y\text{P}_{1-y} \) layers of different compositions on InP substrates. The thin active region in a VCSEL increases the demands on the mirror reflectivity of more than 99%. This can be achieved by the introduction of a Distributed Bragg Reflector (DBR), i.e. a multi-stack of quarter wavelength layers with alternating refractive indices. The most promising DBR material system for long wavelength VCSEL applications is that of GaAs/Al(Ga)As. Up to now, the most successful 1.55 µm VCSEL has been developed at the University of California in Santa Barbara (UCSB) using wafer fusion [9]. Figure 1.1 depicts their structure, which requires two wafer fusions. The GaAs-based top and bottom mirrors are fused to the InP-based laser cavity on both the p and the n side.
To optimise this double fused VCSEL, the fused junctions between GaAs and InP need to be understood. Recently at KTH, Salomonsson investigated the interface of wafer fusion between p-doped InP and GaAs, which corresponds to the top fused interface of a double-fused VCSEL [10]. The present work concentrates on the fused junction between n-doped InP and GaAs.

Since wafer fusion is a new technique, further investigation is needed to fully understand the physics involved. Up to now the role of doping concentration as well as other fusion parameters are not fully understood or have not been examined. This work can be seen as a continuation of Salomonsson's work on the influence of the doping concentration but it also contains an investigation of another fusion parameter: the temperature.
Important requirements on the fused interface are high conductivity for electrical pumping of the active region and low absorption and scattering of light in the desired wavelength. A poor electrical conductivity is believed to be the main problem. The major part of this work is to characterise the junction with respect to the electrical conductivity. The results are then discussed with respect to Secondary Ion Mass Spectroscopy (SIMS) and Transmission Electron Microscopy (TEM) analysis and current transport simulations.

1.3 Outline of the Report

In chapter 2, a detailed description of the fusion process is given. The sample preparation prior to fusion as well as the preparation for the current voltage (I-V) analysing are explained. Preparation and cleaning steps of the samples to be fused are discussed. After the fusion the mesas and contact rings are processed to perform the I-V-measurements. This work was carried out in the clean room of the semiconductor laboratory at KTH.

General explanations of the measurement equipments and principles used in this study are presented in chapter 3. This is essential for a correct interpretation of the data.

Chapter 4 includes all the results and discussions concerning the effect of the doping concentration on the fused junction. The junction resistance is discussed and theoretical models are introduced in order to create a better understanding of the experiments.

The effect of fusion temperature on the junction resistance is the subject of chapter 5. I-V-measurements indicate the quality of the fused junction. Especially lower fusion temperatures have been investigated to find a minimum temperature which gives good electrical properties.

Chapter 6 deals with the effect of the heat treatment on the quantum wells in an active layer intended for VCSELs. Finally a pilot process of a bottom emitting single fused VCSEL is presented.
2. Sample Preparation

2.1 Epitaxy

The GaAs and InP-based materials, used in this study, are grown by low pressure MOVPE systems at the Semiconductor Laboratory (HLB) at KTH. MOVPE uses metal-organic precursors for the group-III elements and hydrides precursors for the group-V elements and the n-doping, i.e. trimethylgallium for Ga, trimethylaluminium for Al, trimethylindium for In, arsine for As, phosphine for P and silane for Si. Monocrystalline layers are grown from the vapour phase on the substrate. The chemical reaction takes place at 700 °C for the GaAs wafers and 680 °C for the InP based wafers. The n-doping of both materials is achieved with silicon doping. All samples are grown on [001] oriented substrates. The InP structures contain two In_{0.47}Ga_{0.53}As etch top layers (figure 2.1). The need for two etch stop layers will be explained in section 2.5.

![Figure 2.1 Schematic diagram of the wafer structures](image)

The growth takes place on 2” wafers, which are subsequently cleaved along the [110] and [1 $\overline{1}$0] axes to 12 mm x10 mm sized pieces. The rectangular shape is important to
keep track of the crystallographic orientation of the sample. The influence of the orientation on the electrical conductivity is not clear\(^1\). To avoid any influence from the orientation, all fusions in this work are performed with the same orientation.

### 2.2 Channels

To improve the fusion results, it has been found necessary to etch channels into one of the surfaces. These channels are thought of as a means for desorbing molecules to leave the interface during the heat treatment. Therefore, it is important that the channels continue all the way to the edge of the sample. If the gases can not escape they may cause bubbles in the epitaxial fused layer. Fusion without channels result in cracking of the samples. The reason for these cracks is not clear but one explanation could be that the expansion of the enclosed gasses will locally give high pressures which cause cracking. Another explanation may be that the channels relax the strain which occurs after the heat treatment due to the difference in thermal expansion of the two semiconductors.

![Figure 2.2 Schematic diagram of the InP-wafer after channel etching](image)

1 Okuno et al. compared anti-phase with in-phase direct bonding. Anti-phase bonding means bonding in which the lattice orientations for both samples are parallel. For in-phase bonding the samples have a 90° misalignment compared to the anti-phase. First Okuno et al. [11] claimed that there is a difference in electrical and optical properties between the two orientations. Later in [12] a difference in properties of the two orientations is dismissed. However for another interface between zinc blend structures, fused GaInP/GaP, the difference between in phase and anti-phase alignment is significant [13].
The channels are etched into the InP surface with a HCl : H₃PO₄ : CH₃COOH 1:1:2 solution with a very high selectivity against the InGaAs etch stop layer. A photoresist mask with channels in one dimension with a pitch of 150 µm is used. The groove width of the mask was about 3 µm. The resulting channels have a width of 10 µm and a depth of 300 nm. Figure 2.3 shows a Scanning Electron Microscopy (SEM, see chapter 3) picture of a cleaved test sample of a fused InP (top)/GaAs (bottom) interface. The cleaving is perpendicular to the channels which are represented by the little dark horizontal stripes at the interface. This InP wafer contains no InGaAs etch stop layer. The terraced InP surface (vertical stripes) can be explained by the small rotated misalignment, i.e. twist, during the mounting of the wafers before fusion.

![Figure 2.3 SEM picture of a cross section of a fused InP/GaAs interface perpendicular to the channels.](image)

The pitch between the channels is 150µm.

### 2.3 Cleaning and Mounting

Prior to bonding, the two surfaces have to be properly cleaned. This cleaning procedure can be divided in several steps. Both InP and GaAs samples undergo exactly the same procedure. First the samples are placed in respectively acetone and boiling trichloroethylene. Afterwards the remaining photoresist and other unwanted hydrocarbons are removed during an ashing treatment in a low power oxygen plasma
etcher for one hour. After ashing for such a long time an oxide layer on top of the surfaces has been formed. After the ashing process the samples are placed in water and not exposed to air before the mounting.

The oxide layer is removed by placing the samples in a solution of hydrofluoric and hydrochloric acid, $\text{H}_2\text{O} : \text{HF} : \text{HCl} \ 20:1:5$ at room temperature for 15 minutes. After rinsing with water, the samples are placed in a 25% ammonia solution ($\text{NH}_4\text{OH}$). In this liquid the samples are mated together, aligned and slightly pressed with a pair of tweezers. Another possibility is to perform the mating of the surfaces dry. The advantage of that method over the wet mating is that there are no liquids trapped between the surfaces during the fusion. However, this still does not eliminate the problem of the adsorbates at the surface which desorb only at elevated temperatures during fusion. Besides, the disadvantage is that oxygen in the air easily reacts with oxide-free surfaces. Therefore it might be necessary to perform the mating in an inert atmosphere. Because of the good experience in the past, the former method of wet mating was chosen.

A fixture, depicted in figure 2.4, is used to press the pieces together during the heat treatment. This fixture consists of a massive stainless steel base, two similar elastic top plates and a soft graphite dome, which distribute the pressure uniformly. The fused samples are sandwiched between two silicon pieces.

![Figure 2.4 Schematic outline of the fusion fixture](image-url)
The top plate is screwed on the base with three screws, two screws on one side and one on the other side. The pair of screws is fixed and the solitary screw is tightened with a torque wrench to regulate the pressure. A torque-pressure calibration curve has been made using a piezoelectric force sensor. In this study a pressure of roughly $2.5 \times 10^6$ Pa at room temperature is applied. The pressure was found to be very important. Too low pressures will result in a poor bonding, while too high pressures will increase the risk of sample cracking. The most suitable pressure at room temperature was empirically determined. The actual pressure during the heat treatment is not known.

### 2.4 Heat Treatment

The fixture is loaded into a converted LPE furnace, which is pumped down to 50 mbar is created and thereafter filled with hydrogen. This action is repeated several times to create a proper inert H$_2$ ambient gas. Under continuous hydrogen flow the furnace is heated to the fusion temperature, usually 655 °C except in the experiments in chapter 5. This takes roughly 30 minutes. Subsequently it is kept at the same temperature for an additional 30 minutes. The cooling down procedure lasts for six hours after which the fixture can be dismounted and the fusion process is finished (figure 2.5).

Figure 2.5 Schematic diagram of the InP/GaAs sample after fusion
2.5 Substrate Removal

To examine the fused interface the InP substrate and the first etch stop layer are removed. This is done in two steps. First the InP is removed by leaving the sample in HCl : H₂O 3:1 solution for about 35 minutes (T=20 °C). Since the HCl etches InP rather violently, the surface is roughened during the etching. The high selectivity against InGaAs retrieves the smoothness. 

Finally, the etch stop layer is removed using a H₃PO₄ : H₂O₂ : H₂O 1:8:40 solution in 60 seconds at room temperature. The end of the etching can be noticed by the difference in reflection of InGaAs and InP. The ternary compound gives a more yellowish reflection compared to the bright InP.

![Diagram](image-url)

Figure 2.6 Schematic diagram of the sample after removing of the InP substrate and an etch stop layer

In the beginning of this study, InP wafers were grown with just one etch stop layer, with the aim of using this layer as etch stop for etching the channels from one direction and etching the substrate from the other side. Unfortunately this layer turned out to be too thin, which causes it to collapse above the channels during substrate removal. This resulted in an unacceptable underetch from the collapsed channels, which destroyed the fused InP layer, before all the substrate had been removed. Later on the deposited contacts would short-circuit the fused interface. Figure 2.7 is a plan view image of a fused sample with one etch stop layer that shows this situation. On the right side, the collapsed channels with the underetch (top), and the substrate mountains (bottom) are visible. After this experience I decided to continue the study
with a structure with two etch stop layers, which is the same structure as used for the p-p-studies in our lab.

Figure 2.7 Plan view picture of a fused sample after substrate removal with collapsed channels due to a too thin top layer.

### 2.6 Mesa Etching

The circular mesas with a diameter of 280 μm are dry etched by a Reactive Ion Etching (RIE) with a CH$_4$:H$_2$:Ar = 35:7:2 chemistry. In this process a simple photoresist mask is not sufficient. Therefore a silicon-nitride (Si$_3$N$_4$) layer of 145 nm is deposited on the sample in a Plasma Enhanced Chemical Vapour Deposition (PECVD) system at 300°C in 24 minutes. A photoresist mask with the circular dots protects the silicon nitride during the plasma etching to create an identical mask of silicon-nitride. The plasma etching of the silicon nitride is executed with CF$_4$ at a pressure of 66 Pa and RF power of 100W for 75 seconds. After removing the photoresist the mesas can be etched. The etch rate of the RIE is 33 nm/min for InP and 14 nm/min for InGaAs. Thus the critical etching time is 45 minutes for 0.8 μm InP and 0.3μm InGaAs. To be sure to etch through the fused film, the samples are etched for 65 minutes. The resulting height of the mesas is about 1.4 μm.
During the etching the sample becomes covered with polymers. These can be removed by another ashing treatment of one hour. Figure 2.9a depicts a mesa before the ashing treatment. Particularly on top of the mesa, the polymers are visible, i.e. the dark region. Figure 2.9b shows the same mesa at a higher magnification. A channel can been seen within the mesa. This proofs that etching was sufficiently deep. A print of the channels is visible in the GaAs substrate. Finally the silicon-nitride on top of the mesas is removed by etching in hydrofluoric acid (HF) for a few seconds.

Figure 2.9 SEM picture of the side wall of the mesa that shows the channels within the mesa.

2.7 Contacts

After etching, metal contacts are deposited. They consist of four concentric rings per mesa to enable four points measurements, cf. chapter 3. Two rings are placed on top of the InP mesa and two rings are placed on the GaAs substrate.
The contacts are made using a lift-off technique. A mask of negative photoresist is used, which can have negative slopes at the edges of the photoresist in order to facilitate the lift-off of the metal. An AuGe/Ni/Ti/Pt/Au film is deposited by electron beam evaporation. The resist, with the metal on top, is removed in acetone, see figure 2.11. The contacts are alloyed by a Rapid Thermal Processing (RTP) for 30 seconds at 430 °C.
3. Analysis Equipment

3.1 Current Voltage (I-V) Analysis

The test structure for I-V-analysis enables four points measurements. In this way the contacts for the current injection and voltage measuring are separated. This is necessary in order to exclude the voltage drop over the contact. Since the current through the contacts for the voltage measurement probes is small, the voltage drop over these contacts can be neglected. In this way only the voltage drop over the semiconductor is measured.

During the measurements the current flows from the middle contact on top of the mesa to the outer ring at the substrate. The voltage is measured between the outer ring on top of the mesa and the inner substrate ring. This design has been chosen to achieve a uniform current density over the fused junction and to measure the voltage as close to this interface as possible.

Figure 3.1 shows the results of I-V measurements to determine the voltages over the contacts. These measurements have also been done with a four point method. The current flows in the way as described above but the voltage is measured between the contacts at the same side of the fused junction. Assuming there is no voltage drop over the sense pad, only the voltage across the current contact is measured.
The solid line without squares shows the voltage between two contacts on top of one InP-mesa and the solid line with the squares gives the voltage between the two contact rings around a mesa on the GaAs substrate. The lines are straight, which implies ohmic contacts in this current range. The total resistance is 0.93\,\Omega \text{ respectively 0.77}\,\Omega for the top and bottom contacts. The resistivity can be calculated by multiplying these values by the area of the contact pads. The resistivity is \(73\times10^{-6} \, \Omega\text{cm}^2\) respectively \(448\times10^{-6} \, \Omega\text{cm}^2\) for the top and bottom contact. Transmission Line Measurement (TLM) is a better way for extracting the contact resistance but has not been performed in this study. The contact resistances have a minor influence in the results since a four points method is used.
A set-up depicted in figure 3.2 was built to measure the current voltage characteristics of the fused interfaces. The samples are placed on a copper block including a thermocouple. With a peltier element the temperature can be kept at a given temperature. For measurements at lower temperatures, the copper block is placed on top of a container filled with liquid nitrogen. The temperature can be varied between $T=130K$ and $T=400K$. During measurements in a given temperature range the samples are glued with silicon paste to create a better thermal conductivity.

### 3.2 Capacitance-Voltage (C-V) Profiling

The doping levels of the epitaxial layers are measured using a Polaron C-V (Capacitance-Voltage) profiler before the fusions. C-V profiling is a method for obtaining electrically active carrier concentration profiles. The sample is contacted with a defined area of an electrolyte. A biasing voltage is applied across the semiconductor/electrolyte interface. This is basically a Schottky contact, and the majority carrier concentration at the end of the depletion region is obtained by a detailed analysis of the voltage depending of the capacitance. A depth profile of the concentration is obtained through a electrochemical etching of the sample. Table 3.1 summarises the doping concentration at the surface of the samples used in this study.
Table 3.1 N-type doping concentration at the interface layers before fusion

<table>
<thead>
<tr>
<th>Material</th>
<th>Wafer no</th>
<th>concentration (cm$^{-3}$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>InP</td>
<td>20464 A/B</td>
<td>9x10$^{17}$</td>
</tr>
<tr>
<td>InP</td>
<td>20465 A/B</td>
<td>6x10$^{18}$</td>
</tr>
<tr>
<td>GaAs</td>
<td>1072</td>
<td>2x10$^{17}$</td>
</tr>
<tr>
<td>GaAs</td>
<td>1074</td>
<td>1.5x10$^{18}$</td>
</tr>
<tr>
<td>GaAs</td>
<td>1078</td>
<td>6x10$^{18}$</td>
</tr>
<tr>
<td>GaAs</td>
<td>1111</td>
<td>6x10$^{18}$</td>
</tr>
</tbody>
</table>

### 3.3 Secondary Ion Mass Spectroscopy (SIMS)

In order to obtain more information on the chemical nature of the wafer fused interface, some samples were characterised by Secondary Ion Mass Spectroscopy (SIMS). In this technique the surface is sputtered down with a high energy ion-beam with a sputter rate of roughly 200 nm/min. The energy of the bombarding ions, here oxygen or cesium, ionises some of the sputtered atoms, creating so called secondary ions. The secondary ions are analysed using a mass spectrometer. The spectrometer is set for the desired atomic mass and the detection is monitored as a function of time to produce a depth profile for the chosen element.

The depth resolution and accuracy decrease with the depth because of uneven sputtering, crater edge and memory effects. In these cases ions are detected at a certain time, which do not correspond with the related sputtering zone resulting in a broadening of the signal.

In this analysis, cesium is used as bombarding ion to search for carbon, oxygen silicon and arsenic, while oxygen is used for phosphorus, iron and again silicon and arsenic. During one sputtering, with one kind of primary ion, the spectrometer was set to detect all the desired ions serially. The arsenic and phosphorus has been detected in order to calibrate the sputtering depth. Therefore the thickness of the layers are taken for granted. The quantitative analysis of the concentrations requires calibration runs.
with a standard specimen with known concentrations. Under the assumption that the detected ions per seconds are proportional to the concentration, such a calibration can be made. The SIMS analysis are performed within the laboratory of Solid State Electronics (FTE) at KTH.

3.4 Scanning Electron Microscopy (SEM)

For high resolution studies of the surface morphology Scanning Electron Microscopy (SEM) was used. This technique provides an illusionary three-dimensional view of the sample with a resolution which can be less than 10 nm. The sample is placed in vacuum and scanned by a focused electron beam (acceleration voltage \(\approx 20 \text{ keV}\)). Most of the electrons are absorbed by the material, followed by the emission of secondary electrons. The remaining non-absorbed electrons are backscattered by the surface. The signal of the detected electrons is represented at a cathode ray tube.

3.5 Transmission Electron Microscopy (TEM)

Transmission electron microscopy (TEM) can be used to obtain detailed and direct information about crystalline imperfections; a higher resolution can be reached than with SEM. After acceleration in an electric field (\(\approx 300 \text{ keV}\)), the electron beam is focused to a sample which is so thin that the main part of the electrons can be transmitted. After the passage of the sample, local intensity variation in the electron beam, caused by interaction with electrons in the sample, can be observed. The principle of this microscopy is related to a slide projector.

TEM is a time-consuming and difficult technique, both in sample preparation and image analysis. On the other hand the resolution is very high, in the order of 2-5Å. In this study the TEM analysis were executed by Dr. Laurent Sagalowicz at the École Polytechnique Fédérale de Lausanne (EPFL).

3.6 Photoluminescence (PL) Analysis

The quality of quantum wells in the active layer can be investigated by photoluminescence (PL) analysis. For most of the semiconductors and especially III-
V semiconductors with direct energy bands, the recombination of electron hole pairs is joined by the emission of light. The principal of luminescence measurements is to excite carriers to a higher energy level, and to detect the photon emission afterwards.

Here, the sample with the active layer is excited by a laser with a larger photon energy than the bandgap of the material. Because of the absorption of the photon, an electron-hole pair is created. After the generation, the recombination of the pair can result in the emission of a photon. The energy of the photon corresponds to the energy of the bandgap. The spectra of the emitted light give useful information about the quantum wells. A narrow line width emission, i.e., the photons contain mainly the same energy, indicates high quality wells. In this study a PL analysis of the active layer is performed before and after fusion to investigate the optical losses of the quantum wells during the process.
4. Effect of Doping Concentrations on Junction Resistance

4.1 Introduction

The aim of the first part of this study is to investigate the electrical conductivity of the fused interface between differently n-doped InP and GaAs. For this purpose, samples with different doping levels close to the interface layers are grown by MOVPE, see Table 4.1.

Table 4.1 Doping concentration of the epitaxial samples used in this study.

<table>
<thead>
<tr>
<th>Wafer #</th>
<th>Material</th>
<th>n-doping concentration (cm$^{-3}$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1072</td>
<td>GaAs</td>
<td>2x10$^{17}$</td>
</tr>
<tr>
<td>M1074</td>
<td>GaAs</td>
<td>1.5x10$^{18}$</td>
</tr>
<tr>
<td>M1078</td>
<td>GaAs</td>
<td>6x10$^{18}$</td>
</tr>
<tr>
<td>M1111</td>
<td>GaAs</td>
<td>6x10$^{18}$</td>
</tr>
<tr>
<td>20464 A &amp; B</td>
<td>InP</td>
<td>9x10$^{17}$</td>
</tr>
<tr>
<td>20465 A &amp; B</td>
<td>InP</td>
<td>6x10$^{18}$</td>
</tr>
</tbody>
</table>

As a starting point, doping and impurity concentrations of the fused samples as deduced by SIMS are presented. After that the I-V-curves are discussed and finally different simulation models are introduced to fit the I-V-results in order to extract physical parameters.
4.2 SIMS Analysis

After fusion, samples were sent for SIMS analysis to investigate the distribution of the dopant and other impurity concentrations at the fused interface. These results might be of importance to understand the electrical conductivity of the heterojunctions.

4.2.1 Dopant distribution after fusion

The InP-side as well as the GaAs-side are doped with silicon. The concentration of this dopant as a function of the depth is given in figure 4.1. The figure shows the calibrated silicon concentration. The uncalibrated arsenic signal is included in order to calibrate the sputtering depth.

![SIMS measurement of silicon concentration](image)

Figure 4.1 SIMS measurement of silicon concentration

The analysed sample N10, (see appendix A for data), has a doping concentration of $6 \times 10^{18}$ cm$^{-3}$ for the InP and GaAs layers closest to the fused interface, which
corresponds well with the C-V-analysis. The aim of the analysis was not the confirmation of the level of the doping concentration but to study whether the dopant has diffused during the heat treatment. No significant shifting of the silicon to the interface is perceptible, which corresponds to the literature [14]. The significant As concentration in the InP layers is probably due to the arsine which is still present in the epitaxy chamber after closing the precursor.

4.2.2 Detection of oxides at the interface

A next phenomenon that can may effect the conductivity is the presence of oxides at the interface. In the past, TEM pictures of samples fused by other groups have shown a 5-15Å thick amorphous layer between the two semiconductors, probably consisting of some oxide. A perfect crystalline interface without any intermediate layer has also been reported [15]. Since the samples with a perfect crystalline interface show much better electrical conductivity than those with an amorphous layer, the oxide seems to be detrimental. Therefore it interesting to know how much oxygen is present at the interface. Figure 4.2 shows the SIMS results for oxygen of one sample.
Considering the oxygen peak at the fused interface, it must be noted that the depth resolution of the SIMS technique is not sufficient to deduce a specific oxygen concentration at a specific position. Instead the concentration is integrated over an interval close to the interface, yielding a surface concentration of $2.8 \times 10^{14}$ cm$^{-2}$.

The lattice atoms of InP and GaAs have surface concentrations of respectively $5.8 \times 10^{14}$ cm$^{-2}$, and $6.3 \times 10^{14}$ cm$^{-2}$ in the (100) plane, which is more than twice as much as the oxygen surface concentration. Noting that the oxygen atom is smaller than the semiconductor atoms, it is unlikely that there is any homogenous oxide film of more than one atomic layer at the interface. The cleaning procedure before the fusion seems to be sufficient to remove most of the native oxides.

### 4.2.3 Detection of other contaminations at the interface

Apart from the analysis of the dopant and the oxygen, we also investigated other elements. During the studies of the p-p fusion [10] the GaAs side was doped with
carbon. The SIMS analysis of the carbon concentration showed a increased level close to the interface. Taking into account the low diffusion rate of carbon in GaAs [14], this is somewhat unexpected. Instead of diffusion from the substrate, it is possible that the carbon atoms come from somewhere else and take place at the interface before or during the fusion. In that case the analysis of the present samples, which do not contain carbon, should show a carbon concentration at the fused interface too. This is indeed confirmed in the SIMS curve of figure 4.3. No significant differences of the contamination concentration can be noticed between measurements close or far from channels.

![SIMS measurements of carbon concentration](image)

Figure 4.3 SIMS measurements of carbon concentration

The carbon concentration is negligibly small within the layers but contains a big spike at the fused interface of $8 \times 10^{18}$ cm$^{-3}$. Again the absolute value of the volume concentration is not reliable because of the inaccuracy of the sputtering depth. The same calculations as for the oxygen concentration can be made to find the surface concentration, which yields $5.6 \times 10^{13}$ cm$^{-2}$.  

This concentration is high and its influence can be important. Carbon is a common p-dopant for the epitaxial grow of GaAs, which could neutralise the n doping and decrease the electrical conductivity of the junction. On the other hand, it is not known if the carbon takes place at the group V atoms in the semiconductor as it does when used as p dopant. In InP, carbon is not a p-type dopant.

The origin of the carbon contamination might be due to the stainless steel fixture and screws, which are used for the fusion runs. An inspection of the glass pipe of the former LPE furnace, shows that the atmosphere is not as clean as we want; the glass had been contaminated during the fusion processing. The carbon in the chemicals, used for the cleaning, might be another explanation. If the contamination is due to the fixture it is also worthwhile to examine other contaminants, which could be expected. Figure 4.4 depicts the result of the SIMS analysis for iron, which shows a similar profile as for carbon.

Figure 4.4 SIMS measurement of the iron concentration

The volume peak concentration of $9 \times 10^{17} \text{ cm}^{-3}$ and a calculated surface concentration of $1.5 \times 10^{12} \text{ cm}^{-2}$ are less then the carbon concentrations but still significant. Again the
exact place of the impurity atoms in the lattice is not known, so it is difficult to estimate what kind of influence the iron will have for the electrical conductivity of the junction. It is noted, however, that iron is a well-known deep-level acceptor type dopant in InP inducing semi-insulating properties.

The purpose of fusion is to make high quality interfaces between (lattice mismatched) materials. Therefore any kind of contaminations at the fused interface, even if they would increase the electrical conductivity, are unwanted.

4.3 I-V Measurements

The influence of the doping concentration in the semiconductors on the electrical properties is studied by current-voltage measurements. The measurements show some fluctuations in the current voltage characteristics over the same sample and between different runs of identical wafers. However a systematic trend between the different doping levels can be seen.

The current voltage characteristics at room temperature of the six different combinations of the doping concentrations are shown in figure 4.5. For forward bias, the InP is biased positive with respect to the GaAs. A remarkable trend is observed; it seems that the doping level of the InP in this range has a small effect on the electrical properties. The curves with identical doping concentration in the GaAs samples are very similar. They have the shape of a general isotype heterojunction with exponential slopes in the positive as well as the negative direction. In case of the highest doping concentration in the GaAs the curves look almost linear. The largest differences in the conductivity is seen for negative voltages. The maximum voltage over the junction in this current range is roughly between 3.5V and 75mV. For a double fused VCSEL, the InP in the n-doped junction has a positive bias, so in figure 4.5 positive voltages are the most interesting for that application. For the highest GaAs doping concentration the voltage is 30mV at a current density of 325 A/cm² and even for the lowest doping concentration the voltage drop is still under 400mV.
4.4 Modelling

In this section different theoretical models for fitting the measurements are discussed. First a general discussion of the energy band and carrier transport is presented. A simple model using the thermionic emission theory is introduced to extract the parameters of the model and to compare the results with other groups. Finally a weakness of the model is demonstrated by a comparison to I-V-measurements at lower temperatures, and the model is expanded considering the tunneling and interface states. With this more advanced model the I-V results are well fitted.

4.4.1 Band structure and carrier transport

To calculate the current transport, the band structure close to the interface must be known. A heterojunction in general is defined as a junction formed between two dissimilar semiconductors, such as InP and GaAs, with different energy bands. Important band structure properties are: electron affinity $\chi$ (energy between vacuum level $E_0$ and conduction band $E_c$), ionisation potential $\phi$ (energy between vacuum level $E_0$ and the vacuum level of another material) and bandgap $E_g$ (energy difference between the valence band maximum and the conduction band minimum).
level and valence band $E_v$) and bandgap $E_g$ (energy between conduction band and valence band). These parameters are listed for GaAs and InP in table 4.1.

### Table 4.1 Theoretically derived energy levels for GaAs and InP [10].

<table>
<thead>
<tr>
<th></th>
<th>GaAs</th>
<th>InP</th>
</tr>
</thead>
<tbody>
<tr>
<td>electron affinity $\chi$ (eV)</td>
<td>4.05</td>
<td>4.4</td>
</tr>
<tr>
<td>ionisation potential $\phi$ (eV)</td>
<td>5.47</td>
<td>5.75</td>
</tr>
<tr>
<td>bandgap $E_g$ (eV)</td>
<td>1.42</td>
<td>1.35</td>
</tr>
</tbody>
</table>

The difference in these levels will cause discontinuities of the bands at the interface. When a junction is formed between the two semiconductors, the energy band profile becomes as shown in figure 4.6. This structure fulfils the two basic requirements for the construction of the energy band diagram:

a) The Fermi level $E_F$ must just be the same on both sides of the interface in thermal equilibrium, and

b) the vacuum level must be continuous and parallel to the band edges.
Since the electron affinity and the ionisation potential are different for both semiconductors, the conduction and valence band will have a discontinuity at the interface. The bending of the bands is related to the space charge distribution. A higher doping involves a stronger bending, which causes a more narrow barrier for the carrier transport.

The current transport in an isotype heterojunction is mainly due to majority carriers, i.e. electrons in a n-n-junction. There are three basic transport processes which are responsible for the carrier transport [16]:

1) Transport of the electrons over the potential barrier (thermionic emission).

2) Quantum-mechanical tunneling of carriers through the barrier

3) Transport due to the recombination of the electrons in the space charge region.

### 4.4.2 Thermionic Emission Theory

For high mobility semiconductors the transport of electrons over the potential barrier can be adequately described by the thermionic emission theory limited by the
diffusion current. By introducing an ideality factor n the recombination current is included in this theory. According to Wada et al. [17] and Okuno et al. [18] the current voltage characteristics of the n-n-fused heterojunction can be described by this theory. The basic equation for the current density is[19]

\[ J = A \cdot T^2 \cdot \exp\left(-\frac{q \cdot V_b}{kT}\right) \cdot \left\{ \exp\left(\frac{q \cdot V_I}{n \cdot kT}\right) - \exp\left(-\frac{q \cdot V_H}{n \cdot kT}\right) \right\} \]  

(1)

where \( V_b \) is the barrier height, \( A \) the effective Richardson constant for thermionic emission, \( T \) the temperature, \( q \) the electronic charge, \( k \) the Bolzmann's constant and \( V_I \) and \( V_H \) the voltages applied to the different materials. According to Wada et al. [17] the effective Richardson constant equals 8.4 A/cm\(^2\)/K\(^2\). To simplify the model, Okuno et al.[18] assumed that the ratio of the voltages applied to the GaAs and InP is constant in the measured voltage range.

With these assumptions the measurements in this study are fitted to extract the following parameters.

a) The barrier height \( V_b \) corresponds to the energy difference between the Fermi-level and the top of the conduction band. This is the energy that the electrons at the Fermi level must acquire to pass over the potential barrier, and it has the same value for both current directions.

b) The ideality factor n indicates the dominance of the two different carrier transports, which are included in this theory. When the ideal diffusion current dominates, n is close to 1, whereas when the recombination current dominates, n is close to 2.

c) The asymmetry in the forward and reverse bias D is due to the ratio of the voltage applied in the GaAs and the InP:

\[ D = \frac{V_I}{V_H} = \frac{V_{GaAs}}{V_{InP}} \]  

(2)
The measured I-V-curves are fitted by the least square method, i.e., the sum of the squares of the deviations of the \( J(V) \) curve from the experimental points is minimised. This fitting is done with help of Microcal Origin 4.1. Figure 4.7 depicts the fitting curves of three experiments with the lowest InP doping concentration and also two results of the other groups of Wada et al. and Okuno et al.

![Figure 4.7 J(V) comparing of the present experiments and literature according the thermionic emission theory.](image)

Table 4.2 summarises the results of the parameter extraction of the six experiments and also the results of other groups under almost the same conditions. Okuno et al. have used a lower fusion temperature of 600°C.
Table 4.2 parameter extraction according the thermionic emission theory.

<table>
<thead>
<tr>
<th>Sample</th>
<th>Doping Conc.</th>
<th>barrier height $V_b$ (eV)</th>
<th>ideality factor n</th>
<th>asymmetric constant D</th>
<th>Error indication $\chi^2$</th>
</tr>
</thead>
<tbody>
<tr>
<td>N05</td>
<td>2e17, 9e17</td>
<td>0.46</td>
<td>1.2</td>
<td>10</td>
<td>123</td>
</tr>
<tr>
<td>N12</td>
<td>2e17, 6e18</td>
<td>0.45</td>
<td>1.2</td>
<td>10</td>
<td>90.0</td>
</tr>
<tr>
<td>N11</td>
<td>1.5e18, 9e17</td>
<td>0.37</td>
<td>1.6</td>
<td>3.6</td>
<td>56.6</td>
</tr>
<tr>
<td>N09</td>
<td>1.5e18, 6e18</td>
<td>0.37</td>
<td>1.5</td>
<td>4.0</td>
<td>180</td>
</tr>
<tr>
<td>N07</td>
<td>6e18, 9e17</td>
<td>0.24</td>
<td>1.2</td>
<td>2.1</td>
<td>1.16</td>
</tr>
<tr>
<td>N26</td>
<td>6e18, 6e18</td>
<td>0.23</td>
<td>0.82</td>
<td>1.9</td>
<td>3.19</td>
</tr>
<tr>
<td>Wada's</td>
<td>2e18, 2e18</td>
<td>0.4</td>
<td>1.8</td>
<td>3.5</td>
<td>unknown</td>
</tr>
<tr>
<td>Okuno's</td>
<td>2e18, 2e18</td>
<td>0.35</td>
<td>1.0</td>
<td>1.0</td>
<td>unknown</td>
</tr>
</tbody>
</table>

All the three parameters have a different influence on the I-V-characteristics. The most important is the barrier height. It seems that the variation in the doping concentration in the InP side has no influence on this parameter, while a higher doping concentration in the GaAs side decreases the barrier height. For a higher doping the level of the conduction band is lower (closer or even below $E_F$), which decreases the distance between the Fermi level and the minimum of the conduction band at the junction ($V_b$). More likely is that the notch in the conduction band is more narrow which facilitates the possibility to tunnel through the barrier. Even with the same distance between the Fermi level and the top of the conduction band, the effective barrier height, which actually has been calculated, is smaller. The tunneling effect is not included in this model. This simplification is responsible for the remarkable value of the ideality factor for sample N26. The ideality factor determines the slope of the curves. It is defined as:
\[ n = \frac{q}{kT} \frac{\partial N}{\partial (\ln J)} \]  

If the current transport is solely due to diffusion and recombination, the value of the ideality factor should be between 1 and 2. The value, extracted by the fitting is not within this range and seems to reveal a shortcoming of the model.

### 4.4.3 Temperature Dependence

For heterojunctions with high doping levels, as in this study, significant deviations from the simple theory given above are often observed, due to carrier tunneling. Because of the larger bending of the conduction band, the barriers at the interface will be narrow. It is well known that the tunneling process is almost insensitive to temperature variations, in contrary to the thermionic emission process. For a low temperature, the influence of the tunneling becomes more important. To examine the validity of the former model without tunneling, the conductivity of the samples is measured at a lower temperature.

![Figure 4.8 Current voltage measurements for the different doping levels at T=133K](image-url)

Figure 4.8 Current voltage measurements for the different doping levels at T=133K
Figure 4.8 depicts the I-V-characteristics at $T=133\text{K} \left(=-140^\circ\text{C}\right)$. The same characteristics as for room temperature can be seen, with only a small shift in the "break-down" voltage. Such curves were acquired from -140°C to room temperature.

The applied voltage for a current density of $-325\text{A/cm}^2$ for the different samples is plotted in figure 4.9.

![Figure 4.9 Temperature dependence of the electrical conductivity](image)

No appreciable deviations between the samples has been noticed. Only for the lowest doping in the GaAs samples, a difference can be seen between the two samples. Here the InP doping concentration seems to influence the conductivity at low temperature. The higher doped sample is less sensitive to the temperature, which might be due to an enhanced tunneling effect. Higher doping level facilitates the tunneling process which is almost insensitive for temperatures.

I have tried to fit the curves according to the thermionic emission theory, but the curves fit not properly and the extracted parameters are far outside the acceptable range. This indicates a shortcoming of the model and the need for a more advanced modelling, which includes tunneling and the presence of interface states.
4.4.4 Interface States and Tunneling

It is clear that we have to include tunneling in our model, but there is also another phenomenon that might be of importance: imperfection at the fused junction may give rise to interface states. These interface states could come from the dislocations and the contaminations at the interface. In the edge dislocations or other imperfections at the interface there may exist so-called "dangling bonds" with unpaired electrons. This may either give rise to donor-like or acceptor-like interface states.

A one dimensional model for the carrier transport, including the effect of tunneling and interface states, has been developed by Prof. Joachim Piprek at the University of California in Santa Barbara (UCSB). The presence of the interface states was simulated by adding a delta doping at the interface. The experimental results were fitted by varying the effective conduction band offset and the delta doping concentration. First the effective conduction band offset is tuned in that way that it gives the same value for all experiments. A relative large value of 0.52 eV was assumed to find agreement. Then the curves were fitted by varying the interface acceptor concentration. This was approximated by a 10 nm wide negative space charge layer at the interface. The concentration of the surface states was between $10^{18}$ cm$^{-3}$ and $4\times10^{18}$ cm$^{-3}$ and was mainly related to the doping concentration in the GaAs side. Two dimensional simulations, which take the geometry of the mesas and contacts into account, correspond with the one dimensional model and approve this simplification. The results are summarised in table 4.3.
Table 4.3 Simulated interface concentration for the different combinations with dEc=0.52eV

<table>
<thead>
<tr>
<th>Sample</th>
<th>Doping Conc</th>
<th>δ-doping concentration (cm⁻³)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>GaAs</td>
<td>InP</td>
</tr>
<tr>
<td>N05</td>
<td>2e¹⁷</td>
<td>9e¹⁷</td>
</tr>
<tr>
<td>N12</td>
<td>2e¹⁷</td>
<td>6e¹⁸</td>
</tr>
<tr>
<td>N11</td>
<td>1.5e¹⁸</td>
<td>9e¹⁷</td>
</tr>
<tr>
<td>N09</td>
<td>1.5e¹⁸</td>
<td>6e¹⁸</td>
</tr>
<tr>
<td>N07</td>
<td>6e¹⁸</td>
<td>9e¹⁷</td>
</tr>
<tr>
<td>N26</td>
<td>6e¹⁸</td>
<td>6e¹⁸</td>
</tr>
</tbody>
</table>

Figure 4.10 illustrates the influence of the acceptor like surface states for the energy bands for one case (sample N09). The energy levels, including the vacuum level E₀, are pulled up around the junction. Therefore the barrier for electron transport increases.

Figure 4.10 Band structure for the heterojunction included acceptor like interface states.
Figure 4.11 depicts the I-V-measurements at room temperature again but now including the simulations by J. Piprek.

![Graph of I-V comparison between measurements and simulations according Piprek's model.]

In these simulations the effective conduction band offset and the interface (acceptor) concentration were adjusted. The band offset effects the symmetry of the curves. In the third quadrant the electron flow is from the InP to the GaAs side and the electrons has to overcome the barrier. In the other direction the electron transport is much easier. In the more symmetric curves the surface states dominates the transport process.

### 4.5 Summary

In this chapter the fused interface was investigated for different doping concentrations in the GaAs and InP interface layers. The fused samples has been analysed by SIMS to estimate the diffusion of the dopant and the contamination at the interface. There appears to be no diffusion of silicon. An oxygen concentration spike was visible at the
interface, probably due to insufficient cleaning or oxidation during the fusion. Nevertheless the surface concentration is less than an atomic layer, indicating the absence of any extended oxide at the interface. The SIMS results for carbon and iron give a concentration spike at the interface too. This is probably due to contaminations from the fixture and screws.

The I-V-measurements show the characteristics of a general isotype heterojunction with exponential slopes on the positive and negative direction. The difference in InP doping concentrations seems to have a minor effect of electrical conductivity of the junction. In the case that the InP side is biased positively (operating condition area for a VCSEL) the voltage drop over the junction is between 30 mV and 400 mV at a current density of 325 A/cm². These values are in an acceptable range and comparable with published results of other groups.

Modelling according to the thermionic emission theory shows a shortcoming for such simulations of the measurements at lower temperatures. Therefore a more advanced model, including tunneling and interface states, was introduced. A relative large value of 0.52 eV for the effective conduction band offset has to be assumed to find agreement. The presence of acceptor-type interface states gives a satisfactory fitting of the results.
5. Effect of the Fusion Temperature on Junction Resistance

5.1 Introduction

Apart from the doping concentration, there are more parameters in the fusion process which are important to investigate. It is assumed that the optical losses of a fused interface have only a minor importance in the device of a VCSEL. On the other hand, the heat treatment in combination with the high pressure can give a disordering in the fused structures. Ram et al. found a 3% decrease in the reflectivity of a 10-period DBR after fusion [20]. Yang et al. reported a significant reduction in the PL efficiency of quantum wells located within 2000 Å of the bonded interface, due to the bonding process [21]. In both studies the fusion temperature was 630 °C. In this part of the study the electrical conductivity is investigated for fusion runs at different temperatures, in order to find a minimum fusion temperature with good electrical properties. This could also lead to a better understanding of the mechanism behind the fusion process.

5.2 Physics of Bonding

A model of the physics of wafer bonding has been proposed by Dudley [2]. This model explains why the two mating surfaces are flattened out during the bonding process so that no voids remain after the heat treatment, even though the surfaces have a small roughness from the epitaxial growth. In this model an important factor for the fusion process is the temperature. When the InP and GaAs samples have been mated, they touch at several places while gaps occur elsewhere between the samples. During the heat treatment at sufficiently high temperatures, mass transport takes place to allow the gaps to fill in. Since the energy required to cause evolution of the group V
element vapour phase in the InP is lower than that in GaAs, the dissociation of the former semiconductor is believed to play a major role. The most dominated equilibrium equation during the fusion process is thought to be:

\[ \text{In}(s) + \frac{1}{2} \text{P}_2(g) \leftrightarrow \text{InP}(s). \] (4)

To keep the \( \text{P}_2(g) \) near the InP surface, the GaAs wafer needs to enclose the surface; otherwise the decomposition of InP will result in a metallic indium at the fused interface, something which has not been seen in the TEM analysis. The reaction (4) is driven from right to left in those places where the samples are in touch with a high pressures. Due to the difference in concentration of the In atoms, the In(s) will diffuse along the interface and fill the voids. For a detailed description see Dudley [2].

Foxon et al. studied the species involved in the evaporation of the III-V compounds as a function of temperature [22]. Two temperature intervals play a major role for the evaporation. At lower temperatures, the fluxes of the group III and V elements are approximately equal, which give a so called congruent evaporation. Above a certain temperature, the Congruent Evaporation Temperature (CET), the group V element becomes the most dominant element in the gas. Up to now, wafer fusion has only occurred at temperatures above the CET of at least one of the two materials. The CETs of GaAs and InP are 625 °C and 360 °C respectively and the lowest reported fusion temperature between them is 450 °C [17].

The low CET of GaAs suggests an occurrence of mass transport of \( \text{As}(s) \) during fusions at the current temperature of 650 °C. This could result in a formation of \( \text{InGaAsP} \). Most TEM studies show an abrupt InP/GaAs interface, which indicates the dominance of \( \text{P}_2(g) \) in the vapour pressure.

### 5.3 Process Parameters

The fusion runs in this part of the study are similar in preparation and process except for the fusion temperature. The ramp and the total fusion time (including ramp) are
the same as for the previous fusion runs, i.e. 20 °C/min and 60 min respectively. The temperature range between 305 °C and 705 °C in steps of 50 °C, was investigated. The surfaces of all the samples were completely or largely fused and no trend in the fusion quality was visible in this temperature range. The doping concentration in the InP sample as well as in the GaAs sample is $6 \times 10^{18}$ cm$^{-3}$. This corresponds with the highest doping level in the first part of this study which gave the best electrical conductivity.

5.4 I-V Measurements

The current voltage characteristics at room temperature for the nine different samples are shown in figure 5.1. The sign of the voltage relates to the InP side.

![Figure 5.1 Current voltage measurements for different fusion temperatures](image)

It has already been noticed that, for a fusion temperature of 655 °C, almost no voltage barrier was perceptible. For higher temperatures no large differences can be seen. For
lower temperatures a voltage barrier becomes visible. Below 500 °C, the electrical conductivity decreases rapidly. However, no extreme changes in this trend can be noticed below the CET of InP, i.e. 360 °C. This is illustrated in figure 5.2, which depicts the voltage for a current densities of plus and minus 325 A/cm² with respect to the temperature. Besides the asymmetry in the positive and negative directions, the degrading is both cases is similar.

![Graph](image)

**Figure 5.2** Voltage over the fused junction at a certain current for fusion different temperatures

### 5.5 TEM Analysis

For investigation of the crystalline structure of the fused junctions, TEM analysis has been performed on two samples by Dr. Laurent Sagalowicz at EPFL. The two samples were fused at temperatures of respectively 300 °C and 655 °C.

For the measurements very thin samples must be made, to facilitate the electron transmission and to analyse the deviations of the beam. For both samples, the TEM images show the atomic layers, which means that the samples were correctly
prepared. However for one sample, which was fused at the lowest temperature, no signal of the InP can be seen. It seems that this sample was not properly fused and therefore the bonding was very fragile resulting in a separation of the materials.

Images of the other sample show a crystalline junction without any intermediate layer. At the interface only misfit edge dislocation can be seen. The distance between two atoms in the (001) plane of the semiconductors is $\frac{1}{2}\sqrt{2}$ times the lattice constant, i.e., 3.997 Å and 4.150 Å for respectively GaAs and InP. On the average, the distance between two edge dislocation is 108 Å, which corresponds to the lowest distance where $n$ atoms in InP equals $n+1$ atoms in GaAs. Figure 5.3 shows the cross section of the sample with arrows on the place of the edge dislocations. The misfit dislocations form a network with Burgers vectors in the $\frac{1}{2}[110]$ and $\frac{1}{2}[1\overline{1}0]$ directions[23].

![Figure 5.3 TEM image of a fused interface (fused at 655°C) showing the misfit dislocations](image)

---

- **EFFECT OF THE FUSION TEMPERATURE ON JUNCTION RESISTANCE**
- **PAGE 45**
5.6 Summary

To minimise the problem of structure disordering due to the heat treatment of the fusion, a study is made to find a minimal fusion temperature with good electrical conductivity. It seems that temperatures down to 500°C give a proper result. Fusions at temperatures under the CET of InP have successfully been made. The I-V measurements show no dramatically degrading below this temperature. However, the fusion experiment at this low temperature seemed to be very fragile since the bonding broke during the preparation for the TEM analysis. The sample might not have been properly bonded but it is difficult to draw any conclusion from one failed experiment. The I-V results indicate a better conductivity above 500°C, making this range more interesting for device applications.
6. Wafer Fusion for VCSEL Devices

6.1 Introduction

In this chapter, an investigation on the effect of the fusion on the quality of the Quantum Wells (QWs) is made. This is performed by PL analysis of active layers before and after fusion. The processing and intermediate results of the first fused VCSELs realised at KTH are included. It mainly focusses on the process of the VCSELs and especially on the wafer fusion step.

6.2 Effect of Fusion on the Quantum Wells

The heat treatment in combination with the high mechanical pressure during the fusion is thought to degrade the optical quality of the device [20,21]. To investigate the degradation of the QWs in the active layer PL analyses are performed on the sample before and after fusion. To avoid optical losses in the substrate, one of the two substrates is removed after the fusion to reveal the active region at the surface.

6.2.1 Sample Preparation

In this study an active layer with nine QWs, designed for a double fused VCSEL, is investigated. This device contains an etch stop layer between the active region and the substrate to make it possible to remove the InP substrate. The sample is fused to a n-doped (1.5x10^{18} cm^{-3}) GaAs sample, which is the same structure as in the previous studies. The fusion temperature is 600 °C, corresponding to the fusion temperature used in the process of the single fused VCSEL. The fused sample is cleaved into two

---

2 After the first fusion in the process of a double fused VCSEL, the InP substrate and etch stop layer of the active layer side are removed. After that the second fusion takes place between the active region, including the p-mirror, and the n-mirror.
pieces. The InP substrate (including the etch stop layer) is removed from the first piece and the GaAs substrate from the second. The substrate removal on the InP side is described in chapter 2. The GaAs substrate is removed up to the fused junction. The InP layer is used as etch stop. For the etching a $\text{NH}_3 : \text{H}_2\text{O}_2$ solution at room temperature with a pH of 8.3 is used. Despite the high etch rate of 1.5 $\mu$m/min, this solution has a disadvantage: during the etching, stable oxides are created on the surface, which terminates the etching. A spray etching set-up has been built to avoid this problem. The etchant is continuously sprayed onto the surface preventing it from forming a oxide layer. The etch time is roughly 3½ hour.

6.2.2 PL Results

The PL analysis is performed with three different samples, one unfused and two fused, which only differ in the remaining substrate material, i.e. GaAs or InP. The PL measurements are carried out with two different set ups. The set ups mainly differ in optical pumping source. In the first case a GaAs (880 nm) laser and in the second a Nd:YAG (1064 nm) laser is used. In both systems the light detection is optimised for power coupling in every measurement.
Figure 6.1 shows the results of the PL analysis performed with the GaAs laser. The intensity of the fused samples exhibits large fluctuations over the surface of the same sample. The fluctuations are not fully understood. The uniformity of this fusion run was not optimal, which may effect the quality of the quantum wells. Local high pressures during the fusion may cause damage in the active layer. Damages to the active layer from the substrate etching might be another reason for these fluctuations. Indeed damages on the surface of the active layer can be seen after the fusion, see figure 6.2.
The active layer is not uniform over the wafer and the measurement is carried out at different places of the wafer. This causes the shift in the wavelength between the measurements.

Figure 6.2 surface of the active layer before and after fusion and substrate etching

Figure 6.3 normalised PL intensity of active layer before and after fusion
The linewidth of the spectra gives an indication of the quality of the quantum wells [24]. Normalising the curves to a equal intensity gives similar shapes with the same linewidth. Figure 6.3 depicts the normalised PL intensities for the three different samples. For the fused samples the data correspond to the lowest measured PL intensity (see figure 6.1). This indicates that the fusion process does not affect the properties of the quantum wells.

\[ PL \text{ measurements on InGaAsP active layer (Nd:YAG Laser)} \]

- unfused sample on InP substrate
- fused sample on InP substrate (GaAs removed)
- fused sample on GaAs substrate (InP removed)

Figure 6.4 PL analysis of fused active layer (pumping with Nd:YAG laser)

The results of the PL measurements performed with the Nd:YAG laser give a new indication, see figure 6.4. Generally the new results do not really correspond with the first set-up. The low intensity at 1.45 μm can not be noticed. The detected range of the wavelength is between 1.1 μm and 1.7 μm. In this spectrum a second intensity peak is visible. The unfused sample and the fused sample on the InP substrate show a higher intensity peak around 1.35 μm. This dominating peak is due to the luminescence from the quaternary etch stop layer between the active layer and the InP substrate. The etch
stop layer is roughly 100 nm thick and has a bandgap corresponding to 1.3 \( \mu \text{m} \). For the fused sample no significant PL is detected at the wavelength of the quantum wells. The measurement is presumably carried out on a bad area of the sample, where the quantum wells were damaged. The results of the active layer on the GaAs substrate are similar to the results with the other set-up with the GaAs laser. Since there is no etch stop layer, the intensity peak at 1.35 \( \mu \text{m} \) cannot be seen. For longer wavelengths the pattern of this sample is similar to the unfused sample.

The different results between measurements on the same samples as well as between the different set-ups need more investigation. An examination of the latter problem is necessary to make reliable PL measurements in the future. The former problem is important in the process of the VCSELs. If the removal of the etch stop layer really damages the active region, this method makes it useless for double fused VCSEL processes. There are no clear indications that the fusion affects the quality of the active region.

**6.3 VCSEL Process with one fusion step only**

**6.3.1 Structure**

A long wavelength VCSEL device consists of an InP/InGaAsP active layer, sandwiched between two DBR mirrors. As reported in chapter 1, the best choice of the DBR is the GaAs/AlAs combination because of the large differences in refractive index, low absorption and the good electrical and thermal conductivity. This makes it possible to realise reflection of more than 99.9% with 30 periods of Al\(_{0.67}\)Ga\(_{0.33}\)As/GaAs. Long wavelength VCSELs, containing GaAs based DBRs, can only be made with help of two wafer fusion steps because of the lattice mismatch with the InP based active region. To facilitate the process a second structure has been designed by avoiding one fusion step. The n-type mirror is replaced by a GaInAsP/InP mirror which is lattice matched with the active region. Because of the high mobility of the carriers, i.e., electrons, and the low absorption the properties of this structure might still be acceptable. Figure 6.5 depicts the schematics of this single fused VCSEL design.
An AlAs layer in the top mirror, close to the active layer, is oxidised to get a current confinement in the middle of the mesa. The active layer structure contains nine strained (+1%) InGaAsP QWs with strain-compensating (-0.7%) barriers.

6.3.2 Cleaning

Before fusion the mirror and active region are cleaned following the procedure explained in chapter 2. The solution that etches the oxides after the ashing treatment can damage the structures. This solution contains HF, which etches aluminium containing materials. In some of our structures the top layers is resistant to this etchant and only some underetching of the mirror AlGaAs layers at the border of the sample occur. A problem occurs if the mirror has extraordinary defects from the epitaxy. Near these defects, it seems the etchant can reach the aluminium containing layers. This gives unacceptable damage which makes the mirror useless for fusion. Figure 6.6
depicts the defects before and after the cleaning and shows the etch result of the AlGaAs layers\textsuperscript{3}.

![Defect on the DBR before and after the current cleaning procedure prior to fusion](image)

Figure 6.6 Defect on the DBR before and after the current cleaning procedure prior to fusion

### 6.3.3 Fusion

The fusion is carried out under the previous conditions at a fusion temperature of 600\textdegree{}C. This temperature is 50 degrees lower than most of the common fusions for VCSELs, but is still in the range of the high electrical conductivity as concluded in chapter 5.

### 6.3.4 Mesa etching

When the fusion has been carried out, the substrate of the top mirror is removed by spray etching at room temperature. For this a NH\textsubscript{3} : H\textsubscript{2}O\textsubscript{2} solution with a pH of 8.3 is used. An AlAs layer is used as etch stop and can be removed with HF afterwards.

After this step the top contacts, with diameters between 70 \textmu{}m and 10 \textmu{}m, are deposited by electron beam evaporation. These contacts are used as a mask when wet etching the mesas. A H\textsubscript{2}SO\textsubscript{4}:H\textsubscript{2}O\textsubscript{2}:H\textsubscript{2}O = 5:8:40 solution etches the mesas in roughly 2 minutes. The completion of the etching is detected by noticing the appearance of the

\textsuperscript{3} These defects and related underetching has not been seen for all the mirrors which were cleaned. At this moment too few experiments have been made to conclude if the cleaning procedure must be changed in the future to exclude this phenomenon. This experience makes a test cleaning run with a dummy piece of the mirror necessary.
channels in the InP as well as the end of the reflection changes of the different mirror layers. The mesas have an underetching of about 10 µm and an eye shape due to the differences in lateral etch rates, i.e. anisotropic etching. Figure 6.7 depicts a SEM picture of the single fused VCSELs, which clearly shows the metal contacts and the underetching. For the small mesa dimensions, the underetching destroys the mesa completely. Within the InP the channels of the fusion step can be seen, as the horizontal stripes in the bottom layer.

Figure 6.7 SEM picture of the single fused VCSELs

6.4 Results

In pulsed operation, the single fused VCSEL exhibit lasing at room temperature. The mesas with the largest diameter (= 45 µm after etching) give the best result. These mesas have the smallest ratio between the diameter of the top and the bottom. This geometry has a better current uniformity in the mirror. Figure 6.8 depicts the output power with respect to the current. The threshold current density is 2.3 kA/cm² for room temperature. The threshold voltage over the laser is about 8 V. The voltage drop over the fused junction should have a minor contribution to the total voltage over the
laser [15]. The oxidation for current confinement has no effect on the laser properties. It is assumed that in this sample the oxidation penetrates less than 5 µm within the mesa which seems to be too little to affect the current confinement. The AlAs oxidation layer is a quarter wavelength thick. A thicker AlAs layer will improve the oxidation and thus the current confinement.

![Figure 6.8 P(I) characteristics of the VCSEL in pulse operation.](image)

**6.5 Summary**

In this chapter the effect of the wafer fusion on optical properties of the active layer was investigated. PL measurements have been carried out on samples with QWs before and after fusion. Two different set-ups were used which mainly differ in the optical pumping. Large fluctuation of the PL intensity over the surface can be noticed for the fused samples. Except for the intensity the curves correspond well with that of the unfused sample. The linewidths of the spectra are the same, indicating that the fusion does not cause any disordering of the quantum wells. The intensity fluctuations need more investigation. Damages of the active layer, due to the fusion or substrate removal, might be an explanation.

The process of a single fused VCSEL was reported. Problems occur during the cleaning of the mirror prior to fusion. Around epitaxial defects, the HF containing
cleaning solution etches into the mirror. This phenomenon was not seen for all of the mirrors and depends on the size of the defects. The VCSELs exhibit lasing at room temperature under pulsed operation.
7. Conclusions and Recommendations

7.1 Effect of Doping Concentration

Fused interfaces with different doping concentrations in the GaAs and InP interface layers were investigated. The fused samples were analysed by SIMS for estimating the diffusion of the dopant and the contaminations at the interface. There appears to be no diffusion of silicon. An oxygen concentration peak was visible at the interface, probably due to insufficient cleaning or oxidation during the fusion. Nevertheless, the surface concentration is less than an atomic layer, indicating the absence of any extended oxide at the interface. The SIMS results for carbon and iron also give concentration peaks at the interface. This is probably due to contaminations from the fixture and its screws.

The I-V-measurements show the characteristics of a general isotype heterojunction with exponential slopes in the positive as well as in the negative direction. The difference in the doping level in the InP side seems to have a minor effect on the electrical conductivity of the junction. A higher doping concentration in the GaAs side increases the electrical properties of the junction.

A model which included tunneling and interface states was introduced for fitting the I-V-results. A relative large value of 0.52 eV for the effective conduction band offset has to be assumed to find agreement. The presence of acceptor type interface states gives a satisfactory fitting of the results.

7.2 Effect of Fusion Temperature

For minimising the problem of layer disordering, due to the heat treatment of the fusion, a study was made to find a minimal fusion temperature with acceptable
electrical conductivity. Bonding at a temperature above 550 °C gives acceptable result. Fusions at temperatures under the CET of InP, which is 360 °C, have been made. The I-V measurements show no extreme decrease of conductivity underneath this temperature. However, a fusion experiment fused at 300 °C seemed to be very fragile since the bonding broke during the preparation for the TEM analysis. Even if the electrical measurements give no clear indications of poor fusion, samples fused below the CET may not be properly bonded. However it is difficult to draw any conclusion after one experiment. The I-V results indicate a better conductivity above a fusion temperature of 550 °C, above which fusion might be interesting for device applications.

7.3 Effect of Fusion on Quantum Wells

The effect of the fusion process on the optical properties of the active layer was investigated. PL measurements before and after fusion have been carried out on samples with quantum wells. Two different measurement set-ups were used which mainly differed in the optical pumping source. Large fluctuation of the PL intensity over the surface can be noticed for the fused samples. Beside the intensity fluctuations, the spectra corresponds well with the unfused sample. The linewidths are similar, indicating that the fusion does not cause any disordering of the quantum wells. The intensity fluctuations need more investigation. Damages to the active layer, due to the fusion or substrate removing, might be an explanation. For reliable PL analysis, further investigation on the problem of the different results between the set-ups is necessary.

In the processing of the single fused VCSEL, the cleaning of the mirror prior the fusion showed up to be problematic. Around epitaxial defects, the cleaning solution etches into the mirror. This phenomenon was not seen for all the mirrors and depended on the size of the defects. The VCSELs exhibit lasing at room temperature for pulse operation. The laser properties can be presumably improved by optimising the fabrication process. Dry mesa etching, which produces vertical mesa wall, and a deeper oxidation into the mesa for current confinement should increase the current density in the middle of the mesa.
In the last few years it has been proved that wafer fusion is a valuable technique for creating a new generation optoelectronic devices with lattice mismatch systems with good electrical and optical properties. The next step in the development of this new technique must be the facilitating of the fusion process itself for making it industrially applicable.
Appendix A  Wafer Fusion Runs

Table A.1 Wafer numbers and n-doping concentration at the interface to be fused

<table>
<thead>
<tr>
<th>Material</th>
<th>Wafer no</th>
<th>concentration (cm⁻³)</th>
</tr>
</thead>
<tbody>
<tr>
<td>InP</td>
<td>3762</td>
<td>6x10¹⁸</td>
</tr>
<tr>
<td>InP</td>
<td>20464 A/B</td>
<td>9x10¹⁷</td>
</tr>
<tr>
<td>InP</td>
<td>20465 A/B</td>
<td>6x10¹⁸</td>
</tr>
<tr>
<td>GaAs</td>
<td>M1072</td>
<td>2x10¹⁷</td>
</tr>
<tr>
<td>GaAs</td>
<td>M1074</td>
<td>1.5x10¹⁸</td>
</tr>
<tr>
<td>GaAs</td>
<td>M1078</td>
<td>6x10¹⁸</td>
</tr>
<tr>
<td>GaAs</td>
<td>M1111</td>
<td>6x10¹⁸</td>
</tr>
</tbody>
</table>

Table A.2 properties of the wafer fusion runs

<table>
<thead>
<tr>
<th>sample #</th>
<th>InP #</th>
<th>GaAs #</th>
<th>analysis</th>
<th>temp (⁰C)</th>
<th>Remarks (file)</th>
</tr>
</thead>
<tbody>
<tr>
<td>N04</td>
<td>3762</td>
<td>M1074</td>
<td>SIMS</td>
<td>655</td>
<td>collapsed channels</td>
</tr>
<tr>
<td>N05</td>
<td>20464A</td>
<td>M1072</td>
<td>I-V</td>
<td>655</td>
<td>(-)</td>
</tr>
<tr>
<td>N06</td>
<td>20464A</td>
<td>M1074</td>
<td></td>
<td>655</td>
<td>Misaligning</td>
</tr>
<tr>
<td>N07</td>
<td>20464A</td>
<td>M1078</td>
<td>I-V</td>
<td>655</td>
<td>(d)</td>
</tr>
<tr>
<td>N09</td>
<td>20465A</td>
<td>M1074</td>
<td>I-V</td>
<td>655</td>
<td>(-)</td>
</tr>
<tr>
<td>N10</td>
<td>20465A</td>
<td>M1078</td>
<td>I-V, SIMS</td>
<td>655</td>
<td>(same as N26)</td>
</tr>
</tbody>
</table>

* InP structure contains one etch stop layer instead of two.
<table>
<thead>
<tr>
<th>Sample #</th>
<th>InP #</th>
<th>GaAs #</th>
<th>Analysis</th>
<th>Temp (°C)</th>
<th>Remarks (file)</th>
</tr>
</thead>
<tbody>
<tr>
<td>N11</td>
<td>20464A</td>
<td>M1074</td>
<td>I-V</td>
<td>655</td>
<td>(-)</td>
</tr>
<tr>
<td>N12</td>
<td>20465A</td>
<td>M1072</td>
<td>I-V</td>
<td>655</td>
<td>(-)</td>
</tr>
<tr>
<td>N13</td>
<td>20465A</td>
<td>M1078</td>
<td>SIMS</td>
<td>655</td>
<td>Mo-fixture</td>
</tr>
<tr>
<td>N14</td>
<td>20465A</td>
<td>M1078</td>
<td>SIMS</td>
<td>655</td>
<td>stainless steel screws</td>
</tr>
<tr>
<td>N15</td>
<td>20465B</td>
<td>M1078</td>
<td>I-V</td>
<td>560</td>
<td>(c)</td>
</tr>
<tr>
<td>N16</td>
<td>20465B</td>
<td>M1078</td>
<td>I-V, SIMS</td>
<td>510</td>
<td>(b)</td>
</tr>
<tr>
<td>N17</td>
<td>20465B</td>
<td>M1078</td>
<td>I-V</td>
<td>460</td>
<td>(-)</td>
</tr>
<tr>
<td>N18</td>
<td>20465B</td>
<td>M1078</td>
<td>I-V</td>
<td>410</td>
<td>(a)</td>
</tr>
<tr>
<td>N19</td>
<td>20465B</td>
<td>M1078</td>
<td>I-V</td>
<td>360</td>
<td>(same as N21)</td>
</tr>
<tr>
<td>N20</td>
<td>20465B</td>
<td>M1111</td>
<td></td>
<td>305</td>
<td>bad contacts (N23)</td>
</tr>
<tr>
<td>N21</td>
<td>20465B</td>
<td>M1111</td>
<td>I-V, SIMS</td>
<td>360</td>
<td>(c)</td>
</tr>
<tr>
<td>N22</td>
<td>20465B</td>
<td>M1078</td>
<td>I-V</td>
<td>610</td>
<td>(c)</td>
</tr>
<tr>
<td>N23</td>
<td>20465B</td>
<td>M1111</td>
<td>I-V</td>
<td>305</td>
<td>(c)</td>
</tr>
<tr>
<td>N24</td>
<td>20464A</td>
<td>M1072</td>
<td>SIMS</td>
<td>655</td>
<td>without channels, wet</td>
</tr>
<tr>
<td>N25</td>
<td>20464A</td>
<td>M1072</td>
<td>SIMS</td>
<td>655</td>
<td>without channels ,dry</td>
</tr>
<tr>
<td>N26</td>
<td>20465B</td>
<td>M1111</td>
<td>I-V</td>
<td>655</td>
<td>(a)</td>
</tr>
<tr>
<td>N27</td>
<td>20465B</td>
<td>M1111</td>
<td>I-V</td>
<td>705</td>
<td>(c)</td>
</tr>
<tr>
<td>N28</td>
<td>203675</td>
<td>M1074</td>
<td>TEM</td>
<td>305</td>
<td>20nm InP on GaAs</td>
</tr>
</tbody>
</table>

5 p-doped InP designed for TEM analysis; thinner InP layer at fused interface (200Å).
Appendix B  References


