MASTER

Smartcell
modulaire amplifier

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SMARTCELL
Modulaire amplifier

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De Faculteit der Elektrotechniek van de Technische Universiteit Eindhoven
aanvaardt geen verantwoordelijkheid voor de inhoud van stage- en afstudeerverslagen.
Abstract

A novel implementation of paralleling converter modules without a master is proposed and analysed.

Generally, the paralleling of power-converters offers a number of advantages over a single high power, centralised power supply. Performance-wise, the advantages include higher efficiency, better dynamic response due to a higher frequency of operation. System-wise, paralleling allows for redundancy implementation and expandability of output power.

A simple, high efficiency, "autonomously" dynamic (DC/AC) current sharing module is proposed and implemented. Each module operates either as a stand-alone unit or as a parallel module.

A converter module consists of a half-bridge with an inductor and a capacitor plus a control circuit. The half-bridge controls the current in the inductor, which is set to critical discontinuous. Due to switching at zero current, high efficiency is obtained. Drawback is the relatively large current ripple.

Each module contains a synchronisation circuit, which synchronises the phase of multiple modules, to reduce the ripple at the common output. This synchronisation circuit uses a single wire (plus return) between the modules to provide an equal phase and current distribution. Initial conditions and disturbances determine the mutual position.

The proposed circuit is verified for two modules of 125[W] each. The stability of the synchronisation circuit for two DC/AC amplifiers is experimentally demonstrated.
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Preface

During the final phase of my study at the Technical University Eindhoven, Philips Centrum Fabrikage Technologie (CFT) gave me the opportunity to do my final project. This project concerned power electronics. This is the report of the project.

I thank my mentor at CFT Ir. J.W. Coenders and my mentors at the TUE P.J.M Smidt and professor Rozenboom for their support. I also want to thank my colleagues at CFT, specially my room colleagues John Compter and Lucas Koorneef.
### Abbreviations

<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>C</td>
<td>Capacitor which stands in parallel with the load</td>
</tr>
<tr>
<td>CFT</td>
<td>Centrum Fabrication Technology</td>
</tr>
<tr>
<td>DAC</td>
<td>Digital Analog Converter</td>
</tr>
<tr>
<td>DAP</td>
<td>Domestic Applications and Personal care</td>
</tr>
<tr>
<td>ECP</td>
<td>Electro Chemical Process</td>
</tr>
<tr>
<td>EMI</td>
<td>Electro Magnetic Interference</td>
</tr>
<tr>
<td>EPLD</td>
<td>Electrical Programmable Logic Device</td>
</tr>
<tr>
<td>$I_{res}$</td>
<td>Resonance frequency</td>
</tr>
<tr>
<td>HSS</td>
<td>High Side Switch of a half-bridge</td>
</tr>
<tr>
<td>$I_{inductor}$</td>
<td>Current which flows in the inductor of the half bridge</td>
</tr>
<tr>
<td>$I_{load}$</td>
<td>Current which flows in the load</td>
</tr>
<tr>
<td>$I_{set}$</td>
<td>Desired output current</td>
</tr>
<tr>
<td>L</td>
<td>Inductor connected with a half-bridge</td>
</tr>
<tr>
<td>$L_{load}$</td>
<td>Inductive element of the series impedance of the load</td>
</tr>
<tr>
<td>LSS</td>
<td>Low Side Switch of a half bridge</td>
</tr>
<tr>
<td>PCB</td>
<td>Printed Circuit Board</td>
</tr>
<tr>
<td>$R_{load}$</td>
<td>Resistive element of the series impedance of the load</td>
</tr>
<tr>
<td>$U_c$</td>
<td>Voltage across the capacitor C</td>
</tr>
<tr>
<td>$U_{supply}$</td>
<td>Voltage source which is connected to the half-bridge</td>
</tr>
</tbody>
</table>
Chapter 1

Introduction

This report describes the design of a high power amplifier. Domestic Appliances and Personal Care (DAP) Drachten makes in large numbers shaving heads. The shaving head is partly machined with ECP (Electro Chemical Processes) technique. ECP is a process for machining metals by anodic dissolution. The workpiece and the tool are held together; an electrolyte flows through the gap in between. When an electric current passes the electrolyte, the metal of the anode dissolves locally.

![Figure 1.1: ECP process](image)

The waveform of the electrical current has great influence on the ECP performance. Using high current pulses, with steep ramps, improves the process. So the power supply of the ECP process can be seen as a high power current amplifier.

DAP Drachten already uses a power amplifier, which was developed at CFT. There was a need for a redesign of the existing amplifier. The goals were: reducing costs and size, improving the electrical efficiency, the possibility of being used as a current or voltage source. Another requirement was the need for modularity. When an ECP process needs more current than one power supply can handle, more supplies shall be used in parallel.

DAP Drachten withdrew half way during the project, so an other application had to be found. The new application is to drive an actuator. The main difference between ECP and the actuator is the impedance of the load. The impedance of the ECP process is resistive, the impedance of the actuator is inductive.
In chapter 2 a topology, suited for the ECP demands, is chosen. Chapter 3 studies in depth the topology chosen. Because modularity was demanded, in chapter 4 the stability and effects of combining multiple supplies are described. In chapter 5, the chosen topology is worked out in an electrical scheme. To evaluate the performance of the proposed topology two modules were built. Measurements of the prototype can be found in chapter 6. Final conclusions and recommendations will be given in chapter 7.
Chapter 2

Topology Choice

In this chapter a topology suited for the ECP process will be chosen. The choice of the topology depends on many aspects and is certainly not a black/white case. Beside aspects as performance, price and simplicity also the "acceptance of the new concept" plays a role.

DAP Drachten already uses a high power amplifier for the ECP process. This amplifier was developed at CFT. So in the past CFT had chosen a topology. When CFT suggests a different topology, DAP Drachten wonders; "what is wrong with the old topology"?

2.1 Specifications

Specifications have first to be set up, before a topology can be chosen. The specifications are set up by DAP. Although DAP withdrew, still the DAP specifications are used as a reference.

This section is split into four parts namely; design goals, load impedance, specifications current mode and specifications voltage mode.

2.1.1 Design goals

DAP Drachten has the following goals:

- **Miniature.** The existing down converter and linear stage are bulky. Floor area has a price [ft/m²]. So, reducing the size of the power supply saves money.

- **Reduce Costs.** Costs are always important in an industrial environment. Costs can be split into fixed and variable costs. Fixed costs are mainly determined by the (number of) components used and by the PCB. Fixed costs
are once-only! Contrary to variable costs, which still return. An important variable cost is the electricity bill.

A small calculation of the effect of one percent efficiency improvement on the electricity bill.

Given; 100 power supplies of $50[A]$, $50[V]$. Relative On-time 0.2. $1[kWh] = \frac{fl}{0.25}$

$$\frac{1}{100} \cdot 356[\text{day}] \cdot 24[\text{h}] \cdot 50[A] \cdot 50[V] \cdot 0.2 \cdot 0.25[fl/kWh] = 10950 \left( \frac{fl}{\text{year}} \right) \quad (2.1)$$

- **Back-pulse** When the current is alternate, the tool dissolves instead of the workpiece. Normally, this is not a desired situation. However this reversed current (back-pulse) can also be used for cleaning the tool. A back-pulse is given after a number of normal pulses. This means that the topology must be suited for bipolar currents.

- **Modularity.** DAP needs a power supply, which can work as a current source or as a voltage source. Each supply can be seen as a module. Some processes need more current or voltage than one module can deliver. In this situation the modules can be used parallel (current mode) or in series (voltage mode). Putting together modules must be easy. For those who are familiar with windows $95M$; Just plug and play.

### 2.1.2 Current wave form

Fig.2.1. shows the desired current wave form for the ECP process. The dotted line represents the back-puls which is given after a number of normal pulses.

![Figure 2.1: Desired current wave form](image)
2.1.3 Current mode

<p>| | | |</p>
<table>
<thead>
<tr>
<th></th>
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</tr>
</thead>
<tbody>
<tr>
<td>Output current</td>
<td>0-50</td>
<td>[A]</td>
</tr>
<tr>
<td>Output voltage</td>
<td>max 50</td>
<td>[V]</td>
</tr>
<tr>
<td>Bandwidth</td>
<td>≥2</td>
<td>[kHz]</td>
</tr>
<tr>
<td>Overshoot</td>
<td>≤5</td>
<td>[%]</td>
</tr>
<tr>
<td>Ripple</td>
<td>2</td>
<td>[%]</td>
</tr>
<tr>
<td>Efficiency</td>
<td>≥90</td>
<td>[%]</td>
</tr>
</tbody>
</table>

Table of the desired specifications in the current mode.

2.1.4 Voltage mode

<p>| | | |</p>
<table>
<thead>
<tr>
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</tr>
</thead>
<tbody>
<tr>
<td>Output current</td>
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<td>[%]</td>
</tr>
<tr>
<td>Efficiency</td>
<td>≥90</td>
<td>[%]</td>
</tr>
</tbody>
</table>

Table of the desired specifications in the voltage mode.

2.2 Candidates

A few topologies have been examined. Linear solutions fell off, because of their high energy consumption. Finally, two candidates remained. These two candidates are further explained in the next sections. From these candidates, one has to be chosen. Aspects, which have played a role in the decision process were; experience with the concept, output zero current and simplicity of combining supplies.

2.2.1 Redesign existing power amplifier

As stated before, CFT has already designed a power amplifier for DAP Drachten. The principle of that power amplifier is explained with the aid of Fig.2.2. It consists of a buffer, a down-converter and a linear source. The down-converter is a 3-phase inverter connected to a three phase transformer. At the primary side of the transformer, an AC-current is generated by switching the MOS-fets. This current is uptransformed and rectified at the secondary side. Control of the current is done by varying the switching frequency.

The down-converter delivers a current, which is used for the ECP process. If the converter delivers more current, the capacitor in parallel with the down converter is charged. The current is controlled, so that the voltage across the capacitor is equal to the process voltage plus a fixed voltage. The linear source needs the
voltage drop, to work properly. In short; the coarse current is delivered by the converter, fine shaping is done by the linear source.

This concept has three major disadvantages. First, a relatively high voltage drop is necessary across the linear source, which causes unwanted energy losses (≈30%). The second disadvantage is caused by the down-converter. The current is controlled by varying the switching frequency. Zero current (together with zero voltage) coincides with an infinitely high frequency, which is in practice not possible. The last problem is that the current is rectified and can not be reversed.

A redesign could eliminate the linear source. The two other problems still remain.

### 2.2.2 Half bridge

Another candidate was the half-bridge. The principle of the half-bridge is declared with the aid of Fig.2.3. The current $I_1$ is called positive when flowing into the load. The circuit consists of two switches, an inductor and a capacitor. The load is modelled as an inductor in series with a resistor. The switches $S_1$ and $S_2$ are closed alternately.

![Half bridge](image)

Figure 2.3: Half bridge

When switch $S_1$ conducts, the current increases. The situation changes when $S_1$ is switched off and $S_2$ is switched on. The polarity of the voltage across the inductor is reversed. Due to the inductor, the current $I_1$ will not immediately reverse, but
decrease with a fixed slope. When $S_2$ is switched on, the current commutates from the $+U_{supply}$ to the $-U_{supply}$. This is called DC-commutation. Of course $S_1$ and $S_2$ may never conduct simultaneously.

**Control of the half-bridge**

Generally, there are three methods to control a half-bridge, namely Puls Width Modulation (PWM), hysteresis switching and resonant switching. Width PWM and hysteresis switching, the controllable switches are operating in a switch mode where they are required to turn on and off the entire load current. In this situation the switches are subjected to high switching stresses and high switching power loss. Another drawback is the electromagnetic interference (EMI) produced due to the large di/dt and du/dt.

These drawbacks are avoided when switching at the inductor current levels of zero and at $I_{peak}$. Fig.2.4. shows the current shape through the inductor. With this switching scheme, the half-bridge acts as a current source, with an average current of $\frac{1}{2}I_{peak}$.

When zero current is requested, a problem arises. The switching frequency tends to infinite. Therefore zero current is made by switching between $+I_{peak}$ and $-I_{peak}$. Now the average current equals zero. Of course, in this situation there are switching losses but they are minimised when $I_{peak}$ is chosen as low as possible with minimal current.

![Figure 2.4: Critical discontinuous current of the inductor in the half-bridge](image)

Drawback of the control method of Fig.2.4. is the large ripple of $\frac{1}{2}I_{peak}$. However, this ripple can be decreased by using more "modules", when the current peaks are equidistant (see Fig.2.5). By using more modules also the ripple frequency increases.

**2.3 Final choice**

DAP Drachten redrew. This fact simplified the decision, because now there was no need to justify the chosen topology to DAP Drachten. The same topology will be used for the new specification.
Figure 2.5: Total current shape, with two modules

The new electrical characteristics of the load are an inductor of $30\,\text{mH}$ in series with a resistor of $5\,\Omega$. This impedance is that of the MiniLimms. MiniLimms is a linear actuator, which has been developed at CFT. This specification deviates from the ECP process. The load in the ECP process is resistive.

The half-bridge topology has been chosen. At CFT, there is experience with a three phase half-bridge, which also uses critical discontinuous switching. New aspect is the synchronisation mechanism.
Chapter 3

Smartcell

This chapter will study more in depth, the critical discontinuous switched half-bridge. Topics are to find the dimensions of the components of the half-bridge, to calculate the power losses and the theory to control the half-bridge. However, started is with the description of the smartcell.

3.1 Description of Smartcell

Smartcell is a simple current source module. The DC/AC (DC/DC) module works with a half-bridge. High efficiency is obtained by switching at zero current and voltage. Unfortunately, zero current switching introduces a relatively large ripple. To obtain more current than one amplifier can deliver, smartcells can be used in parallel. So, smartcells can be used autonomously or in parallel. To reduce the output ripple, the modules are synchronised. The synchronisation circuits only need a single wire (plus return), between the different modules. So there is not a master, which has a total survey. Fig.3.1. identifies the major functional blocks of "smartcell".

![Figure 3.1: Block scheme of smartcell](image-url)

16
The smart cell consists of a fast "inner" loop, which controls the switching of the half bridge. Therefore the current which flows in the inductor is compared with given levels, \( I_{\text{high}} \) and \( I_{\text{low}} \). \( I_{\text{high}} \) and \( I_{\text{low}} \) are generated by a block called "level shift". This block translates the output of the PID into the two switching levels. Delays in this inner loop are minimised.

The exterior of the inner loop consists of an outer slower loop. In this loop the current, which flows into the load, is fed back. This feedback information is used to control \( I_{\text{load}} \).

Furthermore there is a circuit which controls the synchronisation of the amplifier. A single wire is used for communication between the modules. The multiple modules concept is worked out in the next chapter.

### 3.2 MOSFETS

In practice the switches are electronic devices like, power MOS-FET's or IGBT components. These components are not ideal. Most important restraint is the time delay for switching the devices. So a MOS-FET nor an IGBT can change its state (open or closed) in a infinitely small time.

Mosfets will be used as switching devices. The body diodes of the mosfets take part in the switching actions. Fig.3.2. shows the half-bridge with the diodes.

![Figure 3.2: Half bridge with MOSFET's](image)

When \( S_1 \) is closed the current increases. At a given level, \( S_1 \) is opened. Now the current is taken over by diode \( D_2 \). The voltage drop across the mosfet equals the forward voltage of the body diode. Next step is to close \( S_2 \). When \( S_2 \) is closed the current through \( D_2 \) is taken over by \( S_2 \). When the current reaches zero \( S_2 \) is opened. In practice, a time delay causes the current to become negative. The previous sequence will repeat.
3.3 Specifications for one Smartcell

To evaluate the theory and performance of the smartcell four scale models will be built. This number is quite arbitrary. However, with an even number and when no output is required \((I_{set}=0)\), the theoretical current ripple is almost zero. The next table shows the desired overall parameters. With four cells, the maximum current of the smart cells become \(4 \cdot 2.5 = 10 \text{[A]}\). Note; the supply voltage is quite arbitrary, but must be larger than the desired output voltage.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>(U_{\text{supply}})</td>
<td>(\pm 100 \text{[V]})</td>
</tr>
<tr>
<td>(U_{\text{load}})</td>
<td>50 \text{[V]}</td>
</tr>
<tr>
<td>(I_{\text{load}})</td>
<td>(\pm 2.5 \text{[A]})</td>
</tr>
<tr>
<td>(f_{\text{min}})</td>
<td>10 \text{[kHz]}</td>
</tr>
<tr>
<td>(f_{\text{max}})</td>
<td>150 \text{[kHz]}</td>
</tr>
<tr>
<td>Bandwidth</td>
<td>(\geq 2 \text{[kHz]})</td>
</tr>
</tbody>
</table>

3.4 Components \(L\) and \(C\)

In this section the component values of the inductor \(L\) and capacitor \(C\) of smartcell are determined.

3.4.1 Inductor \(L\)

The inductor \(L\) and the capacitor \(C\) in Fig.3.2. form a lowpass filter. The voltage across the capacitor (equal to \(U_{\text{load}}\)), is considered as constant during switching. This assumption is valid when \(f_{\text{switching}} \gg f_{\text{resonance}}\). The current slope is determined by the supply voltage, the inductor value and the output voltage.

\[
U_{\text{inductor}} = L \frac{di}{dt}
\]  

(3.1)

The switching frequency depends on \(I_{\text{peak}}, U_{\text{load}}\) and \(U_{\text{supply}}\).

\[
T = LI_{\text{peak}} \left( \frac{1}{U_{\text{supply}} - U_{\text{load}}} + \frac{1}{U_{\text{supply}} + U_{\text{load}}} \right) \]  

(3.2)

\[
f_{\text{switching}} = \frac{1}{T} = \frac{U_{\text{supply}}^2 - U_{\text{load}}^2}{2I_{\text{peak}}LU_{\text{supply}}} \]  

(3.3)

The minimum frequency occurs at maximum \(I_{\text{peak}}, \text{maximum } U_{\text{load}}\) and minimum \(U_{\text{supply}}\). So the maximum value of \(L\) is determined.

\[
L = \frac{U_{\text{supply}}^2 - U_{\text{load}}^2}{2I_{\text{peak}}U_{\text{supply}}f_{\text{switching}}} = \frac{100^2 - 50^2}{2 \cdot 5 \cdot 100 \cdot 10^3} = 750 \mu \text{H} \]  

(3.4)
Chosen is for a inductor 200[\mu H] to maintain proper functioning at a lower supply voltage and to simplify the inductor design. The inductor has been designed with the aid of the software program "CONV". A RM14i core has been used, with 33 turns of 160*0.071[mm²] wire. This litze wire reduces the skin and proximity losses. Appendix A. shows the output of CONV.

3.4.2 Capacitor C

The capacitor C smooths the current pulses of the inductor. The filtering depends on the ratio between the impedance of the capacitor and the impedance of the load. Worst case occurs with minimum switching frequency (10kHz).

\[
\frac{Z_{\text{load}}}{Z_{\text{capacitor}}} = \frac{2\pi f L_{\text{load}}}{\frac{1}{\frac{2\pi f C}}}
\]  

(3.5)

In the next section it will be shown that the value of C affects the bandwidth of the system. For maximum bandwidth, C has to be as small as possible.

The output ripple (2\%) is determined by the capacitor (and \(L_{\text{load}}\)). Simulations with CASPOC give a minimum value of the capacitor of 3\mu F. CASPOC is a simulation program for electronic power circuits. This gives a ratio of

\[
\frac{Z_{\text{load}}}{Z_{\text{capacitor}}} = \frac{2\pi \cdot 10^3 \cdot 30 \cdot 10^{-3}}{\frac{1}{2\pi 10^3 3 \cdot 10^{-6}}} = 355
\]  

(3.6)

3.5 Total power losses

Minimising energy losses is an important aspect. This section estimates the power losses in the smart cell. The main losses are caused by the switching devices and the inductor \(L\). Losses in the switching devices and inductor \(L\) are estimated. Losses depend on the desired current and voltage output level. One extreme situation is examined; full load (\(U_{\text{load}} = 50[V], I_{\text{max}} = 2.5[A]\)).

3.5.1 Power losses in switching devices

In switching applications the total power dissipation is composed of switching losses and on-state losses. At low frequencies the MOS-FET switching losses are small enough to be ignored. However, as frequency increases the losses will eventually become significant. In our concept the on-state losses are dominant, with maximum current and low frequency. However, with minimum power output, the switching losses predominate. Appendix B estimates the power losses in the switching devices. Fig.3.3. shows the main results.
3.5.2 Losses in the inductor $L$

Power losses in the inductor are determined with the aid of the simulation software CONV. With the parameters: core type, core material, winding number, wire type, airgap and current shape the program calculates the losses in the inductor at maximum output power.

Losses are split into; core losses (hysterese), winding losses and high frequency (hf) losses from skin and proximity effects. A pie diagram shows how the total losses of the inductor are composed of different loss sources. This is done for a triangular current of $I_{\text{top-top}} = 1\, \text{A}$ with a frequency of 125[kHz] (Fig. 3.4A) and a triangular current $I = 0\, \text{A}-6\, \text{A}$ with a frequency of 10[kHz] (Fig. 3.4B). Appendix A. displays the complete output of CONV.

Figure 3.4: Power losses [mW] in the inductor, A) no load, B) maximum load.

3.6 Dynamic model of the smart cell

As stated before, a good model of the power circuit is essential to guarantee stability and enhance performance. The model of the single cell is obtained in two different ways.
1. A model valid for $f_{\text{switching}} \gg f_{\text{res}}$ of the $L_{\text{load}}C$-filter.

$$f_{\text{res}} = \frac{1}{2\pi \sqrt{L_{\text{load}}C}} \quad (3.7)$$

2. A non-linear discrete time-model [1], [2].

The first method has more advantages compared to the second. The second method requires a large number of calculations, in contradistinction to the first method. The first method also gives more insight into the problems. A drawback of method one, is the validity of the model for switching frequencies in the neighbourhood of $f_{\text{res}}$ of the LC filter. Method 2 is also based on simplifications. Therefore the exact non-linear discrete time-model also loses its validity at $f_{\text{res}}$.

3.6.1 Estimated linear model

The half bridge is switched, between $I_{\text{inductor}}=0$ and $I_{\text{inductor}}=I_{\text{peak}}$. Due to the switching control, the half-bridge acts as an current source, with a large rimple. If we assume $f_{\text{switching}} \gg f_{\text{res}}$, then the capacitor $C$ and the inductor $L$ act as a low-pass filter (see Fig.3.2). The LC-circuit now is inductive. The high-frequency components of the inductor current ($L$) are attunated, so the cell can be seen as a continuous current source, under the constraint $f_{\text{switching}} \gg f_{\text{res}} (L, C)$ and $Z_{\text{load}} \gg Z_{\text{capacitor}}$ at $f_{\text{switching}}$. The average current is equal to half $I_{\text{peak}}$.

![Figure 3.5: Equivalent circuit](image)

The half-bridge with inductor is replaced by a current source, parallel to a capacitor. Fig.3.5. shows the circuit. Now the transfer functions become:

$$\frac{U_c}{I_{\text{peak}}'} = \frac{1}{2} \frac{sL_{\text{load}} + R_{\text{load}}}{s^2L_{\text{load}}C + sR_{\text{load}}C + 1} \quad (3.8)$$

$$\frac{I_{\text{peak}}}{I_{\text{load}}'} = \frac{1}{2} \frac{1}{s^2L_{\text{load}}C + sR_{\text{load}}C + 1} \quad (3.9)$$

In the denominator we recognise a second order circuit with the well known parameters $\beta$ and $\omega_0$.

$$H(s) = \frac{1}{s^2 + 2\beta \omega_0 s + \omega_0^2} \quad (3.10)$$

$$\beta = \frac{1}{2} \frac{R}{\sqrt{\frac{C}{L}}} \quad \omega_0 = \sqrt{\frac{1}{LC}} \quad (3.11)$$

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Feedback of $U_c$

The response of the system with a small $\beta$ gives large overshoot at the resonance frequency of the capacitor and the inductor of the load. The overshoot is reduced when $U_c$ is fed back. In mechanics terms, this is called velocity feedback. Fig.3.6 shows the block diagram. The new transfer function becomes:

$$\frac{I_{load}}{I_{peak}} = \frac{1}{2L_{load}C} \frac{1}{s^2 + s \left( \frac{R_{load}}{L_{load}} + \frac{K_d}{C} \right) + \frac{1+K_d R_{load}}{L_{load}C}}$$

(3.12)

Figure 3.6: Transfer function with $K_d$ feedback

Feedback of $U_c$ changes the second order parameters $\omega_0$ and $\beta$, see Eq.3.13. The natural frequency increases slightly with $K_d$. However, $K_d$ has a large effect on the damping factor $\beta$. If $K_d$ increases, the damping of the system will also increase, so the overshoot decreases.

$$\beta = \frac{1}{2} \frac{1}{L_{load}C} \frac{R_{load}C + K_d L_{load}}{1 + R K_d}$$

$$\omega_0 = \sqrt{\frac{1 + K_d R_{load}}{L_{load}C}}$$

(3.13)

Figure 3.7: Simplified transfer function, with $K_d$ feedback.

Desired is a critical damped system with $\beta = \frac{1}{\sqrt{2}}$. With $K_d=0.01$, Eq. 3.13 becomes $\omega_0=2\pi 563$ [rad/s] and $\beta=0.6$. A $\beta$ of 0.6 means a slightly resonant peak in the frequency domain.

The model can be made more accurate by introducing a dead time. The system only reacts at discrete time steps. So there is a time delay between supply and demand. The average time-delay is equal to half the period of the switching frequency. This delay is not a fixed parameter, but depends on the desired load current. Worst situation, occurring at a maximum current through the load (minimum switching frequency), will give a delay of approx $\frac{1}{2 \times 10^3 \text{kHz}} = 50 \mu s$. 
3.6.2 Sampled-data representation

Also a sampled-data representation is calculated. This model describes perturbations about a nominal cyclic steady state. In App. C step by step procedures of the method are presented. Although this model has not been used, it could be useful for further investigations.

3.7 Controller I-mode

To meet the bandwidth specification, a controller has to be designed. This section describes the development of the controller for the current mode of smartcell.

Fig. 3.8 shows the bode diagrams of the power system, with $K_d$ feed back. The bandwidth is defined as the minimum frequency where the closed loop reaches the -3dB point or 90°, which ever come first. (Closed loop: transfer function of Fig. (3.7.) with controller). In theory the system is never unstable, because the phase shift of 180° is never reached. However, in practice, small delays will cause 180° degrees phase shift, and thus potential instability.

![Bode Diagram](image)

Figure 3.8: Simulated Bode diagram of Fig.3.7.

The -3dB point (563[Hz]) is determined by $C$ (3μF) and $L_{load}$ (30mH). The inductor is determined by the load and cannot be changed. Only the capacitor can be varied. However when the capacitor is chosen too small, the model of the discontinuous switching half-bridge loses its validity.

A limitation of smartcell is the voltage of the half-bridge. This voltage determines the current which can be handled. The impedance of the inductor is proportional to the frequency. With the given half-bridge voltage and the given inductor value, the maximum current, which can be handled at the desired bandwidth of 2[kHz]
is

\[ I_{\text{peak}} = \frac{U_{\text{peak}}}{|Z|} \]  

where \( Z = \sqrt{(L\omega)^2 + R^2} \) \hspace{1cm} (3.14)

For \( U_{\text{peak}}=100\,[\text{V}] \), \( f=50\,[\text{Hz}] \), \( L=30\,[\text{mH}] \) and \( R=5\,[\Omega] \), \( I_{\text{peak}} \) is only 265[mA]! With an DC-bias the situation tends to be worse, because the voltage swing decreases.

### 3.7.1 PID

For control of the steady state and transient errors a PID controller is used, see Fig.3.9. The PID controller is split into a lead and an integrator part.

\[
\text{Figure 3.9: Total transfer function}
\]

The transfer function of the PID controller is:

\[
H_{\text{control}} = K_p \left( \frac{s + \frac{1}{\tau_{\text{lead}}}}{s} \right) \left( \frac{s + \frac{1}{\tau_{\text{lead}}}}{s} \right)^{0.5} \left( \frac{(s+R+K_d)(s+R+K_d)}{\tau_{\text{lead}}} \right) \frac{L}{C} \]

\hspace{1cm} (3.15)

Where \( \gamma > 1 \)

To increase the bandwidth the lead compensation is used. The lead compensation lifts the phase. The frequency where the phase is maximum, is given by:

\[
\omega_{\text{max}} = \frac{\sqrt{\gamma}}{\tau_{\text{lead}}} \]  

(3.16)

with a maximum phase contribution of

\[
\sin\phi_{\text{max}} = \frac{\gamma - 1}{\gamma + 1} \]  

(3.17)

Fig.3.10. shows a the (stylised) bode plot of the controller. Fig.3.11. shows the stylised bode plot of the controller plus the half-bridge (=plant). The bodediagram of the plant is lifted up 6[dB]. This is caused by the implementation and will be explained in section 5.6

The maximum phase contribution occurs midway between the break-point frequencies \( f_2 , f_3 \). Maximum phase contribution is desired at the desired bandwidth, 2[kHz]. With \( \gamma=6 \), the break-point frequencies are known, \( f_2=800\,[\text{Hz}] \) and \( f_3=4800\,[\text{Hz}] \). With a slope of 6[dB]/decade (first order), \( A_2 \) equals \( A_1+16\,[\text{dB}] \).
The phase contribution at 2[kHz] is 58°. An openloop gain (controller+plant) of 0[dB] at 2[kHz] will give a closed loop response of about [-3dB]. The open loop gain of the plant equals -22[dB] at 2[kHz]. Now A1 and A2 are known, A1=22-6=16[dB], A2=22+6=28[dB].

The lag compensation is used to minimise steady state errors. The lag part may not have a phase contribution when the lead part already has started. Breakpoint $f_1$ is placed at 80[Hz].

The controller is a bottleneck of the system. The controller is designed for a specified load. When the induction, $L_{load}$, decreases, the crossover frequency (-3dB) increases. When the crossover frequency is greater than the frequency $f_3$ of the controller, the phase shift of the system plus the phase shift of the controller reaches $-180°$. With an openloop gain of more than unity, the gain margin

\[
H_{\text{integrator}} = \frac{(s + 2 \cdot \pi 60)}{s} \quad H_{\text{lead}} = \frac{(s + \frac{1}{6} \cdot 2\pi \cdot 4.8 \cdot 10^4)}{(s + 2\pi \cdot 4.8 \cdot 10^4)}
\] (3.18)
becomes marginal. Another problem occurs when the crossover frequency of the plant lies left of $f_2$. The phase of the integrator plus the phase of the plant cross $-180^\circ$. Conclusion; for proper functioning a proper induction must be connected to the output.

### 3.8 Protections

Only the minimum switching frequency of the half-bridge will be protected. When the capacitor is charged, the voltage across the capacitor can reach the supply voltage. In this situation the voltage drop across the inductor is too small and $I_{\text{inductor}} = I_{\text{peak}}$ will never be reached! So the upper switch remains closed. Now an unwanted situation occurs. The current will decrease to zero and reverse direction. An oscillation starts with a frequency of $f = \frac{1}{2\pi}\frac{1}{\sqrt{L_{\text{load}}C}}$.

The minimum switching frequency is protected by measuring (indirectly) the voltage drop across the inductor. The voltage drop directly determines the current rise/fall time (slope) $[A/s]$. If the voltage drop is smaller than a fixed voltage, the switches are toggled on/off (depends on the previous state), whether $I_{\text{peak}}$ is reached or not. Note that now there is a kind of "protection mode", so the previous model in section 3.6 loses its validity.

#### 3.8.1 Timing in the protection mode

When smartcell gets into the "protection mode", other problems arise with the existing configuration.

In the protection mode the voltage drop across the inductor, $|U_{\text{capacitor}} - U_{\text{supply}}|$, becomes too small. See also Fig.3.2. As a result the current in the inductor increases/decreases slowly.

Now the protection comes into action and demands toggle, regardless of the value of inductor current. The inductor current will not have reached $I_{\text{peak}}$. When the half-bridge is toggled, the voltage drop across the inductor will have a value of about twice $|U_{\text{supply}}|$. So current increases/decreases with a steep slope. Now the system works normally and switch when the inductor current reach his desired value.

One cycle is not sufficient to discharge or charge the capacitor to a safe voltage level $(U_c)$. As a result the protection mode still remains, so the protection demands toggle! Switching will occur as fast as possible, only limited by internal delays. Conclusion; the protection circuit which guards the minimum voltage drop of the inductor has to be inactive for some time. This time must be smaller than the period of the minimum switching frequency.
Bibliography


Chapter 4

Multiple Smart Cells

When a ECP process needs more current than one power supply can handle, more smartcells can be used in parallel. For minimum output current ripple, the triangle shaped output currents have to be equidistant in time. Beside the reduced ripple, the ripple frequency increases to twice the switching frequency of one module. A higher frequency ripple requires a simpler low-pass filter.

Synchronisation needs an extra control circuit. This chapter describes the control principle, which keeps the current triangles equidistant. To maintain modularity, this circuit has to be independent of the number of paralleled smartcells.

4.1 Principle

Fig.4.1 shows the inductor current of two smartcells. A small $\Delta I$ is applied to the input of one smartcell. The position of the current top (A) changes with respect to his neighbour (B). The dotted line represents the trajectory (A), when no $\Delta I$ was applied. The current top of A is changed in relation to the current of smartcell B. So by changing $I_{peak}$ the output current can be synchronised! In other words, the phase between the different modules is changed by changing the frequency of a module. When a module has information about its position, it can control its phase. Fig.4.2. shows a block diagram of the control system.

For convenience the triangular shaped currents can be represented as racecars on a circular race circuit. The distance in time between the top of the triangular currents, represents the distance between the cars. When the period of all currents is equal, the length of the racecircuit is equal to this period.

In our race model, the distance between the cars has to be equal. Each "car" has to slow down or speed up until its distance between the car in front is equal to the car behind. Speed up coincides with a lower frequency, slow down with a higher frequency.
A $\Delta I$ can be applied at the current top, current bottom or both. The half-bridge switch at zero inductor current to prevent forced commutation of the body diode current. Therefore applying a $\Delta I$ at the bottom may cause forced commutation. Therefore, chosen is to change the current level at the current top only. Now the synchronisation control affects directly $I_{load}$. In practice each car has its own synchronisation mechanism. When a car has to speed up, another car has to slow down. So the resulting effect on $I_{load}$ is cancelled.

4.1.1 Measuring position

When the half-bridge commutates from conducting the high side switch (HSS) to the low side switch (LSS) ($I_{peak}$), a small "synchro" pulse is generated. When a
positive current is demanded the pulses are given at $I_{peak}$, with a negative current the pulses are given at zero current. Only positive currents will be considered.

When a module has the possibility to measure the time between his pulse and the pulses given by its neighbours, he posseses all the information in order to determine its position.

Each module measures the time difference between its own synchro pulse and the pulses of its neighbours. This information becomes available after the pulse of the last neighbour. The time-error signal is translated into current level. Together with $I_{set}$ it forms the demanded current of a module.

Time-error information becomes available in discrete time-intervals. Feedback information is not used at once, but must wait until $I_{peak}$ is reached.

### 4.2 Control algorithms

As stated before we want modularity, so we do not want a master (dictator). A driver must work autonomously. So a driver has to know his position in respect to the car in front and behind.

Two control algorithms were simulated in CASPOC. CASPOC is a software program for simulation of electric circuits and dynamic systems. In the first algorithm (Fig.4.4A), the relative position is determined. The second algorithm (Fig.4.4B) has no preference in which order the cars are driving. Initial conditions determine the sequence.

![Diagram](image)

**Figure 4.4: Algorithm 1 and 2**

**Algorithm 1.** Four cars are labeled A, B, C and D. The cells are hardwired in a circle, so the position of the cars are fixed. Each driver wants to drive exactly between the car in front of and the car behind. Simulations with CASPOC have shown an unexpected stable mode. At the end, the drivers A, B, C and D drove along each other. Distance between the cars A and B, B and C, C and D, D and A were equal. So the enforced conditions were fulfilled. This unexpected state is unwanted, but legal!
Another problem occurred when a large external disturbance was applied. When a car passes another car, for example B passes C, B speeds up, instead of slowing down. B passes D and A, until it drives (old situation) between A and C. In the mean time the complete loop is disturbed, which is not a desirable situation.

**Algorithm 2** All cells deliver a pulse on the wired-or bus, when they reach the current top ($I_{peak}$). Fig. 4.4B shows the principle of algorithm 2. Initial conditions and disturbances determine the mutual position between the current triangles. The pulse in front of his own pulse and the pulse behind gives a cell the information of his position between his neighbours. From the information of the bus, a car knows the position of his neighbours.

When a car passes another car, i.e. caused by a disturbance, a new arrangement occurs. At start up, this system will also reach a stable situation faster. Therefore, algorithm 2 will be implemented in the prototype.

### 4.3 Model identification

A model of the "phase control" is necessary to guarantee stability. All smartcells together can be seen as a multiple-input multiple-output system (MIMO). Each cell has as input $I_{set}$ and as output, its position error (in seconds) between the driver in front off and behind. One situation, with two modules will be examined. In this situation one module is freerunning (A) and the other module (B) locks to cell A.

Information of the position of a car, is not continuously available. Information becomes available in discrete steps. In this way we can treat the system as time discrete.

Fig.4.5. shows the inductor current of two modules and the output of the phase comparator. At $t_1$ a $\Delta I$ is applied at one input. Both cells react in time. The output of the cell A where the input has been disturbed is equal to;

$$y_1(t_2) = D_1 - D_2 = \left( I_{set}\frac{di}{dt} + \Delta I\frac{di}{dt} \right) - \left( I_{set}\frac{di}{dt} - \Delta I\frac{di}{dt} \right)$$

$$y_1(t_4) = D_3 - D_4 = 4\Delta I\frac{di}{dt}$$

The output diagram, Fig.4.5. is split into intervals. The time intervals are equal to the period of module B. The output ($h(nT)$) of an input pulse $\Delta I$ of unity height, translated into the $z$-transferfunction.

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Figure 4.5: Impulse response synchronisation circuit

\[ H_1(z) = \sum_{n=0}^{\infty} h(nT)z^{-n} \]  
\[ H_1(z) = \frac{d^{i-1}}{dt} \left( \frac{0}{z^0} + \frac{1}{z^1} + \frac{2}{z^2} + \frac{2}{z^3} + \ldots + \frac{2}{z^\infty} \right) \]

Simplifying the result;

\[ H_1(z) = \frac{d^{i-1}}{dt} \left[ \left( \frac{2}{1-z^{-1}} \right) - \left( 2 + \frac{1}{z} \right) \right] = \frac{d^{i-1}}{dt} \frac{z + 1}{(z-1)z^1} \]

The slope \( \frac{di}{dt} \) depends on the supply voltage and the inductor value.

\[ \frac{di}{dt} = \frac{U_{\text{supply}}}{L} = B^{-1} \]

Fig.4.6. shows the rootlocus of the transfer function of 4.6. The settling time is minimal and there is no overshoot at the breakout point \( K_1 \). At \( K_2 \) the rootlocus leaves the unit circle \( |z|=1 \), the system gets unstable. The values of \( K_1 \) and \( K_2 \) can be calculated with the equation;

\[ 1 + H(z)K = 0 \Rightarrow z^2 + z(BK - 1) + BK = 0 \]

**K1**

At the breakout point, the discriminant of Eq. 4.8 equals zero.

\[ D = 0 \Rightarrow (BK)^2 - 6BK + 1 = 0 \]
\[ BK_1 = 6 - \sqrt{36 - 4} = 0.17 \]
\[ BK_2 = 6 + \sqrt{36 - 4} = 5.8 \]
Figure 4.6: Rootlocus of phase transfer function

Only $B K_1$ is useful, at $B K_2$ the poles come together at the real axis.

$$B = 2 \times 10^{-6} \quad K_1 = \frac{B K_1}{B} = 0.17 \cdot 0.5 \cdot 10^6 = 34 \cdot 10^3 \left[\frac{V}{s}\right] \quad (4.12)$$

**K2**

At K2 the solution of Eq. 4.8 fulfills the condition $|z| = 1$.

$$z = -j \quad \Rightarrow K_2 = \frac{1}{B} = 2 \cdot 10^6 \left[\frac{V}{s}\right] \quad (4.13)$$
Chapter 5

Implementation

In the previous chapters, the ideas and theory of smartcell were explained. This chapter treats the practical implementation. This is done with the aid of a block diagram, placed in appendix D. In the next sections the different blocks are translated into an equivalent electrical circuit. Netnames in the text will be named as UXXX-Y, where UXXX refers to the component number and Y refers to the pin number.

5.1 Measurements of variables

This section describes the measurements of variables used to control smartcell. Values which have to be measured are \( I_{\text{inductor}} \), \( I_{\text{load}} \) and \( U_C \). Fig 5.1 shows the definitions.

Deviations in these measurements cause switching decisions at wrong current levels, which give degradation of the system performance. Measurements for protections will be described in section 5.7. Current measurements shall have a ratio of one, which means 1[V] coincides with 1[A].

![Figure 5.1: Definitions of variables](image)

Generally, there are two ways to measure a current, namely by means of either a resistor or a current sensor.
The resistor is placed in the current path, where the voltage drop across the resis­t­tor is proportional to the current. Advantage of this method is its simplicity. Dis­ad­vantage is the dissipation of power, which makes this method less suitable for measuring large currents. The resistor solution also demands a differential amplifier, because (often) none of the measuring points can be connected to earth. DC-currents can also be measured with a module, which works with a compensation principle (often called LEM). The current $I$, to be measured, is surrounded by a magnetic circuit. This flux is detected by a hall-sensor. There is a second compensation winding on the magnetic circuit. A compensation current is applied to this winding to keep the magnetic flux zero. So this current is proportional to the current to be measured. Advantages are; galvanic isolation, suited for large currents and freedom of connecting the compensation winding. Drawbacks are the size, limited bandwidth, DC-offset and the price.

5.1.1 $I_{\text{inductor}}$

Measuring $I_{\text{inductor}}$ is the most difficult. With $I_{\text{load}}=0\,[\text{A}]$ (no load), $I_{\text{inductor}}$ has a low amplitude and a high frequency spectrum with no DC-component. With $I_{\text{load}}=2.5\,[\text{A}]$ (maximum load) this situation reverses. The inductive impedance of the load in parallel to the capacitor of the half-bridge, limits the bandwidth of $I_{\text{load}}$. The low-frequency components ($<2\,[\text{kHz}]$) of $I_{\text{inductor}}$ flow in the load, the high frequency components flow in the capacitor.

The current $I_{\text{inductor}}$ is composed of the current $I_{\text{load}}$ and $I_{\text{capacitor}}$ (Kirchhoff). For control of $I_{\text{load}}$, $I_{\text{load}}$ has to be measured. So, by measuring $I_{\text{capacitor}}$ as well, $I_{\text{inductor}}$ can be reconstructed. Fig. 5.2 shows a block diagram of the measuring circuit. The complete circuit diagram can be found in App.G.

![Diagram](image)

Figure 5.2: Block diagram of measuring circuit of $I_{\text{capacitor}}$ and $I_{\text{load}}$

The resistors (R430/R431), App.H, are placed in series with the load. To obtain the value of $I_{\text{load}}$ the voltage drop across both resistors (R430/R431) is measured. The resistors are implemented in a SMD package and have a value of $51\,[\text{m\Omega}]$ (5%,
Itnductor

\[ I_{\text{inductor}} = I_{\text{load}} \cdot (R_{430} + R_{431}) \cdot G_4 \cdot G_3 + I_{\text{capacitor}} \]  

(5.1)

\[ I_{\text{load}}^* = I_{\text{load}} \cdot (R_{430} + R_{431}) \cdot G_4 \cdot G_3 \]  

(5.2)

The impedance of the measuring resistors is relatively low with respect to the impedance of the load at maximum frequency of \( I_{\text{load}} \). The ratio of common mode voltage versus differential mode voltage is equal to the ratio of both impedances.

\[ 20 \log \left( \frac{U_{\text{common}}}{U_{\text{differential}}} \right) = 20 \log \left( \frac{|Z_{\text{load}}|}{|Z_{\text{resistor}}|} \right) \]  

(5.3)

An extreme situation occurs with maximum frequency (2[kHz]) of \( I_{\text{load}} \). With \( L_{\text{load}} = 30[\text{mH}], f = 2[\text{kHz}] \) and \( R_{430} + R_{431} = 0.102[\Omega] \), Eq. 5.3 becomes 72[dB]! So a high common mode rejection ratio (CMRR) of the differential amplifier is required.

As differential amplifier the INA117 is used, followed by two opamps U440 and U450. The INA117 is a precision unity-gain difference amplifier with very high common-input voltage range (±200V) and a bandwidth of 200[kHz]. At 2[kHz] the common-mode rejection ratio is (still) 80[dB]. So there is only a difference of 8[dB] between the common mode voltage and the differential voltage. Therefore, to improve the CMMR, the INA117 is provided with an extra potentiometer. Unfortunately a potmeter has to be trimmed for maximum CMMR.

To obtain a ratio of 1[V/A], the output of the INA has to be amplified with a gain of \( \frac{1}{0.102} \). Therefore, the gain, \( G_2 \) and \( G_3 \), is set to \( \frac{1}{0.102} \).

\[ G_2 = \frac{R_{441}}{R_{442} + R_{443}} \]  

(5.4)

\[ G_3 = \frac{R_{452}}{R_{450} + R_{451}} \]  

(5.5)

5.1.2 \( I_{\text{capacitor}} \)

Because the current \( I_{\text{capacitor}} \) has no DC-component, a current transformer is used. Advantages of a transformer are freedom of connecting the secondary side to the analogue earth and galvanic isolation. The primary side of the trafo is placed in series with the capacitor. The secondary side is terminated with a low ohmic resistor, \( R_T \). The voltage drop across the resistor is proportional to the current in the primary winding.

\[ -I_{\text{capacitor}}^* = I_{\text{capacitor}} \cdot \frac{1}{N} \cdot R_T \cdot G_1 \]  

(5.6)

No suitable commercial products were found, so the current trafo was home-made with a small ferrite core. The minimum value of the bandwidth has to be 300[Hz] at
least. With this specification it is possible to measure at the resonance frequency of $L_{load}$ and the capacitor ($L_{load}=30\,[\text{mH}], C=3\,[\mu\text{F}], f_{osc}=520\,[\text{Hz}]$. Design and specification of the current transformer are placed in appendix E.

The voltage drop across the resistor is measured with a differential amplifier, built around $U400$, $U410$ and $U420$. The current transformer has a current transformation ratio of $\frac{1}{80}$ and is terminated with $3\,[\Omega]$. This gives a voltage current ratio of $3/80\,[\text{mV/A}]$. So, the amplifier ($G_3$) has to have a gain of $80/3$. The gain of the amplifier is determined by:

$$G_3 = \left( \frac{R_{404} + R_{405} + R_{410}}{R_{405}} \right) \left( \frac{R_{421}}{R_{420}} \right)$$

(5.7)

$$R_{422} = R_{423}$$

(5.8)

5.1.3 $U_c$

$U_c$ is used to damp the system and as voltage feedback in the "voltage mode". By integrating $I_c$, $U_c$ is obtained. Small current spikes are eliminated by the integrator.

$$U_c = \frac{1}{C_{\text{half bridge}}} \int_0^t i_C(\tau) \, d\tau$$

(5.9)

In the Laplace-domain;

$$U_c = \frac{1}{s \cdot C_{\text{half bridge}}} = \frac{1}{s(C_{705} + C_{706})}$$

(5.10)

A pure integrator always suffers from ever existing offsets. Therefore this method can not be used as voltage feedback in the voltage mode. However, in case of system damping, only voltage variations are important. In this situation a integrator will be used, which starts from a few hertz. Fig. 5.1.3 shows the circuit of the integrator. $U_{in}$ is connected with $M5=I_{\text{capacitor}}$. App.G shows the complete electrical circuit diagram.

$$H(s) = \frac{U_{out}}{U_{in}} = \frac{1}{s + \left( \frac{1}{R_{424}C_{422}} + \frac{1}{R_{424}C_{422}} \right) R_{424}C_{422}}$$

(5.11)
When $R_{344} \gg R_{424}$ and $\omega \gg \frac{1}{C_{422}R_{424}}$

$$H(s) \approx \frac{1}{sC_{422}R_{424} + 1} \approx \frac{1}{sC_{422}R_{424}}$$  \hspace{1cm} (5.12)

Desired is a feedback of $\frac{1}{100} \cdot U_c$, see paragraph 3.6.1. The left term represents the desired transfer function, the term on the right represents the simplified transfer-function of Fig. 5.1.3.

$$\frac{1}{100} \cdot \frac{1}{s(C_{705} + C_{706})} \leftrightarrow \frac{1}{sR_{424}C_{422}}$$  \hspace{1cm} (5.13)

With $C_{422}=100[\mu F]$

$$\frac{1}{(1.5[\mu F] + 1.5[\mu F]} \leftrightarrow \frac{100}{100[\mu F]R_{424}}$$  \hspace{1cm} (5.14)

$$R_{424} = \frac{3k\Omega}{(5.15)}$$

Resistor R344 is chosen to be $20[k\Omega]$. So the system "mimics" an integrator for frequencies higher than $\frac{1}{2\pi R_{424}C_{422}}=530[Hz]$. DC gain of the circuit is equal to;

$$A = \frac{R_{344}}{R_{344} + R_{424}} = 0.8$$  \hspace{1cm} (5.16)

### 5.2 Driving power MOS-FETS

The block, driving the POWER MOS-FETs, translates the input signals from block "logic" (App.D.) into turning on or off the MOS-FETs (T700, T710), see App.H. The IR2110 (U340) from International Rectifier (IR), is used to drive the MOS-FETS. The IR2110 has an independent high and low side driver. The drivers have a source/sink capability of $\pm 2[A]$. The driver charge the gate-source and gate-drain capacitors of the MOSFETs. R341 and R343 limit the maximum current to:

$$I_{max} = \frac{U_{driver}}{R_{341}} = \frac{15[V]}{10[\Omega]} = 1.5[A].$$  \hspace{1cm} (5.17)

The high side driver works with the bootstrap principle. When the low-side driver is on, the voltage level of U340-6 is equal to GND\_PWR. In this situation C340 is charged. When the low-side driver is off, U340-6 is set to a higher voltage level (+V\_PWR). D340, a fast recovery diode, prevents C340 from discharging. Due to the peak shaped current, an extra RC-circuit (R340, C341) is used to prevent pollution of the 15\_PWR supply current. Capacitor C340 must be charged during the on-time of the LSS. Therefore the time constant of the RC-circuit must be smaller than the minimum on-time of the lower side switch (LSS). Thus

$$R_{340}C_{340} \ll \tau_{minimum \_on\_time}$$  \hspace{1cm} (5.18)
Another constraint for proper function is

\[ Q_{\text{gate}} < Q_{C340} \]  

(5.19)

The IR2101 has logic non inverting CMOS inputs which are Schmitt-triggered. The high and low side drivers have independent inputs. In this concept the user has to create an external dead time (none of the MOS-FETs conducting). This circuit (for the LSS) is built around D322, R326, R327 and uses the Schmitt-triggered inputs. C323 is slowly charged via R329 plus R326. The voltage across C323 is equal to:

\[ U_{C323}(t) = 5V_{PWR} \left( 1 - e^{-\frac{t}{C323(R326+R329)}} \right) \]  

(5.20)

Desired is a dead-time of 800[\text{ms}]. When \( U_{C323} \approx 3[\text{V}] \) the output is switched on. Discharging of \( C_{323} \) (MOS-FET off) must be done as fast as possible. Discharging is limited by the maximum sinking current of the opto-coupler.

The driver circuit is galvanically isolated from the low-power side. This is done by using optocouplers and a galvanically isolated DC-DC power supply, U300. Note: the high-power side is not completely isolated. Measurements are directly-done at the high-power side. Still a high ohmic loop is created, so currents of the high-side will not flow in the low-power side.

5.3 POWER

The components mentioned in this section refer to App.H. The power section consists of the MOSFETs (T700, T710), the decoupling capacitors (C702, C703, C704, C731, C734, C732, C735), the inductor (L700), dV/dt limiting capacitors (C700, C701, C710, C711) and the capacitors of the half-bridge (C705/C706).

Demands of the MOSFETs are; low resistance, \( U_{DS} \geq 250V \), current handling of a continuous current of 5[A]. MOSFETs for this voltage range are not common and as a result difficult obtainable. The BUZ255 of Siemens was an exception. Properties of the BUZ255 are TO220 case, Rds=0.24[\Omega], Id continuous=13[A], Id peak=52[A].

Decoupling of the +V.PWR/GND_PWR is done in two stages. The first stage is the capacitors C730, C701, C710 and C711. These capacitors are implemented in SMD-cases and are placed directly beside the MOSFETs. SMD for high voltages are difficult to obtain. Therefore, two capacitors are placed in series. Now "standard" capacitors can be used. A resistor network R700/R701 fixes the DC-potential of the capacitors at half +V.PWR. The second stage is the through-hole electrolyte capacitors C702/C703.
5.3.1 $\frac{dV}{dt}$ limitation

The common point of the LSS and HSS has a voltage swing between $+V_{\text{PWR}}$ and GND_PWR. The $dV/dt$ of this point is only limited by parasite capacitors to the power supply. This high $dV/dt$ may cause interference to other circuits on the PCB. Capacitors (C700, C701, C710, C711) are connected to the common point to reduce the voltage slope.

5.3.2 Heatsink

A heatsink for the power MOS-fets is necessary to limit the temperature of the junction. Chosen is for a horizontally placed heatsink in respect to the PCB, which reduces the height of the PCB. Drawback is the reduction of cooling capacity (factor 0.8). Also through-hole components can not be placed near the MOS-FETS.

Both heatsinks (low/high side) are electrically isolated from the MOS-FETS. The TO220 case of the MOS-FETS is electrically connected to the drain. The potential of the HSS case equals $+V_{\text{pwr}}$, the potential of the LSS case has a large voltage swing (node of the half-bridge). The heatsink acts as a capacitor to the cases and to the PCB. To lead the inevitable capacitive currents, both heatsinks are connected to GND_PWR with shunt leads.

Thermal aspects

Fig.5.4 shows the equivalent electrical diagram of the heat conduction. The heat source is the junction, with a value of 3[W] (see App.B). The ambient temperature is set to 50 degrees. In this configuration the junction temperature becomes 101°C, which is far below the absolute maximum temperature of 150°C according to the datasheet.

![Figure 5.4: Equivalent electrical diagram of the thermal circuit](image)

Declaration of variables:

<table>
<thead>
<tr>
<th>Variable</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{th,JC}$ Junction-to-Case</td>
<td>1.67°C/W</td>
</tr>
<tr>
<td>$R_{th,CS}$ Case-to-Sink</td>
<td>0.5°C/W</td>
</tr>
<tr>
<td>$R_{th,SA}$ Sink-to-Ambient</td>
<td>15°C/W</td>
</tr>
<tr>
<td>Ambient</td>
<td>50°C</td>
</tr>
</tbody>
</table>
5.4 PID

The PID is built around a single opamp U110, see App.F. Fig. 5.5 shows the circuit plus bode diagram, where C1=C111/C110, R1=R110 and R2=R114.

![Circuit of the PID controller](image)

**Figure 5.5: Circuit of the PID controller**

With the components $C_1=200\,\text{nF}$, $C_2=33\,\text{nF}$, $C_3=10\,\text{pF}$, $R_1=10\,\text{kΩ}$, $R_2=150\,\text{Ω}$, $R_3=560\,\text{kΩ}$ and $R_4=2.2\,\text{MΩ}$ the gain levels ($A_1$, $A_2$, $A_3$) are given by:

$$A_1 = \frac{R_3 + R_4}{R_1 + R_2} \quad A_2 = \frac{R_3}{R_2} \quad A_3 = \frac{R_3}{R_2}$$  \quad (5.21)

With the same components the break points are given by:

$$f_1 = \frac{1}{2\pi R_4 C_2} \quad f_2 = \frac{1}{2\pi R_1 C_1} \quad f_3 = \frac{1}{2\pi R_3 C_2} \quad f_4 = \frac{1}{2\pi R_2 C_1} \quad f_5 = \frac{1}{2\pi R_5 C_3}$$  \quad (5.22, 5.23)

The levels ($A_2$, $A_3$) and the breakpoints ($f_2$, $f_3$, $f_4$) are set on the values given in section 3.7.1. The break points $f_1$ and $f_5$ are not mentioned in section 3.7.1. $f_1$ limits the DC-gain, $f_5$ limits the gain at frequencies higher than the bandwidth of 2[kHz]. The components $C_3$ and $R_4$ in are not displayed in App.F, these components are added in a later stage.

5.5 LOGIC CIRCUIT

The logic circuit is implemented in a EPLD. Because a EPLD can be programmed many times, flexibility is guaranteed. App.K. shows the overview of the inside of the EPLD. The logic circuit can be split into two functional parts. One part controls the switches (gating, App.L), the second part takes care for synchronisation (cntctrl, App.M).
5.5.1 Switch control

The block "gating" is worked out in appendix L. To avoid confusion, digital signals will be printed bold. Function of the different digital inputs are

- **I\text{high}**. High when the inductor current is higher than \( I\text{high} \) (\( I_{\text{inductor}} > I_{\text{high}} \)).

- **I\text{low}**. High when the inductor current becomes below level \( I\text{low} \) (\( I_{\text{inductor}} < I_{\text{low}} \))

- **Toggle\_low**. Output from protection circuit, guards the minimum switching frequency. High when the voltage drop across the inductor becomes too small.

- **Toggle\_high**. Output from protection circuit, guards the minimum switching frequency. High when the voltage drop across the inductor becomes too small.

- **SD\_n**. Shutdown, low active. Forces the outputs Q\text{not} and Q high, by which both FET's are turned off.

- **Bus**. Connected with the synchronisation bus

- **Enable\_V\_prot**. Enables the inputs Toggle\_low and Toggle\_high.

- **Clock**. Clock input, 50[MHz]

Function of the different digital outputs are

- **Q**. Drives the LLS (Low=LSS conducts)

- **Q\text{not}**. Drives the HSS (Low=HSS conducts)

- **Flank\_eigen**. Generates a pulse when Q changes from 1→0.

- **Flank\_bus**. Signals are equal to input BUS. However the BUS is disabled during Flank\_eigen is high.

The main part of "switch" control is a SR-flipflop (SR-FF). The output Q drives the LSS, the inverse output Q\text{not} the HSS. Roughly, the set-input of the SR-FF is connected to I\_low and Toggle\_low, the reset-input is connected to I\_high and Toggle\_high.

Switching of the half-bridge causes disturbances in the measuring circuits. Fortunately, there is a time-delay between changing the outputs of the SR-FF and the the truly switching of the half-bridge. To avoid false triggering, the input I\_high and I\_low of the SR-FF the inputs are disabled for a short period after the output
The disable time, $\text{Dis}_1$, in Fig 5.6, must maximally last the period of the minimum switching frequency (maximal load). The pulse must minimally last the period of the maximum switching frequency. Of course, pulse $\text{Dis}_1$, is much longer than the disable time $\text{Dis}_2$.

The "disable times" are made with retriggeable one-shots. Both signals, the input and "disable time", are lead to an AND-gate. The output of the gate is connected to the input of the SR-FF. Each change of $Q/Q\not$, (=switching of the half-bridge) starts the oneshot.

The one-shot consists of a counter and a SR-FF, see Fig.5.7. Each pulse at the input resets the counter ("deler") and sets the SR-FF. The counter counts the clock frequency of 50[MHz]. The $n^{th}$ bit of the counter is connected with the reset of the SR-FF. Thus at each change of $Q$, a pulse is given of $2^n\times20[\text{ns}]$.

Four of these one-shots are used;
1.) Disable time of $2^5\times20[\text{ns}]=1.28[\mu\text{s}]$ for the inputs $\text{I}_\text{low}$ and $\text{I}_\text{high}$.
2.) Disable time of $2^{10}\times20[\text{ns}]=20[\mu\text{s}]$ for the inputs $\text{toggle}_\text{high}$ and $\text{toggle}_\text{low}$.
3.) Disable time of $2^{4} \times 20[\text{ns}] = 320[\text{ns}]$ the input $BUS$.

4.) Generation of a pulse $2^{3} \times 20[\text{ns}] = 160[\text{ns}]$, $\text{Flank.eigen}$. The signals $\text{Flank.eigen}$ and $\text{Flank.bus}$ are inputs for the synchronisation circuit. $\text{Flank.eigen}$ is the output of a two-input AND-port with inputs $Q$ and the output of the oneshot, only with a positive $Q$, the pulse is passed through. This pulse is placed on a common wired-or bus, and serves a "phase" information for the other modules connected to this bus. Without the AND-gate, two pulses would be given in one single switching period.

Each module "listens" to the wired-or bus. By disabling the bus-input, a module distinguishes its own-pulse from a pulse of each of the other modules. Normally, $\text{Flank.bus}$ equals the Bus input, the bus is disabled during twice the pulse length of $\text{Flank.eigen}$. Disabling the bus-input also prevents races in the synchronisation circuit.

The signals $\text{Trigger}$, $\text{Qn.delay1}$, $\text{Qn.delay2}$, $\text{Qn.delay3}$ and $\text{Qn.delay4}$ which are shown in the appendix I. are not used. In a later stage, the functions of these signals were replaced by one-shots.

5.5.2 Synchronisation

The other part of the logic circuit takes care of the synchronisation of multiple smartcells. Each smartcell has to determine its position (in time) between its direct neighbours. This position is found with the aid of an up/down counter, a latch and a state machine. The state machine controls the counter and latch. Fig. 5.8 shows the interconnections.

![Figure 5.8: Interconnections of counter, latch and state machine](STSTLT.EPS)

Fig. 5.9 shows the "counter" principle. Each time a module closes its LSS, a small pulse is placed on the line $\text{Flank.BUS}$. The counter resets and starts counting.
When the smartcell itself closes his LSS (Flank\_eigen), the counter counts down. On the first signal on the line Flank\_bus, after Flank\_eigen, the counter stores its value, resets and starts to count up. The stored counter value contains the phase information of of the cell, in respect to his neighbours. Possibilities; positive number; $t_1 > t_2$, negative number; $t_1 < t_2$, zero; $t_1 = t_2$.

![Figure 5.9: Bus information](image)

Fig.5.10. shows the states of the state machine. Double circle means a stable state, a single circle corresponds with an unstable state.

![Figure 5.10: States of the state machine](image)

The inputs Flank\_eigen and Flank\_bus are outputs of the block gating. The input of the counter is the clock frequency of the crista1 oscillator. So the clock rate is proportional to the accuracy of phase determination.

The length of a pulse has also an influence on the phase determination. With the implementation used, there is an error of half the pulse length, see Fig. 5.9.

The stored number has to be translated into a $\Delta I$, to "speed up" or "slow down" the triangular current. This is done with a digital analogue converter, U640 App.I.

### 5.5.3 Digital Analog Converter

The output of the counter is applied parallel to the DAC, U640 (App.I). The DAC translates the counter value into a "discrete" voltage. The DAC has a 12-bits input. The most significant bit (MSB) is used as polarity indicator. The output may varies from $(1 ........ 1) +10[V]$ to $(0 ........ 0) -10[V]$. So the LSB has a value of $10[V]/2^{11}$. 

45
The DAC is set into the transparent mode. The latch is implemented in the EPLD.

Gain

The counter counts the crystal frequency of 50[MHz]. In one microsecond, fifty pulses are counted. Now the output of the DAC is:

\[
\text{Number of counts} \cdot \text{value of LSB} = 50 \cdot \frac{10}{2^{11}} = 240 \left[ \frac{mV}{\mu s} \right]
\]  

(5.24)

The output of the DAC is amplified by the opamp U650. Desired gain is (see section 4.3) 34[mA/\mu s]. The gain of U650 must be 0.14. Gain of the circuit built around U650, App.I, is equal to:

\[
A = \frac{R_{642}}{R_{641}}
\]  

(5.25)

5.5.4 Wired-or

Each time the HSS is turned off and the LSS is turned on, the output Flank eigen of the EPLD generates a positive pulse of 160[ns]. Fet T670 (App.I) translates this signal into a negative pulse on the wired-or bus.

Only one wired-or resistor is necessary, irrespective of the number of used modules. Therefore the wired-or resistor has to be placed on the backpanel.

The value of the terminating resistance is not critical. The ideal value is equal to the characteristic impedance of the bus-line. However the impedance is not constant over its distance, the impedance lies in the neighborhood of 200[\Omega].

5.6 Levelshift

The levelshift circuit translates the input I, into two signals \(I_{\text{high}}\) and \(I_{\text{low}}\). The current \(I_{\text{inductor}}\) is compared with \(I_{\text{high}}\) and \(I_{\text{low}}\). The comparator output is lead to the block "Logic", App.D. The outputs are used to determine the switching moment of the half-bridge. As a result the triangular \(I_{\text{inductor}}\) has a maximum and minimum equal to \(I_{\text{high}}\) and \(I_{\text{low}}\). The average current is equal to \(\frac{1}{2} (I_{\text{high}}-I_{\text{low}})\).

Fig. 5.11 shows the desired graph. For negative currents \(+I_{\text{high}} = 0\) and \(-I_{\text{low}} = 2I_{\text{set}}\), for positive currents \(+I_{\text{high}} = 2I_{\text{set}}\) and \(-I_{\text{low}} = 0\). For currents smaller than \(I_{\text{min}}\), \(I_{\text{high}} = I_{\text{set}} + \frac{1}{2}I_{\text{min}}\) and \(I_{\text{low}} = I_{\text{set}} - \frac{1}{2}I_{\text{min}}\).

\(I_{\text{min}}\) directly determines the maximum switching frequency (§3.4.1). Therefore, \(I_{\text{min}}\) is set until the maximum allowed switching frequency is obtained at zero output current and maximum supply voltage.

\[
I_{\text{max}} = \frac{\frac{di}{dt}}{2 \cdot I_{\text{min}}} = \frac{U_{\text{supply}}}{2 \cdot L_{c}}
\]  

(5.26)
The levelshift circuit is built around $U_{200}$, $U_{210}$ and $U_{220}$, see App.F. Imin is set with the resistors $R_{200}$ and $R_{201}$.

$$I_{\text{min}} = 2 \cdot 10^6 \frac{R_{201}}{R_{201} + R_{200}}$$

(5.27)

The characteristics of $U_{210}$ and $U_{220}$ are displayed in Fig.5.12. The diodes in the feedback loop of opamp $U_{210}$ and $U_{220}$, App.F, conduct depended from the polarity of the input, $M5+U_{200}-7$. The none-linearities of the diodes are eliminated by the feedback loop. By combining the outputs the desired functions, $I_{\text{high}}=M3$ and $I_{\text{low}}=M4$, are obtained.

The block "protection" guards the minimum switching frequency. This is done by measuring, indirectly, the voltage across the inductor of the halfbridge. This
block will give a signal to block 'logica' App.D, to toggle the half bridge, if the voltage drop across the inductor is too small. App.J. shows the electrical circuit. Measured is

\[ (+V\_PWR-A) \cdot G \]

(5.28)

\[ (A\_GND\_PWR) \cdot G \]

(5.29)

which represents the voltage across the inductor. G represents the attenuating factor of the differential amplifier. (A\_GND\_PWR) is measured with a differential amplifier, built around U500, U520, U510. (+V\_PWR-A) is built around U540, U550 and U560. These circuits are identical, therefore only one circuit will be explained.

Maximum voltage of the power circuit is 200[V]. This voltage has to be attenuated with a factor 20 to 10[V], a voltage which the opamps can handle. This is done with a voltage divider, built with R500, R501 and R502. The gain of the circuit is equal to;

\[ G = \frac{1}{2} \left( \frac{R_{502}}{R_{500} + R_{501} + R_{502}} \right) \cdot \left( \frac{2 \cdot R_{503} + R_{504}}{R_{504}} \right) \cdot \left( \frac{R_{521}}{R_{520}} \right) \]

(5.30)

where

\[ R_{520} = R_{521} = R_{522} = R_{523} \]

(5.31)

\[ R_{503} = R_{513} \]

(5.32)

\[ R_{501} = R_{511} \]

(5.33)

With the used components values, the total gain is \( G = 20^{-1} \).

Two comparators, U530 and U570, compare these values with a fixed user defined voltage of

\[ 10[V] \ast \frac{R_{583}}{R_{583} + R_{582}} \]

(5.34)

The outputs of the comparators, Toggle\_low and Toggle\_high, are lead to the block "logic". The output of the comparator becomes high when;

\[ \frac{|U\_inductor|}{20} \leq 10[V] \cdot \frac{R_{583}}{R_{582} + R_{583}} \]

(5.35)

Now the circuit "LOGIC" have information about the voltagedrop across the inductor and indirect information over the switching frequency.
Chapter 6

Measurements

To evaluate the performance of the proposed circuits, two identical modules have been built (50[V]/2.5[A]). The first three sections evaluate a single module, the last three sections evaluate multiple module performance.

The major component values in the power stage are; \( C=3[\mu F] \), \( L_1=200[\mu H] \) and \( L_{\text{load}}=30[mH] \).

6.1 Time delays

Time delays in the "innerloop", §3.1, are measured. Delays in this loop cause switching at wrong current levels. As reference is taken \( I_{\text{inductor}} \), measured with a current probe. Fig 6.1 shows the different blocks of the innerloop with their time-delays. The total delay time equals 720[ns]. This time-delay is a good result and will be hard to decrease.

![Diagram of time delays](image)

Figure 6.1: Time delays in the innerloop

6.2 Current/switching frequency

Fig.6.2. displays the graphic of the switching frequency versus \( I_{\text{set}} \). The dotted line represents the theoretical frequency (Eq 3.2);

\[
\tilde{f}_{\text{switching}} = \frac{1}{T} = \frac{U_{\text{supply}}^2 - U_{\text{load}}^2}{2I_{\text{peak}}L_1U_{\text{supply}}}
\] (6.1)
Parameters: \( U_{\text{load}} = R_{\text{load}} \cdot I_{\text{set}}, \) \( R_{\text{load}}=15[\Omega], \) \( U_{\text{supply}}=50[V]. \)

The maximum frequency, at small values of \( I_{\text{set}}, \) is limited by switching of \( I_{\text{inductor}} \) between \( \Delta I. \)

The value of \( \Delta I \) is set until the maximum frequency is reached at maximum supply voltage (100[V]) and \( I_{\text{set}}=0[A]. \) The maximum frequency in Fig.6.2. is not reached, due to the low supply voltage.

\[
\begin{align*}
\text{Switching frequency} \\
\begin{array}{c|c|c}
\text{frequency} & \text{Iset [A]} \\
\hline
15 & -2.50 \\
30 & -1.60 \\
45 & -0.50 \\
60 & 0.50 \\
75 & 1.50 \\
90 & 2.50 \\
\end{array}
\end{align*}
\]

Figure 6.2: \( f_{\text{switching}} \) versus \( I_{\text{out}} \)

6.2.1 Output current versus \( I_{\text{set}} \)

Fig.6.3. shows the openloop (PID removed) characteristic of \( I_{\text{out}} \) versus \( I_{\text{set}}. \) The straight line (thin) represents the theoretical expectation, the dotted line represents the first order curve fit of the measured current.

The deviation between the theory and measurements is caused by the simplicity of the model. The model assumes a constant voltage across the capacitor. As a result, the voltage across the inductor of the half-bridge is constant and the inductor current increases /decreases linearly. The inductor current is perfectly triangular.

In practice, see Fig.6.4. the current shape is a LC-curve. In case of a high output voltage, the LC-curve differs significantly from the straight line. The average current is larger than the "theoretical" model.
6.3 Frequency response

The frequency response describes how the system responds to sinusoidal inputs. In section 3.6 a linear model is made of a single module. The frequency response is used for model validation, or better model invalidation. Validation is done by comparing the measured and simulated outputs, also called face validation. Note that differing to much is a rather subjective criterion.

Three frequency transfer functions are measured:

a) Transfer function of the openloop half-bridge. Fig.6.5. shows the measuring circuit. To measure the openloop response, resistor R114 (App.F.) is removed. App.N. shows the measured results.

b) Transfer function of the PID-controller. In section 3.7.1 a PID controller is described. The transfer function of the PID controller is measured, see Fig.6.6. Input is $I_{\text{set}}$ and output U110-1. The resistors R103, R114 and
R104 (App.F.) were removed. The measured transfer function can be found at App.N.

c) Transfer function of the closed loop system. Appendix N shows the measured transfer function, Fig.6.5. shows the measuring circuit. In contradistinction with a) and b) the resistors R114, R103 and R104 are placed on the PCB. App.N. shows the measured results.

Note: The voltage feedback is always present.
Settings of smartcell: Usupply=60[V], Z_{load}=30mH+10Ω. Settings of HP-analyser:
Source:200[mV]/pkpk,

![Figure 6.5: Measuring circuit frequency response](image)

Conclusion: All measured responses are in accordance with the theoretical expectations.

### 6.4 Adaption of the circuit

For correct functioning of Smartcell some adoptions were done. These "minor adjustments" can be split into adjustments for autonomous operation (Adaption;1) and parallel operation (Adaption;2,3).

**Adaption 1**

An integrator is used to obtain voltage variations of $U_{\text{cap}}$, see paragraph 5.1.3. The voltage variations are used to damp the system at its resonance frequency of
520[Hz] ($L_{load}$ and C). The described circuit mimics an integrator from 530[Hz], which is too high for correct functioning.

As a temporary solution the voltage measurement is used, see App.G. M25 is connected with an external resistor to R115, see AppF. R460 and R463 are replaced by a capacitor of 100[nF]. The output of the opamp U460 is given by:

$$M25 = \text{Gain} \cdot U_{\text{capacitor}} = \frac{R_{462}}{R_{461}} U_{\text{capacitor}} \quad (6.2)$$

Gain of U460 is set to 0.01, see §5.1.3.

**Adaption 2**

The measuring circuit of $I_{load}$ is not capable of measuring high frequency currents. Bandwidth of the differential amplifier (INA117, App.G.) is limited to 200[kHz]. With multiple module the switching AC-current will flow between the modules instead of flowing into the capacitor.

$I_{inductor}$ is composed of the load current and the capacitor current. Because the load current is not properly measured, the current through the inductor $L_1$, can not be reconstructed.

In order to reconstruct the current $L_1$, a resistor 3[Ω] is placed in series with each module output. The high frequency ($f>17$[kHz]) current is now forced into the capacitor, the current which can be measured.

$$f_{3dB} = \frac{1}{2\pi R_{\text{series}}C} = \frac{1}{2\pi \cdot 3 \cdot 310^{-6}} = 17[\text{kHz}] \quad (6.3)$$

Drawback of the series resistor is its energy consumption. Therefore, in a redesign the current measurement of $I_{load}$ must have a larger bandwidth.

**Adaption 3**

The synchronisation circuit works with variations of $I_{set}$. The phase between modules is corrected by applying a $\Delta I$ to $I_{set}$. With a positive $I_{set}$ and a positive $\Delta I$ the requested (absolute) $I_{set}$ increase, so the output frequency will decrease. However, with a negative $I_{set}$ and a positive $\Delta I$ frequency will increase.

The synchronisation mechanism does not distinguish a negative or positive value of $I_{set}$. So in one situation the synchronisation circuit works properly. In the other situation the system is unstable (inverse feedback).

The synchronisation also will not work with small DC-currents. With small currents, both levels, $I_{high}$ and $I_{low}$ are affected ($I_{high}+\Delta I$, $I_{low}+\Delta$). As a result the switching frequency will not change, see §5.6.

To solve this problem an extra circuit is necessary. This additional circuit controls the polarity of $\Delta$ dependent on the polarity of $I_{set}$. However the problem with small currents still remain.

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6.5 Synchronisation

The synchronisation circuit is tested for two input signals: a step-input and a half wave sinusoidal. In all situations; one module is freerunning, the other module wants to synchronise. Both modules operate in openloop (no feedback of $I_{load}$).

a). Step input. Setpoint 0.75[A] and 0.45[A]. Load 30mH/12[Ω]. The step input causes a phase error. After a few periods the synchronisation is "repaired", see App.O.

b). Settings as in a). App.P. shows the output of the module without synchronisation. The figure shows a perfect match between $I_{set}$ and the inductor current.

c) Input half-wave sinus of 2[kHz], 1.2[V_{peak}] DC-offset=0.4[A]. Load=8[Ω], App.Q. shows the key-waveforms of the synchronisation principle.

The synchronisation actions are clearly visible. The output current has a delay on the output due to the capacitor of the half-bridge. The output current shows a ripple caused by a mismatch in the phase of the two modules.

6.6 Imperfections

This section describes the imperfections of the synchronisation model and the impact of system imperfections on the synchronisation. Investigated system imperfections: time delays, deviations of the inductor value and current measurements. Investigated is the final (static) situation. In all these situations the DC-loopgain is considered as infinite.

6.6.1 Synchronisation model

Experiments showed a model inaccuracy. Situation; one module freerunning, the other module locks on the freerunning module. The synchronisation gain is increased until the synchronisation gets unstable. This is done for different DC-values of the input current.

A relation between the input value of $I_{set}$ and the gain was found. With large desired currents, a larger gain was prohibited before unstability occurs. However with small desired current a smaller gain was allowed.

The used model in section 4.3 does not depend on the desired current value. The model assumes a gelijkbenige triangular shaped current. A test is done with a short circuit output. In this situation both slopes are equal. In this situation, short circuit output, the oscillation gain did not depend on $I_{set}$.  

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The model can be made more accurate by introducing not equally shaped inductor currents. However, the reason of dependency of $I_{set}$ is not clear.

### 6.6.2 Time delays

The innerloop is not infinitely fast. There is always a delay between the command "switch" and the real switching of the MOS-FETs. The synchronisation circuit reacts on the command "switch". Fig.6.7. shows the effect on the synchronisation mechanism. Module B is perfect, module A has a delay in the innerloop.

![Figure 6.7: Influence of a time delay on the synchronisation mechanism](image)

The conditions of the synchronisation circuit, $t_1 = t_2$, are fulfilled. However, the real phase is disturbed. Conclusion; different time-delay of the modules is to the disadvantage of the output ripple. There is no effect on the DC load current-sharing between the modules. Fortunately, delays are normally (order [ns]) small and as result negligible.

### 6.6.3 Inductor value

The synchronisation mechanism takes care of equal switching frequencies of the different modules. The switching frequency depends primarily on $U_{load}$, $I_{set}$, the supply voltage and $L_1$ (Eq.6.1).

To maintain equal frequency with a different inductor value, the synchronisation mechanism corrects $I_{set}$. So the DC-current sharing accuracy depends linearly on the equality of the inductor values in the different modules. In practice there is a difference of about 2% between the inductor values.

Fig.6.8. displays the effect. Module A is ideal, while module B has a larger inductor value with respect to module A. To maintain equal phase, $\Delta I$ is applied to module A. Although the phase is correct, different inductor value in two modules increases the output current ripple.
6.6.4 Measurements

Deviations in the current measurements have no effect on the DC-current sharing accuracy and phase. Fig.6.9. shows the inductor current of two modules. Module B is perfect, module A has a measuring error.

A measurement error coincide with a different $I_{set}$. The synchronisation circuit adjusts $I_{set}$, with $\Delta I$, until the measuring error is cancelled.

The DC gain of the PID is considered as infinite. $\Delta I$ is equal to the loop gain multiplied with the difference of $t_1$ minus $t_2$. In practice the loop gain is finite and $t_1$ minus $t_2$ will not be zero. Now a measurement error affects the phase.
Chapter 7

Conclusions

A topology with a half-bridge, which uses critical discontinuous switching, is proposed to meet the specifications of DAP-Drachten. The topology choice is verified on a scale model. Since modularity was required, two modules were used to test the required modularity. Although the system has proven to meet the demands, there are some aspects to consider.

An important aspect of the half-bridge is the measurement of the variables $I_{\text{load}}$ and $I_{\text{capacitor}}$. The capacitor current is measured with a current transformer, which has a high-pass characteristic. In order to measure lower frequency components, the transformer has been adapted. The measuring circuit of $I_{\text{load}}$ has two problems, therefore this circuit needs to be adapted. $I_{\text{load}}$ is measured with a low ohmic resistor in series with the load impedance. The first problem is the common mode rejection ratio (CMRR) due to the low impedance relative to the impedance of the load. The second problem arises with the use of multi-modules. In this situation, the AC-current (switching frequency) flows between the modules. The bandwidth of the used differential amplifier is $200\,\text{kHz}$. This is too small for correct reconstruction of the triangular currents with a frequency of $200\,\text{kHz}$. Therefore it is suggested to split the measurement of the inductor current into two parts. The low frequency components can be measured with a resistor and the high frequency components with a current transformer.

Two important system characteristics, the bandwidth and the output current ripple, are determined by the capacitor $C$ and the inductor value of the load. The inductor value is fixed, contrary to the capacitor value. The value of $C$ can be decreased by using multi-modules. With multiple modules the AC-current flows between the modules, instead of flowing into the capacitor. However, phase errors between the modules will have an increasing influence on the output current ripple. Phase errors arise from varying the input $I_{\text{set}}$. These errors lead directly to output current ripple, because the synchronisation is disturbed. Therefore, abrupt changes of $I_{\text{set}}$ have to be avoided.
To minimise output current ripple, the synchronisation circuit has to be as fast as possible. The settling time of the synchronisation circuit depends on the switching time. High switching frequency is preferred, because it reduces the settling time. However, the drawback of this high switching frequency is that it increases the switching losses.
Appendix A

Output of the program CONV

CONV is an internal Philips product, developed at PHILIPS Aken. Conv contains a program for "Magnetic Design". First the program needs information about the core type, wire type, maximum airgap and maximum field B[Vs/A] in the coil former. Now the program calculates the number of turns and the desired air-gap, taking into account the maximum B[Vs/A]. If the number of turns does not fit into the winding area of the coil former, a warning is given. The number of windings can be changed manually. If this is done, the program will adjust the airgap. If the wire does not fit into the winding window, a warning is given.

User-Data : L
L = 0.2 W
Arbitrary current shape; frequency = 125 kHz;

\[
R_{th} = 26.00 \text{ K/W}
\]

<table>
<thead>
<tr>
<th></th>
<th>rms skin prox. total</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>0.022 0.000 0.009 0.001</td>
</tr>
</tbody>
</table>

specific eddy_cur.

Core | 0.068 0.026 0.094 |

Total Losses : 0.125 W

Losses & temperature rise

\[
L = 0.200 \text{ W}
\]

\[
R_{dc} = 0.065 \Omega
\]

\[
R_{tot} = 0.374 \Omega
\]

Equivalent circuit

winding fits

Winding layout
\( L = 0.2 \ \text{mH} \)

Arbitrary current shape; frequency = 10 kHz;

- Equivalence circuit
  - 33 turns
  - 160\( \times \)0.071 mm wire
  - 18.4 mm

\[ \begin{align*}
  R_{\text{th}} &= 26.00 \ \text{K/W} \\
  \text{airgap} &= 1.71 \ \text{mm} \\
  \mu_e &= 51.6 \\
  A1 &= 183.7 \ \text{mH} \\
  \text{B} &= 0.025 \ \text{mm} \\
  \mu_r &= 3900 \\
  \text{H} &= 0.028 \ \text{mm} \\
  \text{R}_{\text{dc}} &= 0.072 \ \text{A} \\
  \text{R}_{\text{tot}} &= 0.074 \ \text{A} \\
  \text{L} &= 0.200 \ \text{mH} \\
  \text{R}_{\text{sw}} &= \frac{6[I]}{\text{A}} \\
  \text{f} &= 10 \ \text{kHz} \\
  \text{R}_{\text{sw}} &= \frac{-1[I]}{\text{A}} \\
  \text{f} &= 125 \ \text{kHz}
\]
Appendix B

Power losses in the switching devices

The switching diagram of the smart-cell is optimized for minimum switching losses. Switching losses are reduced by zero-current switching. In normal situation, power losses in the MOSFET’s can be divided into resistance losses and switching losses.

B.0.5 Resistance losses

The on-resistance $R_{DS(on)}$ of a power MOSFET is an important figure of merit because it determines the amount of current the device can handle. The average $R_{DS}$ power dissipation:

$$P_{R_{DS}} = \frac{1}{t_1} \int_0^{t_1} i(t)^2 R_{DS} dt$$  \hspace{1cm} (B.1)

With triangular current waves the power dissipation for both switches is equal to;

$$i(t) = \left(\frac{U}{L}\right) t \quad P_{R_{DS}} = \int_0^T R_{DS} \left(\frac{U}{L}\right)^2 t^2 dt \quad \text{with } T = \frac{I_{\text{peak}}}{U}$$  \hspace{1cm} (B.2)

$$P_{R_{DS}} = \frac{R_{DS}}{3} I_{\text{peak}}^2 [W]$$  \hspace{1cm} (B.3)

Worst case situation occurs with maximum current ($I_{\text{peak}} = 5[A]$),

$$R_{DS} = 0.24[\Omega] \quad P_{R_{DS}} = \frac{0.24}{3} 5^2 = 2[W]$$  \hspace{1cm} (B.4)

The duty-cycle (on-time/(on- + off-time)) of the switches depends on the output voltage. Assume a worst case duty-cycle of 0.9, which means that 90% of the resistance losses are generated in one MOSFET.
B.0.6 Switching losses

Switching losses can be subdivided into; conducting of the body diode, shortcut of the drain source capacitance and not immediately conducting of the FET.

Fig. B.1 gives the different states of the MOSFET in relation to the current through the inductor. The drawings below refer to the equivalent circuit of the half-bridge. In this example a positive current is chosen. For a negative current, the situation reverses between the HSS and the LSS.

\begin{figure}[h]
\centering
\includegraphics[width=0.5\textwidth]{mosfet_states.png}
\caption{States of the MOSFETs}
\end{figure}

- A. The HSS is turned off. Current and voltage shapes across the MOS-fet are estimated as in Fig. B.2. Powerloss is equal to:

\begin{align}
P &= f_{\text{switching}} \int_{0}^{t_{\text{off}}} i(t)U_{t}\,dt \\
&\approx 90[\text{ns}] \\
(P.5) \\
\int_{0}^{\epsilon_{\text{switching}}} = \frac{1}{6}I_{\text{max}}U_{\text{max}}t_{\text{off}} \\
&= (B.6) \\
\int_{0}^{\epsilon_{\text{switching}}} = 10 \cdot 10^3[\text{Hz}] 200[\text{V}] 5[\text{A}] 90[\text{ns}] = 900[\text{mW}] \\
(P.7)
\end{align}

Now the inductor is considered as a continuous current source, with \( I=I_{\text{peak}} \). Consider the equivalent circuit of Fig.B.3 where I is a current source in series with the stray capacitance at the common node of the MOSFET's. This stray capacitor exist of the drain-source capacitance. The simplification of a constant current source is only valid when;

\[ E_{\text{inductor}} \gg E_{\text{capacitor}} \] (B.8)
The inductor of the half-bridge acts as a current source and discharge the drain-source capacitance. This stray capacitance will be discharged completely during a fraction of the dead-time, thus before the LSS conducts. So the drain source capacitance will not be short circuited.

The capacitor voltage will fall below PWR\_GND. When this voltage exceeds $U_{\text{forward}}$ of the body-diode, the diode starts conducting. Now the current of the current source flows through the body-diode causing losses in the diode. The power losses are equal to:

$$P = f_{\text{switching}} \int_0^{t_{\text{dead}}} i(t) U_{\text{forward}} dt$$
$$P = 10 \cdot 10^3 [Hz] \cdot 800 [\text{ns}] \cdot 5 [\text{A}] \cdot 2 [\text{V}] = 80 [\text{mW}]$$

- **B.** The LSS is turned on. The MOSFET takes over the current which flows in the body diode. Since this is done with almost zero voltage ($U_{\text{forward}}$), these losses are negligible.

- **C.** The LSS is turned off. This is done with zero current, so the losses are neglected. The current in the inductor is zero, and will not discharge the drain/source capacitance.

- **D.** The HSS is turned on. The capacitor is not discharged. The capacitor is short circuited by the HSS switch.

$$P = f_{\text{switching}} \frac{1}{2} CV^2$$
\[ P = 10.000 \cdot \frac{1}{2} \cdot 100 \cdot 10^{-12} \cdot 200^2 = 20 \text{[mW]} \] (B.12)

Notes at C. The losses caused by short circuiting the capacitor are proportional to the switching frequency. The examined situation, full load = lowest switching frequency, causes the lowest losses.

The dV/dt capacitors are not taken into account in the calculations. These capacitors are connected to the common node of the half-bridge and will increase the losses.

When at C the LSS is turned off at exactly \( I_{\text{inductor}} = 0 \text{[A]} \), then capacitance at the common point of the switches are short circuit at point D. This is an undesirable situation, due to the extra power losses. In practice the switch is not opened at \( I_{\text{inductor}} = 0 \text{[A]} \), but at a small negative value. This is caused by the time-delays in the innerloop, between the command "open switch" and the really opening.

The negative current charges the capacitor. When the voltage exceeds \( +V_{\text{PWR}} + U_{\text{forward}} \) the body diode of the HSS starts to conduct. In this situation there are no 'short circuit losses'.

Conclusion. In the worst case situation (5[A] peak, 10[kHz]) the MOSFETs dissipates 3[W].
Appendix C

Sampled Data Model

For the purpose of providing the design of a controller, a small signal sampled-data model of the unity-cell will be derived. The derivations are worked out following an analytical procedure.

The unity-cell is characterized as follows. The system operates cyclically. In one cycle two configurations can be considered, see Fig. 2.3. In the first configuration S1 is closed. I1 will increase and when $I_1 = I_{set}$ then S2 is closed. This is the second configuration. When $I_2$ reaches zero, S1 is closed and the cycle starts again. Fig. C.2 shows the two possible converter topologies.

The electrical equations of the circuit:

$$U_o - L_1 \frac{dI_1}{dt} - U_c = 0$$
$$U_c - L_2 \frac{dI_2}{dt} - RI_2 = 0$$
$$I_1 - I_2 - C \frac{dU_c}{dt} = 0$$

Choosing the state vector as:

$$\begin{align*}
\begin{bmatrix}
U_c \\
I_1 \\
I_2
\end{bmatrix}
\end{align*}$$
All the circuit topologies can be described by linear time invariant state-space equations of the form given by

\[ \frac{d\xi(t)}{dt} = A_i \xi(t) + B_i \]  
\[ y(t) = C_i' \xi(t) + D_i \]

With the matrices \( A, B, C \) and \( D \) for the different topologies.

\[ A_i = \begin{bmatrix} 0 & 0 & \frac{1}{L_1} & \frac{1}{L_2} \\ 0 & 0 & \frac{R}{L_2} & 0 \\ \frac{1}{C} & \frac{1}{C} & 0 & 0 \end{bmatrix} \]

\[ B_1 = -B_2 = \frac{U_0}{L_1} \begin{bmatrix} 1 \\ 0 \\ 0 \end{bmatrix} \]

\[ C_i' = \begin{bmatrix} 0 \\ 1 \\ 0 \end{bmatrix} \quad D_i = 0 \]

The set \( p_k \) of the chosen controlling parameters, that can act independently on the circuit are \( I_{set} \) and the input voltage \( U_0 \).

\[ p_k = \begin{bmatrix} I_{set} \\ U_0 \end{bmatrix} \]
The transition times between the different topologies being collected into the vector $T_k$, see Fig.C.3

![Figure C.3: Transition times](image)

$$T_k = \begin{bmatrix} T_{1,k} \\ T_{2,k} \end{bmatrix} \quad (C.9)$$

Constraint equations relate each cycle the transition times to the state variables and the controlling parameters. In general the constraints can be specified as

$$
c_k(x(t), p_k, T_k) = 0 \quad (C.10)
$$

In the particular case of the circuit of Fig.C.2, by taking into account of the switching sequence of Fig.C.3, $c_k$ becomes;

$$c_k = \begin{bmatrix} u_x(T_{1,k}) - I_{set} \\ u_x(T_{1,k}) \end{bmatrix} = 0 \quad (C.11)$$

with

$$l = \begin{bmatrix} 1 \\ 0 \\ 0 \end{bmatrix} \quad (C.12)$$

Steady state conditions

The inductor $L_1$ and $C$ acts as a low-pass filter. We assume that no AC current passes $L_2$. So in steady state the average voltage across $U_C$ is equal to $R \cdot I_{load}$.

$$T_1 = \frac{I_{set}L_1}{U_o - \frac{1}{2}RI_{set}} \quad (C.13)$$

$$T_2 - T_1 = \frac{I_{set}L_1}{U_o + \frac{1}{2}RI_{set}} \quad (C.14)$$

$$U_R = \frac{1}{2}I_{set}R \quad (C.15)$$

$$U_C(T_{1,k}, T_{2,k}) = \frac{1}{2}I_{set}R \quad (C.16)$$

Steady state:

67
\[
\begin{align*}
\mathbf{x}(t_{k,1}) &= \begin{bmatrix} 0 \\ \frac{1}{2}I_{set} \\ \frac{1}{2}I_{set}R \end{bmatrix} \\
\mathbf{x}(t_{k,2}) &= \begin{bmatrix} I_{set} \\ \frac{1}{2}I_{set} \\ \frac{1}{2}I_{set}R \end{bmatrix}
\end{align*}
\]  
(C.17)  
(C.18)

**Small signal model**

Carrying out multivariable Taylor series expansion, it is possible to obtain a small-signal model describing perturbations about a nominal cyclic steady state. Defining

\[
\Phi_i = \exp\{A_i(T_i - T_{i-1})\} 
\]  
(C.19)

\[
g_i(x, T_j) = A_i(T_j) + B_i
\]  
(C.20)

Taking partial derivatives, with respect to the state vector

\[
\begin{bmatrix} \frac{\partial f}{\partial x} \\ \frac{\partial g}{\partial x} \end{bmatrix} = \begin{bmatrix} \frac{\partial z(T_2)}{\partial x(T_1)} \frac{\partial z(T_1)}{\partial x(T_0)} \end{bmatrix} = \Phi_1 \Phi_2
\]  
(C.21)

\[
\begin{bmatrix} \frac{\partial c}{\partial x} \\ \frac{\partial c}{\partial z} \end{bmatrix} = \begin{bmatrix} \Phi_1 \\ \Phi_2 \end{bmatrix} = \begin{bmatrix} \frac{\partial \Phi_1}{\partial x} \\ \frac{\partial \Phi_2}{\partial x} \end{bmatrix}
\]  
(C.22)

Taking partial derivatives, with respect to the time vector

\[
\begin{bmatrix} \frac{\partial f}{\partial T_1} \\ \frac{\partial f}{\partial T_2} \end{bmatrix} = \begin{bmatrix} \frac{\partial f}{\partial T_1} \\ \frac{\partial f}{\partial T_2} \end{bmatrix}
\]  
(C.23)

where

\[
\begin{bmatrix} \frac{\partial f}{\partial T_1} \\ \frac{\partial f}{\partial T_2} \end{bmatrix} = \Phi_2 \left[ -g_2(x, T_1) + g_2(x, T_1) \right]
\]  
(C.25)

\[
\begin{bmatrix} \frac{\partial f}{\partial T_1} \\ \frac{\partial f}{\partial T_2} \end{bmatrix} = -g_2(x, T_2)
\]  
(C.26)

Taking partial derivatives with respect to the controlling-parameter vector

\[
\begin{bmatrix} \frac{\partial x}{\partial \mathbf{c}} \\ \frac{\partial x}{\partial \mathbf{d}} \end{bmatrix} = \begin{bmatrix} \frac{\partial x}{\partial c_1} \\ \frac{\partial x}{\partial c_2} \end{bmatrix}
\]  
(C.27)
\[
\begin{bmatrix}
0 & 0 \\
\frac{1}{2} & 0 \\
\frac{1}{2}R & 0
\end{bmatrix}
\] (C.28)

\[
\begin{bmatrix}
\frac{\partial T}{\partial I} \\
\frac{\partial T}{\partial U}
\end{bmatrix} = \begin{bmatrix}
\frac{\partial T_1}{\partial I_{set}} & \frac{\partial T_1}{\partial U_0} \\
\frac{\partial T_2}{\partial I_{set}} & \frac{\partial T_2}{\partial U_0}
\end{bmatrix}
\] (C.29)

with

\[
\frac{\partial T_1}{\partial I_{set}} = -L_1 U_o 
\] (C.30)

\[
\frac{\partial T_1}{\partial U_o} = \frac{-L_1 U_o}{(U_o - \frac{1}{2} R I_{set})^2}
\] (C.31)

\[
\frac{\partial T_2}{\partial I_{set}} = \frac{L_1 U_o}{(U_o + \frac{1}{2} R I_{set})^2} + \frac{L_1 U_o}{(U_o - \frac{1}{2} R I_{set})^2}
\] (C.32)

\[
\frac{\partial T_2}{\partial U_o} = \frac{-L_1 I_{set}}{(U_o + \frac{1}{2} R I_{set})^2} + \frac{-L_1 I_{set}}{(U_o - \frac{1}{2} R I_{set})^2}
\] (C.33)

The final results read;

\[
\bar{x}_{k+1} = F_0 \bar{x}_k + G_0 \bar{u}_k
\]

\[
\bar{x}_k = H_0 \bar{x}_k + J_0 \bar{u}_k
\] (C.34)

Figure C.4: Pole-zero map of Eq.C.34

Fig.C.4 shows the pole-zero map of Eq.C.34 (input $I_{set}$, output $I_2$). There are two complex poles near the unity circle. A disturbance applied on the input, $I_{set}$, causes the output to oscillate (poorly damped) with a frequency which is much smaller than a system cycle.

The sampled-data representation gives roughly the same result as the estimated linear model, §3.6.1. However the sampled data method does not give insight in the components which cause the oscillation.
Appendix D

Block diagram
Appendix E

Current transformer

Fig. E.1 shows the physical view of the current transformer. The equivalent electrical scheme of the current transformer is displayed in Fig. E.2. The trafo has a high pass transfer function. The -3dB point is determined by

\[ f_{-3dB} = \frac{R_s}{N^2 2\pi A_L N_p} \]  \hspace{1cm} (E.1)

Abbreviations:
\[ U_{\text{secondary}} = U^* \cdot N = I_{\text{primary}} \frac{R_{\text{sec}}}{N} \]  \hspace{1cm} (E.3)

A TN6/4/2-3FS core is used. The winding number is limited by the core size and the wire diameter. Used is a TN6/4/2-3FS core with \( A_L = 250 \text{[nH]} \), \( N_p = 1 \), \( N_s = 80 \), \( R_s = 3 \text{[Ω]} \) and a wire (Cu) diameter of 0.315[mm]. Now the theoretical -3dB point is 300[Hz].
Appendix H

Circuit Diagram POWER
Appendix I

Circuit Diagram
SYNCHRONISATION

PROJEKKT: SMARTCELL
PROJEKT: PRODRIVE

CODE

DATE

REV

PROJECT S C T

SUBJECT

SYNCHRO

DESIGNER: P.J.H. VILNIUS

PRODRIVE B.V.

Eindhoven

The Netherlands

TÉL. +31.40.2461268

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Signal Processing
Electronic Controls
Power Electronics

POWER COMPONENTS:
VIN, VCC, BIRD
LEVEL SHIFT
INP/OEL 44
MOSFET
MEASUREMENT
PROTECTION
SYNCHRONISATION
POWER
SPARE
SPARE
Appendix K

EPLD Overview
Appendix L

EPLD Gating
SUBDESIGN deler
(
    CLK : INPUT ;
    reset : INPUT ;
    value[10..0] : OUTPUT ;
)

VARIABLE
    counter[10..0] : DFF;

BEGIN
    COUNTER[].CLK = CLK ;
    if reset then
        counter[] = 0;
    else
        counter[] = counter[] + 1;
    end if;
    value[] = counter[];
END;
Appendix M

EPLD Synchronisation

%==================================================================================================
=
= COUNTER CONTROLLER =
= by P. v Gils date 17-09-1996 =
=
==================================================================================================%

Function b11count (CLK,CLRn,SETn,LDrn,Dnup,L,K,J,I,He,F,E,D,C,B,A,Gn)
RETURNS (QL,QK,QJ,QI,QH,QG,QF,QE,QD,QC,QB,QA)

TITLE "UP/DOWN counter" ;

SUBDESIGN CNTCTRL
(
    CLK : INPUT ;
    Output_CNT[11..0] : OUTPUT ;
    QFlank_bus : INPUT ;
    QFlank_eigen : INPUT ;
)

VARIABLE

% INTERNAL SIGNALS %

    COUNTER[11..0] : node ;
    Output_CNT[11..0] : DFFE ;
    RESET : DFFE ;
    CLKENAB : SOFT ;

    Flank_bus : DFFE ;
Flank_eigen : DFFE ;

UPDOWN : MACHINE
OF BITS (STATE)
WITH STATES (ST_UP=1, ST_DOWN=0);

BEGIN

%============================ Synchronize inputs ========================%
Flank_bus.CLK = CLK ;
Flank_eigen.CLK = CLK ;
Flank_bus = Qflank_bus ;
Flank_eigen = Qflank_eigen ;

%===== connect state machine clock and reset lines =====================%
UPDOWN.CLK = CLK
RESET.CLK = CLK

%===== define state transitions =======================================%
CASE UPDOWN IS

WHEN ST_UP => IF Flank_eigen
ELSEIF Flank_bus
END IF

WHEN ST_DOWN => IF Flank_bus

END IF

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END CASE

%========== Counter definition ========================================%

counter[11..0] = B11COUNT (CLK,vcc,vcc,!RESET,!STATE,GND,GND,GND,
GND,GND,GND,GND,GND,GND,GND,GND,GND,GND,GND,GND,GND)

%========== CLKENAB definition ========================================%

Output_CNT[].clk = CLK ;
Output_CNT[].ena = CLKENAB ;
Output_CNT[10..0]= COUNTER[10..0];
END;
Appendix N

Frequency responses

Source: Level: 149.8966 mVpk  [SINE]  Offset: 0 V  Ramp Rt: 0 Vpk/s
Date: 09-03-96  Time: 10:28:00 AM

A: Freq Resp 2/1  X:10 Hz  Y:-0.5017 dB

B: Freq Resp 2/1  X:10 Hz  Y:-1.7685 deg

OPEN LOOP
<table>
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<tr>
<th>Freq</th>
<th>Strt: 1 Hz</th>
<th>Resolutn: AUTO</th>
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<tbody>
<tr>
<td>[SINE] Stop: 9.991 kHz</td>
<td>Est Swp Tm: 151.18 s</td>
<td></td>
</tr>
<tr>
<td>Date: 09-04-96</td>
<td>Time: 12:33:00 PM</td>
<td></td>
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</table>

A: Freq Resp2/1 X:2.13636 kHz Y:24.7421 dB

<table>
<thead>
<tr>
<th>dB Mag</th>
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<tr>
<td>55 dB</td>
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<table>
<thead>
<tr>
<th>dB</th>
</tr>
</thead>
<tbody>
<tr>
<td>5 dB</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>/div</th>
</tr>
</thead>
<tbody>
<tr>
<td>5 dB</td>
</tr>
</tbody>
</table>

B: Freq Resp2/1 X:2.13636 kHz Y:-132.735 deg

<table>
<thead>
<tr>
<th>Phase</th>
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<tr>
<td>-100 deg</td>
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<table>
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<tbody>
<tr>
<td>20 deg</td>
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<table>
<thead>
<tr>
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</tr>
</thead>
<tbody>
<tr>
<td>-300 deg</td>
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</tbody>
</table>

PID
Appendix O

Synchronisation 1

Two modules parallel, both modules control their relative phase. Settings; Open-loop, $L_{\text{load}}=30\,[\text{mH}]$, Setpoint=0.75[A] to 0.45[A]

![Diagram of PM3380A with ch1 and ch2](image)

ch2: $dT=6.8\,\mu\text{s}$, $dV=101\,\text{mV}$
Appendix P

Synchronisation 2

CH1 $10 \text{[mV]} = 1 \text{[A]}$, other channels $1 \text{[V]} = 1 \text{[A]}$
Appendix Q

$\Delta: 910\text{mV}$
$\Theta: -1.89\text{V}$

CH1 10[mVΩ]=1[A], other channels 1[V]=1[A]
SMARTCELL
POWER AMPLIFIER

LITERATUURONDERZOEK

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Faculteit: Elektrotechniek
Vakgroep: Elektromechanica & Vermogenselektronica
Hoogleraar: Prof Rozenboom
Mentoren: Ir J. Coenders (Philips), Ir M. Smidt (TUE)
Inhoudsopgave

1 Samenvatting afstudeeropdracht
2 Opdracht literatuuronderzoek
3 Concept inhoudsopgave afstudeerverslag
4 Het literatuuronderzoek.
   4.1 Geraadpleegde bronnen
   4.2 Zoektermen en synoniemen
   4.3 VUBIS
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   4.5 Science Citation Index
   4.6 Inspec CD
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5 Sneeuwbal- en citatiemethode
6 Conclusies
7 Literatuurlijst
Hoofdstuk 1

Samenvatting afstudeeropdracht.


De effectiviteit en prestatie van het ECP is afhankelijk van de stroomdichtheid, stroomvorm en de steilheden van de aangeboden stroomimpuls.

In het verleden is door Philips CFT (Centrum fabrication technologie) voor DAP Drachten een voeding ten behoeve van dit ECP process ontwikkeld. Deze voeding bestaat uit twee delen. Een schakelende voeding voor de grove regeling en een lineair deel voor de fijnregeling. DAP Drachten zou graag een wijziging aan deze voeding willen toepassen waarbij:
1. De complexiteit vermindert.
2. Het energetisch rendement toeneemt.
3. Modulaire opzet (Meer stroom, meer modules)
4. Bipolaire stroom

De taak van de afstudeerder is om vanuit de gewenste specificaties een haalbaarheidsstudie te doen voor een aantal topologien. Na een selectie van de “meest” geschikte topologie zal een prototype gerealiseerd worden.
Hoofdstuk 2

Opdracht literatuuronderzoek

Een deel van de afstudeeropdracht bestaat uit het bepalen van een geschikte topologie. Hierbij lijkt een volledige vrijheid van keuze te zijn. Echter topologien waarbij het CFT geen enkele ervaring is, zijn vrijwel kansloos. De kans op succes is dan voor DAP Drachten te klein.

(Knelpunten zijn nog niet bekend)

Het doel van literatuur onderzoek heeft twee samenhangende doelen:
• Wordt er onderzoek gedaan naar toepassingen van vermogens elektronika voor ECP. Er bestaat veel literatuur over voedingen (zowel stroom als spanning). Bestaan er voeding die specifiek zijn voor het ECP.
• Zo ja, welke topologien worden dan toegepast en zijn deze dan geschikt voor gebruik in Drachten.

De literatuur moet dus ingaan op een schakelende topologie. Lineaire oplossingen vallen af vanwege hun slecht rendement. Belangrijk is dat van de besproken oplossing ook meetrapporten aanwezig zijn, waarin de algemene prestaties zichtbaar zijn.


Tijdschriftartikelen en congresartikelen lijken de meeste kans op succes te hebben. Gezien de korte tijdsduur van afstuderen, moeten de artikelen binnen twee weken beschikbaar zijn.

Nog enkele criteria waaraan de gevonden referenties dienen te voldoen:
• De besproken topologie maakt gebruik van een DC ingangsspanning.
• Rendement is een belangrijk item dus alleen schakelende oplossingen zijn welkom.
• Bij voorkeur maken de referenties gebruik van zero voltage switching (ZVS) en/of zero current switching (ZCS).
• Artikelen in andere talen dan Engels of Duits worden niet meegenomen in dit onderzoek.
Table 1

<table>
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Table 1

4.5 Inspec (CD-ROM)

In INSPEC werd gezocht met de zoekterm “(EDM or ECP or ECM or machining) and POWER”. Zoekacties zijn alleen gedaan in de “Basic Index”

4.6 Inspec (gedrukte vorm), EEA

De CD versie loopt achter op de gedrukte vorm (tot maximaal een half jaar). Om toch de meest recente gegevens te vinden is de gedrukte vorm van Inspec geraadpleegd. Dit zijn de delen januari t/m mei 1996. Gezocht is onder de classificatie B8620, Manufacturing industries en B8360 Power converters and power supplies to apparatus. Hieruit werden geen artikelen gevonden.

4.7 Science Citation Index (SCI)

In het zoekveld “title” is gezocht met de eerder aangegeven zoekterm. Het zoekveld “author” komt aan bod bij de citatie methode. Hieruit volgde geen selecties.

4.8 Philips CFT.

Op de afdeling bij Philips bleken er enkele jaargangen aanwezig te zijn van de EPE conferenties. Hieruit is 3. geselecteerd.
Hoofdstuk 3
Concept inhoudsopgave afstudeerverslag

HFD1 Introduction

HFD 2 Topology choice

HFD 3 Smartcell

HFD 4 Multiple Smartcells

HFD 5 Implementation

HFD 6 Measurements

HFD 7 Conclusions
Hoofdstuk 4

Literatuuronderzoek

4.1 Geraadpleegde bronnen

Onderstaande lijst bevat de gebruikte media en indien bij afwijking de perioden waarin deze media werd onderzocht.

- Vubis, bibliotheek catalogus van de TUE
- Compendex CD-ROM periode 1985-1995
- INSPEC CD-ROM periode 1989-1995
- Science Citation Index (SCI) CD-ROM
- Science Citation Index (SCI) Gedrukte vorm periode

4.2 Zoektermen en synoniemen

Electro chemical machining (ECM) komt onder de volgende vormen terug in de literatuur; electro chemical processing (ECP) en onder de naam electrical discharge machining (EDM)

De media werd onderzocht met behulp van onderstaande zoektermen:
(EDM or ECP or ECM or machining) and POWER en de voluit geschreven zoektermen.

4.3 Vubis

In Vubis werd gezocht op woord in titel. Gebruikte titelwoorden waren EDM, ECP, ECM and machining. Er werden geen referenties geselecteerd.
De verwachting is ook niet dat er een boek bestaat gewijd aan power elektronica t.b.v. ECP. De gevonden referenties waren chemisch van aard.

4.4 Compendex

De zoekterm “(EDM or ECP or ECM or machining) and POWER” in de basic index. In het tijdsinterval 1985-1995 leidde dit tot 3 referenties. Hiervan bleken er 2 interessant. Dit artikelen zijn echter niet op de TUE aanwezig. Via Philips zijn deze artikelen aangevraagd.

<table>
<thead>
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Hoofdstuk 5

Sneeuwbal & Citatiemethode.

4.8 Sneeuwbalmethode

De sneeuwbal methode is uitgevoerd met artikel 3 dat overeenkomt met het doel van de zoekactie. Dit artikel verwijst naar "algemene" power converters en niet naar specifieke elektrochemische toepassingen. Toch heb ik deze referenties in een sneeuwbal diagram uitgezet. De waarde van zo'n sneeuwbal diagram is echter beperkt.

1995 3
1994
1993 4
1992
1985 5

4.1 Citatie analyse

Door in een bepaald jaar in de zoekoptie “citation” te kiezen kan men door het opgeven van een auteursnaam alle artikelen van dat jaar selecteren die verwijzen naar de opgegeven auteur. Dit is uitgevoerd voor de auteurs Langehorsten, Greg en Baenko, I. I. De artikelen van deze auteurs voldoen aan het gewenste zoekprofiel. M.b.v. de CD is gezocht tot 1990, echter geen enkele citatie. Met de gedrukte vorm is gezocht tot 1985. Ook hier geen enkele citatie.
Hoofdstuk 6

Conclusies & aanbevelingen

Het onderwerp, een voeding voor een electro chemisch proces, blijkt toch heel specifiek te zijn. Weinig referenties gingen specifiek in op dit onderwerp. Bij veel zoekactie, bleken de gevonden referenties chemisch van aard te zijn. Opvallend was de bijdrage in Russische referenties. Het electro chemisch bewerken is echter als eerste in Rusland toegepast.

De gevonden literatuur blijkt achteraf van weinig nut te zijn geweest. De specificaties van de gebruikte voeding blijken te ruim te zijn. Het aspect, modulaire, wordt zelfs niet genoemd.

Een tweede zoekactie zou meer specifiek moeten gaan over de voeding, zonder echt naar de toepassing te kijken. Gedacht wordt aan zoektermen zoals “current control”, “modules”, “parallel” en “dynamic”
Hoofdstuk 7

Literatuur

Tot betrekking van Hoofdstuk 1

1. Baenko, I. I.
   *DC Power Supply for Electrochemical Machining*, (for the Ekh-10B machine).

2. Langehorst, Greg
   *Update on Wire EDM*.

3. Holme P. R. and C. D. Manning
   *Assessment, Modelling and Simulation of an EDM Power Supply using Saber*.

4. Holme P. R. and C. D. Manning
   *Digital control of high frequency PWM converters*

5. Stevens R. P. and G. Bloom
   *Modern DC-to-DC Switchmode Power Converter Circuits*.
   New York: Van Nostrand Reinhold, 1985

Lectuur niet in belang van het literatuuronderzoek maar toch van belang van het afstudeer onderzoek.

HFD2/3
   Mohan, Ned and Undeland, Tore M. Robbins, William P.
   *Power Electronics, converters, applications and design*.
   New York: Wiley, 1989

HFD4
   Franklin, Gene F. and Powell, David J., Emami-Naeini Abbas.
   *Feedback Control Of Dynamic Systems*, 3nd ed.
   Massachusetts: Addison-Wesley, 1994