DESIGN OF A 5 W MINIATURIZED FLYBACK CONVERTER

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ABSTRACT

The purpose of this assignment was to develop a 5W galvanic isolated power supply with 7V output voltage and a maximum output current of 700mA. The power supply unit has to charge batteries that are used, for instance, in a notebook. As soon as the maximum output current of 700 mA has been reached, the output voltage has to drop and at the same time the output current has to stay 700 mA when the output voltage drops further down to a value of 4.5V. While the size of the power supply has to be roughly equal to that of a plug, the accent on miniaturisation was very important. The volume taken in by the power supply has to be smaller than 40cm³.

Because of its versatility, efficiency, size and its cost price, the switching power supply is preferred above the linear power supply. For the power supply a flyback converter was used.

The heart of the supply is the transformer. Because of safety requirements the output has to be isolated from the mains input voltage, and the distance between the primary and secondary winding has to be 6 mm. This 6 mm takes a lot of space and has an important impact on the aspects of miniaturisation. This problem can be circumvented by taking a triple isolated wire (triple because it is build up with three layers of teflon) for the secondary winding. The advantage is that this isolated wire can be wound on the top of the primary winding without breaking the safety requirements and thus avoiding 6mm of space!

For the control circuit a choice was made between two different IC’s: The Motorola MC 44603 and Power Integration Topswitch IC. The Motorola is a 16 pins IC and the Topswitch a 3 pins. The Motorola was capable of creating its own current foldback feature but unfortunately not within the specified limits. The Topswitch IC is very compact and with a few extra components it was possible to make a current foldback feature within the specifications.

Every switching device, like the switching power supply, creates noise. To attenuate this noise a common mode filter was used. The largest noise peak occurred at the switching frequency and the higher harmonics of this frequency.

All the specifications, measurements, results and conclusions are described in this report.
During my project I have learned a lot from the people within the 'Power Modules' development. I think it is very instructive for a student to work for a period of time in a company like for instance in my case: Philips. You are getting a lot of information from all kinds of different people from which you have to make a selection what is needed for your project. Within the half year stage period you have to learn as much as possible in order to finalise your project in this time period.
I think I was lucky to have a project that was as well theoretically as well as practically very interesting.
There is also another aspect that is very interesting, namely 'the organisation'. At the University you are not confronted with the different aspects within a company. Here you have to work more in a team. In a company the realisation of a target (budget) is very important for its survive, which puts more pressure on you.
Not only I learned a lot, but on the other hand I hope I contributed something to 'Power modules' too. There are a lot of people I want to thank. Firstly I want to thank Prof.ir.J Rozenboom who helped me to get this project and secondly Jan Cox who assisted me and learned me very much during my stage period at Philips. Also I want to thank Henk Vos and Jan van Laar who managed me and guided me in developing the converter. Further I want to thank all the ,very motivated, members of the 'Modules' crew:

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INTRODUCTION

At the finish of one's studies at the 'Technical University in Eindhoven' every student has to fulfil a project during half a year. This project can be inside as well outside the University. After this the student has to write a report about the things he has done and accomplished during his project.

Because I am very interested in power electronics I took a course 'Mini Power Electronics' from Prof.ir.J.Rozenboom. This same person helped me to get a project at the Philips company in Eindhoven within the Product Group 'Electronic Power Modules (EPM)' from the Business Unit 'Wire Wound Components (BU WWC)'. EPM develops switched mode power supplies (SMPS). Recently this Product Group has moved from Tilburg to Eindhoven. The production of SMPS is done in Ovar (Portugal).

Several SMPS are already in production and used in the CDI and the 'magic fax'. The applications of SMPS are various it can be used for transportation, telecommunication and commercial purposes. The market for SMPS is still expanding.

The reason why they make SMPS instead of linear power supplies is because the advantages are greater: the costs are lower, the size smaller and the weight lighter.

The specifications of the SMPS are made by the customer like for instance: power, size, costs etc. Usually it is difficult to combine them all, every extra specification from the customer will increase the costs. During the development of the SMPS you have to take in account all these aspects.

Nowadays the rising demand for battery-powered portable systems, ranging from PC's, cellular telephones, and camcorders to medical and industrial instruments and systems has stretched the performance of low-voltage SMPS to the limit. Moreover, the SMPS must combine minimum system cost with minimum size. The SMPS I had to develop had to be very small in size (<40 cm³). The idea is to develop a SMPS that looks like, or has approximately the same size, as a plug. The purpose of this SMPS is to charge batteries.

To protect the batteries and the SMPS an overvoltage and overcurrent protection must be included. Because every electrical switching device like a switched mode power supply creates noise, you have to apply a filter to attenuate this noise. There is a limit to this noise. An electrical noise source can be the cause of disturbances if it is in the neighbourhood of very sensitive receivers, like for instance wireless telephones. Therefore many limits were set-up to deal with this noise problem. In order to limit the noise below this specification you have to use a filter.
CHAPTER 1: POWER SUPPLIES

1.1 why use switching power supplies?

The choice whether to use a switching or linear power supply in a particular design is significantly based on the needs of the application itself. Each has its own disadvantage and advantage.

A great advantage of the linear power supply is its simplicity. One can purchase an entire linear regulator in a package and simply add two filter capacitors for storage and stability. The second major advantage is its quiet operation and load-handling capability. The linear regulator generates little or no electrical noise on its output, and its dynamic load response time -the time it takes to respond to changes in the load current is very short. The disadvantages of the linear-type regulator are its limit range of applications. First, it can be used only as a step-down regulator, which means that the designer must somehow develop an input voltage that is at least 2 to 3 V higher than the required output voltage. Second, each linear regulator can have only one output. So for each additional output voltage required, an entire separate linear regulator must be added. Another major disadvantage is the average efficiency of linear regulators. In normal applications, linear regulators exhibit efficiencies of 30 to 60 percent.

The switching regulator circumvents all of the linear regulator's shortcomings. Firstly the switching supply exhibits efficiencies of 70 to 90 percent regardless of the input voltage, thus drastically reducing the size requirement of the heatsink and hence its cost. The power transistors within the converter operate at their most efficient points of operation: saturation and cutoff. This means that the power transistors can deliver many times their power rating to the load and the less expensive, lower-power packages can be used. Since the input voltage is chopped into an AC waveform and transformed by a magnetic element, additional windings can be added to provide for more than one output voltage. Secondly, in case of transformer isolated switching supplies, the input voltage can vary above and/or below the level of the output voltages without affecting the operation of the supply. Since their frequency of operation is very much greater than the 50 Hz line frequency, the magnetic and capacitive elements used for energy storage are much smaller and the cost to build the switching supply becomes less than the linear supply. All of these advantages make the switching power supply a much more versatile choice, with a wider range of applications, than the linear supply. The disadvantages of the switching supply are minor and usually can be overcome by the designer. Firstly the converter is more complicated than the comparable linear supply. Secondly, considerable noise from the switching supply is generated on its outputs and input and radiated and conducted into the environment. This can be difficult to control and certainly cannot be ignored during the design phase. Generally additional filtering has to be added to the supply to limit the effects of the noise. Thirdly, since the switching supply chops the input voltage into time-limited pulses
of energy, the time it takes the supply to respond to changes in the load and the input is slower than the linear power supply.

In summary, because of its versatility, efficiency, size, and cost, the switching power supply is preferred in most applications. The advances in component technology and novel topological design approaches will only add to the desirability of power supplies in most applications. From now on we will use the word converter if we are talking about 'switched mode power supplies'.

1.2 applications of power supplies [12]

The applications for converters are various. They cover a wide power range from a few watts to several hundred megawatts. A few applications are given below.

*residential:*
  - refrigeration and freezer
  - air conditioning
  - lighting
  - personal computers

*commercial:*
  - heating, ventilating, and air conditioning
  - computers
  - elevators

*industrial:*
  - pumps
  - compressors
  - robots
  - industrial lasers
  - induction heating

*transportation:*
  - electric vehicles
  - battery chargers for electric vehicles
  - electric locomotives
  - trolley buses
  - subways

*telecommunications*
  - battery chargers
  - power supplies

These are only a few examples in which power supplies are used. The market for converters is still expanding and growing these days.
1.3 classification of converters.

If you are going to use a switched mode power supply or converter, you will have to make a choice between different topologies. Fig 1 gives you an example of the possibilities (SOPS stands for 'Self-Oscillating Power Supplies').

![Diagram of converter classification]

There are two types in this schematic that we will further discuss, namely: the flyback and forward type. Usually the forward converter is only designed for the continuous mode. For the converter we have to make a choice between flyback and forward. These are the most used types. Both systems have their own advantages and disadvantages.

1.4 specifications of the converter

If you are going to make a choice between flyback and forward, you should carefully keep in mind the most important specifications of the converter. All the specifications of the converter are given below. Specifications are made by the customer and the designer has to fulfill these requirements. The specifications given by the customer can be very high and difficult to accomplish. Mostly the costs of a converter are proportional to the demands of the customer. There are many items that can make the converter expensive, for instance: high precision, overcurrent and overvoltage protection, variable input voltage, high efficiency, size, etc. Sometimes it is difficult to
combine them all. For example: for every extra item you are going to use, you will need extra components that cause the efficiency to go down and increase the size of the converter.

In this case we have to develop a transformer-isolated 5 Watt converter and make it as small as possible. The reason for this is very simple: the demand for small converters on the market is very large. The volume taken in by the converter should be smaller than 40 cm³. The purpose of this converter could be for instance a battery charger. Further specifications are given below.

A) electrical specifications:

1. input voltage range: 100-15%; 240+10% Vrms
2. input frequency: 47-66 Hz
4. output voltage: 7V ±5 %
5. current mode:
   5.1. current mode I: 700 mA ± 10%
      output voltage: 4,5-7,35 V
   5.2. current mode II: 0-770 mA
      output voltage: 0-4,5 V

![Fig. 2: Foldback characteristic of the current](image)

6. ripple/noise: <100 mVpp
7. overvoltage protection 10 V<Vout<12,4 V
8. efficiency roughly 70 %

B) EMI/safety specifications:

1. UL1310 Direct plug-in Units
2. VDE 0871/6,78 EMI specifications level B
C) Mechanical specifications:

1. size: <40 cm³
2. cable: 1.5 m

There are two types of converters we are going to discuss further namely: the forward and the flyback converter. You will see in the next chapter that each has its own advantages and disadvantages. In order to make a choice between them, more research is necessary.
CHAPTER 2: FLYBACK AND FORWARD CONVERTER

2.1 forward or flyback converter?

If we want to make a the right choice between flyback and forward, we have to look at the advantages and disadvantages of both topologies.
In case of miniaturisation for example you can look at the quantity and size of the components that are needed to make the converter. Following items are going to help us to make our choice:

- transformer (costs and size)
- coil
- costs
- collector (drain) voltage
- output voltage(s)
- maximum drain current
- number of components to make the converter
- ripple current on the output

First we shall take a look at the forward and then the flyback converter. At the end I will give you an overview of these two topologies. The conclusions that will be made, are based on the given specifications. It doesn't mean that these conclusions will be the same for an other converter with other specifications.

2.2 the forward converter

A schematic circuit diagram of the forward converter is given in fig.3.\

\[\text{fig.3: forward converter}\]
Energy transfer takes place during on time of the transistor. The transformer acts as a real transformer (this is different with the flyback converter as you will see further on).

The forward converter needs a second electromagnetic element, namely the coil \( L \). During the on time \((\delta T_s)\) of the transistor, the diode \( D_2 \) will conduct and energy is stored in the inductor \( L \). When the transistor is off \((1-\delta)T_s\), the energy of the inductance will be transferred to the output. The forward converter (in this case) always runs in continuous mode, this means that the secondary current never reaches zero, see fig.4. A third winding in series with \( D_1 \) has been added to allow the magnetizing current to flow back into the source. The relation between the output and input voltage is found by the following rule [5]:

the average voltage during a period over an inductor is zero

If we apply this to the forward converter we find:

\[
\overline{V_L} = \frac{1}{T_s} \int_0^{\delta T_s} v_L \, dt
\]  
(1)

\[
\overline{V_L} = \frac{1}{T_s} \left[ \int_0^{\delta T_s} \left( \frac{V_1}{n} - V_o \right) dt - \int_{\delta T_s}^{T_s} V_o \, dt \right] = 0
\]  
(2)

finally:  \[\delta \left( \frac{V_1}{n} - V_o \right) - V_o (1 - \delta) = 0 \implies V_o = \delta \frac{V_1}{n}\]  
(3)
We can calculate the minimum transfer ratio by use of equation (3). We shall make the following assumption: a maximum duty cycle of 0.45 occurs at minimum input voltage \( V_{1,\text{min}} \) and maximum output current. In reality, the ratio can be made smaller because the output acts as a voltage source (the output capacitor and coil will hold the output voltage constant). For the transfer ratio we find:

\[
n = 8 \frac{V_{1,\text{min}}}{V_0} = 0.45 \cdot \frac{85 \sqrt{2}}{7} \approx 8
\]  

(4)

\( a) \) \textit{calculation of the coil } \( L \)

The minimum value of the inductor is determined by the minimum output current. At minimum output (10 mA), the current through the coil has to stay in continuous mode, see fig. 5. Between \( 0 < t < \delta T_s \), the current through the coil is:

\[
I_L = \frac{1}{L} \left( \frac{V_1}{n} - V_o \right) t \quad (5)
\]

At \( t = \delta T_s/2 \) the current through the coil is equal to the average output current \( I_o \). Keeping in mind that the largest swing in the inductor current occurs when \( V_1 = V_{1,\text{max}} \), the formula for \( L_{\text{min}} \) changes in:

\[
I_{o,\text{min}} = I_L (\delta T_s/2) = \frac{1}{2L_{\text{min}}} \left( \frac{V_{1,\text{max}}}{n} - V_o \right) \delta T_s
\]  

(6)

Substituting \( \delta = V_o n / V_1 \), \( T_s = 1/f \), and \( I_{o,\text{min}} = P_{0,\text{min}} / V_0 \):

\[
L_{\text{min}} = \frac{V_o^2 \left( \frac{V_{1,\text{max}}}{n} - V_o \right) n}{2P_{0,\text{min}} f \cdot V_{1,\text{min}}}
\]  

(7)

With:

\[
V_{1,\text{max}} = 270 \sqrt{2} = 381 \text{ V}
\]

\( n = 8 \)

\( V_0 = 7 \text{ V} \)

\( f = 100 \text{ kHz (chosen)} \)

\( P_0 = I_o V_o = 10 \text{ mA} \cdot 7 \text{ V} = 70 \text{ mW} \)

\( \Rightarrow \ L_{\text{min}} = 3 \text{ mH} \)
For the choice of the coil we also need the maximum current:
The maximum output current is 700 mA. Because the coil is very large, the maximum current won’t be much larger than 700 mA. With equation 8 and 9 we can solve the maximum current $I_p$ (at $t=\delta T_s$) and average current $I_o$.

\[ I_p = i L_{(0)} + \delta \frac{T_s}{L} \left( \frac{V_1}{n} - V_0 \right) \quad (8) \]

\[ I_o = i L_{(0)} + \frac{\delta T_s}{2L} \cdot \left( \frac{V_1}{n} - V_0 \right) \quad (9) \]

![fig.6: output current at maximum load](image)

Out of these two equations we find $I_p = 710$ mA. For the coil we can choose the $U_{10}$ or the $U_{11}$ type. The sizes of smallest one, $U_{10}$, are as follows:

-groundsface: $16 \times 10 \text{ mm}^2$
- height: 16 mm

This is a rather large and expensive component. The reason for the high value of $L$ is the minimum current at which the converter has to stay in continuous mode.

b) **transformer:** For the transformer we will use the E13/7/7 type. This is the smallest available transformer.

-groundsface: $15 \times 15 \text{ mm}^2$
- height: 15 mm

c) **ripple current:** The output current is always in continuous mode, therefore the output ripple current will be very low, especially when the output coil is large.

d) **collector (or drain) voltage** [3]: If the turn ratio between primary and tertiary winding is equal to one (which usually is), the maximum collector (or drain) voltage will be:

\[ V_{ce, \text{max}} = 2V_1 \]

e) **multiple outputs:** For every output there has to be an extra coil. At minimum load one of the outputs can go into discontinuous mode while the others are still operating in continuous mode. As a result, the unloaded output will be charged to $V_1/n$ in stead of $\delta V_1/n$. Because only one output can be regulated, one or more outputs will deviate...
from their nominal value.

f) maximum collector (or drain) current \(^{[3]}\): If we neglect the alternating current through the coil, and if we suppose \(u_1\) to be constant during a period, than:

\[
i_c = \frac{P_0}{5\eta V_1}
\]  

(10)

g) output filter: Because of the low output ripple current, the output filter can be made very small.
2.3 the flyback converter

A schematic of the flyback converter is given in fig. 7. The inductance action is integrated in the transformer. This is done by an airgap in the core, so that energy can be stored. At the on time of the transistor, the magnetic energy is stored in the transformer. During the off-time, the energy is given to the secondary side. The waveforms are given in fig. 8. The discontinuous mode occurs when the current has reached zero before the end of the period, fig. 8. If the current stays above zero, the converter is in the continuous mode, fig 9.

\[ D \]

\[ i_0 \]

\[ V_0 \]

\[ i_2 \]

\[ C \]

\[ R_L \]

\[ V_1 \]

\[ n:1 \]

\[ i_1 \]

\[ vce \]

\[ \Sigma n.i \]

\[ \delta T_1 \]

\[ \delta T_2 \]

\[ T_s \]

\[ \Sigma n.i \]

\[ i_0 \]

\[ \delta T_1 \]

\[ \delta T_2 \]

\[ T_s \]

\[ fig.7: \text{flyback converter} \]

\[ fig.8: \text{waveforms of the flyback converter, discontinuous mode} \]

\[ fig.9: \text{waveforms of the flyback converter continuous mode} \]
Out of the volt-second balance of the transformer it follows \[^{[5]}\]

\[
\frac{V}{n} \cdot \delta_1 \cdot T_s = V_0 \delta_2 \cdot T_s \Rightarrow \quad V_0 = \frac{\delta_1}{\delta_2} \frac{V}{n}
\]  \quad (11)

In continuous mode, \(\delta_1\) becomes \(\delta\) and \(\delta_2 = (1-\delta)\):

\[
V_0 = \frac{\delta}{1-\delta} \frac{V}{n}
\]  \quad (12)

We can calculate the minimum transfer ratio by means of equation 12. Maximum duty cycle \(\delta=0.45\) occurs at minimum input voltage \(V_{1,\text{min}}=85\sqrt{2}=120\) V and maximum output current.

\[
n = \frac{\delta_{\text{max}} \cdot V_{1,\text{min}}}{V_0 (1-\delta_{\text{max}})} \quad \Rightarrow \quad n = 14
\]  \quad (13)

2.3.1 flyback converter continuous

The waveforms of the flyback converter in the continuous mode are given in fig.9.

a) calculation of the coil \(L\):

We will use the primary current to calculate the minimum value of the inductance \(L_{\text{min}}\)

\[
i_1(t) = i(0) + \frac{1}{L} \int_0^t V_i \, dt
\]  \quad (14)

\[
\overline{i_1} = \frac{1}{T_s} \int_0^{\delta T_s} (i(0) + \frac{V_i}{L} \cdot t) \, dt
\]
or:
\[
\overline{I_1} = \delta i(0) + \frac{\delta^2 V_1}{2Lf}
\]  \hspace{1cm} (15)

The minimum average current occurs when \(i(0) = 0\):

\[
I_{1,\text{min}} = \frac{\delta^2 V_1}{2Lf}
\]  \hspace{1cm} (16)

Consider the worst case, \(V = V_{1,\text{min}}\) and substituting \(P_{0,\text{min}} = I_{1,\text{min}} V_1\) (the minimum power delivered to the load) and \(\delta = n \cdot V_0 / V_{1,\text{min}} + n \cdot V_0\) in formula (16), gives us the minimum value of the inductor value:

\[
L_{\text{min}} = \left( \frac{n \cdot V_0 \cdot V_{1,\text{min}}}{V_{1,\text{min}} + n \cdot V_0} \right)^2 \cdot \frac{1}{2 \cdot P_{0,\text{min}} f}
\]  \hspace{1cm} (17)

\[
= I_{\text{min}} = 200 \ mH
\]

The value of the inductor is much too high, we can therefore exclude the flyback converter in continuous mode.

### 2.3.2 Flyback Converter Discontinuous

The waveforms of the flyback converter in discontinuous mode are given in fig.8. At the moment the switch is closed, a certain amount of energy is stored in the transformer. During the off time, this energy is totally transformed to the output. If the inductor \(L\) has a too high value, the current cannot increase sufficiently. So there is a

![fig.11: primary current, flyback discontinuous](image-url)
limit on the maximum allowable value of L. Because of the fact that with increasing input voltage the required amount of current is reached in a shorter time, the limit case occurs at minimum input voltage.

\( a) \) calculation of the minimum inductor value:

In this case there is no direct relation between input and output voltage. Nevertheless some limits exist. During \( T_{on} \) the current increases linearly, starting from zero. At the moment that the switch is opened, a certain amount of energy is stored in the transformer. From magnetic theory, this energy equals \( \frac{1}{2}LI^2 \). During the off time of the switch this energy is totally transferred to the secondary. So, the amount of power, delivered to the output, equals the energy times frequency:

\[ P_0 = \frac{1}{2}LI^2 f. \]

The current \( I \) is the primary current at \( t = \delta T \):

\[
i_1 = \frac{1}{L} \int_0^t V_i dt = \frac{1}{L} V_i t \quad \text{at: } t = \delta T \quad \Rightarrow \quad i_1 = I_1 = \frac{1}{L} V_i \delta T
\]

For the maximum value of the inductor, we substitute \( \delta_{\text{max}} = nV_o(V_{i,\text{min}} + nV_0) \) and \( P_{0,\text{max}} = I_{o,\text{max}} V_0 \) in equation 18:

\[
\Rightarrow \quad L_{\text{max}} = \frac{T}{2P_{0,\text{max}}} (\frac{V_{i,\text{min}} + nV_0}{nV_0 + V_{i,\text{min}}})^2 = 3 \text{ mH}
\]

\( b) \) transformer: For the transformer we can use the El3/7/7 type. This is the same transformer as we chose for the forward converter in continuous mode. The coil value that we have calculated in formula 19 is large. In reality, as we will see this later on, this value will be a lot smaller (we have calculated the maximum value).

\( c) \) ripple current: For the flyback converter the output ripple will be a lot larger than the ripple for the forward converter, because the output current is not continuous. In reality we will have to put an extra filter in the output to filter out the noise and higher harmonics due to the high ripple current.

\( d) \) collector (or drain) voltage: during the flyback period the drain-collector voltage will be equal to: \( V_{ce} = V_1 + nV_0 \) (in practice this will be higher because of the leakage inductance of the transformer).

\( e) \) multiple outputs: It is very simple to create multiple outputs for the flyback converter, this is a great advantage. For every output, an extra winding on the core, a diode and an capacitor will satisfy. If, due to a heavy load, an output voltage is going to
drop, current will be delivered to the output.

\textit{f) maximum collector current:} In discontinuous mode the collector current can be found by means of the power $P_0$ \cite{5}:

$$P_0 = \frac{1}{T_s} \int_0^{T_s} \eta V_i i_1 \, dt \approx \frac{\eta \delta V_i i_1}{2}$$

$$= \quad i_1 = \frac{2P_0}{\eta V_i \delta_{\text{max}}}$$

(20)

\textit{f) output filter:} As explained before, the output filter is large because of the high ripple of the current.
2.4 comparison between forward and flyback

A short overview is given in table 1, in order to make a choice between the forward or flyback converter. An important thing to keep in mind is the word 'miniaturisation'. The number of components is therefore very important. A comparison is made between the forward converter in continuous mode and the flyback converter in discontinuous mode. You should carefully keep in mind that the calculations were specifically made for the converter with given specifications. This doesn't mean that for another application another converter than this one will be more suitable!

<table>
<thead>
<tr>
<th>Flyback discontinuous</th>
<th>Forward continuous</th>
</tr>
</thead>
<tbody>
<tr>
<td>inductor</td>
<td>integrated in the transformer, value &lt;3mH</td>
</tr>
<tr>
<td></td>
<td>⊗</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>transformer</td>
<td>E13/7/7</td>
</tr>
<tr>
<td></td>
<td>voll=3375 mm²</td>
</tr>
<tr>
<td>maximum current prim.</td>
<td>2P_0/(ηV_Lδ_{max})</td>
</tr>
<tr>
<td></td>
<td>twice as much as forward</td>
</tr>
<tr>
<td>collector voltage</td>
<td>V_{ce}=V_1 + nV_o</td>
</tr>
<tr>
<td>multiple output</td>
<td>very suitable for multiple output</td>
</tr>
<tr>
<td></td>
<td>⊗</td>
</tr>
<tr>
<td>output filter</td>
<td>large output filter</td>
</tr>
<tr>
<td></td>
<td>⊗</td>
</tr>
<tr>
<td>number of semiconductors and EM components</td>
<td>1 transistor 1 secondary diode 1 transformer</td>
</tr>
</tbody>
</table>

Table 1: comparison between the flyback and forward converter

⊗ = best performance for the relative item

Every converter has its own advantage and disadvantage, for this application where miniaturisation is the keyword and looking to the number of components, the flyback gives us the best opportunities. Because of the low minimum output current, the forward converter needs an extra 'large' coil at the output.

-17-
3.1 introduction

Before we are going to do some measurements on the flyback converter, we shall first take a look into the control methods of converters\textsuperscript{11}. This introduction will be very brief, but it gives you an idea about how you can look at the converter as a controlled system. In reality, the converter is a closed loop system and can be described in terms of three major elements, fig 12.

\textit{fig.12: control loop block diagram}

\(G_1(s):\) Transfer function of error amplifier and compensating networks.  
\(G_2(s):\) Transfer function of pulse width modulator and power switching circuit.  
\(H_c(s):\) Transfer function of the output power filter

What I want to show you is a part out of the control loop diagram namely: \textit{the control method}. We can distinguish three major control methods:

- direct duty cycle control
- voltage feedforward control
- current mode control

3.1.1 direct duty cycle control

The oldest and most common method used is the direct duty cycle control. A control voltage \(V_c\) is compared to a linear sawtooth ramp voltage \(V_r\). The comparator output
provides rectangular fixed frequency pulses which drives the power switch (transistor or fet). The duty cycle is controlled by variation of Vc, see fig 13.

These two signals are compared at the input of an opamp. The output of the opamp will be a pulse which the duty cycle varies when Vc changes. Mostly Vs is generated by an oscillator.

*advantage:*
- good load regulation

*disadvantage:*
- poor open loop line regulation (right half plane zero)
- two pole system resulting in poor dynamic control
3.1.2 voltage feedforward control

The principle is almost the same as direct duty cycle control. The difference is that the sawtooth ramp is not constant in amplitude, but varies in direct or partly direct proportion to the input voltage, fig 14. If \( V_c \) is fixed the duty cycle varies inversely with the input voltage, so that the volt-second product \( V_{in} \delta T \) remains constant without any control change.

advantages:
- open loop line regulation is very good.
- good dynamic response.

3.1.3 current mode control

fig.15: current mode control
Current mode also controls the duty cycle by comparing the control voltage to a fixed frequency sawtooth ramp. The sawtooth ramp voltage is sensed via a sense resistor $R_{\text{sense}}$. This current is the current through the inductor and the transistor. The innerloop is formed by feeding the inductor current back to the control comparator. The outerloop is formed by comparing the output voltage to a reference voltage. The control voltage directly programs the inductor current via the innerloop and no longer controls directly the duty cycle. This control mode is often used, the UC 3842 provides such a current mode control.

advantages:
- good open loop operation
- simplified loop, inductor pole and 2nd order characteristic eliminated
- no loop stability problems
- less complexity/cost

disadvantages:
- worse DC open loop regulation
- noise immunity is worse
- peak average current error and instability
CHAPTER 4: MEASUREMENTS OF THE CONVERTER

4.1 waveforms measurements

A theoretical description of the flyback converter and its waveforms are described in chapter 2. In this chapter we will take a look at the most important waveforms of the flyback converter and compare the theory with measurements taken from a flyback converter. I will also explain to you why the measured waveforms do not match the theoretical ones. We will discuss the following waveforms:

- drain voltage
- output voltage

In order to keep things as simple as possible, we will give a simple schematic (fig 16) of the flyback converter. In reality the converter (from which we took the measurements) was much more complicated. I believe that giving the whole schematic would only distract the attention from the reader, so only the most important components are given in fig.16.

![diagram of flyback converter]

fig.16: flyback converter

4.1.1 drain voltage

The drain voltage gives you much information about the state of the converter. You can derive the input voltage, output voltage, leak inductance and duty cycle from the waveform, fig 17 and 18.

Point 1 indicated in fig 17 is equal to \( V_i + n.V_o \), point 2 is equal to \( V_i \).
The primary duty cycle is equal to $\delta_1 T_\pi$, the secondary is $\delta_2 T_\pi$. You can see in fig. 17 and 18 that the measured wave drainform differs a lot from the theoretical one. Oscillations are appearing on the drain. In practice, the voltage on the drain can reach a value up to 500-600 volts, or even more. In order to keep the fet or transistor alive, the drain has to be protected against these high voltages. These protection circuits are called 'peak clamps'. The oscillations are a result of oscillations between the leakage inductance of the transformer and other parasitic capacitances. The explanation of these ringings are given below.

In order to understand the oscillations on the drain, we have to investigate the transformer an it's leakage inductance.

4.1.1.1 the effect of leakage inductance on the drain voltage

First we have to keep in mind that the transformer is not ideal. There are also primary and secondary dispersing fluxes as you can see in fig.19. We can replace the transformer by an ideal transformer and represent the dispersing fluxes by two extra leakinductances, fig 20. $n_p$ and $n_s$ are the ideal transformer and $L_p, L_s$ the leakage inductances for respectively the primary and secondary winding. The leakage induc-
tance is a parasitic element, it can cause excessive power switch dissipation and high voltage stress levels. These leakage inductances can cause high voltage peaks and destroy the transistor. Apart from the leakage inductance, the transformer also contains a leakage capacitance. We can put all these inductances and capacitances in a model for the flyback converter, fig 21. $C_s$ contains the leakage capacitance of the transformer and the capacitance of the switch (fet or transistor).

![fig.20: equivalent-circuit diagram of a transformer](image)

4.1.1.2 drain-waveform explained

We can divide the drain period into 4 pieces, namely:

a) $0 < t < t_1$: transistor is on  
b) $t_1 < t < t_2$: transistor is off, secondary diode doesn’t conduct and there is no power transfer to the output.  
c) $t_2 < t < t_3$: transistor is off, diode is conducting and power is transferred to the output.  
d) $t_3 < t < t_4$: secondary current is zero.
Fig. 22: drain voltage, primary and secondary current

Fig. 22 shows the drain voltage which is divided into 4 time intervals. The primary and secondary current are also represented.

a) $0 < t < t_1$

During this interval, the transistor is on. The voltage over the primary winding of the transformer is equal to the input voltage $u_1$. The voltage over the drain-source is equal to $V_d = R_{ds}I_1$ (Rds is the drain-source or collector-emitter resistance). For the primary current between $0 < t < t_1$ we can write:

$$i_p = \frac{1}{L_p} \int L_p dt = \frac{1}{L_p} V_1 t$$

This is a linearly rising current. The primary current is shown in fig. 22.

b) $t_1 < t < t_2$

The transistor is off in this time interval, but there is no energy transfer to the output. After switchoff the capacitance $C_s$ will charge with $dv/dt = Ip/C$, and the drain voltage will rise. When the 'transformer' of the flyback converter would not have any leakage inductance, the voltage would stop at $V_d = V_1 + nV_o$. However, due to the leakage inductance, the drain voltage will be much higher. The voltage on the drain has to raise a $\Delta V$ in order to push a current $\Delta I$ through the secondary leakage inductance, fig 23.
c) \( t_2 \leq t \leq t_3 \):

After the voltage has reached \( V_d = V_1 + nV_0 + \Delta V \) the secondary diode starts to conduct. The circuit diagram is depicted in fig 23. Now the circuit can be described as a current source (validated by the fact that \( L_p \gg L_s \)), and a L-C parallel connection clamped by the output voltage. The result is that through the diode a current flows, consisting of a superposition of a decaying sawtooth \((-nV_0/L_s t)\) and a sinusoidal current due to the \( L_s-C \) oscillation. During the very first part of the conduction time the sinusoidal component is the dominant one, see interval \( t_3 \) to fig 22. Roughly the oscillation frequency is equal to:

\[
f_{2,3} = \frac{1}{2\pi/\sqrt{C L_{s2}}}
\]  

(22)

d) \( t_3 \leq t \leq t_4 \):

Between \( t_3 \) and \( t_4 \), the secondary current is equal to zero (see fig.22). The oscillation will take place between \( C, L_p \) and \( L \). Because \( L_p \gg L_s \), the oscillation frequency will be much lower than the frequency \( f_{2,3} \). The circuit diagram is given in fig 24. The oscillation frequency is now equal to:

\[
f_{3,4} = \frac{1}{2\pi/\sqrt{C \left(L_{s2}, L\right)}}
\]  

(23)

After \( t_4 \), the switch is turned on again and a new period is started. As you can see, the drain voltage can give you much information about the state of the converter. If you are doing measurements it is always handy to observe this drain waveform.
4.1.2 Output voltage

The ripple on the output voltage can be influenced by two things namely:

- output current
- rectified input voltage

The output current will produce a ripple on the output with a frequency equal to the switching frequency. The rectified input voltage produces a ripple with a frequency equal to the line frequency. Usually, the ripple due to the rectified input voltage is very small. With a good regulation this ripple will almost be entirely eliminated.

4.1.2.1 Output ripple caused by the input ripple

Only variations of the rectified input voltage will effect the ripple on the output. The voltage over the input capacitor, after the bridge rectifier, not only contains a high DC-component but also an AC-component, fig.25a. This AC-component can also be seen on the output, fig.25b. This phenomenon appears to be most visible at minimum input voltage. This is because the ripple on the input capacitor will be relatively 'high' compared to the DC value. If the input capacitors are large and if the converter has a good regulation and control circuit, this effect will hardly be visible on the output.

4.1.2.2 Output ripple caused by the output capacitor

The output current can cause a ripple in the output voltage. This can be explained by replacing the output capacitor with the equivalent circuit diagram fig.26. The output capacitor is not an ideal element, apart from its capacitance, it also contains a ESR (equivalent series resistance) and ESL (equivalent series inductor). The triangular output current will cause a voltage drop over the ESR. This voltage drop can be seen on the output voltage, with a frequency equal to the switching frequency, fig.27. If the ripple on the output voltage is too high, we will have to filter it out. Usually 2 capacitors and a choke will be sufficient to deal with these noises. The output filter will be discussed in a next chapter.
fig. 26: equivalent circuit diagram of the output capacitor

fig. 27: output current and ripple in output voltage
CHAPTER 5: DIMENSION OF A 5 WATT CONVERTER

In this chapter, following three items will be discussed:

- input circuitry
- transformer
- output filter

All these dimensions and measurements are based on the given specifications given in chapter 1.

5.1 input circuitry

The basic function of the input circuitry is to convert the AC input voltage into a smoothed DC voltage, which in turn serves as the input voltage for the power supply itself. The basic circuit is therefore a bridge rectifier, followed by a smoothing capacitor, which also acts as energy storage device, during that part of the 50/60 Hz mains cycle when the instantaneous voltage is low. The bridge rectifier, storage capacitor C and load currents are represented in fig. 28. Sometimes the main voltage can disappear completely for a half cycle or several cycles. During drop out no current can be drawn from the mains, and thus no power. During this drop out, a minimum of voltage has to be maintained across the input capacitor in order to keep the converter working. One can imagine that the value of the input capacitor(s) will be very important. If the capacitance value is too low, the rectified voltage can drop so much that the converter doesn't work properly anymore, it can go into a hick-up mode (switching on and off). There has to be a minimum value of the input capacitor. A description of variables are given below:

\[ V_p = V_{1,\text{min}} \cdot \sqrt{2} \]
\[ V_{\text{max}} = V_p - V_v \]
\[ V_{\text{min}} = V_{\text{max}} - V_r \]

- \( V_{1,\text{min}} \) (minimum input voltage, ac)
- \( V_v = 5 \) (voltage drop across diode)
- \( V_r = 40 \) (allowable peak to peak ripple)
There can only be a current during that part of the mains cycle when the instantaneous voltage is higher than $V_c$, fig 28. The length of time during which no charging current flows into the capacitor is given by eq.24.

$$t = a \cdot T \left( \frac{T}{2\pi} \right) \left( \arcsin \frac{V_{\text{max}}}{V_p} \right) \left( \arcsin \frac{V_{\text{min}}}{V_p} \right)$$  \hspace{1cm} (24)$$

The factor $a$ in formula 24 is constant. If the mains drops out for a half-cycle then $a=0.5$, for one full-cycle $a=1$ and for continuous mains voltage $a=0$. The required input capacitor for a half-cycle mains failure $a=0.5$ becomes:

$$C_i = \frac{2 \cdot t}{V_{\text{max}}^2 - V_{\text{min}}^2} \left[ \text{F} \right]$$  \hspace{1cm} (25)$$

With

$V_{1,\text{min}} = 85 \text{ VAC}$

$V_{\text{max}} = 115 \text{ V}$

$V_{\text{min}} = 75 \text{ V}$

$t = 0.016 \text{ s}$

remark: The capacitor will be charged to approximately the peak voltage of the mains. However due to the voltage drop across the diode and other series impedances the actual peak voltage will be somewhat lower. The voltage will even be lower when the load increases.

For the input capacitor we will connect two capacitors of 3.3 $\mu$F (total 6.6 $\mu$F) in parallel.

5.2 transformer

In chapter 2 we have already calculated that the maximum value for a flyback converter in discontinuous mode is equal to 3 mH. The energy stored in the inductor during the on time is [69]:

$$W = \frac{1}{2} L \cdot I_p^2$$  \hspace{1cm} (26)$$

During the off time of the switch this energy is totally transferred to the secondary. So, the amount of power, delivered to the output, equals the energy times frequency:

$$P_0 = W \cdot f = \frac{1}{2} L \cdot I_p^2 \cdot f$$  \hspace{1cm} (27)$$

If we substitute $I_p$ equation 21 in $P_0$, the value for $L$ becomes, eq.28.
We want to transfer 5 Watt to the output. Also in the worst-case condition the transformer has to deliver its power to the output:

\[
V_1 = V_{1,\text{min}} = 110 \text{ V}
\]

\[
\delta_{\text{max}} = 0.45 \text{ (at maximum load)}
\]

\[
f = 100 \text{ kHz}
\]

\[
P_o = P_{o,\text{max}} = 10 \text{ Watt}
\]

We chose a high value for the output power because we want the transformer to stay alive when the output will be short circuit. With these values the inductor becomes:

\[
L = 1.2 \text{ mH}
\]

Before we are going to calculate the number of windings we should keep in mind an important Maxwell formula, namely \[29\]:

\[
\text{rot} (E) = \dot{B} \quad \text{or} \quad \oint_E ds = n_1 \int_A \dot{B} dA
\]

If the transformer core has a constant cross-section (which is true in our case) eq.29 can be written as \[30\]:

\[
u_1 = \oint_E ds = n_1 \cdot \dot{B} A
\]

\[
\rightarrow u_1 \cdot \delta \cdot T = n_1 \cdot dB \cdot A
\]

And if \( B \) starts at zero:

\[
u_1 \cdot \delta \cdot T = n_1 \cdot B A
\]

We have to calculate the number of turns for the worst-case conditions \[32\]. We have chosen for core material with a \( B_{\text{max}} = 320 \text{ mT} \) and an E13/7/7 core type, with \( A = 25.3 \text{ mm}^2 \).

\[
\rightarrow n_1 = \frac{u_{1,\text{min}} \cdot \delta \cdot \text{prim, max}}{f \cdot B_{\text{max}} \cdot A}
\]

\[-31-\]
\[ n_1 = 63 \text{ turns} \]

For a fixed frequency converter: \( \delta_{\text{sec}} \leq 1 - \delta_{\text{prim}} \) (\( \delta_{\text{prim}} \) and \( \delta_{\text{sec}} \) are marked in fig.22). For the primary we have chosen 0.45, for the primary \( \delta_{\text{prim}} = 0.55 \). With the values we have calculated in formula 32 we can determine the number of secondary windings.

\[
\frac{u_{1, \text{min}} \delta_{1, \text{max}}}{n_1 \cdot f} = B_{\text{max}} \cdot A = \frac{u_0 \delta_{2, \text{max}}}{n_2 \cdot f} \tag{33}
\]

\[
n_2 = \frac{n_1 \cdot u_0 \delta_{2, \text{max}}}{u_{1, \text{min}} \delta_{1, \text{max}}} = 5
\]

With eq. 27 we can calculate the primary peak current:

\[
I_1 = \sqrt{\frac{2 \cdot P}{L \cdot f}} = 0.44 \text{ A} \tag{34}
\]

All these calculations can be made with a program called "TRAFO-DESIGN" written by Uwe Mandler division 'Wire Wound Components', Philips. This program will calculate in the same way the desired values to develop your transformer (flyback discontinuous mode). An example of such a calculation is given in annex nr.3 page 85-88.

For safety requirements there has to be 6 mm air and creepage distance between the primary and secondary winding. This 6mm can cost you a lot of space especially when miniaturisation is involved. One can circumvent this problem by taking a triple isolated wire (triple because it is build up with three layers of Teflon) for the secondary winding. The advantage is that you can wind this isolated wire on top of the primary winding without breaking the safety requirements and thus avoiding 6mm of space! The secondary leads are flying as you can see in fig.29.

\[ \text{fig.29: transformer with secondary flying leads} \]
5.3 output filter

The ripple on the output is caused by the output current and the ESR of the output capacitor (see 3.2.2.2). We can reduce this ripple by placing a filter in the output. The output filter is built up with two capacitors C1 and C2 and a choke L, see fig.30. The first capacitor C1 acts as a storage capacitor, L and C2 are added to filter out the ripple-current. The turnover frequency has to be chosen far below the ripple frequency. The turnover frequency of the filter is equal to:

\[ \omega_0 = \frac{1}{\sqrt{LC_2}} \]

\[ f_0 = \frac{1}{2\pi \sqrt{LC_2}} \]  (35)

*note: this is only true for all frequencies until \( \omega \cdot ESL = 1/\omega \cdot C_2 \)*

A choke with value L=6,8 \( \mu \)H and a capacitor C2=470 \( \mu \)F gives a crossover frequency equal to \( f_0 = 3 \)kHz. Because the filter is a second order network, it will have a second order roll-off so that signals, with a frequency high above the crossover frequency, are strongly attenuated. If we omit the filter, the output ripple would be too high and the accuracy wouldn't meet the required specifications (5% ripple). The high ripple in a flyback converter is a disadvantage and a large and expensive filter has to be added in the output.
In recent years, a large variety of IC's have emerged in the marketplace that have facilitated the implementation of higher-level functions within a switching power supply. The selection of the best controller IC should be done after the designer knows the level of functionality that is expected of the system. Although control ICs can have very different block diagrams, they have certain common circuit functions, including:

1. An oscillator that sets the basic frequency of operation of the supply and also generates a ramp waveform for use in voltage to PWM conversion.
2. Output drivers that provide enough drive current for low-and medium-power applications.
3. A voltage reference that provides the overall power supply 'ideal' reference to which the output voltages are compared. It also can provide a stable voltage for other control functions.
4. A voltage error amplifier that performs the high gain voltage comparison between the output voltages and the stable reference.
5. An error voltage-to-pulsewidth converter that sets the duty cycle output in response to the level of the error voltage from the voltage error amplifier.

These functional blocks form the basic PWM control IC. Other functions are sometimes included in the IC provide some higher level of functionality like:

1. An overcurrent amplifier that protects the supply from abnormal overcurrent conditions within the load.
2. A soft-start circuit that, as the name implies, starts the power supply in a smooth fashion, reducing the inrush current exhibited by all switching power supplies during this period.
3. Undervoltage lockout to prevent the supply from starting when there is insufficient voltage within the control circuit for driving the power switches into saturation.
4. An overvoltage protection that will save the supply when the output voltage is too high.
In this chapter two 'new' IC's will be discussed namely

- Motorola IC MC 44603
- Power Integration Topswitch IC

A choice has to be made between these two IC's. The Motorola IC is a 16 pins IC and the Topswitch a 3 pins IC. One can imagine that an 16 pins IC can give you more possibilities. This is true, but do we need them all? On the other hand, a 3 pins IC can save you much space because of its simplicity. We will first start with the Motorola IC.

6.1 Mixed frequency Motorola MC 44603 IC

In fig.31 a block diagram is depicted of the converter with secondary voltage sensing. The Motorola IC is placed on primary side between the opto-coupler and the power switch.

The control circuit MC 44603 is an universal controller which can operate in various conduction modes:

- The controller can be used in the continuous and discontinuous mode. In the continuous mode the controller operates in the fixed frequency mode.
- In the discontinuous mode the controller is able to operate in a fixed frequency mode, a variable frequency mode or in a mixed mode (fixed and variable).
- The device has the unique feature to reduce the switching frequency at a low power level ⇒ stand-by mode. Both the frequency reduction and the power level at which frequency reduction occurs, can be externally programmed. This feature improves
the efficiency of the system at this low power level.

- The IC has been optimized as a current mode controller but it also possible to apply it as a duty-cycle controller. In fig. 32 an overview of the various operation modes of the MC44603 is given.

In our case only the discontinuous conduction mode is important, because the converter works in discontinuous mode. An interesting feature that is included in the MC44603 is the foldback function (for specifications chapter 1).

The frequency reduction mode is an interesting feature but not really necessary for our application. In fact this IC is specially made for television applications. For a television in stand-by it is important to have a low power consumption, this can be realised by means of the frequency reduction mode in this IC.

The total electric circuit diagram is given in annex 2 page 84. The most important components in this diagram are:

- power switch: Fet FRC20 (nr.70011)
- transformer: E 13/7/7 type
- bridge rectifier: S1NB80 (nr.7000)
- motorola IC: 44603 (nr.7008)
- error amplifier: TL431 (nr.7040)
- opto coupler: CNX82A (nr.7030)
- start up network
6.2 primary side

We shall first take a look at the components at the primary side. To isolate the secondary side from the primary we will use an opto-coupler. The last paragraph will handle the secondary side. At the secondary side, the variation of the output voltage will be measured by means of the TL431. This device is applied as a differential amplifier with a built-in reference voltage of 2,5V.

5.2.1 start up network

In the supply block three threshold levels are defined for well defined starting-up and switching off behavior.

starting-up threshold
after reaching this level (14,5V) in upward direction the IC is fully functional

disable voltage level 1 (UVLO1)
When this level (9V) is reached downwards after turn on the slow start capacitor will be discharged and consequently the duty cycle will be reduced.

disable voltage level 2 (UVLO2)
At this level (7,5V) the output stage will be blocked and all the functions are disabled. The initial phase is activated.

The $V_{cc}$ treshold levels are shown in fig.33. The IC is supplied via a bleeder resistor with a value of 220 kΩ (resistance nr.3001 in schematic annex 2 p 84).

At a minimum input voltage of 120V, the input current will be $120/220.10^3 = 0.5$ mA. This current is sufficient to supply the IC with enough current (0,3 mA needed, see fig.34). During starting-up, the capacitor of $47\mu F$ has to be charged via the rectified mains, the startup resistor of 330k and $47\mu F$. It will take some time to charge this capacitor. If the charging time is too high, it will take the converter

\[ \text{fig.33: } V_{cc} \text{ treshold levels} \]
too long to start-up (the output capacitors have the time to discharge again during the off time). If the charging time is too low, the capacitors on the output will not be fully charged because the time is too short. After starting-up the IC-supply voltage should be taken over by an auxiliary winding (see fig.34) on the switched mode transformer. This voltage should be related to the output voltage \( V_0 \) in order to generate a hick-up mode at overload. It should be guaranteed, especially at low load, that during take over the supply voltage should stay above 9,4V. The VCC-supply voltage should be above 9,4V and below the minimum overvoltage protection level of 16,1V; so \( 9,4V < V_{CC} < 16,1V \). We have chosen for a value of 13V, see trafo file annex 3 page 90 and 91. The filter network, 10Ω and 220 nF, reduces the spikes on the supply voltages \( V_{CC} \). A zenerdiode has been placed over the 47\( \mu \)F capacitor to keep the voltage below 16V.

6.2.2 overvoltage protection

The overvoltage protection is intended to protect the power supply against a too high output voltage, e.g. incase of an open feedback loop. During the start-up phase, switch S is opened to prevent an increase of the start-up current. Switch S will be closed after 5\( \mu \)s. This delay is necessary to guarantee no false triggering of the overvoltage protection. The IC is supplied via the flyback winding on the transformer, therefore the supply voltage \( V_{CC} \) is related to the output voltage. In this way the output voltage can indirectly be protected. An overvoltage condition is detected if a signal on pin 6 has a duration of at least 2\( \mu \)s and exceeds the level of 2,5V. Via the latch the output is blocked and consequently the power switch is switched off. This results in a decrease of the supply voltage \( V_{CC} \). The supply capacitor is discharged by the IC-supply current. As soon as \( V_{CC} \) is below 7,5V the latch is reset and the initialisation phase will be activated.
6.2.3 foldback function

The foldback feature can be created with pin 5. This feature implies less dissipation during overload and will protect the circuit. The voltage on pin 5 influences the current sense threshold level $V_{CS\text{th}}$. The transfer function of the foldback function is shown in fig 36. The input of pin 5 should be connected, via a resistor divider, to the IC-supply voltage $V_{CC}$, which is related to the regulated output voltage, see fig. 37.

![fig.36: foldback transfer function](image)

![fig.37: foldback function](image)

If the load is increased the output voltage $V_{CC}$ will decrease as soon as the maximum peak current has been reached (see peak current 5.2.4). If $V_{0}$ decreases also $V_{CC}$ will decrease and consequently the voltage on pin 5 decreases.

A decrease of pin 5 results in a reduction of the peakcurrent, which causes the output voltage to decrease even further. In this way the foldback function is created. In order to prevent the foldback voltage from influencing the current sense threshold during normal operation, $V_{pin5}$ should be above 1,05V. However to realize an optimal foldback function which is activated slightly above the maximum load level, $V_{pin5}$ has to be only slightly above 1,05V. For the voltage divider we have chosen the resistance value equal to 150k and 15k (see nr.3020 and 3017), the voltage on pin 5 will be equal to 1,18V.
6.2.4 maximum peak current

The IC has been optimized as a current mode controller (see par.3.1.3). The duty cycle is controlled by comparing the control voltage to a fixed frequency sawtooth ramp. In this case the control voltage is the output voltage of the error amplifier. The sawtooth is taken from a current sense resistor in the source, see fig.38. When the voltage $V_{CS}$ is higher than $V_{\text{EIA out}}$, the current sense comparator resets the latch. The set-pulse of the latch is generated by the positive edge of the output voltage of the oscillator $V_{\text{osc}}$. The error amplifier output signal controls the peak current on a cycle-by-cycle basis and varies the duration of the output signal $V_{\text{out}}$. The maximum peak current is limited by an internal clamp (1V) of the error signal. Therefore the maximum current is:

$$I_{\text{max}} = \frac{1}{R_{\text{sense}}} = \frac{1}{2.4\,\Omega} = 0.41\,\text{A}$$

The value of the maximum current is chosen in relation to the foldback function as explained in 6.2.3. If the load is increased the output voltage $V_{CC}$ will decrease as soon as the maximum peak current has been reached. The foldback function has to start when the output current reaches a value of 700mA. For currents higher than this, the output voltage has to go down. The sense resistor value of 2.4 $\Omega$ (nr.3005) turned out to be a good choice. Often it is just a matter of trying out and see what gives you the best results. To eliminate the spike across the sense resistor, which causes instability, a RC-filter is added (330$\Omega$, 2.2nF). Further on in this chapter we will see that the measurement of the peakvoltage from $V_{\text{sense}}$ depends on the input voltage, which causes inaccurate measurement.
6.2.5 switching transistor

For the switching transistor we have chosen a FRC20 FET. The MC44603 contains a high current totem pole output which is specially designed for driving a power-MOSFET. The output stage is shown in fig.39, namely the resistors 3009, 3003 the buffer and the MOSFET. \( R_{3009} + R_{3003} \) determine switch-on behavior. Soft switching is advantageous for EMI and a reduced current spike across \( R_{\text{sense}} \). Soft switching is disadvantageous for switching losses. \( R_{3003} \) determines switching off behavior. Fast switching off is advantageous for switching losses. In fig.39 you can see the effect of soft and fast switching on the drain voltage and the drain current.

The gate of a MOSFET can often be viewed as a capacitor from gate to source whose value can range from 900 to 2000 pF. If the gate current is high, the 'capacitor' of the fet will be charged very quickly and the fet will be turned on very fast.

The transformer has a parasitic capacitance which will act as a short-circuit due to the high slope of the drain voltage (high frequencies). This short-circuit will cause a high current peak through the drain (see fig.40). When the fet is turned off very fast, the voltage on the drain will rise due to the leakage inductor of the transformer. These peaks can cause much unwanted radiation and is a disadvantage for EMI. If the gate current is low the transistor will be turned on softly. The time during switching on and off will be much longer which results in higher switching losses because the product \( V_d I_d \delta \tau_{\text{on(Toff)}} \) is high.

The best way to find the right gate resistance value, is to put the drain voltage and current on the scope and watch the waveforms. For the gate resistance we took a value of 200Ω.

![Diagram](image_url)
6.2.6 peak clamp

In chapter 4 paragraph 4.1.1, I have explained that the drainvoltage can rise so high, $V_i + nV_0 + \Delta V$, that it can damage the switching transistor. At maximum input voltage the drainvoltage can rise up to 600 or 700 volts. The fets we are using are not capable of resisting these high voltages. In order to protect the drain, we have to put in a protection circuit to eliminate the spike on the drain. For this we will use a 'peak clamp', see fig.41.

When the voltage on the drain is too high, the zenerdiode will conduct and will eliminate the spike on the drain. The voltage on the drain can rise to:

$$ V_d = nV_0 + V_i + \Delta V $$

(37)

With the zenerdiode you can reduce $\Delta V$. The voltage on the drain is not allowed to exceed $V_{d,max}$, so:

$$ V_z + nV_0 + V_i \leq V_{d,max} $$

The zener has to conduct when the voltage on the drain exceeds:

$$ V_d = V_{i,max} + nV_0. $$

Because $V_z = V_d - V_i$ the minimum zenervoltage is given by: $V_z > nV_0$

With:

$$ V_{i,max} = 270/2 = 380 \text{ V} $$
$$ V_{d,max} = 700 \text{ V} $$
$$ n = N_t/N_x = 63/5 = 12 \text{ (see par.3.2)} $$
$$ V_0 = 7 \text{ V} $$

We have chosen for a zenervoltage of 150 V. If you choose this value too low, the dissipation will be large because the large spike has to be fully dissipated in the zener. A too high value of the zener voltage can cause disturbances and radiation because of the large spike.

6.3 mains isolation: the opto-coupler

The control info is transferred from the mains-isolated side to the not-isolated side by means of the opto-coupler, see fig.42. The RC-filter 2012 and 3016 reduces the switching
ripple. The resistor $R_{3016}$ determines the setting current "Ie" of the photo transistor. For the photo transistor current yields:

$$I_c = -V_{EA\,out} \frac{R_{3015}}{R_{3014}} + V_{ref} \left(1 + \frac{R_{3015}}{R_{3014}}\right) \cdot \frac{1}{R_{3016}}$$

Fig. 42: primary side: error amplifier and photo transistor. Secondary side: secondary error amplifier (TL431) and photodiode

The current "Ie" shouldn't be chosen too small because of sensitivity for interferences, it shouldn't be chosen too high because of reduction of linearity factor. A good choice for "Ie" is: $1\text{mA} < I_e < 8\text{mA}$. The maximum current occurs when the photo transistor is in saturation. The collector-emitter current will be equal to:

$$I_c = \frac{V_{aux}}{R_{3016}} = 6.5 \text{ mA}$$

We have chosen an emitter resistance (nr.3016) of 2k, see fig.42. At starting or in case of an overload the control current "Ie" carried by the opto-coupler is zero. In this situation the output of the error amplifier $V_{EA\,out}$ should be high ($V_{OH}$) in order to prevent a limitation of the peak current. This means that $V_{OH}$ should be at least 4.4 V. To guarantee this the input of the error amplifier (pin 14 from the IC) must be smaller than 2.5V. If we assume that $R_{3015} >> R_{3016}$ the following equation can be written:

$$V_{OH} \cdot \frac{R_{3015}}{R_{3014} \cdot R_{3015}} < 2.5V \quad \text{or:} \quad R_{3015} < 1.3R_{3014}$$

-43-
We will choose \( R_{3015} = R_{3014} \). The minimum value for \( R_{3015} + R_{3014} \) is given by the minimum source current of the error amplifier of 0.2 mA and the value of \( V_{EAout} (V_{OH}) \) to reach the current sense threshold of 1 V.

\[
R_{3015} + R_{3014} \geq \frac{4.4}{0.2 \cdot 10^{-3}} \\
R_{3015} + R_{3014} \geq 22 \text{ k}\Omega
\]

We will choose both values equal to \( R_{3015} = R_{3014} = 15 \text{ k}\Omega \).

6.4 Output error amplifier

The secondary-referenced error amplifier shown in fig.40 controls only the output voltage and is implemented with a TL431 shunt regulator. This device consists of an accurate 2.5V bandgap reference, error amplifier and driver. The non inverting input of the error amplifier is internally connected to the bandgap reference voltage. The output voltage is sensed, divided by \( R_{3043} \) and \( R_{3044} \), and applied to the inverting input of the error amplifier. We will choose \( R_{3043} = 20 \text{ k}\Omega \) and \( R_{3044} = 10 \text{ k}\Omega \) in order to get 2.5 V on the inverting input with an output voltage of 7V. The frequency response of the error amplifier is determined by the resistor and capacitor in the feedback loop of the opamp (TL431).

6.4.1 Secondary photodiode

The maximum forward current for the photodiode is limited to 100 mA. We will take a series resistor of 100 \( \Omega \) to set the diode current. Suppose the output from the TL431 is zero volt, than the maximum current with 100 \( \Omega \) will be 70 mA.
6.5 performance measurements on the MC 44603

We will do some measurements on the Motorola converter to see if it meets the specified requirements. We will take a look to the following items:

- foldback characteristic and maximum peak current
- efficiency
- precision

6.5.1 foldback characteristic and maximum peak current

The foldback characteristic will be measured at different input voltages. The load variation at the output will be done with a variable resistor. As explained in 5.2.3, the output voltage will decrease as soon as the maximum peak current has been reached. The input voltage and load variation are as follows:

\[ V_i: 120V, 200V, 250V, 300V \]
\[ I_0: \text{from } 0 \text{ to } >700mA \]

The characteristics are shown in fig.43. When the output current has reached a maximum, the output voltage will go down and the output current will decrease until a hick-up mode has been reached. The hick-up mode (converter is switching on and off) starts at an output voltage of approximately 4.5-5V. You can also see that the foldback depends on the input voltage (see 1, 2, 3, 4, fig 43). At \( V_i=120 \) V it starts at \( I_0=680 \) mA, with \( V_i=300 \) V it starts at \( I_0=800 \) mA. The circuit will go into hick up mode at \( V_o\approx4.5V \).

The foldback doesn't show a current mode in it's characteristic. In the specifications (paragraph 1.4, fig 2) you can see that the required foldback characteristic differs a lot from this one. For battery chargers, characteristic nr 1, fig.2, is the most preferable one. The measured characteristic don't fall within the specified accuracy requirements. You can also see that the foldback depends on the input voltage. The explanation for this is quite simple. The IC cannot measure in an infinite short time. The output voltage is going down from the
moment that the maximum primary peak current has been reached. The reason why the foldback depends on the input voltage is caused by error measurement of the peak current, see fig.44. The primary peak current is measured via a source resistor. The maximum peak current is limited by an internal clamp of 1V.

The slope at minimum input voltage will be much lower than the slope at maximum input voltage. Suppose the IC takes a time $t_s$ to measure the peak from the primary current, than the peak at maximum voltage has to rise further to reach the time $t_s$. In this way you make an error at high input voltages.

It is very difficult to tune $I_{max}$ and $I_{0,\text{max}}$ to each other so that the foldback takes place at the right moment.

### 6.5.2 efficiency

Efficiency is the amount of power the supply must use (or waste) in order to provide power to its loads. The major portion of this internally generated power is converted into heat by the various components.

In order to measure the efficiency, we will use a Watt-meter at the input and a volt and amperemeter at the output. The output power will be regulated with a variable output resistor. Annex 1 page 80 gives you a measurement of the efficiency at an input voltage of 220V AC. The efficiency is higher than 70%, as required.

### 6.5.3 precision

To measure the precision, we will vary the load and measure the output voltage. We will repeat this measurements for different input voltages. The precision of the output voltage has to be within 5%, see table 2.
<table>
<thead>
<tr>
<th>$V_i$ [V]</th>
<th>$V_{out}$ [V]</th>
<th>$I_{out}$ [mA]</th>
<th>$\Delta V$ [%]</th>
</tr>
</thead>
<tbody>
<tr>
<td>120</td>
<td>7,5</td>
<td>100</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>7,2</td>
<td>700</td>
<td>4</td>
</tr>
<tr>
<td>200</td>
<td>7,5</td>
<td>100</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>7,3</td>
<td>700</td>
<td>2,7</td>
</tr>
<tr>
<td>250</td>
<td>7,5</td>
<td>100</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>7,4</td>
<td>700</td>
<td>1,3</td>
</tr>
<tr>
<td>300</td>
<td>7,5</td>
<td>100</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>7,4</td>
<td>700</td>
<td>1,3</td>
</tr>
</tbody>
</table>

Table 2: accuracy of the output voltage with variable load and input voltage.

The nominal output voltage is 7,5 V. The output voltage is within the required specification of 5%, the maximum deviation is 4%.

6.6 conclusion

Unfortunately the motorola IC doesn’t fullfill all the required specifications. The output voltage is within the specification, as well as the efficiency, but the foldback characteristic is far from the desired one. This doen’t mean that it is always desirable to have such a square characteristic. In many applications this is not required. For this application the foldback principle depents too much upon the input voltage and the hick-up mode starts to early (about 4,5V). We have to look out for another IC that has the capability of creating the 'square' foldback characteristic.
6.7 Power Integrations Topswitch IC

The Topswitch family implements, with only three pins (see fig.45), all functions necessary for a switching power supply. Compared to discrete MOSFET and controller implementations, a TOPSwitch integrated circuit can reduce the total number of components. This is an interesting feature, because miniaturisation and size are very important in our application. The device combines a high-voltage N-channel output MOSFET with a fully integrated voltage-mode switching power supply controller. The data sheets are given in annex page 80. The pin functional description is as follows:

- **drain pin**: (see D fig.45) output mosfet drain connection. Provides internal bias current during start-up operation via an internal switched high-voltage current source. Internal current sense point.
- **control pin**: (see C fig.45) error amplifier and feedback current input pin for duty cycle control. Internal shunt regulator connection to provide internal bias current during normal operation. Trigger input for latching shutdown. It is also used as the supply bypass and auto-restart compensation capacitor connection point.
- **source pin**: (see S fig.45) output MOSFET source connection. Primary-side circuit common, power return, and reference point.

6.7.1 internal control circuit

During normal operation, the internal output MOSFET duty cycle linearly decreases with increasing CONTROL pin current as shown in fig.46. An external bypass capacitor closely connected between the control and source pin is required to supply the gate driver current. The total amount of capacitance connected to this pin also sets the auto-restart timing as well as control loop compensation. In annex 2 page 80 you can see this capacitor on the control input, it's value is equal to 47μF. If you take a look into the IC, you can see that $V_c$ (on control pin) current is supplied from a high-voltage switched current source.
connected internally between the drain and control pins. The current source provides sufficient current to supply the control circuitry as well as charge the external bypass capacitor. During normal operation (when the output voltage is regulated) feedback control current supplies the $V_c$ supply current. The shunt regulator keeps $V_c$ at typically 5.7 V by shunting control pin feedback current exceeding the required DC supply current through the PWM error signal sense resistor $R_E$.

If the control pin external capacitance should discharge to the lower threshold, than the output mosfet is turned off and the control circuit is placed in a low-current standby mode. The high voltage current source is turned on and charges the external capacitance again. The hysteretic auto-restart comparator keeps $V_c$ within a window of typically 4.7 to 5.7 V by turning the high-voltage current source on and off. The auto-restart circuit has a divide-by-8 counter and prevents the output mosfet from turning on again until eight discharge-charge cycles have elapsed.

**oscillator:** The internal oscillator linearly charges and discharges the internal capacitance between two voltage levels to create a sawtooth waveform for the pulse width modulator. The oscillator sets the pulse width modulator/current limit latch at the beginning of each cycle. The nominal frequency is 100 kHz.

**current limiting:** The cycle by cycle peak drain current limit circuit uses the output mosfet on-resistance as a sense resistor. A current limit comparator compares the output mosfet on-state drain-source voltage with a threshold voltage. High drain current causes $V_{DS}$ to exceed the threshold voltage and turns the output mosfet off until the start of the next clock cycle. The current limit comparator threshold voltage is temperature compensated to minimize variation of the effective peak current limit due to temperature related changes in output mosfet.

**disadvantage:** because there are only 3 pins on the ic, the possibilities are limited. The frequency and primary current are fixed and cannot be changed. However it is a great advantage that ,due to the minimum of three pins, the IC is compact . So you have to make a compromise between the advantages and disadvantages and see what is best for your application.

### 6.7.2 external components

some components will be the same as in the motorola application,namely:

- peak clamp
- rectifier bridge and input storage capacitors
- transformer is identical, only the primary voltage will be different.
- output capacitors and output filter
Many of these items are already discussed in chapter 4. Step by step I will take you to the final circuit. You will notice that during the development the circuit will become more complex. I will first start with the most simple circuit and explain to you why it doesn’t perform well or why it does. Everything is based on simplicity, this means: make a converter with as few as possible components.

6.7.3 converter with primary feedback

The primary (bias) winding is, just like the secondary winding, a flyback winding. This means that the voltage on the primary winding reflects the output voltage. If the output voltage is going down, the bias voltage is going down too. So why not use the primary winding and regulate it instead of the secondary winding? If you are able to control and regulate the primary voltage, the secondary voltage will be regulated too. In order to guarantee a good regulation for the output voltage, you have to make sure that the magnetic coupling between the primary winding and secondary winding is very good (approximately equal to 1). One can improve the coupling between secondary and primary by bifilar winding. You can find the trafo design file in annex 3 page 92 and 93. The number of turns on the primary winding are the same as the secondary ones. After I have made the trafo I wanted to know if the coupling between primary and secondary winding (\(k_{12}\) and \(k_{21}\)) was good enough. We can calculate the coupling factor with the equivalent-circuit diagram of fig 47. In this schematic the primary winding is \(n_1\) and the secondary \(n_2\). The measurements below are important to calculate the coupling factor.

\[
\begin{align*}
L_{11} &: \text{trafo inductance measured at primary side, with secondary open.} \\
L_{12} &: \text{trafo inductance measured at primary side, with secondary short.} \\
L_{22} &: \text{trafo inductance measured on secondary side, with primary open.} \\
L_{21} &: \text{trafo inductance measured on secondary side, with primary short.}
\end{align*}
\]

With these measurements and with \(n_1=n_2=5\) we can calculate the coupling factor and if you wish to, the leakage inductance.
\[ k_{12} = \frac{n_1}{n_2} \sqrt{\frac{L_{22} - L_{21}}{L_{11}}} \]  
\[ k_{21} = \frac{n_2}{n_1} \sqrt{\frac{L_{11} - L_{12}}{L_{22}}} \]

and leakage inductances:

\[ L_{a1} = L_{11}(1 - k_{12}) \]  
\[ L_{a2} = L_{11} \cdot k_{12} \left( \frac{1}{k_{21}} - 1 \right) \]

With the measured values \( L_{11}, L_{12}, L_{22}, L_{21} \) the coupling factors and leakage inductances becomes:

\[
\begin{align*}
L_{11} &= 11.74 \mu\text{H} & \Rightarrow k_{12} &= 0.995 \\
L_{22} &= 11.96 \mu\text{H} & k_{21} &= 0.976 \\
L_{12} &= 348 \text{nH} & L_{a1} &= 59 \text{nH} \\
L_{21} &= 335 \text{nH} & L_{a2} &= 287 \text{nH}
\end{align*}
\]

The secondary leakage inductance is larger than the primary one. This is due to the triple isolated secondary wire. The leakage inductance due to this isolated wire is much larger.
than the primary one. The coupling factor between the primary and secondary winding is very good (close to one). Now we can try out the primary feedback principle, see fig 48 and annex 2 p.85. We know that the current into the control pin is inversely proportional to the duty cycle, see fig 46. The output voltage will be regulated as follows: if \( V_{\text{out}} \rightarrow V_h \rightarrow I_{\text{control}} \rightarrow \delta \rightarrow V_{\text{out}} \). In the configuration fig.48 we can write for the control current:

\[
\frac{V_a - V_z - 5.7}{R_z} = I_c
\]  

(45)

The control pin always stays at a voltage level of 5.7 V (internally). With a voltage on the primary winding of 8 V and a zener of 1 V2, the control current and and series resistor \( R_z \) becomes:

\[- \quad I_c = 4 \text{ mA} \]

\[- \quad R_z = 330 \text{ } \Omega \]

You can improve your sensitivity by taking a higher zener voltage so that the numerator of the equation (45) will be closer to zero. So that a \( \Delta V_z \) will give you a larger \( \Delta I_c \). The measurements were done with a zener diode of 2 V2 and a series resistor of 25 \( \Omega \).

\[ V_{i_n}: 85 \rightarrow 270 \text{ } V \quad \rightarrow \Delta V_{\text{out}} = 0, 2 \text{ } V \]

\[ I_0: 0 \rightarrow 700 \text{ } mA \quad \rightarrow \Delta V_{\text{out}} = 1, 2 \text{ } V \]

The total variation of the output voltage can be 15 to 20%! This is too much and unacceptable.

**explanation:** If you are looking to the voltage on the primary winding you will see that it is very stable. This is very logic because you are in fact regulating the primary winding and not the secondary winding.

The situation on the primary winding differs from that on the secondary winding. On the secondary winding you have a load variation, this is not on the primary winding (only a small value \( \Delta I_{\text{control}} \)). This load variation causes a voltage drop over the input impedances of the secondary winding. The situation on the primary winding is totally different, it is almost a constant load. The voltage variation on the primary winding is only 0.2 V when the secondary load varies from 0 to 700 mA.

I have tried out this feedback principle with different zeners and number of turns on the primary winding, but it didn’t improve the accuracy. We have to conclude that this regulation via the primary winding is not good enough for our application.
6.7.4 converter with secondary feedback with opto-coupler and zener-diode

We know now that if we want to have a good regulation with a stable output voltage we have to regulate the secondary output voltage itself. We have to create a steady reference voltage and compare it with the output voltage. The simplest way to do this is by means of a zener-diode on the output as shown in fig. 49 and annex 2 p. 86.

The output voltage is compared with the zener-voltage. The difference between the zener-voltage and output voltage gives you a current through the opto-diode that changes if the output voltage is changing. If for instance \( V_{out} \rightarrow I_{opto-diode} \rightarrow I_{emitter} \rightarrow I_{control} \rightarrow R \rightarrow V_{out} \). The collector-voltage for the opto-coupler is delivered by the primary winding. The allowable collector voltage for the opto-coupler CNX82A is between \( \approx 3V \) and 50V (current source area). High sensitivity will be achieved if the zener-voltage is chosen near the output voltage. If you look into the data sheets you can see that a zener-voltage of 5V1 gives the best performance. It is the less temperature dependent one and the most voltage dependable zener-diode. The precision of the circuit depends upon the precision of the series resistor and zener-diode. We will therefore take a 1% resistor and a 1% zener-diode. If we choose the current through the photo-diode equal to 20mA, the series resistor \( R_s \) will be equal to:

\[
R_v = \frac{V_{out} - V_{zener}}{I_{photo}} = \frac{7V - 5.1V}{20mA} = 100\Omega
\]  

We will measure the accuracy by varying the input voltage and output current.

\[ V_{in}: 85 \rightarrow 270V : \quad \rightarrow \Delta V_{out} = 0.3V \]
\[ I_0: \ 50 \rightarrow 700 \ mA: \quad \Rightarrow \Delta V_{out} = 0, \ 5 \ V \]

note: we let the output current start from 50mA, this is done with a purpose because at low output current the zener diode will go out of its linearly area and the zener voltage will be no longer equal to 5V1. You can prevent this by adding a resistor in the output (fig. 49, resistor \( R_p \), parallel with the load) to create a bias current.

The output depends too much upon the input voltage, you can eliminate this by placing a resistor from the rectified input voltage to the control input of the Topswitch, fig. 49 resistor \( R_c \). This is a forward regulation, if the input voltage is rising, the current through this resistor into the control pin will rise too, the duty cycle will go down and the output voltage will decrease. With this forward regulation I was able to lower the \( \Delta V_{out} \) to 0.1V.

The output accuracy is still too low, namely 8.5%. The efficiency is, due to \( R_p \) and \( R_c \) which dissipate much, very low (55% maximum). If we want to have the output voltage within 5%, we will have to try something else. In a good regulation a small \( \Delta V_{out} \) will gives you a 'large' \( \Delta I \) through the opto-diode. This can be accomplished with a TL431 shunt regulator.

6.7.5 converter with secondary feedback with opto-coupler and shunt regulator

A TL431 shunt regulator directly senses and accurately regulates the output voltage see also annex 2 p 87. It regulates the output voltage by controlling optocoupler LED current (and Topswitch with duty cycle) to maintain an average voltage of 2.5V (internally accurate bandgap reference) at the TL431 input pin. The TL431 was also used in the Motorola IC (44603) and many other applications. The circuit is given in fig. 50.
The accuracy is very high, if we vary the input voltage and output current:

\[ V_{in}: 85 \rightarrow 270V \quad \text{and} \quad I_0: 0 \rightarrow 700mA : \quad \Rightarrow \Delta V_{out} = 0,2V \]

The variation in the output voltage is within 5%, namely 2.8%. Measurements on the efficiency, taken at different input voltages, are given in annex 1 page 81. The efficiency is about 70% maximum, this is sufficient for the application. 

**Conclusion**: it seems that the shunt regulation performs good. The output voltage is within 5% and the efficiency is around 70%. The only thing that is missing is:

- current foldback
- overvoltage protection

There is only a primary current limit protection in the Topswitch IC (internally via a comparator). When the primary peak current is too high, it automatically turns off the Topswitch fet. There is no foldback principle as required in the specifications, so we have to make the foldback ourselves.
6.12 over current protection

The easiest way to get the information from the output current is via a resistor in series with the source, it is called 'direct current sensing' because the output current is directly flowing through this current sense resistor [2], fig. 51. The general idea is as follows: the voltage from the current sense resistor is compared to a voltage at the input of an opamp, when a certain output current level has been reached (700 mA) the output voltage has to decrease. If the output current is lower than the maximum allowable current, the foldback regulation has to be out of order and may not influence the output voltage regulation. Because there are two opamps available in the NE532 8-pins IC, we can use the second one for voltage regulation. So we have

- opamp 1 that regulates the foldback
- opamp 2 that regulates the output voltage

The converter acts as a constant voltage/constant current output unit, dependent on the load conditions. The two regulations have to be independent to one another. The output and current/voltage regulation is shown in fig.51 and annex 2 page 88.

The output current is sensed via a sense resistor in the output (see R, fig.51). When the load current increases, the voltage drop across this resistor becomes greater. The voltage divider resistors 15k and 39Ω (see fig.51) also takes part in forming the error signal and the output characteristic. As the resistance of 39Ω is increased, the foldback of the output characteristic also becomes greater, see fig.52. In this way, the short-circuit current can be reduced essentially to zero if you want to. The supply voltage for the opamps and current/voltage regulation is provided via the rectified secondary forward winding and voltage stabilizer MC78L08 (8 Volt output).
The regulated converter of constant-voltage/constant-current characteristic shown in fig.52, is a capable feature of resisting any overload. Such a converter acts as a constant-voltage or constant current unit, dependent on the load conditions. The current characteristic is just what we need, it will be achieved when $R_s$ is equal to 22mΩ. The output voltage and current can be varied at will up to the maximum permissible limits by potentiometers $P_1$ and $P_2$. 
6.13 overvoltage protection

A zenerdiode can be used to limit the output voltage as shown in fig.53. We will use the primary winding to detect an overvoltage, because when the output voltage is going to rise, the primary voltage is also going to rise and gives you an indication of the output voltage. If an overvoltage situation occurs, the converter has to go into a hick up mode, this can only be accomplished if the control current is lower than 2mA or higher than 50mA. You can create this by sourcing the current out of the control pin into the negative flyback voltage, fig.53. When \( V_{\text{out}} = V_{\text{prim}} = 11V \), the converter has to go into the 'auto-restart' mode. The zenervoltage has to be:

\[
V_z = V_{\text{control}} - V_{\text{prim}} = 5,7 \times 11 = 16V
\]  

For the series resistor we took a value of 12 \( \Omega \) (practical value).

6.14 measurements on the voltage and current control Topswitch

We will do some measurements on the converter to see if it satisfies the requirements. We shall take a look at:

- accuracy
- foldback
- efficiency
- dissipations

The accuracy of the output voltage should be within 5%, the foldback characteristic should have the same form as fig.2 page 4. The efficiency of the converter has to be around the 70%. If the efficiency is low, it means that there is much dissipation lost within the converter.
6.14.1 accuracy

The measurement will be taken at different input voltages and cross-load (minimum and maximum load). The results are summarized in table 3.

<table>
<thead>
<tr>
<th>Vin (Vac)</th>
<th>Vout (v)</th>
<th>I₀ (mA)</th>
<th>ΔVout [%]</th>
</tr>
</thead>
<tbody>
<tr>
<td>100</td>
<td>7.05</td>
<td>10</td>
<td>0.7</td>
</tr>
<tr>
<td></td>
<td>7.03</td>
<td>650</td>
<td>0.4</td>
</tr>
<tr>
<td>130</td>
<td>7.05</td>
<td>10</td>
<td>0.7</td>
</tr>
<tr>
<td></td>
<td>7.00</td>
<td>650</td>
<td>0</td>
</tr>
<tr>
<td>170</td>
<td>7.05</td>
<td>10</td>
<td>0.7</td>
</tr>
<tr>
<td></td>
<td>7.01</td>
<td>650</td>
<td>0.1</td>
</tr>
<tr>
<td>220</td>
<td>7.05</td>
<td>10</td>
<td>0.7</td>
</tr>
<tr>
<td></td>
<td>7.01</td>
<td>650</td>
<td>0.1</td>
</tr>
<tr>
<td>270</td>
<td>7.06</td>
<td>10</td>
<td>0.8</td>
</tr>
<tr>
<td></td>
<td>7.01</td>
<td>650</td>
<td>0.1</td>
</tr>
</tbody>
</table>

*Table 3: accuracy of the Topswitch converter with voltage and current regulation*

The highest deviation of the output voltage is 0.8%, this is far below the required 5%. Above 700 mA the output voltage is going down because of the current regulation.

6.14.2 foldback characteristic

Now we have created the current regulation we can test it out to see if it meets the specifications. The load variation is done with a variable output load resistance. The measurements were taken at different input voltages.

The characteristic is taken in fig.54. The limits of the current and voltages are within specification (compare it with fig.2). If you wish you can change the characteristic by means of P₁ and P₂, see fig.52. For our application this 'square' V-I characteristic is

*fig.54: foldback characteristic with current regulation*
just what we want. In the next paragraph we will take a look at the efficiency of this converter.

6.14.3 efficiency and dissipation

With the shunt regulator and opto-coupler we saw that the efficiency was just above the 70%. Looking to the number of components that are used within the current/voltage regulator (let's call this regulator 'foldfly' from foldback and flyback) I expect that the efficiency will be a lot lower than in case of the shunt regulator. There is one comfort: losing more than 30% efficiency in 5W is less worse than losing it in an application of 50W!

Annex 1 page 82 gives you the efficiency plots at different input voltages. The maximum efficiency is around 60%. This is very low. The low efficiency is a result of dissipations within the foldfly. We can locate this dissipation by temperature measurements. The temperature gives you an indication of the dissipation of the relative component because dissipation is transformed into heat. The temperatures were taken with an infra-red temperature sensor. Temperature measurements were taken from:

- Topswitch IC
- transformer
- rectifier bridge
- opto-coupler
- peak clamp

6.14.3.1 dissipation Topswitch IC

All the measurements were taken with:

\[
\begin{align*}
V_{\text{in}} &= 220V \\
I_{\text{in}} &= 22 mA \\
V_{\text{out}} &= 7V \\
I_{\text{out}} &= 400 mA
\end{align*}
\]

\[ \Rightarrow P_{\text{in}} = 4.90 \text{ W}\]

\[ \Rightarrow P_{\text{out}} = 2.84 \text{ W}\]

The power loss in the converter is equal to: \( P_{\text{dis}} = 4.90-2.84 = 2\text{ W}\). This is the dissipation in the converter like: transformer, IC, peak clamp, and other components.

It is not always simple to calculate the dissipation of a component when its temperature is known. For the Topswitch it is not so difficult.

The temperature on the surface of the Topswitch IC is equal to \( T_{\text{top}} = 60^\circ\text{C}\). We can calculate the power dissipation in the Topswitch by using the Thermal impedance \( \theta_{JA}\). The thermal impedance of the Topswitch is given in the data sheets and is equal to \( \theta_{JA} = 110^\circ\text{C/W} \ (R_{th})\), this means that if the temperature from junction to ambient changes 110°C the dissipation is equal to 1W. Don’t forget to measure the ambient temperature because you have to subtract this from the measured temperature! With \( T_{\text{ambient}} = 23^\circ\text{C} ,\)
the power dissipation is equal to:

$$P_{\text{diss}} = \frac{T_{\text{op}} - T_{\text{amb}}}{R_{\text{th}}} = 0,34 \, W$$

(48)

This is 15% of the total dissipation. The largest dissipation will occur in the power fet (internal).

6.14.3.2 transformer dissipation

It is difficult to calculate the dissipation in the transformer. There is however a rule of thumb that you can use for the dissipation in the trafo.

\[
\text{the increase in temperature depends on the cooled off surface and applied power}
\]

or:

\[
\frac{667}{A} = \frac{\Delta T}{P}
\]

With P the dissipation in Watt, \(\Delta T\) the temperature rise and A the surface of the transformer through which the temperature flows out in the open. With a temperature rise of \(\Delta T = 47^\circ\text{C}\) and a surface \(A = 10,14 \, \text{cm}^2\), the dissipation is:

$$P_{\text{diss}} = \frac{A\Delta T}{667} = 0,71 \, W$$

(49)

This dissipation is 34% of the total dissipation!

6.14.3.3 peak clamp dissipation

There is a way to calculate the dissipation in the zenerdiode. When the switch is turned off, the primary current is going to decrease lineary to zero and the current through the zener is going to increase lineary, see fig.55. The DC- current through the zener during a period is equal to the average primary current during \(\Delta T\):

\[I_1 \, dIz/dt, \Delta T \, dIz/dt\]

(fig.55: circuit diagram for determination of the dissipation in the zenerdiode)
The power in the zener diode is given by:

\[ P_z = V_z I_{dc} \]

where:

\[ I_{dc} = \frac{1}{2} \frac{L_p (1 - k) I_1^2 f_s}{V_z n V_0} \]

and:

- \( L_p = 1.8 \text{ mH} \)
- \( V_z = 150 \text{ V} \)
- \( I_1 = 260 \text{ mA} \) (\( I_0 = 400 \text{ mA} \))
- \( k = 0.99 \)

This is 7.8% of the total dissipation.

### 6.14.3.4 Dissipation Voltage Regulator MC78L08

The dissipation in the voltage regulator is very simple: the output power distracted from the input power gives you the dissipation in the MC78L08. The currents and voltages were done by measurement:

- \( V_{in} = 35 \text{ V} \) \( I_{in} = 6 \text{ mA} \) \( \Rightarrow P_{in} = 0.21 \text{ W} \)
- \( V_{out} = 8 \text{ V} \) \( I_{out} = 6.4 \text{ mA} \) \( \Rightarrow P_{out} = 0.06 \text{ W} \)

The dissipation in the voltage regulator \( P_{diss} = 0.15 \text{ W} \), this is 7.3% of the total dissipation.
6.14.3.5 summary

All the dissipations are put together in table 4.

<table>
<thead>
<tr>
<th>type</th>
<th>ΔT (°C)</th>
<th>dissipation (W)</th>
<th>% loss</th>
</tr>
</thead>
<tbody>
<tr>
<td>Topswitch IC</td>
<td>37</td>
<td>0,34</td>
<td>15</td>
</tr>
<tr>
<td>peak clamp</td>
<td>-</td>
<td>0,16</td>
<td>7,8</td>
</tr>
<tr>
<td>voltage reg.</td>
<td>-</td>
<td>0,15</td>
<td>7,3</td>
</tr>
<tr>
<td>transformer</td>
<td>47</td>
<td>0,71</td>
<td>34</td>
</tr>
</tbody>
</table>

*table 4: power losses*

*conclusion:* It follows that the transformer has the greatest dissipation. The only thing you can do about it is by re-designing the transformer or by choosing another core or larger transformer than the E13/7/7.

In spite of the low efficiency, the Topswitch performs well on the other items. There is only one thing we haven’t looked at yet and that is the noise caused by the converter. Next chapter will go further into the noise problems and how to deal with it.
CHAPTER 7: NOISE AND FILTER DESIGN

7.1 Introduction

Every electrical switching device causes noise or disturbances. A switched mode power supply contains switches and therefore causes noise.

There is a limit to this noise. An electrical noise source can be the cause of disturbances if it is in the neighbourhood of very sensitive receivers, like for instance wireless telephones. The first thing that was dealt with, by the radio control service, was the disturbances for radio receiving; "Radio Frequency Interference, RFI". An international commity with the name 'Comité International pour la Suppression des Perturbations radio-électrique' (CISPR) was set-up. Many noise measurements are based on the activities of the CISPR.

The noise requirements for electrical devices can vary a lot. The requirements for gas-discharge lamps for instance are quite different from the power supplies.

electromagnetic interference (EMI): because of rapid changes in voltages and currents within a switching converter, power electronic equipment is a source of electromagnetic interference with other equipment as well as with its own proper operation.

In this chapter we will discuss several items like:

- EMI-specifications
- how to measure the noise on a converter
- development of a filter to attenuate the noise
- test results taken on the converter

electromagnetic interference specifications vary from country to country, product to product, and also change over time.

EMI can course disturbances in two different ways: by radiation and conduction. The noise caused by conduction often is much greater than the noise caused by radiation. This chapter will therefore only deal with noise caused by conduction.

Various standards and guidelines have been established which specify limits of the magnitudes of harmonic currents and harmonic voltage distortion at various harmonic frequencies. Some of these are as follows [1]:

1. EN 50 006, "The limitation of Disturbances in Electricity Supply Networks caused by Domestic and Similar Appliances Equipped with Electronic Devices," European Standard prepared by Comité Européen de Normalisation Electrotechnique, CENELEC.

2. Standards VDE 0838 for domestic applications, VDE 0160 for converters, and VDE 0712 voor fluorescent lamp ballasts.
The CENELEC, IEC and VDE standards specify the limits on the voltages at various harmonic frequencies of the switching frequency, when the equipment-generated harmonic currents are injected into a network of which the impedances are specified. For the converter, the VDE 0871 standard is specified. A few standard limit lines are shown in fig nr.56.

7.2 EMI measurement by means of a LISN (Line Impedance Simulation Network).

Noise caused by conduction can be measured by means of a LISN. A LISN purpose is to provide a stabilized impedance to conducted emissions, without interfering with the normal power flow required by the Equipment Under Test (EUT). A conceptual schematic of the generator, LISN and load is shown in fig 57a [1].

At the power line frequency $f_p$, the LISN shown in fig 57b [1] provides a low impedance path from the power source to the load impedance and a high impedance path from the load.

fig 57: a) conceptual diagram of the LISNs b) at the power line frequency $f_p$ c) at noise frequency $f_n >> f_p$
to the ground. At the noise frequency, $f > f_n$, the LISN provides a high impedance path from the power source to the load, and it provides an impedance approaching $50 \, \Omega$ at high frequencies from the load to ground, as shown in fig 57c. The low frequency high impedance is provided by a capacitor to ground. The 50 ohm impedance, to ground is actually the input impedance of the spectrum analyzer or EMI meter used to measure the noise.

To understand the impedance stabilizing nature of the LISN, we solve for the load terminal to ground terminal impedance, assuming an ideal voltage source on the line side, fig 58. To determine the input impedance, we use the Thevenin's law by replacing the voltage source by a short. Note that this circuit is simply a RC series network with an inductor shunting it. At low frequencies, the inductor is dominant, so the input impedance is $j\omega L$. At high frequencies, the inductor is a virtual open relative to $50 \, \Omega$, and the capacitor is a relative short. The impedance is then $50 \, \Omega$. Analytically, the expression for input impedance of the circuit in fig.58 is:

$$Z_i = \frac{-\omega^2 LC \cdot 50 + j\omega L}{-\omega^2 LC + j\omega C \cdot 50 + 1}$$

At low frequencies, this simplifies to:

$$Z_i = \frac{j\omega L}{1}$$

while at high frequencies the $\omega^2$ terms dominate so that:

$Z_i = 50\Omega$. A plot of the LISN's impedance is shown in annex nr.4 page 95. The inductance used in the LISN determines at which level of a frequency the input impedance will start to approach $50 \, \Omega$. The plot annex 4 page 96 and 97 shows a noise measurement of the converter without a filter. There are two plots needed for this measurement:

1. Noise measured between 9kHz and 150kHz (page 90).
2. Noise measured between 150kHz and 30 MHz (page 91).

At low frequencies you can clearly see a noise peak at a frequency of 100kHz. This noise
peak is the largest and most dangerous one of all. It is far above the specified limit line and there are more harmonics of this peak frequency that will contribute to the noise. You can see that there is a lot of noise between frequencies of 150kHz and 5MHz. If we can lower the noise peak at 100kHz (switching frequency), the higher harmonics of this frequency will also be a lot smaller.

7.3 conduction modes: common mode and differential mode

There are two types of noise: differential mode (DM) and common mode (CM). Differential noise is the simplest kind of noise. It occurs between the leads of the intentional current path (phase-neutral) as depicted in fig 59. It is also characterized by the currents flowing in the phase and neutral lines being 180° out of phase. Common mode noise is characterized by the noise currents flowing in the phase and neutral lines being in phase. This is shown in fig 60 and 61. There are two subcategories of common mode noise, referred to as type 1 and type 2. Figure 60 illustrates common mode noise type 1. In this mode, the common mode noise is referenced to the chassis, which is in turn, grounded to the reference plane. The current path is through the ground plane, because it has the lowest impedance path. Common mode type 1 on cables is the cause of radiation problems, given good PCB design. This is because the large loop area enclosed by the current path

---

fig.59: single phase differential mode noise source

fig.60: single phase common mode Type 1 noise

fig.61: single phase common mode Type 2 noise
makes a fairly efficient radiator. The differential mode currents, in contrast, enclose a very small loop area. Common mode type 2 typically occurs when the chassis is isolated from the reference plane, fig 61. In that case, a parasitic capacitance is in series with the return path through the reference plane. This high impedance capacitance results in the safety ground wire now appearing as the lowest impedance return path, hence carrying the most of the current. The radiating loop area enclosed by the current path of common mode type 2 is much smaller than that of common mode type 1 and therefore the radiation problem is much less.

The voltage on the switching transistor ( fet) changes from almost zero to \( V_{input} + V_{output}/n \). This voltage swing in turn causes the charging and discharging of the fet insulator capacitance. This causes the fet insulator capacitance to appear as the source. Many other components in the power supply can cause common mode noise. A principle source of differential mode emissions is the impedance of the input ripple filter capacitor. The parasitic elements of the input filter capacitor-ESL and ESR-are of primary importance in determining differential mode emissions. Another source of differential mode emissions is the bridge diodes themselves. The reverse recovery characteristic of the diode at turn off will determine the magnitude and spectral content of the noise generated by the diode.

7.3.1 how to measure CM and DM with a current probe \[3\]

With a current probe we can measure CM and DM currents. The probe creates an output voltage, \( V_0 \) for a given input current, \( I_i \), which defines a transfer impedance, \( Z_t \), such that:

\[
Z_t = \frac{V_0}{I_i} \quad (55)
\]

When you clamp the current probe over both the phase and neutral lines as shown in fig 62a, you measure two times the common mode current. If one of the wires is reversed in direction through the probe, twice the differential mode current will be measured, see fig 62b. In both the situations, the other mode is strongly rejected, so the measurement gives you only CM or DM current!

Annex 4 page 98 and 99 shows a plot of CM noise, page 100 and 101 shows a plot of the DM currents measured of the Top-switch converter without a power supply filter. CM currents occurs at high frequencies. For lower frequencies between 9 and 150 kHz, the CM currents were hardly visible on
the spectrum analyser (see plot). With the DM current measurement setup, the noise peak at the switching frequency was clearly visible. It is often difficult to say if you are measuring CM or DM currents. If you want to do the measurements properly, you should have a 'differential mode rejection network' (which I don't have). The (DMRN) was designed and built to give the filter designer the ability to isolate these two modes. Traditionally, a current probe introduces a frequency dependent amplitude distortion of the signal. Thus, the data from the current probe cannot be directly compared to the data from the LISN measurement unless complex correction factors are used. With the DMRN, no correction factors are necessary. The DMRN effectively 'cancels out' the differential mode portion of the conducted emissions and allows direct measurement of the common mode portion of the conducted emissions.

7.4 EMI filter design [3]

Under certification testing conditions, an individual LISN measures a vector sum of the common mode and differential mode noise components. Essentially, we have one equation with two unknowns. This makes filter development a trial and error process. To have a guideline or approximation in filter design, one could try to calculate the effect of a filter on the conducted noise. You should keep in mind that this will only give you an approximation of the attenuation of the chosen filter. At high frequencies an inductor tends to change into a capacitor, and a capacitor into an inductor and therefore your filter will no longer be the same. If you want to calculate the attenuation properly, you should add all the parasitic elements of the components of the converter and the filter. This is a difficult task because many parasitic elements are unknown. The calculations given in this chapter only gives you an idea how your filter will behave and hopefully give you more insight in filter design.

7.4.1 common mode filter attenuation [3]

Fig.63 gives you the model for common mode emissions from a converter. We can replace the converter by a current source with a parallel resistance $R_1$ and a capacitor $C_1$. The filter consists of a capacitor $C$ and an inductor $L$. The LISNs impedance $Z_l$ is equal to formula nr.52.
Without the filter, the source impedance

![fig 63: conceptual schematic of resonant method](image)
is \( R_1/C_1 \). We call this impedance \( Z_t \). If we set the current \( I_s \) equal to 1A, the current through the LISN \( I_0 \), is:

\[
I_0 = \frac{Z_t}{Z_1 + Z_L} \tag{56}
\]

With the filter in place, the current through the LISN may be solved by current division between two legs: the effective source impedance and the effective output impedance. With the filter in place, the effective source impedance, \( Z_2 \) becomes \( Z_2 \) parallel with capacitor \( C \). Since the filter inductor is in series with the LISNs, the effective output impedance, \( Z_4 \) becomes \( Z_L + L \). Now the current through the LISN with the filter in place, \( I_{(0,f)} \), becomes:

\[
I_{(0,f)} = \frac{Z_2}{Z_2 + Z_3} \tag{57}
\]

With attenuation:

\[
A_{\text{dB}} = 20 \log_{10} \left( \frac{I_0}{I_{(0,f)}} \right) = 20 \log_{10} \left( \frac{Z_4}{Z_2 + Z_3} \right) \tag{58}
\]

Before we are going to calculate the attenuation for several frequencies, we must first know the common mode resistance \( R_1 \) and capacitor \( C_1 \) from the converter. You can do this by measurement by means of the method described below.

### 7.4.2 Source impedance: the resonance method

The resonance method is a way of determining the source impedance of a black box. The underlying theory is to assume that the black box is a Norton circuit with a reactive source impedance. By correct choice of the load impedances for the black box, insight into the source impedance of the black box can be obtained. If the load is a short circuit, the value of the current source is obtained. If the load is reactive and chosen to resonate with the source impedance, the \( Q \) of the source may be found at a single frequency. The \( Q \) of the circuit is defined as:

\[
Q = \frac{I_1}{I_{sc}} \tag{59}
\]

with:
- \( I_1 \) is the current when an inductive load resonates with the source impedance
- \( I_{sc} \) is the short circuit current
Other identities of $Q$ may be used to find the resistive and reactive components of the source impedance.

$$Q = \frac{R}{\omega L} \quad (60)$$

with:
- $R$ is the source resistance
- $L$ is the resonating inductor, and $C$ is the source capacitance

and:

$$Q = \omega CR \quad (61)$$

A conceptual schematic of this test setup is shown in fig 64. The currents are measured with a current probe. The general approach is as follows:

1. Measure $I_w$ at a single frequency
2. Tune the resonating inductor to resonate with the source at a single frequency.
3. Measure $I_1$ at a single frequency
4. Using eq. solve $Q = I_1/I_w$ for $Q$
5. From eq. 60, solve $R = Q \omega L$. Note that $L$ is the value of inductance required to resonate with the source. This is the value of the source resistance.
6. From eq. 61, solve $C = Q/\omega R$. This is the value of the source capacitance.

The common mode test setup is shown in fig 65. Note that the current probe is configured to measure common mode emissions. Additional rejection to differential mode emissions is obtained by the use of a 0.5 $\mu$F line-to-line capacitor. The AC short is implemented by 4$\mu$F capacitors from line to ground. The resonating inductor is the parallel combination of the inductors in each line. The bypass capacitors are retained for a low AC impedance.
path to chassis. Fig 66 shows the common mode equivalent circuit.

![Common Mode Equivalent Circuit](image)

*fig 65: common mode test circuit*

*fig 66: common mode equivalent circuit*

### 7.4.3 Common mode test results

Annex 4 page 102 gives you an example of resonance at a single frequency. Point (1) indicated in the plot is the current $I_1$ when the inductor is tuned and resonates with the source. The attenuation is 26.87 $\text{dB} \mu \text{V}$ at a frequency of 3.4 Mhz. Page 103 annex 4 gives you a plot of the short circuit current, $I_{sc}$. You can see that the attenuation is much less and equal to 6.17 $\text{dB} \mu \text{V}$. We now have the two known currents $I_1$ and $I_{sc}$ and in using those values we are able to calculate the common mode impedance $R$ and $C$, of the source. The measured value of $L_\Lambda$ and $L_B$ are the same and equal to 73 $\mu \text{H}$. Because $L=L_\Lambda/L_B$, the value of $L$ is equal to 36.5 $\mu \text{H}$.

One of the most powerful numerical analysis tools available to the engineer is 'MathCad'.
This allows you to enter an analytic expression, and the software numerically solves the expression. The calculation of the common mode impedance is also done in Mathcad. The results you can find in annex nr.5 page 112-116. The values of the measured and calculated common mode resistance and capacitor are:

\[
\begin{align*}
R_1 &= 8.5 \text{ k}\Omega \\
C_1 &= 60 \text{ pF}
\end{align*}
\]

With this information, we can calculate the attenuation of the filter. Annex 5 p 114 shows a calculated plot of the LISNs impedance and the attenuation of the chosen filter. The formula for the LISNs impedance is given by equation 53 and the attenuation of the filter by equation 58.

Annex 4 page 96 and 97 shows you the noise of the converter without a filter. The noise is far above the specified limit. The highest noise peak occurs at the switching frequency (100 kHz). Higher harmonics of the switching frequency are also visible at high frequencies. Note that Common mode EMI (CM) is proportional to the input voltage and at least to a first order approximation, independent of input current. Differential mode EMI (DM), on the other hand, is proportional to the switched current. The largest switching current occurs at minimum input voltage (±100V) and maximum output current. Because DM noise occurs at lower frequencies than CM noise, we will plot out the frequency range from 9 to 150 kHz at a low input voltage (±100V) and 150 kHz to 30 Mhz at maximum input voltage (±270 V).

For the filter, we will use an L,C combination as shown in fig 67 to reduce the noise. The attenuation is given by formula nr.58. Annex 5 page 114 and 115 gives you an calculated example of a filter with chosen values:

\[
\begin{align*}
L &= 1 \text{ mH} \\
C &= 3300 \text{ pF}
\end{align*}
\]

The calculated attenuation at 100 kHz, at the largest noise peak, is 10 db. This should be just enough to lower the noise under the specified limit. For the inductors we will use TDK sp0406, see annex p. inductors. These components are very small and look just like a resistor. This is very important because you can save a lot of space by using them.

*fig 67: common mode filter before the rectifier bridge*
The filter will be placed before the rectifier bridge, fig 67. The effect of the filter is clearly visible when you look at the EMI plot annex 4 page 104 and 105 and compare it with the plot without a filter annex 4 page 96 and 97. From the plot you can see that the achieved attenuation of the noise at 100 kHz is about 13 dB. The calculated attenuation was 10 dB, a difference of 3 dB. As I have mentioned before; the calculated values are only an approximation and a guideline. Especially for high frequencies the model will not be correct anymore because the value of the inductors and capacitors will change. A much better attenuation will be achieved if you place the filter between the two storage capacitors after the bridge, fig 68. Not only the attenuation will be better, but the capacitor will be much cheaper this way because the voltage after the bridge is a DC voltage. Annex 4 page 106 and 107 shows a plot of the attenuation of the filter when it is placed after the bridge like fig 68. You can see that the attenuation of the 100 kHz peak is at least 5 dB lower than before. We can also choose another value of L and C. Like for example a larger value of C and a smaller value of L. A smaller value of L is a better choice, because it can resist larger currents, see annex p. . The smaller the value of L, the larger the maximum permissible current through the inductor. The maximum inductor value you can choose, without causing any problems with the maximum current going through it, is L=470 μH. For the capacitor we will take a value of 0,015 μF. Annex page 4 page 108 and 109 shows a plot of the noise with filter components: L=470 μH and C=0,015 μF. The noise almost lies under the VDE specification limit. There is still a noise peak visible above the limit line at a frequency of 2.7 MHz. This peak is due to the Q factor of the filter. The effect of the Q on the filter will be explained in next paragraph.

7.5 controlling filter Q

The filter Q will also affect conducted emissions, resulting in an increase of conducted emissions at the resonant frequency. The resonance problem applies only to conducted emissions, and often the filter resonance is below the lowest specification limit frequency. For example, FCC-conducted emissions are measured from 450 kHz to 30 MHz. If a converter is running at 100 kHz with a filter resonance at 10 kHz, the increase of emissions will never be detected. If the unit is to meet VDE class B (10 kHz to 30 MHz), the
resonance can become a significant problem. The single LC (second order) filter is the basic filter for power line applications. Fig 69 shows the filter output impedance versus Q, fig 70 shows filter gain versus Q for an LC filter. It is evident that the underdamped L-C filter can cause a remarkable increase in conducted emissions as well as potential instabilities in the power supply.

The problems caused by filter Q can be reduced by adding additional damping. A shunt, or parallel, resistor may be used to damp the single section L-C filter, fig 71. A shunt resistor on the filter inductor will damp the filter resonance, but above resonance, the filter will have single order roll-off.

The gain of the chosen filter with and without a shunt resistor is calculated and plotted in annex 5 page 116. You can clearly see the effect of the damping resistor in the plots. You have to make a good compromise between gain and roll-off by choosing the value of the shuntresistor $R_s$ (usually 2 times $R_o$). When the value is too high, the effect of damping will almost have no effect, if the value is too small, the roll-off of the filter will decrease. Another possibility is to choose the resonant frequency far below the switching frequency, so that the high Q of the filter doesn't effect the noise in a negative way.

If we practise this theory on the converter, the resonant peak at 2,7 MHz will indeed disappear if we damp the inductor of $470 \mu H$ with a shunt resistor of $1k\Omega$, see plot annex 4 page 111. To be certain that the peak was caused by the Q of the filter, I replaced the...
inductor, equal to 470 μH, by two inductors of 220 μH in series. Plot anex 4 page 110 shows the result: the peak at 2.7 MHz has totally disappeared.
The noise of the converter is now below the specified limit and fulfills the VDE standards.
CHAPTER 8: CONCLUSIONS

The advantages of the switching power supplies are greater than linear power supplies. Since their frequency of operation is very much greater than the 50 Hz line frequency, the magnetic and capacitive elements used for energy storage are much smaller and the cost to build the switching supply becomes less than the linear power supply. For our application this is very important because the volume has to be smaller than 40 cm³. The efficiency of the switched mode power supply can reach up to 70 or 90 percent.

Knowing that we were going to use switched mode power supplies, we had to make a choice between the flyback and forward converter. The choice was based upon the specifications of the converter. For our application, the flyback converter turned out to be the best choice because it takes less components than the forward converter to build it. The forward converter needs a large coil in the output in order to stay in continuous mode at minimum output load. This coil is large and expensive.

The measured waveforms like drainvoltage, output voltage etc. differs a lot from the theoretically ones. Not everything is as beautifull as it seems in theory. There are several things that can influence the current and voltage waveforms like:

- **leakage inductances of the transformer**: this inductance can oscillate with other parasitic capacitors within the output or input circuit and can give rise to oscillations within the converter. Those oscillations can be very annoying because then it can cause the drainvoltage to go up to 600 or 700 V and creates noise within the converter. The noise can be attenuated with a common mode filter.

- The output voltage is not a steady DC value. The ripple on the input storage capacitors can cause a 50 Hz ripple at the output. The storage capacitors have to be large enough to keep the ripple within specifications.

The voltage drop due to the output current and ESR (Equivalent Series Resistance) of the output capacitor can cause a ripple in the output voltage. The frequency of the ripple is equal to the switching frequency. You can reduce this ripple by adding a filter in the output. This is a disadvantage because the output filter can be rather expensive.

Furthermore we have to deal with the noise level. The largest noise within a converter is caused by conduction and can be measured by means of a LISN (Line Impedance Simulation Network). There are two types of noise: common mode and differential mode.
noise. The noise in the converter can be reduced with a common mode filter. The Q factor of the filter can also affect conducted emissions, resulting in an increase of conducted emissions at the resonant frequency. You can prevent this by choosing the resonant frequency of the filter far below the switching frequency or by damping the filter with a shunt resistor. The disadvantage of the shunt resistor is that above the resonant frequency the filter will have a single order roll-off.

After investigation it seemed that two 'new' Ic's were suitable for application in the converter: The Motorola MC44603 and the Power Integration Topswitch. The feedback function from the Motorola IC was, for our application, not suitable because firstly it depends too much upon the input voltage and secondly it was not possible to create a 'square' V-I characteristic (see page 4 fig.2) as required. We have chosen the Topswitch IC for our application. All the basic functions are included in this IC.

Good regulation was made possible via the secondary winding. If the regulation was done via the primary winding, the accuracy of the secondary output voltage was not within the specifications (5%). The reason for this was that the situation on the primary and secondary winding were not the same: the load variation on the secondary winding was variable, which caused a variable voltage drop over the input impedances of the secondary winding, the load variation on the primary winding was constant. If you regulate via the primary winding the coupling factor between the secondary and primary winding has to be very good in order to keep the secondary voltage within the specification. A 10% accuracy is possible with primary regulation.

A disadvantage is that all the extra functions, like foldback and overvoltage protection, are not included in the Topswitch, so you have to add extra components to make them. Because extra components are added to the circuit the efficiency reduces. All the extra components make the Topswitch less attractive. For a converter with only basic functions the Topswitch is very interesting and very compact, if you wish to create other functions you have to add more components to the circuit which enlarges the volume of the converter.
TABLE OF CONTENTS

Annex 1: efficiency graphs
Annex 2: circuit designs
Annex 3: trafo design files
Annex 4: EMI plots
Annex 5: calculated example of filter attenuation
ANNEX 1: efficiency graphs
efficiency Motorola MC44603

input power (W)

efficiency (%)
annex 1: efficiency converter with Topswitch IC via opto-coupler and shunt regulator

efficiency (%) vs. input power (W)

- V1 = 85V
- V1 = 220V
- V1 = 265V

efficiency converter with opto-coupler and shunt regulator
Diagram showing the efficiency of a Topswitch IC with voltage and current feedback. The horizontal axis represents input power (W), and the vertical axis represents efficiency (%). The graph compares the efficiency at 220V, 120V, and 265V input voltage levels.
ANNEX 2: circuit designs
TOPSwitch POWER SUPPLY
PRIMARY FEEDBACK

annex 2: converter circuit diagram with Topswitch IC and primary feedback
TOPSwitch POWER SUPPLY
SIMPLE OPTO FEEDBACK

annex 2: converter circuit diagram with Topswitch IC and opto feedback

- EMI FILTER
- BR1
- C1 33 µF
- R1 20 kΩ
- C2 4.7 nF
- BYV26D
- D1
- D2 MBR1060
- C3 680 µF
- D3 1N4148
- C4 0.1 µF
- T1
- U1 PWR-TOP202YAI
- U2 MOC8101
- R2 47 Ω
- VR1 1N4733A
- C5 0.1 µF
- R3 6.2 Ω
- C6 47 µF

7.5 V

RTN
annex 2: converter with Topswitch IC, without foldback and overvoltage protection
annex 2. converter with Topswitch IC, with foldback and overvoltage protection
ANNEX 3: trafo design files
annex 3: trafo file for converter with Motorola MC44603 IC

Worked on File: WOUTER1.TRA

Date: 25.05.1994
Time: 15:19:25

Comment:

Electrical Data:

Worst Case:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Nominal Case:</th>
</tr>
</thead>
<tbody>
<tr>
<td>$U_{prim,min}$</td>
<td>90.00</td>
<td>$U_{prim,nom}$: 385/00</td>
</tr>
<tr>
<td>$f_{prim}$</td>
<td>63.00</td>
<td></td>
</tr>
<tr>
<td>$D_{prim,max}$</td>
<td>0.45</td>
<td>$D_{prim,nom}$: 0.08</td>
</tr>
<tr>
<td>$B_{max}$</td>
<td>312.00</td>
<td>$B_{nom}$: 391.56</td>
</tr>
<tr>
<td>$I_{p,max}$</td>
<td>0.37</td>
<td>$I_{p,nom}$: 0.47</td>
</tr>
</tbody>
</table>

Nominal Case:

<table>
<thead>
<tr>
<th>Electrical Data:</th>
</tr>
</thead>
<tbody>
<tr>
<td>$U_{prim,nom}$</td>
</tr>
<tr>
<td>$D_{prim,nom}$</td>
</tr>
<tr>
<td>$B_{nom}$</td>
</tr>
<tr>
<td>$I_{p,nom}$</td>
</tr>
</tbody>
</table>

max. throughput Power: [W] 7.54

Winding-Data:

<table>
<thead>
<tr>
<th>Wdg</th>
<th>Imax [A]</th>
<th>Inom [A]</th>
<th>U [V]</th>
<th>No of req is</th>
<th>Turns Lay.</th>
<th>No of B</th>
<th>Conductor</th>
<th>Rdc</th>
<th>Fr</th>
<th>P wdg</th>
<th>Ipeak</th>
<th>Inom</th>
<th>dT</th>
</tr>
</thead>
<tbody>
<tr>
<td>MAIN</td>
<td>0.08</td>
<td>0.02</td>
<td>0.00</td>
<td>0/00</td>
<td>40.7</td>
<td>1.0</td>
<td>14 0.140</td>
<td>1</td>
<td>CUL</td>
<td>1.186</td>
<td>1.0</td>
<td>0.01</td>
<td>0.37</td>
</tr>
<tr>
<td></td>
<td>0.10</td>
<td>0.10</td>
<td>13.00</td>
<td>13.00</td>
<td>11.8</td>
<td>1.0</td>
<td>14 0.140</td>
<td>1</td>
<td>CUL</td>
<td>0.356</td>
<td>1.0</td>
<td>0.01</td>
<td>0.44</td>
</tr>
<tr>
<td></td>
<td>0.78</td>
<td>0.78</td>
<td>8.00</td>
<td>8.00</td>
<td>7.2</td>
<td>1.0</td>
<td>72 0.300</td>
<td>1</td>
<td>CUL</td>
<td>0.053</td>
<td>1.0</td>
<td>0.12</td>
<td>3.47</td>
</tr>
<tr>
<td></td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
<td>40.7</td>
<td>1.0</td>
<td>14 0.140</td>
<td>1</td>
<td>CUL</td>
<td>1.481</td>
<td>1.0</td>
<td>0.01</td>
<td>0.00</td>
</tr>
</tbody>
</table>

90
Nominal load case:

The following losses are to be expected:

Losses induced by airgap io foil-wdgs. \( P_{eddyc} \) [W] 0.00
by screens \( P_{screen} \) [W] 0.00
by \( L_s \) \( P_{Ls} \) [W] 0.01
by \( I^2acR_{ac} + I^2dcR_{dc} \) \( P_{I^2R} \) [W] 0.15
in ferrite core \( P_{core} \) [W] 0.23

Total losses [W] 0.39

For a surrounding temperature of : \( T_a \) [°C] 23.0
a temperature-rise of maximal \( T_d \) [°C] 0.0

can be expected.

the core will have a max \( T_d \) of : [°C] 0.0
and a min \( T_d \) of : [°C] 0.0

the coilformer will have a max \( T_d \) of : [°C] 0.0
and a min \( T_d \) of : [°C] 0.0

Mechanical Data:

Core Data:
Core-type used : E13/7/7
Core-material : 3C8
total airgap : [mm] 0.121

Coil Data:
Coil-geometrie used : E13/7
Coil-orientation : horizontal
with a winding width of : [mm] 6.80
with a winding height of : [mm] 1.47
actual/max winding height : [%] 79.80

Total weight of conductor [g] 0.50
Total weight of isolation [g] 0.00
annex 3: trafo file for converter with Topswitch IC

Worked on File: WOUTER1.TRA
Date: 20.09.1994
Time: 10:46:07

Comment:

Electrical Data:

Worst Case:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Uprim,min [V]</td>
<td>94.00</td>
</tr>
<tr>
<td>Dprim,max [A]</td>
<td>0.50</td>
</tr>
<tr>
<td>Dsek,max [mA]</td>
<td>0.50</td>
</tr>
<tr>
<td>Freq. min [kHz]</td>
<td>100.00</td>
</tr>
<tr>
<td>Bmax [mT]</td>
<td>305.00</td>
</tr>
<tr>
<td>Ip,max [A]</td>
<td>0.26</td>
</tr>
<tr>
<td>Urev [V]</td>
<td>94.00</td>
</tr>
<tr>
<td>L [mH]</td>
<td>1.793</td>
</tr>
<tr>
<td>Ls [µH]</td>
<td>0.448</td>
</tr>
<tr>
<td>L [mH]</td>
<td>0.448</td>
</tr>
<tr>
<td>Bnom [mT]</td>
<td>305.00</td>
</tr>
<tr>
<td>Ip,nom [A]</td>
<td>0.26</td>
</tr>
</tbody>
</table>

Nominal Case:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Uprim,nom [V]</td>
<td>380.00</td>
</tr>
<tr>
<td>Dprim,nom [A]</td>
<td>0.12</td>
</tr>
<tr>
<td>Dsek,nom [mA]</td>
<td>0.50</td>
</tr>
<tr>
<td>Freq. nom [kHz]</td>
<td>100.00</td>
</tr>
<tr>
<td>Bnom [mT]</td>
<td>305.00</td>
</tr>
<tr>
<td>Ip,nom [A]</td>
<td>0.26</td>
</tr>
</tbody>
</table>

Max. throughput Power: [W] 6.16

nominal throughput Power: [W] 6.16

Winding-Data

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>MAIN</td>
<td>0.07</td>
<td>0.02</td>
<td>0.00</td>
<td>0.00</td>
<td>30.5</td>
<td>1.0</td>
<td>14</td>
<td>0.140</td>
<td>1</td>
<td>CUL</td>
<td>1.10</td>
<td>1.0</td>
<td>0.00</td>
</tr>
<tr>
<td>2</td>
<td>PRIM</td>
<td>0.10</td>
<td>0.07</td>
<td>7.70</td>
<td>7.70</td>
<td>5.0</td>
<td>1.0</td>
<td>14</td>
<td>0.140</td>
<td>1</td>
<td>CUL</td>
<td>0.19</td>
<td>1.0</td>
<td>0.01</td>
</tr>
<tr>
<td>3</td>
<td>SEC</td>
<td>0.70</td>
<td>0.70</td>
<td>7.70</td>
<td>7.70</td>
<td>5.0</td>
<td>1.0</td>
<td>73</td>
<td>0.400</td>
<td>1</td>
<td>CUL</td>
<td>0.03</td>
<td>1.0</td>
<td>0.04</td>
</tr>
<tr>
<td>4</td>
<td>MAIN</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
<td>30.5</td>
<td>1.0</td>
<td>14</td>
<td>0.140</td>
<td>1</td>
<td>CUL</td>
<td>1.29</td>
<td>1.0</td>
<td>0.01</td>
</tr>
</tbody>
</table>
Nominal load case:

The following losses are to be expected:

<table>
<thead>
<tr>
<th>Losses induced by</th>
<th>Power</th>
<th>[W]</th>
</tr>
</thead>
<tbody>
<tr>
<td>airgap in ferrite</td>
<td>P eddy</td>
<td>0.00</td>
</tr>
<tr>
<td>by screens</td>
<td>P screen</td>
<td>0.00</td>
</tr>
<tr>
<td>by Ls</td>
<td>P Ls</td>
<td>0.01</td>
</tr>
<tr>
<td>by $I^2acRac + I^2dcRdc$</td>
<td>P $I^2R$</td>
<td>0.05</td>
</tr>
<tr>
<td>in ferrite core</td>
<td>P core</td>
<td>0.38</td>
</tr>
</tbody>
</table>

Total losses [W] 0.43

For a surrounding temperature of: $T_a$ [°C] 60.0
a temperature-rise of maximal $dT$ [°C] 35.2
can be expected.

the core will have a max $dT$ of: [°C] 34.6
and a min $dT$ of: [°C] 33.4

the coilformer will have a max $dT$ of: [°C] 34.8
and a min $dT$ of: [°C] 32.4

Mechanical Data:

Core Data:
Core-type used: E13/7/7
Core-material: 3C8
total airgap: [mm] 0.055

Coil Data:
Coil-geometrie used: E13/7
Coil-orientation: horizontal
with a winding width of: [mm] 6.80
with a winding height of: [mm] 1.47
actual/max winding height: [%] 86.58

Total weight of conductor [g] 0.43
Total weight of isolation [g] 0.00
ANNEX 4: EMI-plots
annex 4: LISN impedance versus frequency

MODEL 3825/2 S/N 1993 L2
A: |Z|   B: θ
A MAX 100.0 Ω
B MAX 180.0 deg

A MIN 0.000 Ω   START 10 000 000 000 000 Hz
B MIN -180.0 deg   STOP 10 000 000 000 000 Hz
annex 4: noise of the converter without filter between 9 and 150 kHz
annex 4: noise of the converter without filter between 150 kHz and 30 MHz
annex 4: common mode noise without filter between 9 and 150 kHz
annex 1: common mode noise without filter between 150 kHz and 30 MHz
annex 4: differential mode noise without filter between 9 and 150 kHz
annex 4: differential mode noise without filter between 150 kHz and 30 MHz
annex 4: measurement for common mode input impedance when an inductive load resonates with the source impedance
annex 4: measurement for common mode input impedance at short circuit current
annex 4: noise measurement at low frequencies with common mode filter

\[C = 3300 \, \text{pF}, \ L = 1 \, \text{mH}, \ V = 110 \, \text{VAC}, \ I_0 = 600 \, \text{mA}\]
annex 4: noise measurement at high frequencies with common mode filter
C=3300 pF, L= 1mH, V=250 VAC, Io=600 mA
annex 4: noise measurement at low frequencies with common mode filter after the bridge $C=3300 \, \text{pF}, \, L=1\, \text{mH}, \, V=250 \, \text{VAC}, \, I_0=600 \, \text{mA}$
annex 4: noise measurement at high frequencies with common mode filter after the bridge \(C=3300 \text{ pF}, L=1 \text{ mH}, V=250 \text{ VAC}, I_0=600 \text{ mA}\)
annex 4: noise measurement at low frequencies with common mode filter after the bridge  
C=0.015 μF, L= 470 μH, V=110 VAC, I₀=600 mA
annex 4: noise measurement at high frequencies with common mode filter after the bridge  $C=0.015\mu F$, $L=470\,\mu H$, $V=250\,VAC$, $I_o=600\,mA$
annex 4: noise measurement at high frequencies with common mode filter after the bridge $C=0.015\mu F$, $L=2\times2.0\mu H$, $V=250$ VAC, $I_0=600mA$
annex 4: noise measurement at high frequencies with shunt resistor $R_s=1\,\text{k}\Omega$
ANNEX 5: calculated example of filter attenuation
1) Determination of the common mode input impedance:

V1 is the measured voltage when an inductive load resonates with the source impedance and Vsc is the measured voltage when the load is a short circuit.

\[ f = 3.43 \cdot 10^6 \text{ Hz} \]

\[ L_A = 73 \cdot 10^{-6} \text{ H} \quad L_B = 73 \cdot 10^{-6} \text{ H} \]

\[ L = \frac{L_A \cdot L_B}{L_A + L_B} = 3.65 \cdot 10^{-5} \text{ H} \]

\[ V_{\text{1dBuV}} = 26.87 \quad V_{\text{1uV}} = 10^{\frac{V_{\text{1dBuV}}}{20}} \quad V_{\text{1uV}} = 22.055 \]

\[ V_{\text{scdBuV}} = 6.17 \quad V_{\text{scuV}} = 10^{\frac{V_{\text{scdBuV}}}{20}} \quad V_{\text{scuV}} = 2.035 \]

With a ferrite-core of 10 ohm:

\[ I_1 = \frac{V_{\text{1uV}}}{10} = 2.205 \]

\[ I_{\text{sc}} = \frac{V_{\text{scuV}}}{10} = 0.203 \]

With the quality factor \( Q \), we can calculate the resistance and capacitance as follows:

\[ Q = \frac{I_1}{I_{\text{sc}}} = 10.839 \]

\[ R_1 = 2 \pi f Q L \quad R_1 = 8.526 \cdot 10^3 \]

\[ C_1 = \frac{Q}{2 \pi f R_1} \quad C_1 = 5.899 \cdot 10^{-11} \]

2) Determination of the filter attenuation on the converter

Specify your frequency range:

\[ f = 10^{-3}, 20 \cdot 10^{-3}, 1 \cdot 10^6 \]

ZL calculates the LISN impedance as function of frequency:

\[ Z_L(f) = \frac{2 \pi f}{(2 \pi f)^2 \cdot 50 \cdot 10^{-6} \cdot 0.22 \cdot 10^{-6} + 2 \pi f \cdot 50 \cdot 10^{-6} + 1} \]
annex 5: filter attenuation

Specify your filter inductor=L and capacitor=C

\[ L = 1 \times 10^{-3} \]
\[ C = 3300 \times 10^{-12} \]

Z1 is the parallel input impedance of the converter, R1 parallel with C1 (without the filter)

\[ Z_1(f) = \left| \frac{R_1}{1 + 2\pi f R_1 C_1 i} \right| \]

Z2 is the common mode source impedance parallel with the filter capacitor C:

\[ Z_2(f) = \left| \frac{R_1}{1 + 2\pi f R_1 (C + C_1) i} \right| \]

Z3 is the filter inductor L in series with the lisn impedance

\[ Z_3(f) = \left| 2\pi f L + \frac{Z_1(f)}{2} \right| \]

A calculates the effect of the filter attenuation:

\[ A(f) = 20 \log \frac{Z_1(f)}{Z_1(f) + Z_3(f)} \]
annex 5: filter attenuation

Output impedance of the chosen filter, $Z_{\text{out}}(f)$:

$$Z_{\text{out}}(f) = 20 \log \left| \frac{\frac{2 \pi f L_i}{1 - (2 \pi f)^2 L C}}{1} \right|$$

Gain of the chosen filter $G(f)$:

$$G_1(f) = 20 \log \left| \frac{1}{1 - (2 \pi f)^2 L C} \right|$$
If your gain at resonance is too high, you can damp the filter with a series resistor $R$:

The damping resistor should be roughly the value of the characteristic impedance of the filter $R_0$:

$$R_0 = \frac{L}{\sqrt{LC}}$$

$$R_0 = 550.482$$

$$R_s = 2R_0$$

$$R_s = 1.101 \times 10^3$$

The filter output impedance is now equal to:

$$Z_{out2}(f) = 20 \log \left[ \frac{2 \pi f L i}{1 + \frac{L}{R_s} \cdot 2 \pi f i - (2 \pi f)^2 L C} \right]$$

The gain of the filter (with damping resistor):

$$G_2(f) = 20 \log \left[ \frac{1 + \frac{L}{R_s} \cdot 2 \pi f i}{1 + \frac{L}{R_s} \cdot 2 \pi f i - (2 \pi f)^2 L C} \right]$$
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