On-chip fully-digital power supply control
a design technology for System-on-Chip applications

Meijer, R.I.M.P.

Award date:
2004
ON-CHIP FULLY-DIGITAL POWER SUPPLY CONTROL.

A design technology for System-on-a-Chip applications.

R.I.M.P. Meijer

Supervisor: prof.dr.ir. R.H.J.M. Otten
Coach: dr. J. Pineda de Gyvez (Philips Research Laboratories)
Date: August 2004
Abstract

New deep sub-micrometer technologies enable a higher integration density that drives single chip solutions. The failure of these technologies to continue with constant process tolerances gives origin to significant challenges for design technologies in terms of power and performance. As the variation of fundamental parameters such as channel length, threshold voltage, thin gate oxide thickness and interconnect dimensions goes well beyond acceptable limits, innovative circuits and systems are needed. Next to that, power efficiency has become a major concern. For instance, high-performance applications, a scaled technology provides higher operating frequencies and a higher level of integration as long as the power constraints of package and cooling parts are not exceeded. Furthermore, the power requirements for portable applications are even more stringent, because battery life depends on energy consumption. Despite advances in battery technology, which have increased battery energy density, the demand for low-cost and small form-factor devices has kept the available energy supply roughly constant by driving down battery size. Design with power-in-mind will be important to further progress in ultra large-scale integration (ULSI) designs.

For a given process technology, adaptive control of the circuit’s power supply voltage can result in a significant reduction in terms of power and energy. This technique is also capable of tracking variations in process parameters and temperature drifts. Several schemes have been proposed in the literature archival, which use either off-chip components to perform DC/DC conversion or use integrated analog solutions. In this work, a fully-integrated fully-digital solution is pursued that is applicable to island-based system-on-chip designs.

This report presents a scheme for adaptive control of the circuit’s power supply voltage. The scheme consists of two independent negative feedback control loops and an on-chip linear device to perform voltage conversion. Feedback control theory was applied to prove loop stability. Analytical models were developed for power and energy consumption, power conversion efficiency and transient response. The individual components of the scheme have been implemented on circuit schematic level in a 0.13μm CMOS technology. An area estimation has been performed and simulation results have been provided.
Contents

Glossary ............................................................................................................................. 9

Acknowledgements ............................................................................................................. 10

1 Introduction ....................................................................................................................... 11
  1.1 Problem description .................................................................................................... 11
  1.2 Organisation .............................................................................................................. 11

2 Power-awareness in digital CMOS circuits ........................................................................ 13
  2.1 CMOS circuit models ............................................................................................... 13
    2.1.1 Power consumption ............................................................................................ 13
    2.1.2 Circuit delay ....................................................................................................... 14
    2.1.3 Energy per operation ......................................................................................... 15
  2.2 The impact of technology scaling .............................................................................. 15
  2.3 Trade-offs involved in low-power designs ................................................................. 17

3 Power supply voltage scaling ............................................................................................ 18
  3.1 Voltage scaling effects .............................................................................................. 18
  3.2 Circuit delay scaling of CMOS gates ......................................................................... 19
  3.3 Prior art in voltage scaling techniques .................................................................... 21
    3.3.1 Static supply scaling ........................................................................................ 21
    3.3.2 Dynamic supply scaling .................................................................................. 21

4 The proposed scheme ....................................................................................................... 24
  4.1 System perspective .................................................................................................... 24
  4.2 Proposed system architecture ................................................................................... 25
  4.3 Proposed power supply actuator .............................................................................. 27
  4.4 Performance models .................................................................................................. 28
    4.4.1 Power consumption ......................................................................................... 28
    4.4.2 Energy per operation ....................................................................................... 30
    4.4.3 Conversion efficiency ...................................................................................... 30
    4.4.4 Transition time ............................................................................................... 30
    4.4.5 Application to a CMOS circuit ...................................................................... 31

5 μ-supply control ................................................................................................................. 35

© Koninklijke Philips Electronics N.V. 2004
References ........................................................................................................66

A  Flow diagrams of the μ-supply sensor .......................................................69

B  Flow diagrams of the μ-supply controller ..................................................71
## Glossary

<table>
<thead>
<tr>
<th>Abbr.</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>ASIC</td>
<td>Application Specific Integrated Circuit</td>
</tr>
<tr>
<td>CAD</td>
<td>Computer Aided Design</td>
</tr>
<tr>
<td>CGU</td>
<td>Clock Generation Unit</td>
</tr>
<tr>
<td>CPU</td>
<td>Central Processing Unit</td>
</tr>
<tr>
<td>CMOS</td>
<td>Complementary Metal Oxide Semiconductor</td>
</tr>
<tr>
<td>DC</td>
<td>Direct Current</td>
</tr>
<tr>
<td>DLL</td>
<td>Delay Locked Loop</td>
</tr>
<tr>
<td>GALS</td>
<td>Globally Asynchronous Locally Synchronous</td>
</tr>
<tr>
<td>I/O</td>
<td>Input Output</td>
</tr>
<tr>
<td>IC</td>
<td>Integrated Circuit</td>
</tr>
<tr>
<td>IP</td>
<td>Intellectual Property</td>
</tr>
<tr>
<td>LUT</td>
<td>Look-up Table</td>
</tr>
<tr>
<td>MOS</td>
<td>Metal Oxide Semiconductor</td>
</tr>
<tr>
<td>NMOS</td>
<td>n-channel MOS</td>
</tr>
<tr>
<td>PDP</td>
<td>Power Delay Product</td>
</tr>
<tr>
<td>PMU</td>
<td>Power Management Unit</td>
</tr>
<tr>
<td>PMOS</td>
<td>p-channel MOS</td>
</tr>
<tr>
<td>PWL</td>
<td>Piece Wise Linear</td>
</tr>
<tr>
<td>SoC</td>
<td>System on Chip</td>
</tr>
<tr>
<td>SRAM</td>
<td>Static Random Access Memory</td>
</tr>
<tr>
<td>TUBE</td>
<td>Tuning for Best Execution</td>
</tr>
<tr>
<td>ULSI</td>
<td>Ultra Large Scale Integration</td>
</tr>
<tr>
<td>VCO</td>
<td>Voltage Controlled Oscillator</td>
</tr>
<tr>
<td>VHDL</td>
<td>VHSIC Hardware Description Language</td>
</tr>
<tr>
<td>VHSIC</td>
<td>Very High Speed Integrated Circuit</td>
</tr>
</tbody>
</table>
Acknowledgements

This report is the result of my graduation project as has been performed in the group Digital Design and Test of Philips Research Eindhoven.

First and foremost I would like to thank dr. J. Pineda de Gyvez of Philips Research Eindhoven for his insight, guidance and encouragement through the course of the project. The many discussions we had were always a source of inspiration. I also would like to thank prof. dr. ir. R.H.J.M. Otten of the Eindhoven University of Technology for supervising my graduation project. Furthermore, I would like to thank my colleague mw. Rohini Krishnan, M.Tech. for the fruitful discussions on the topic of loop stability and for reviewing this report. I also acknowledge prof. dr. J. Rius Vazquez’s insight in performance modelling. Finally, I would like to thank all colleagues who supported me with my graduation.

Maurice Meijer,

Eindhoven, August 2004
1 Introduction

The research carried out in the group Digital Design and Test of Philips Research Eindhoven aims to enable the integration of ULSI designs in state-of-the-art and future CMOS technologies. The project TUBE (Tuning for Best Execution) aims at developing and enabling an IC design technology capable of reaching a prescribed IP electrical performance within process and manufacturability constraints. The graduation project described in this report is performed as part of the TUBE project.

1.1 Problem description

The failure of deep sub-micrometer technologies to continue with constant process tolerances gives origin to significant challenges for design technologies in terms of power and performance. As the variation of fundamental parameters such as channel length, threshold voltage, thin gate oxide thickness and interconnect dimensions goes well beyond acceptable limits, innovative circuits and systems are needed. The performance of a SoC implemented in sub-100nm technologies may severely be hampered by excessive transistor leakage, by the impact of local and global process variability, and by reduced noise margins. Focus lies on schemes to improve the overall system performance in terms of manufacturability, robustness, power-delay product, and on the development and IP integration of new logic families conforming to new design technologies.

The objective of the TUBE project is to adapt a chip, e.g. an isolated IP or a SoC, so that a certain level of performance is guaranteed in terms of both speed and power in a (sub) optimal way. This can be achieved by modifying the chip's operating conditions. The adaptive behaviour is not on a global basis, but it is achieved with locality. A SoC using TUBE technology is partitioned into islands. Islands are a set of IPs or modules that have common electrical and activity characteristics. A distinction is made between computation and interface islands. Computation islands are electrically independent, e.g. each island has a distinct power supply voltage $V_{DD}$, threshold voltages $V_{th}$, and operating frequency $f_{CK}$. The clock generation is performed within each computational island. Interface islands are aware of the distinct electrical characteristics of the various islands. The described partitioning of the system allows optimising the IC locally to achieve best performance within process and manufacturability constraints.

The question to be addressed in this graduation project is how to perform on-chip fully-digital power supply control for each computational island with each island having its own (varying) performance requirements.

1.2 Organisation

Chapter 2 gives background information on the importance of power awareness in digital CMOS circuits. In this chapter, simple CMOS circuit models will be presented that provide insight into which circuit parameters are important to control power. Next, the impact of technology scaling and trade-offs in low-power designs is addressed. Chapter 3 focuses on the effects introduced by scaling of the power supply voltage for a given process technology. Its impact on several digital CMOS gates is presented and a short overview of the prior art is given.

Chapter 4 introduces the proposed scheme for adaptive control of the power supply voltage. A general overview of the proposed scheme is given. Our solution contains two independent negative feedback control loops. Simple analytical models are introduced for calculating a number of
important parameters when using the proposed scheme. Chapters 5 and 6 describe the details of both feedback control loops. The circuit implementation and simulation results are presented in chapter 7. Finally, chapter 8 presents the conclusions.
2 Power-awareness in digital CMOS circuits

While CMOS technology has been scaling towards smaller feature sizes, the performance of digital systems has been increasing exponentially due to increased clock frequencies ($f$) and higher level of integration. Unfortunately, power consumption of digital systems has also increased, and has become the primary concern. Modern high-performance microprocessors may consume up to 100W [10][17], and require expensive package and complex cooling solutions. For those applications, the performance increase obtained from a scaled technology may be limited by power constraints on the package and cooling requirements. Power requirements for portable applications are even more stringent because battery life depends on energy consumption. Despite advances in battery technology, which have increased battery energy density, the demand for low-cost and small form-factor devices has kept the available energy supply roughly constant by driving down battery size. Design with power-in-mind will be important to further progress in ultra large-scale integration (ULSI) designs.

This chapter starts by introducing simple models of power consumption, circuit delay and energy consumption applicable to digital CMOS circuits. Next, the impact of technology scaling on these parameters is discussed. The chapter will be concluded with the trade-offs involved for low-power circuit designs.

2.1 CMOS circuit models

2.1.1 Power consumption

In general, there are four main sources of power consumption for CMOS circuit designs: (i) dynamic switching power due to charging and discharging of the circuit capacitances, (ii) short-circuit dissipation due to the finite signal rise and fall times, (iii) leakage power due to currents from pn-junction diodes, subthreshold currents and gate-oxide tunnelling currents, and (iv) static biasing power found in other types of logic styles. For most CMOS applications, the dynamic switching power dominates the total power consumption. However, with the increasing integration density, the decreasing gate-oxide thicknesses and threshold voltages of the transistors, leakage power is becoming more and more important. Reducing leakage to the lowest value possible is important because it constrains the power consumption when the circuit is idle or in a standby mode, i.e. there is no dynamic switching power. The short-circuit dissipation only occurs during switching, and its contribution to the total power is relatively small for a properly designed circuit [22]. Therefore, the short-circuit dissipation will be ignored for the remainder of this report. The dynamic switching power of synchronous digital CMOS circuits can be expressed as:

$$ P_{\text{dyn}} = a \cdot C \cdot V_{DD}^2 \cdot f_{CK} $$

(1)

where $a$ is the average switching activity of the circuit, $C$ is the total circuit capacitance, $V_{DD}$ is the power supply voltage, and $f_{CK}$ is the frequency of operation.

The leakage power contains contributions of the following components for every logic gate in the circuit: (i) the junction diode leakage, (ii) the subthreshold leakage, and (iii) leakage caused by gate-oxide tunnelling currents [19]. For modern technologies, however, the major components are due to subthreshold conduction and gate-oxide leakage. The junction diode leakage may be significant for those cases where no nominal well bias voltage is applied. The leakage power
consumption can is given by:

\[
P_{\text{leak}} \approx \sum_i \left( V_{bs} |I_i| + V_{DD} |I_{\text{sub}}| + V_{DD} |I_{\text{gate}}| \right)
\]  

(2)

where \( V_{bs} \) is the voltage applied between body and source of a transistor, \( I_i \) is the junction leakage current, \( I_{\text{sub}} \) is the subthreshold leakage current, and \( I_{\text{gate}} \) is the gate-oxide leakage current. The index \( i \) runs over all logic gates in the circuit. The subthreshold leakage current is proportional to \( e^{-V_{th}/nU} \), where \( V_{th} \) is the threshold voltage of the transistor, \( U \) is the thermal voltage, and \( n \) is a constant close to 1. The gate oxide leakage current depends on the gate oxide thickness \( t_{OX} \) of the transistor, its relative permeability \( \varepsilon_r \), and the voltage across the gate dielectric.

As a first-order approximation, the total power consumption of synchronous digital CMOS circuits can be expressed as:

\[
\text{Power} = a \cdot C \cdot V_{DD}^2 \cdot f_{CK} + V_{DD} \cdot I_{\text{leak}} + |V_{bs}| \cdot I_j
\]

(3)

where \( I_{\text{leak}} \) is the off-state current of the circuit due to subthreshold and gate-oxide leakage. Typically \( I_{\text{leak}} \gg I_j \), therefore the contributions of \( I_j \) will be neglected in the remainder of this report.

To reduce power consumption it is necessary to reduce one or more of \( a, C, V_{DD}, f_{CK}, \) or \( I_{\text{leak}} \). The largest power savings may be obtained from \( V_{DD} \) reduction due to its quadratic relation with dynamic switching power, and its linear relation to leakage power as can be observed in (3).

### 2.1.2 Circuit delay

The delay of digital CMOS circuits depends on four main parameters: (i) process, (ii) temperature, (iii) supply voltage, and (iv) capacitive loading. Process parameter variations result in chips that exhibit a spread of performance due to variations in device thresholds, oxide thicknesses, doping profiles, etc. Operating conditions also affect performance. Temperature affects the mobility of holes and electrons, and also the transistor's threshold voltage. Lastly, circuit delay strongly depends on supply voltage as well on the size of the capacitive load.

Typically, digital circuits are driven at their maximum possible operating frequency. The maximum operating frequency can be approximated by the following expression [20]:

\[
f_{\text{max}} = \frac{K_f}{L_G} \cdot \frac{(V_{DD} - V_{th})^\alpha}{V_{DD}}
\]

(4)

where \( K_f \) is a constant for a given process technology and circuit design, \( L_G \) is the logic depth of the critical path, \( V_{DD} \) is the power supply voltage, \( V_{th} \) is the transistor threshold voltage and \( \alpha \) is a circuit parameter that models velocity saturation. For low electric fields, \( \alpha \) is around 2, but for modern IC technologies \( \alpha \) can be as low as 1.28 (0.13μm CMOS).

This maximum operating frequency is just the inverse of the critical path delay, which is proportional to the delay of a single CMOS gate. The delay of a single static CMOS gate can be approximated by using (4):
where \( C_{\text{load}} \) is the load of the gate, and \( \beta(V_{DD} - V_{th})^\alpha \) models the device current.

Lowering \( V_{DD} \) offers significant power savings as has been found in section 2.1.1. However, from (5) it can be observed that the circuit delay increases with decreasing \( V_{DD} \), which may lower the chip’s operating frequency, and thus, degrade circuit performance. So there exists a trade-off between circuit performance and power consumption.

### 2.1.3 Energy per operation

For portable applications, an interesting parameter to consider is energy consumption due to its relation to battery life. Power consumption is the rate of change of energy. A common measure of energy consumption is the power-delay product (PDP)[3]. In this figure of merit, the delay is often related to the critical path delay, which gives the energy per clock cycle.

An interesting figure of merit is the energy per operation [3], which can be found by multiplying the PDP by the number of clock cycles it takes to complete the operation. This results in the following expression:

\[
\frac{\text{Energy}}{\text{operation}} = \left( a \cdot C \cdot V_{DD}^2 + V_{DD} \cdot I_{\text{leak}} \cdot T_{CK} \right) \cdot N
\]  

(6)

where \( N \) represents the number of clock cycles to complete an operation and \( T_{CK} \) is the clock period. In (6), the first term represents the energy per operation consumed by the active circuit parts and the second term is the energy per operation consumed due to off-state leakage.

A common fallacy is that reducing operating frequency \( f_{CK} \), thus increasing \( T_{CK} \), is energy efficient. In this case, the energy per operation increases due to off-state leakage as shown in (6). Reducing \( V_{DD} \), however, is energy-efficient but this is at the expense of increasing circuit delay as shown in (5).

### 2.2 The impact of technology scaling

The ongoing miniaturization of the integrated circuit feature sizes has a significant impact on the chip’s size, performance, and power consumption. In the constant-field scaling scenario, the dimensions of the on-chip devices are scaled by a factor \( S \), where \( S \approx 0.7 \) for consecutive migration between technology nodes. When a chip is transitioned to a new-scaled technology, both \( C \) (\( \sim S \)) and \( V_{DD} \) (\( \sim S \)) are reduced for this chip. The gate delays are improved (\( \sim 1/S \)) such that the scaled chip can operate at higher frequencies. As a result, the chip may run at an increased operating frequency as well as at a reduced dynamic power consumption (\( \sim S^2 \)).
For many applications, however, the level of integration is increased when scaling to a new technology. Therefore, power consumption may not be reduced, or in fact it can even increase. The improved circuit performance obtained for the scaled technology is the result of shorter transistor channel lengths, lower threshold voltages, and reduced gate-oxide thicknesses. This, however, will lead to increased leakage power due to increased subthreshold leakage and gate oxide tunnelling currents. From 90nm technology onwards, leakage power becomes as important as dynamic switching power in many applications. Figure 1 plots the technology scaling trends of dynamic switching power and leakage power for high-performance microprocessors as predicted by IBM [17].

Another issue of technology scaling is the fact that as geometries shrink deeper into the nanometre regime, the variation of process parameters influences the chip performance and yield [16]. The impact of process parameter variation on circuit performance can be illustrated by the results of recent 90nm CMOS ring-oscillator measurements. The nominal power supply voltage equals a value of 1V.

Figure 2 shows an example of inter-die performance spread in which oscillation frequency is plotted against power supply voltage for eleven different samples of a ring-oscillator in 90nm CMOS. Samples were selected as “fast”, “typical” and “slow” with nominal frequencies of 822MHz, 713MHz, and 640MHz, respectively. The total frequency spread of the limited sample set is 180MHz. From these results, it should be clear that the measures have to be taken accordingly in order to maintain the design robustness.
2.3 Trade-offs involved in low-power designs

From the previous sections, the following can be summarised: The power consumption of a circuit fabricated in a given technology can be lowered by reducing one or more of the following circuit parameters: (i) the average switching activity \( a \), (ii) the circuit capacitance \( C \), (iii) the power supply voltage \( V_{DD} \), (iv) the frequency of operation \( f_{CK} \), (v) the off-state current \( I_{leak} \).

The switching activity \( a \) and the circuit capacitance \( C \) are parameters that are strongly related to the type of application for which the circuit has been designed. Next to that, the circuit capacitance \( C \) increases with an increasing integration density. Therefore, the optimisation of parameters \( a \) and \( C \) is trivial from a circuit point-of-view, and design for low-power is the result of optimisation of the remaining parameters \( V_{DD}, f_{CK}, \) and \( I_{leak} \).

Reducing \( V_{DD} \) is the primary way to lower both power and energy consumption, because of its quadratic relationship to dynamic power and its linear relationship with leakage power. However, \( V_{DD} \) reduction increases gate delays, and thus deteriorates circuit performance. As a result, one has to reduce \( f_{CK} \) to avoid hazards and to obtain power and energy savings. This has been illustrated in Figure 3, where the normalised dynamic portion of the energy per operation is plotted against the normalised operating frequency in case of \( V_{DD} \) reduction. Therefore, \( V_{DD} \) reduction can only be applied to those cases where peak performance is not required.

Reducing \( f_{CK} \) will provide linear power savings, but will not provide any energy savings; on the contrary, it will be less energy efficient due to the presence of off-state currents. A common technique to achieve power savings is clock gating, where the clock signals of unused circuit parts are turned off. Clock gating is a valuable technique for those cases where lower power (not energy) consumption is required.

Reducing \( I_{leak} \) will provide power and energy savings for the inactive circuit parts. The leakage current can be reduced by increasing the device's threshold voltages (reducing subthreshold leakage), thicker gate-oxides (reducing gate-oxide leakage), or \( V_{DD} \) reduction. The increased device's threshold voltage can be achieved statically, i.e. high-\( V_{th} \) devices, or dynamically, i.e. transistor body biasing. Increasing the gate-oxide thickness while maintaining transistor performance can only be done the current gate-oxide dielectric is replaced by one with a higher permeability.

\[ \text{Normalized Energy/operation} \]

\[ \text{Normalized Clock Frequency} \]

Figure 3 Relation between energy per operation and clock frequency in case of \( V_{DD} \) reduction [3].
3 Power supply voltage scaling

Aside from technology scaling, reducing just the power supply voltage for a given technology enables significant power and energy savings. However, voltage reduction comes at the expense of higher gate delays and there exists basically a trade-off between circuit performance and power reduction.

3.1 Voltage scaling effects

The impact of supply voltage scaling on circuit delay and power has been investigated for a 0.13μm static CMOS inverter. An inverter is the simplest CMOS logic circuit, and it is very much used in digital circuit designs. Circuit simulations have been performed using an in-house circuit simulator called PSTAR, and using MOS Model 11 (MM11) compact transistor models. Figure 4 shows the results of propagation delay and energy per operation as a function of supply voltage; the curves are normalized against nominal conditions, e.g. $V_{DD}=1.2$V. These trends can also be approximated by using the simple circuit models as presented in (3) and (5) respectively.

![Figure 4 Normalised propagation delay and normalised energy per operation versus supply voltage for a 0.13μm CMOS inverter in case of nominal process conditions.](image)

The lower bound of the supply voltage is set by the larger of the devices’ threshold voltages, i.e. $V_{th,n}$ and $V_{th,p}$, which is close to 0.35V for a 0.13μm CMOS technology. Beyond this voltage, the MOS transistors operate in the subthreshold region and their delay increases exponentially. The upper bound of the supply voltage is determined by the breakdown voltage of the gate-oxide. Operating at a supply voltage close to the upper bound is not recommended for long-term reliability.

From Figure 4 it can be observed that the inverter delay increases by about a factor of 3 when the supply voltage is scaled from its nominal value of 1.2 volts down to 0.7 volts ($\sim 2V_{th}$). For this range, the energy per operation is reduced by a factor of 3. When the inverter operates at its maximum performance, the power consumption equals the product of $energy \times (delay)^2$. For this case, the power consumption reduces by about a factor of 10 for the specified supply voltage range.
For modern deep-submicron technologies, the variability of the circuit performance due to process and temperature variations requires that conventional designs incorporate design margins to guarantee proper circuit operation under worst-case conditions (slow process, 125°C). For other than worst-case conditions, the circuit design can operate at a higher circuit performance than targeted. Properly controlling the power supply voltage can help to exploit this increased performance by tracking the circuit performance with respect to (local) process and temperature variation to operate at a more efficient energy efficient point. Figure 5 shows the operating frequency versus the energy per operation of a 0.13μm CMOS inverter for the best-case, typical-case, and worst-case operating conditions. The frequency and energy are normalised against their value obtained at a nominal supply voltage of 1.2 volts.

![Figure 5 Normalised frequency versus normalised energy per operation for the best-case, typical-case and worst-case conditions.](image)

Conventional designs are designed to run at frequencies lower than the normalised peak performance, e.g. 70% of the peak performance for this 0.13μm technology (slow-case condition). Designs under fast and typical conditions can operate at the same operating frequency with a lower supply voltage as compared to the slow condition. By reducing the supply voltage accordingly, energy can be conserved as compared to the fixed supply voltage case.

### 3.2 Circuit delay scaling of CMOS gates

The performance of digital CMOS circuits is limited by their slowest delay path, i.e. the critical path. For every circuit design, the impact of supply voltage scaling should be investigated for the critical path. However, designers normally balance delay path in the design. Therefore, it is difficult to identify one single critical path that remains critical over the range of supply voltage, process and temperature. The critical path is assembled by various complex CMOS gates. Circuit simulations have been performed on different 0.13μm CMOS gates as function of supply voltage. The circuit delay results of a 2-input nand, 2-input nor, 2-input exclusive-or, 2-input multiplexers, a scannable d-flipflop, and a 4-input and-or are shown in Figure 6, where they are normalised against the normalised inverter delay.
Over a wide supply voltage range, the circuit delay of the multiplexer, exclusive-or and the flip-flop does not track the inverter delay closely. A difference of up to 16% is observed in the supply voltage range between 0.7 and 1.2 volts. If one considers modelling the critical delay path using inverter gates only, one should incorporate delay margins to guarantee operation for the full supply voltage range. Furthermore, from the previous figure one can observe that the flip-flop is limiting the lowest bound of the supply voltage, e.g. 0.7 volts for 0.13μm CMOS.

Figure 7 shows the normalised propagation delay versus operating condition for the same set of CMOS gates. It can be observed that the lines are quite flat (≤10%), which means that all cells track the delay of the inverter quite well.
3.3 Prior art in voltage scaling techniques

A literature search has been performed as part of this graduation project. A detailed overview of prior art is presented in [15]. In this section, an overview of the main schemes will be given. There are basically two ways of lowering the power supply voltage without compromising system performance, namely static supply scaling and dynamic supply scaling.

3.3.1 Static supply scaling

Static supply scaling refers to the technique that assigns a minimum supply voltage to a circuit design such that it just meets its performance requirements. This minimum (or optimal) supply voltage value is determined during the design phase of the circuit design. Static supply scaling can be applied to a complete chip, but it is most effective when used for local supply voltage optimisation of individual voltage domains. For the latter case, one can partition the IC into different functional regions of which each is powered by its own dedicated supply voltage. Since the performance requirements of the non-critical regions are lower than those of the critical ones, their supply voltage is lowered in order to save power without degrading system performance.

Figure 8 shows an example of static supply scaling where two supply voltages are employed. A nominal (or high) supply voltage is applied to the performance-critical region, while the non-critical region is powered of a reduced supply. Communication between the regions should be performed through level shifters to avoid static currents.

![Figure 8 Example of two functional regions communicating through level shifters.](image)

The reduced supply voltage may either be generated off-chip, or on-chip from the nominal power supply. Both supplies require separate power grids and on-chip decoupling capacitors. Interfacing between both functional regions should be done using static power free level conversion circuits.

In 2002, Lackey et.al. [13] presented the concept of voltage islands and their application to SoC designs. The authors present voltage islands as the solution to dramatically reduce active and standby power consumption of SoCs.

3.3.2 Dynamic supply scaling

There are many examples in signal processing and general-purpose processing where the computational workload varies with time [2][8][14][17][22]. Dynamic supply scaling exploits the temporal domain to perform power supply optimisation at run time. The technique dynamically varies both operating frequency and supply voltage in response to workload demands. In this way, a processing unit always operates at the desired performance level while consuming the
minimal amount of power. During reduced workload periods, dynamic supply scaling lowers supply voltage and slows down computation instead of working at a high supply voltage and allowing the processing unit to idle. Even if the workload is fixed, e.g. independent of time, the power consumption can be lowered by tracking the process and temperature variations, thus, keeping the supply voltage at the lowest level possible. Dynamic supply scaling can decrease the system’s average power consumption during operation, without sacrificing the system performance.

Dynamic supply scaling can be applied to a complete chip or to individual functional units. It requires three components: (i) a circuit that can operate over a wide supply voltage range, (ii) a power manager that intelligently can vary the frequency of operation, and (iii) a feedback control loop to set a minimum supply voltage for the desired frequency. The power manager can be implemented either in software or in hardware. An example of an hardware implementation is a power management unit (PMU) [21]. The feedback control loop consists of three main components: (i) a performance sensor, (ii) a control unit, and (iii) a power supply actuator. A simplified block diagram is shown in Figure 9.

![Figure 9 General block diagram of a dynamic supply scaled system.](image)

The performance sensor models the critical delay path of the circuit-under-control, and monitors how the circuit reacts to process, temperature and supply voltage variations. The control unit receives input from the performance sensor, and compares it with a performance reference applied by a PMU or software. Then the controller decides to adapt the supply voltage when necessary, and controls the power supply actuator accordingly. The power supply actuator is an on-chip or off-chip DC/DC converter that can be anything ranging from a linear device to a more sophisticated loss-less device. The type of control required is fundamentally different from standard voltage regulators because in addition to regulate voltage for a given performance, it must also change the voltage when a new performance level is requested.

In 2000, Burd et.al. [2] presented a dynamic voltage scaled microprocessor system used in portable electronic devices. Digital control of power supply voltage is enabled using a dedicated IC containing a buck converter type of DC/DC converter. A buck converter requires additional external components, i.e. the loop filter (L and C). An overview of the system architecture is given in Figure 10. When this solution is used for island-based SoCs, each island requires either a buck converter for the case the island power supply is dynamically controlled, or a buck converter with multiple taps, one for each island. Since the buck converter is off-chip, the global power distribution of the SoC would become increasingly difficult when the number of islands to be controlled is increasing.
In 1999, Carley et al. [4] proposed a completely on-chip voltage regulation technique for locally generating an adaptive low voltage power supply from a given higher voltage power supply. A series linear regulator was used for controlling the power supply of the digital circuit without requiring any external components as it is the case when using a buck converter. A disadvantage of this approach is that part of the control and the linear regulator have been implemented by an analog solution; it is not easy to port an analog design across technology nodes.

In 1999, Carley et al. [4] proposed a completely on-chip voltage regulation technique for locally generating an adaptive low voltage power supply from a given higher voltage power supply. A series linear regulator was used for controlling the power supply of the digital circuit without requiring any external components as it is the case when using a buck converter. A disadvantage of this approach is that part of the control and the linear regulator have been implemented by an analog solution; it is not easy to port an analog design across technology nodes.

Summarising: Solutions using off-chip DC/DC converters are not suitable for island-based SoCs when the power supply of a large number of islands need to be controlled. Since each island requires its own DC/DC converter, off-chip solutions are expensive in terms of external components, number of supply pins of the chip and global power grid distribution. However, high power conversion efficiencies have been reported [22]. Current on-chip solutions propose analog implementations of linear power supply regulators, which are not easily portable to new CMOS technologies. In addition, they are more sensitive to digital supply noise and contain static biasing currents as compared to the case when the implementation is done in a digital fashion.
4 The proposed scheme

The aim of this work has been to develop a scheme to enable adaptive power supply control in System-on-Chip (SoC) type of applications. In contrast to prior art, the proposed scheme is able to perform power optimisation locally for the IC using fully-digital control. The scheme is particularly useful in those applications where the IC is subdivided into a number of functional regions. In this way, the scheme is fully compatible with the concept of voltage islands.

This chapter starts by introducing the system perspective. Next, the proposed system architecture is presented for the scheme enabling the adaptive control of power supply voltage. This chapter concludes with performance models developed for the proposed scheme.

4.1 System perspective

Figure 12 shows a block diagram of a SoC, which is partitioned into a number of functional regions, e.g. islands. Islands are fully electrically isolated from each other by means of triple-well shielding (substrate), and by means of the local supply actuator from the global power network. Because the power supply voltage conversion is fully integrated on chip, no external components are needed as it is the case for off-chip DC/DC converters. The proposed scheme does not affect the global power \( V_{DD} \) and \( V_{SS} \) distribution network as in case of off-chip DC/DC converters, which is advantageous during the chip implementation.

An island may contain a single IP or multiple IPs that require power characteristics unique from the rest of the design. Adaptive control of the island’s power supply voltage is enabled through feedback control, i.e. monitor, controller and actuator. Each island contains interfacing blocks to allow inter-island and off-chip communication. For such systems, a power management unit (PMU) supplies a performance reference to each island. This performance reference consists of the mode of operation, i.e. active and standby mode, and required island performance, i.e. its frequency of operation. In the active mode, the island is operational and the island’s power supply is reduced such that the island always runs at the minimum supply voltage possible for the reference performance as indicated by the PMU. In the standby mode, the island is inactive and its power supply is fully turned-off to reduce the power consumption to the lowest value possible. In this way, local optimisation of the chip’s...
power consumption is enabled while maintaining the system performance requirements.

Figure 13 shows a more detailed block diagram of an island. An island contains the following number of basic components: (i) a single or multiple synchronous IP cores, (ii) one or more local clock generating units (CGUs), (iii) a system to enable adaptive control of power supply voltage, (iv) input and output ports, and (v) voltage level converters for input/output signals.

![Block diagram of an island](image)

Dynamic supply scaling requires control over the frequency of operation and the power supply voltage as indicated in section 3.3.2. Since clock generation is done locally within each island, the CGU should support adaptive control of frequency. The CGU can be implemented as a ring-oscillating inverter chain, and frequency control is enabled by scaling its power supply voltage. The input and output ports are required for data buffering in case of inter-island or off-chip communication. The communication can be done in a synchronous [8] or asynchronous fashion, i.e. globally asynchronous locally synchronous (GALS) [5].

At the island’s boundary, voltage level conversion is required to translate the global signal levels (nominal supply) to island’s signal levels (island supply) and vice versa. This is required in order to maintain signal integrity at global level, because different island can operate at different supply voltages. As a consequence, one has to deal with potential short-circuit dissipation. Conventional level shifters can be used to eliminate short-circuit dissipation [25].

The focus of this investigation is on a scheme that enables the adaptive control of the power supply voltage within each island. The details of this scheme will be presented in the remainder of this report.

### 4.2 Proposed system architecture

The proposed adaptive power supply control scheme has been implemented by means of a fully-digital solution. This gives the advantage that the scheme is less sensitive to digital supply noise, avoiding static currents, it is easily portable to next process generations as compared to analog implementations, it does not require external components and its time response is very fast. The proposed scheme is driven by performance requirements as provided by a PMU, or it can be directed by software. Figure 14 shows a block diagram of the proposed system architecture as applied to an island.
The proposed scheme consists of two independent negative feedback control loops of which one controls the average supply voltage value (µ-supply control) and the other one controls average activity variations on a clock cycle basis (σ-supply control).

The µ-supply control loop consists of the µ-supply sensor, the µ-supply controller, and the power supply actuator. Average supply voltage control is performed periodically such that the island can meet its performance requirements and it is also used to compensate global process variations and temperature drifts. The µ-supply sensor monitors the actual silicon performance for a fixed period of time \( T_{\text{COUNT}} \gg T_{\text{CK}} \), and compares it with the required performance level as indicated by the PMU. Reference performance values are stored in a local look-up table such that the comparison is always done against design time values. Based on the performance difference, the µ-supply controller will set the appropriate control signals to the supply actuator to compensate any performance difference. The µ-reg and O-reg registers represent storage elements for the control signals as provided by the µ-supply controller. The µ-supply control is done for both the CGU and the IP core.

The σ-supply control loop consists of the σ-supply sensor, the σ-supply controller, and the power supply actuator. Its purpose is to compensate changes in the average circuit activity of the IP core due to e.g. computational load changes. The σ-supply sensor detects phase difference between the clock edge and its delayed version, where the delay is set equal to the critical path delay of the IP core. The delay line is powered from the supply voltage of the IP core, and there will only be a phase difference as a result of supply voltage fluctuations. The σ-supply controller will set the appropriate control signals to the supply actuator of the IP core to compensate for the phase difference. The σ-reg register represents a storage element of the control signals as provided by the σ-supply controller. This control is done on a cycle-to-cycle basis of the CGU clock frequency.

Figure 15 shows the normalised average current of a typical IP core versus the supply voltage with the operating regions of the µ-supply and σ-supply control loops. The µ-supply control is performed for a constant value of the data activity. The data activity is taken into account by σ-supply control.
The next sections will present the proposed power supply actuator and the related performance models. Chapter 5 will discuss the \( \mu \)-supply control, while the \( \sigma \)-supply control will be discussed in chapter 6.

### 4.3 Proposed power supply actuator

The basis for the scheme lies on the power supply actuator, which combines the option of supply voltage control in active operation mode of the IC, and an inactive standby mode. The actuator is implemented as a variable resistor between the circuit-under-control and its power supply terminals. In this way, no changes have to be made to the global power supply network of the IC.

The variable resistor has been implemented by segmented header (PMOS) and footer (NMOS) transistors. Each header and footer transistor segment or a subset of transistor segments is controlled by a dedicated complementary control signal. In this way, a discrete digital control of resistance value introduced by the series transistors is enabled. The control signals can be (re)programmed at runtime, thus, enabling adaptive control of power supply voltage. The number of transistor segments and their geometry determine the resolution (step size) and the supply voltage control range. Figure 16 shows a simplified diagram of the power supply actuator.

In Figure 16, \( V_{DD} \) and \( V_{SS} \) are the global power supply lines, which provide the nominal supply voltage to the IC. The supply voltage of the CMOS circuit equals \( V_{DD} - \Delta V \) in which \( \Delta V \) is the voltage drop across the segmented series transistors. The capacitor \( C \) models the following capacitances: \( i) \) the internal capacitance of the non-switching parts of the circuit and \( ii) \) the internal decoupling capacitance. The size of \( C \) needs to be well-sized in order to cope with voltage fluctuations of \( \Delta V \). Since capacitor \( C \) supplies the current peaks to the circuit, the current flowing through both series transistors is mainly the average current consumed by the circuit, and the voltage drop \( \Delta V \) will remain approximately constant.

![Figure 15 Normalised average current versus supply voltage for different data activities.](image)

The current is normalised to its value at \( V_{DD} = 1.2 \text{V} \).
The transistor segments of the power supply actuator always operate between cut-off \((V_{GS}=0)\) and the linear region \((V_{GS}>0\ \text{and} \ V_{DS}<V_{GS}-V_{th})\). The power supply actuator acts as a linear resistor that adds series resistance between the global power supply and the CMOS circuit. A footer (header) transistor segment is conducting when its control signal \(CTL_n (nCTL_v)\) is at high (low) level. The control signals of header and footer transistors are complementary signals. The CMOS circuit can be put in a standby mode when both header and footer transistors are fully turned-off, i.e. \(CTL_f=0\) and \(nCTL_l=V_{DD}\), reducing the power consumption of the circuit to a minimum value. In active mode of the circuit, both transistors are conducting. Different degrees of conduction can be achieved by applying the proper control signals, thus, changing the resistance value introduced by the series transistors and controlling the supply voltage of the circuit accordingly. The series transistors can be implemented as high-\(V_{th}\) transistors to minimise leakage power when the circuit is in standby mode.

### 4.4 Performance models

This section presents simple analytical models for power consumption, energy per operation, and the conversion efficiency when using the proposed power supply actuator to control power supply voltage. Furthermore, its transient response has been modelled. These models are based on the simple circuit models as presented in section 2.1.

#### 4.4.1 Power consumption

In section 2.1.1 it was found that in the first-order the total power consumption of synchronous digital CMOS circuits can be expressed as:

\[
Power = a \cdot C \cdot V_{DD}^2 \cdot f_{CK} + V_{DD} \cdot I_{leak} \tag{7}
\]

where \(a\) is the average switching activity of the circuit, \(C\) is the total circuit capacitance, \(V_{DD}\) is the power supply voltage, \(f_{CK}\) is the frequency of operation, and \(I_{leak}\) is the off-state current of the circuit due to subthreshold and gate-oxide leakage.

From (7) it is possible to derive an equivalent resistance of the switching CMOS circuit, which yields:

\[
R_{circuit} = \frac{1}{a \cdot C \cdot f_{CK} + \frac{I_{leak}}{V_{DD} - \Delta V}} \tag{8}
\]
where \( V_{DDO} \) is the non-controlled global power supply voltage, \( \Delta V \) represents the voltage drop across the series resistance introduced by the header and footer transistor of the power supply actuator. Since both header and footer transistor operate in the linear region \( (V_{DS}<V_{GS}-V_{th}) \), this series resistance can be expressed as:

\[
R_{series} = \frac{K_p}{W_p} + \frac{K_n}{W_n}
\]  \( (9) \)

where \( K_p \) and \( K_n \) are constants for a given process technology for the PMOS header and NMOS footer transistor respectively when the transistor operates in linear region and \( W_p \) and \( W_n \) are the corresponding transistor channel widths. By using (8) and (9), the voltage drop \( \Delta V \) across the series resistance and the effective supply voltage \( V_{DDO}-\Delta V \) of the circuit-under-control can be expressed as:

\[
\Delta V = \frac{\left(\frac{K_p}{W_p} + \frac{K_n}{W_n}\right)(aCf_{CK} \cdot V_{DDO} + I_{leak})}{1+\left(\frac{K_p}{W_p} + \frac{K_n}{W_n}\right) \cdot aCf_{CK}}
\]  \( (10) \)

\[
V_{DDO} - \Delta V = \frac{V_{DDO} - \left(\frac{K_p}{W_p} + \frac{K_n}{W_n}\right) \cdot I_{leak}}{1+\left(\frac{K_p}{W_p} + \frac{K_n}{W_n}\right) \cdot aCf_{CK}}
\]  \( (11) \)

Both (10) and (11) can be used to determine the power consumption of the circuit-under-control, and of the power supply actuator. This yields the following results:

\[
P_{circuit} = \frac{(aCf_{CK} \cdot V_{DDO} + I_{leak}) \left( V_{DDO} - \left(\frac{K_p}{W_p} + \frac{K_n}{W_n}\right) \cdot I_{leak} \right)}{\left(1+\left(\frac{K_p}{W_p} + \frac{K_n}{W_n}\right) \cdot aCf_{CK}\right)^2}
\]  \( (12) \)

\[
P_{series} = \frac{\left(\frac{K_p}{W_p} + \frac{K_n}{W_n}\right)(aCf_{CK} \cdot V_{DDO} + I_{leak})^2}{\left(1+\left(\frac{K_p}{W_p} + \frac{K_n}{W_n}\right) \cdot aCf_{CK}\right)^2}
\]  \( (13) \)

The total power consumption is the sum of (12) and (13):

\[
Power = \frac{(aCf_{CK} \cdot V_{DDO} + I_{leak}) \cdot V_{DDO}}{1+\left(\frac{K_p}{W_p} + \frac{K_n}{W_n}\right) \cdot aCf_{CK}}
\]  \( (14) \)
By comparing (7) and (14), it can be observed that a scaling term in the denominator is added to the power expression in case the proposed power supply actuator is used. Furthermore, it is not possible to find a closed-form solution for power consumption when combining (4) and (14). For this case, a numerical solution has to be used instead.

4.4.2 Energy per operation

The energy consumption can be found by dividing (14) by the frequency of operation $f_{CK}$. This results in the following expression:

$$\text{Energy} = \frac{\left( \alpha C_{f_{CK}} \cdot V_{DDO} + I_{\text{leak}} \right) \cdot V_{DDO} \cdot N}{1 + \left( \frac{K_p}{W_p} + \frac{K_n}{W_n} \right) \cdot \alpha C_{f_{CK}}}$$

(15)

where $N$ is represents the number of clock cycles to complete an operation.

4.4.3 Conversion efficiency

The conversion efficiency (CE) is defined by the ratio of the circuit's power consumption and the total power consumption. Dividing (12) by (14) gives the conversion efficiency:

$$CE = \frac{V_{DDO} - \left( \frac{K_p}{W_p} + \frac{K_n}{W_n} \right) \cdot I_{\text{leak}}}{V_{DDO} \cdot \left( 1 + \left( \frac{K_p}{W_p} + \frac{K_n}{W_n} \right) \cdot \alpha C_{f_{CK}} \right)}$$

(16)

The maximum conversion efficiency (100%) can be found when the supply voltage of the circuit-under-control is at its maximum (nominal) value. When the effective supply voltage of the circuit decreases, the power loss across the series resistance introduced by the power supply actuator increases, and the conversion efficiency will decrease. A linear relationship is found between conversion efficiency and the effective power supply voltage of the circuit. This reducing conversion efficiency is the main disadvantage of this type of power supply actuator as compared to high-efficient off-chip DC/DC converters.

4.4.4 Transition time

This section presents an expression for calculating the dynamic voltage drop $\Delta V(t)$ across the series transistors of the power supply actuator. With this expression, it should be able to calculate the voltage transition time, e.g. the time to reach from one steady-state value to another one. The following expression can be derived for the case that the operating frequency remains constant:

$$\Delta V(t) = \frac{R_{k+1} \cdot V_{DD}}{R_{k+1} + R_{\text{circuit}}} + \frac{(R_k - R_{k+1})R_{\text{circuit}} \cdot V_{DD}}{R_k + R_{\text{circuit}}(R_{k+1} + R_{\text{circuit}})} e^{-t / \tau}$$

(17)
with \[ \tau = \frac{R_{k+1}R_{\text{circuit}}}{R_{k+1} + R_{\text{circuit}}} \]

where \( R_{\text{circuit}} \) is the equivalent resistance of the circuit-under-control, \( R_k \) and \( R_{k+1} \) are two consecutive series resistance values introduced by the power supply actuator respectively, \( V_{DD} \) is the non-controlled global supply voltage and \( C \) is the non-switching circuit capacitance. From (17) one can derive a transition time, which is the time that it takes to switch the effective supply voltage between 1% and 99% of its end steady state value. The transition time is determined by the equivalent circuit resistance, the amount of non-switching capacitance and the resistance introduced by the series transistors. It is assumed that the series resistance \( R_k \) is changed to \( R_{k+1} \) instantaneously before the transition is started. Therefore, the dependency between transition time constant \( \tau \) and series resistance is expressed by \( R_{k+1} \) only. For a decreasing supply voltage the transition time will increase due to the increased value of \( R_{k+1} \). Therefore, a transition from a higher voltage to a lower one is slower than the opposite transition between these voltages. In case the operating frequency runs at its maximum possible value \( f_{\text{max}} \), the equivalent circuit resistance \( R_{\text{circuit}} \) will vary as function of the effective supply voltage. For a decreasing supply voltage, the equivalent circuit resistance will increase, thus, higher transition times are found than in the case in which the frequency is kept constant.

### 4.4.5 Application to a CMOS circuit

The presented performance models have been applied to a standard-cell based CMOS circuit in a 0.13µm technology with an area of 1mm². Typical circuit parameters are: (i) an average circuit activity of 0.3, (ii) a total circuit capacitance of 2nF, (iii) an operating frequency of 200MHz, (iv) a nominal power supply voltage of 1.2 volts, (v) a threshold voltage of 0.35V, and (vi) a total off-state leakage current of 27.3µA.

#### 4.4.5.1 Power consumption

The power consumption has been determined using expression (14) for the case in which the operating frequency is kept constant at 200MHz and in the case in which the operating frequency is scaled with the supply voltage according to (4). The obtained results are shown in Figure 17 and Figure 18 respectively. In these figures, the power consumption is normalised to its maximum value at nominal supply voltage of 1.2 volts.

**Figure 17 Normalised power consumption versus the effective supply voltage for a constant operating frequency.**
For both cases it can be observed that the total power and circuit power decreases when the effective supply voltage $V_{DD} - V$ decreases. The power consumed by the series transistors of the supply actuator will increase to a maximum value and then decrease, because of the decreasing average current of the circuit-under-control. Since the average current decreases faster when the frequency is not constant, the power consumed by the series transistors will reach earlier its maximum value for this case. The turn-over point in which the power consumption consumed by the series transistors alone is greater than for the circuit is reached at about half the supply voltage.

4.4.5.2 Energy per operation

Figure 19 plots the normalised energy per operation versus the effective supply voltage as obtained from (15). The normalisation is done with respect to the maximum value of the energy per operation as found at the nominal supply voltage value of 1.2 volts.
Since energy is not dependent on frequency, the same curve has been found when using expression (15) in case of a constant or variable operating frequency. The energy per operation is linearly related to the effective power supply voltage across the circuit-under-control due to the power loss in the series transistors of the power supply actuator.

### 4.4.5.3 Conversion efficiency

The conversion efficiency expresses how efficient the power conversion is done by the proposed power supply actuator. Figure 20 shows the conversion efficiency as function of the effective supply voltage as obtained from (16).

![Figure 20 Conversion efficiency versus the effective supply voltage.](image)

From this figure it can be observed that the conversion efficiency is linearly related to the effective supply voltage. This is a typical characteristic of the proposed power supply actuator, because it is a linear voltage regulator. When the effective supply voltage decreases by a factor of 2, also the conversion efficiency will decrease by a factor of 2.

### 4.4.5.4 Transition time

From (17) it can be observed that the worst-case transition time is found when the next resistance value of the series transistors is larger than the previous one \((R_{k+1} > R_k)\). This is the case when the effective power supply voltage switches from a high value to a lower one. The worst-case transition time occurs for the case that the effective power supply voltage reduces from its maximum value to its minimum one, e.g. half the maximum supply voltage. Figure 21 shows the drop voltage across the series transistors for the case as obtained by (17).

It can be observed that a steady state value (~0.6 volts) has been reached after 200ns. This shows that the proposed power supply actuator is capable of reducing the effective supply voltage within a short period of time. Off-chip DC/DC converters cannot reach the low transition times due to the presence of a loop filter. For those converters, typical transition times are in the order of tens of microseconds [2].

© Koninklijke Philips Electronics N.V. 2004

33
Figure 21 Drop voltage across the series transistors versus time.
5 μ-supply control

The purpose of μ-supply control is to adapt the average supply voltage value of the island to meet its required performance. The control method consists of a negative feedback control loop, which is operated at a periodic time-base much larger than the island’s clock period. Figure 22 shows the block diagram of the μ-supply control loop. This type of control is also able to compensate for global process variations as well as temperature drifts.

![Block diagram of the μ-supply control loop.](image)

This chapter starts with the concept of performance-based control. Next, the individual components of the μ-supply control loop are discussed.

5.1 Performance-based control

Circuits run at their peak performance when biased at their nominal power supply voltage. When peak performance is not required, the clock frequency and the supply voltage are lowered in order to save power and energy. The μ-supply control supports the selection of different operating frequencies by the performance scheduler, e.g. a PMU. The supported frequencies are referred to as major frequencies, which are used for coarse-grained control of the operating frequency to set the required circuit performance. Fine-grained frequency control is enabled through the so-called minor frequencies. These frequencies determine the frequency resolution, and are used for tracking variations in global process parameters and operating conditions. The minor frequencies cannot be selected by the PMU, they can only be accessed by the μ-supply control loop.

The major frequencies are indicated by \( f_0, f_1, \ldots, f_{K-1} \), where \( K \) the number of frequencies that can be selected. The difference between two consecutive frequencies is referred to as major frequency step. This step size \( \Delta f_{\text{major}} \) can be any value, but in practice it is limited to only one size or it may take a limited number of values. For the case of a constant \( \Delta f_{\text{major}} \), the step size between two consecutive major frequencies can be expressed as:

\[
\Delta f_{\text{major}} = f_{i+1} - f_i
\]

(18)

where \( i \) is an integer value in the range between 0 and \( K-2 \) and \( K \) represents the number of major frequencies.
frequencies

The required frequency resolution determines the number of minor frequencies required for each major frequency step. This resolution is determined by the difference between two consecutive minor frequencies. It is referred to as minor frequency step $\Delta f_{\text{minor}}$ and can be expressed as:

$$\Delta f_{\text{minor}} = \frac{\Delta f_{\text{major}}}{N}$$  \hspace{1cm} (19)

where $N$ is the number of minor frequencies per major frequency step. When $\Delta f_{\text{major}}$ is chosen to be constant, $N$ will also be constant. For this case, the frequency of operation can be expressed as:

$$f_m = f_0 - (m-1) \cdot \Delta f_{\text{minor}}$$  \hspace{1cm} (20)

where $f_0$ represents that maximum operating frequency of the circuit, $\Delta f_{\text{minor}}$ determines the frequency resolution and $m$ is an integer value that runs from 1 to $K \cdot N$; $K$ represents the number of major frequencies, and $N$ indicates the number of minor frequencies per major frequency step.

A high frequency resolution comes at the expense of design complexity, i.e. more transistor segments, as well as control complexity, i.e. more segments to be controlled. Therefore, trade-offs must be made when determining the frequency resolution.

5.2 $\mu$-supply power actuator

The power supply actuator is implemented as segmented header and footer transistors that are placed in series with the circuit-under-control as shown in section 4.3. In this section, the transistor segment sizing and the segment control for $\mu$-supply control will be discussed.

5.2.1 Transistor segment sizing

The voltage drop across the series transistors is dependent on the (average) current consumed by the CMOS circuit. Therefore, the transistor segment size needs to be determined proportionally to the circuit-under-control. At design time, characterisation of the circuit is needed to determine its average current for every major frequency. This should be done for the lowest supply voltage possible for the circuit such it can just meets its performance requirement. Next, Ohm's law can be applied to determine the segment's resistance, and the transistor segment size for all major frequencies.

One could use the same procedure to determine the segment size for all minor frequencies. However, this is not preferred because the major frequency steps are typically at least one order of magnitude larger as compared to the minor frequency step. There is a non-linear relationship between frequency and actuator's series resistance, e.g. constant frequency steps result in non-constant resistance steps. By combining (4) and (11) it is not possible to find a closed-form expression for calculating the transistor segment sizes. Therefore, for ease of implementation, a piece-wise linear (PWL) approximation has been used to obtain such closed-form expression for the minor frequencies. With this approximation the frequency is now linearly related to the series resistance. The PWL approximation is based on the frequency-series resistance pairs determined for the major frequencies.

Figure 23 shows the operating frequency versus actuator series resistance in which major frequencies (black circles) and minor frequencies (gray circles) are indicated.
In this figure, the major frequencies are indicated by $f_{(i, j=0)}$ and the corresponding actuator series resistance values are indicated by $R_{(i, j=0)}$, where $i$ is an integer value that represents the major frequency points and $j$ the minor frequency points. By using the PWL approximation, the delta resistance between two consecutive minor frequencies $\Delta R_{\text{minor}}$ is constant for each $\Delta f_{\text{major}}$ range. Therefore, the following expression holds:

$$\Delta R_{\text{minor}} (i) = R_{(i, j=n+1)} - R_{(i, j=n)} = \frac{R_{(i+1, j=0)} - R_{(i, j=0)}}{N}$$ 

(21)

where $i$ is an integer between 0 and $K-2$ representing the major frequency, $n$ is an integer between 0 and $N-2$ representing the minor frequency and $N$ is the ratio $\Delta f_{\text{major}}/\Delta f_{\text{minor}}$.

The actuator series resistance at each frequency point can be expressed as:

$$R_{(i, j=n)} = R_{(i, j=0)} - n \cdot \Delta R_{\text{minor}} (i) = \frac{1}{\sum_{j=0}^{n} \frac{1}{R_{S(i, j)}}}$$

(22)

where $i$ is an integer between 0 and $K-1$ representing the major frequency, $n$ is an integer between 0 and $N-1$ representing the minor frequency and $R_{S(i, j)}$ represents the resistance value of one individual transistor segment.

The actuator series resistance represents the equivalent resistance of a parallel resistance network as shown in Figure 24.

Figure 24 Parallel resistance network as introduced by the power supply actuator.
Using (22), the resistance value of each individual transistor segment can be calculated by the following expression:

\[
R_{S(i,j=n)} = \frac{\left( R_{S(i,j=0)} - (n-1) \cdot \Delta R_{\text{minor}}(i) \right) \cdot \left( R_{S(i,j=0)} - n \cdot \Delta R_{\text{minor}}(i) \right)}{\Delta R_{\text{minor}}(i)}
\]

(23)

where \(i\) is an integer between 0 and \(K-1\) representing major frequencies and \(n\) is an integer between 1 and \(N-1\) representing the minor frequencies. The value of \(R_{S(i,j=n)}\) represents the sum of the resistance as introduced by a single header and footer transistor segment. Due to the symmetric implementation of the actuator, the header and footer segment resistance equals half the value as calculated in (23).

### 5.2.2 Smart segments

Every transistor segment requires an individual control signal that indicates its conductivity. The number of control signals required to control each individual segment will be as large as the total number of segments used in the power supply actuator. Reducing control complexity can be done by using complementary control for PMOS header and NMOS footer transistors. A simple inverter gate can be used to generate these complementary control signals. However, when the actuator supports the selection of \(K\) major frequencies and \(N\) minor frequencies per major frequency step, the number of control signals required will be equal to the product of \((K-1)\) and \(N\).

As an example, for \(K=5\) and \(N=25\) the number of control signals required will be equal to 100. A 100-bit wide control bus and 100 inverters would be required to control the actuator.

A binary coding scheme has been applied in order to minimise control complexity. This coding scheme enables categorization of the transistor segments for a given frequency control range. The transistor segments have been categorized into \((K-1)\) segment ranges, where \(K\) equals to the number of major frequencies. A graphical representation is shown in Figure 25.

![Figure 25 Segment ranges of the power supply actuator](image)

A segment range is selected based on the major frequency selected by the PMU. The transistor segments that are part of the selected segment range are controlled, while all other transistor segments are set to be either conducting or non-conducting. As an example, just consider the case that the segment range \(i+1\) is selected (see Figure 25). The corresponding transistor segments are controlled, while those of segment range \(i\) are set to be non-conducting, and the ones of segment range \(i+2\) are set to be conducting. A segment range is selected by a binary-coded address, while its transistor segments are controlled through binary-coded control. This results that the power supply actuator can be controlled by \(\log_2(K)+\log_2(N)\) bits. As a consequence of the binary-coding
scheme, each segment range requires a segment decoder as indicated in Figure 26.

Every segment decoder has a unique address that corresponds to a particular segment range. A segment range is selected when its address is found at the \( \log_2(K) \)-bits major bus. In this case, the decoder converts the binary-coded control signals found at the \( \log_2(N) \)-bits minor bus to the equivalent control signals for the transistor segments. When the segment range is not selected, the decoder sets the transistor segments to be either conducting or non-conducting based on the address found at the major bus. For the example of \( K=5 \) and \( N=25 \), only a 8-bit wide control bus will be required as compared to the 100-bit control bus for non-coded control signals.

Next to that, two additional control bits have been added to the segment decoder, namely standby and bypass. Both bypass and standby are provided by the PMU. The standby signal is used to put the circuit-under-control in standby mode. An active standby signal sets all transistor segments to be non-conducting. The bypass signal is used to set all transistor segments to be conducting. It is used to bypass the control signals generated by the \( \mu\)-supply controller. Two additional control lines are needed for providing the standby and bypass signals.

The control complexity is significantly reduced by using segment decoders. Their function has been been implemented in VHDL code using combinatorial logic only.

### 5.3 \( \mu\)-supply sensor

Digital control requires analog signals translated into digital ones to be able to process them with digital functional units. The \( \mu\)-supply sensor uses the CGU to perform the voltage-to-frequency conversion, followed by a counter to convert the oscillating frequency to a digital representation [24]. A block diagram of the \( \mu\)-supply sensor is shown in Figure 27.

\[
f_{\text{CK}} \quad \text{Counter} \quad N_{\text{COUNT}}
\]

\[
f_{\text{COUNT}} = 1 \text{MHz}
\]

Figure 27 Block diagram of the \( \mu\)-supply sensor.

The sensor output \( (N_{\text{COUNT}}) \) is a binary representation that depends on the counter interval \( (T_{\text{COUNT}}) \) by the following expression:
\[ N_{\text{COUNT}} = \frac{T_{\text{COUNT}} }{T_{\text{CK}}} = \frac{f_{\text{CK}} }{f_{\text{COUNT}}} \]  

(24)

where \( T_{\text{CK}} \) represents the clock period. Basically, \( N_{\text{COUNT}} \) represents the number of oscillation periods within the counter interval \( T_{\text{COUNT}} \), which relates to the average CGU supply voltage within the counter interval. At the end of each interval, \( N_{\text{COUNT}} \) is stored and the counter resets to zero for the next count. Longer counter intervals or shorter oscillator periods enable higher resolution of the output. In order to avoid variations of \( T_{\text{COUNT}} \) due to process and operational drifts, \( f_{\text{COUNT}} \) should be generated by an off-chip reference oscillator, i.e. a crystal oscillator. The \( \mu \)-supply sensor requires a count frequency of 1 MHz.

The implementation of the \( \mu \)-supply sensor has been done in behavioural VHDL code. The corresponding flow diagrams are given in the appendix.

5.4 \( \mu \)-supply controller

The \( \mu \)-supply control is done using a simple integral controller. Basically, the controller consists of four components, which are a shifter, an adder, and two counters. A simplified block diagram is shown in Figure 28.

![Block diagram of the \( \mu \)-supply controller.](image)

Figure 28 Block diagram of the \( \mu \)-supply controller.

For closed-loop operation, the input to the controller are the reference performance and the measured performances values. The reference performance \( N_{\text{REF}} \) is a digital representation of a major frequency. As an example, a major frequency of 200 MHz is represented by an \( N_{\text{REF}} \) of 200 \((f_{\text{COUNT}} = 1 \text{MHz})\). The \( N_{\text{REF}} \) values are determined at design time, and they are stored in the island’s look-up-table (LUT). The measured performance \( N_{\text{COUNT}} \) is provided by the \( \mu \)-supply sensor. The outputs of the controller are the binary-coded control signals for the power supply actuator.

The difference \( N_{\text{REF}} - N_{\text{COUNT}} \) is referred to as error count \( N_e \), which is converted to a value \((\Delta O_{\text{COUNT}})\) to update the O-counter. This conversion can be expressed as follows:

\[ \Delta O_{\text{COUNT}} = \frac{f_{\text{COUNT}} \cdot N_e }{\Delta f_{\text{minor}}} \]  

(25)

For ease of implementation, the ratio \( \Delta f_{\text{minor}}/f_{\text{COUNT}} \) is chosen to be equal to a power-of-two. This
means that in case of $f_{\text{COUNT}}=1\text{MHz}$, the frequency resolution $\Delta f_{\text{minor}}$ is constrained to $2^X \text{MHz}$, where $X$ is an integer value. This constraint yields in a implementation in which a simple shifter can be used to perform the division instead of a more complex multiplication unit.

The controller contains two counting units, namely $\mu$-counter and O-counter, which provide the control signals to the transistor segments of the power supply actuator. Each combination of counter values results in a required discrete operating frequency $f_{(k,n)}$, where $k$ represents the $K$ major frequencies and $n$ represents the $N$ minor frequencies per major frequency step. As an example, $f_{(0,0)}$ is the 1st major frequency that corresponds to $\mu$-counter=0 and O-counter=0. Frequency $f_{(1,20)}$ is the 20th minor frequency in the segment range=1 that corresponds to $\mu$-counter=1 and O-counter=20. In this way, each counter value combination relates to an unique operating frequency. At the edge of each segment range, the O-counter gives an overflow/underflow signal and the $\mu$-counter is updated accordingly. The O-counter operates in a closed-loop, and it is basically an integrator. When the PMU requests a new major frequency to be set by the controller, the change frequency signal becomes active and the $\mu$-counter is updated with the new performance reference in an open-loop approach.

The implementation of the $\mu$-supply controller has been done as finite state machine in behavioural VHDL code. The corresponding flow diagrams are given in Appendix B.

The operation of the $\mu$-supply control is now as follows: In the island's active mode, the PMU points to the required $N_{\text{REF}}$. Each counter interval $T_{\text{COUNT}}$, an error count $N_e$ is calculated. This error count represents the difference between the reference $N_{\text{REF}}$ and the measured value $N_{\text{COUNT}}$. When $N_e=0$, the island operates at the required performance level. When $N_e>0$, the island operates at a lower performance than required, thus, the average supply voltage value is too low. When $N_e<0$, the island operates at a higher performance than required, and the average supply voltage is too high. Since the comparison is done against design time values, the $\mu$-supply control loop is capable of tracking variations of process parameters and operating conditions.

### 5.5 Loop stability analysis

Given that the CGU clock frequency $f_{\text{CK}}$ is at least one order of magnitude higher than the count frequency $f_{\text{COUNT}}$, a frequency domain transfer function of the IP core including the power supply actuator can be approximated by the following expression:

$$H(s) = \frac{1}{s + \left(\frac{1}{R_{\text{series}}} + \frac{1}{R_{\text{circuit}}}\right) \cdot C_{\text{non-sw}}}$$

where $R_{\text{series}}$ is the series resistance introduced by the power supply actuator as can be calculated from (9), $R_{\text{circuit}}$ is the equivalent circuit resistance as can be calculated from (8), and $C_{\text{non-sw}}$ is the non-switching circuit capacitance.

The $\mu$-supply controller is implemented by a simple integrator of which the frequency domain transfer function can be expressed as:

$$C(s) = \frac{K_I}{s}$$

where $K_I$ is the gain coefficient of the controller.
The block diagram of the μ-supply control loop is shown in Figure 29.

![Block diagram of the μ-supply control loop.](image)

The input to this system is the reference count \( N_{\text{REF}} \), and the output is the effective power supply voltage of the circuit, i.e. \( V_{\text{DDC}} \). \( K_{\text{DEC}} \) represents the μ-supply segment decoder gain in [V/count], \( K_{\text{VCO}} \) represents the CGU gain in [Hz/V] and \( S(s) \) represents the transfer function of the μ-supply sensor which is essentially a sampler unit. Please note that under the assumption \( f_{\text{CK}} \gg f_{\text{COUNT}} \), \( C(s) \) and \( H(s) \) behave as the continuous part of the system. In this case, no discrete transfer function can be derived for the system, because the input is not sampled before applied to the continuous system parts. Therefore, the sampler can be modelled by a product of the gain coefficient \( K_{\text{sampling}} \) in [count/Hz] and the loop delay term \( e^{-sT_{\text{COUNT}}} \). The loop stability analysis can be performed in the Laplace domain. The loop gain can be expressed as:

\[
\text{Loop gain} = \frac{K_{\text{I}}}{s} \cdot K_{\text{DEC}} \cdot H(s) \cdot K_{\text{VCO}} \cdot K_{\text{sampling}} \cdot e^{-sT_{\text{COUNT}}}
\]

(28)

The gain coefficient \( K_{\text{I}} \) can be determined by taking into account the shifter and the counter (integrator) blocks of the μ-supply controller. In this analysis, the shifter performs a divide-by-4 operation and the counters use 6 clock cycles of the CGU clock. Therefore, \( K_{\text{I}} \) can be calculated as:

\[
K_{\text{I}} = \frac{K_{\text{SHIFTER}}}{N_{\text{int}} \cdot T_{\text{CK}}} = \frac{f_{\text{CK}}}{24}
\]

(29)

where \( K_{\text{SHIFTER}} \) represents the gain coefficient of the shifter in [count/count], and \( N_{\text{int}} T_{\text{CK}} \) represents the integration time of the counter.

The decoder gain coefficient \( K_{\text{DEC}} \) translates the count value as supplied by the μ-supply controller to a voltage representation. In this analysis, the decoder enables 100 minor frequencies over a supply voltage range between 0.7 volts and 1.2 volts. Therefore, \( K_{\text{DEC}} \) can be calculated as:

\[
K_{\text{DEC}} = \frac{V_{\text{DDC,max}} - V_{\text{DDC,min}}}{M} = 0.5
\]

(30)

where \( V_{\text{DDC,max}} \) and \( V_{\text{DDC,min}} \) represent the maximum and minimum effective supply voltage of the circuit respectively, and \( M \) represents the total number of minor frequencies over the supply voltage range.

The CGU gain coefficient \( K_{\text{VCO}} \) represents the relationship between CGU frequency and the effective supply voltage. Its value can be determined by:

\[
K_{\text{VCO}} = \frac{f_{\text{CK}}}{V_{\text{DDC}}}
\]

(31)
The sampler gain coefficient $K_{sampling}$ translates the CGU frequency value into an equivalent count value. The sampling delay introduces another pole in the system around the sampling frequency, which results in additional phase shift impacting loop stability. The transfer function of the $\mu$-supply sensor $S(s)$ can be expressed as [7]:

$$S(s) = K_{sampling} \cdot e^{-sT_{COUNT}} \approx \frac{1}{s + f_{COUNT}} \tag{32}$$

where $f_{COUNT}$ represents the sampling frequency. In this analysis, a sampling frequency of 1MHz has been used.

![Open-loop Frequency Response](image)

**Figure 30** Open-loop frequency response of the $\mu$-supply control loop. Solid line: $V_{DDC}=0.7$ volts and dashed line: $V_{DDC}=1.2$ volts.

Figure 30 shows the open-loop frequency response of the system for the two supply voltage limits ($V_{DDC}=0.7$V and $V_{DDC}=1.2$V). The related phase and gain margins are indicated. Phase margins of 58.8 degrees and 21.5 degrees are found for $V_{DDC}=0.7$V and $V_{DDC}=1.2$V, respectively. Gain margins of 27dB (0.7V) and 49.5dB (1.2V) are found. From Figure 30, it can be observed that the loop gain is less than 1 at the sampling frequency of 1MHz, thereby, ensuring system stability.
6 σ-supply control

The purpose of σ-supply control is to control the supply voltage value on a cycle-to-cycle basis of the CGU clock frequency. The purpose of this control is to correct for changes in the average circuit activity. A delay-locked-loop (DLL) has been used for this purpose. Figure 31 shows a block diagram of the σ-supply control loop.

Figure 31 Block diagram of the σ-supply control loop.

This chapter starts with the concept of activity-based control. Next, the individual components of the σ-supply control loop are discussed.

6.1 Activity-based control

The activity factor \( a \) is a circuit parameter that represents the average probability of two signal transitions occurring at each circuit node within a single clock period. The circuit activity can be split into two components, which are clock activity \( a_{CK} \) and data activity \( a_D \). Clock activity \( a_{CK} \) is related to circuit nodes of the clock network. It can reach values up to a maximum of 1, which is equivalent to two transitions within the clock period. Lower activity values can be obtained when clock gating is applied for power management. The data activity \( a_D \) is related to the circuit nodes other than those of the clock network and it can reach values up to a maximum of 0.5. The data activity value depends on the type of application, i.e. audio or video, as well as on the computational workload.

The charge stored on the non-switching circuit capacitance supplies current peaks to the circuit caused by instantaneous activity changes. As a result, the power supply supplies only an average current, which can be expressed as:

\[
I_{\text{average}} = a \cdot C \cdot V_{DD} \cdot f_{CK} + I_{\text{leak}}
\]

(33)

where \( a (=a_{CK}+a_D) \) is the average switching activity of the circuit, \( C \) is the total circuit capacitance, \( V_{DD} \) is the power supply voltage, \( f_{CK} \) is the frequency of operation, and \( I_{\text{leak}} \) is the off-state current of the circuit due to subthreshold and gate-oxide leakage. For a given \( V_{DD} \) and \( f_{CK} \), the average current is about linearly related to the activity factor \( a \).
For the proposed power supply actuator, the voltage drop $\Delta V$ across the series transistors is directly proportional to $I_{\text{average}}$. On one hand an increasing circuit activity will increase $I_{\text{average}}$, which in turn increases $\Delta V$. As a result, the effective supply voltage $V_{\text{DD}} - \Delta V$ and also $I_{\text{average}}$ will decrease. On the other hand, an increasing circuit activity will decrease the circuit resistance $R_{\text{circuit}}$ as can be observed in expression (8). Since the actuator acts as a voltage divider, $\Delta V$ will increase proportionally with the circuit activity, and thus, it will decrease the effective supply voltage across the circuit-under-control. The opposite happens for a decreasing circuit activity. The $\sigma$-supply control adjusts the series resistance of the actuator to compensate for the supply voltage variation as a result of a change in circuit activity.

Discrete activity levels are indicated by $a_0, a_1, \ldots, a_{M-1}$, where $M$ the number of activity levels that can be distinguished. The difference between two consecutive activity levels is referred to as activity steps. Basically, the activity step size $\Delta a$ can be any value, but in practice they are limited to only one value or maybe a few different values. In case of $\Delta a$ constant, it can be expressed as follows:

$$\Delta a = a_{i+1} - a_i$$  \hspace{1cm} (34)

where $i$ is an integer value in the range between 0 and $M-2$. The parameter $M$ represents the number of activity levels.

### 6.2 $\sigma$-supply power actuator

The power supply actuator is implemented as segmented header and footer transistors that are placed in series with the circuit-under-control as shown in section 4.3. In this section, the transistor segment sizing and the segment control for $\sigma$-supply control will be discussed.

#### 6.2.1 Transistor segment sizing

The power supply actuator operates as a voltage divider to set the effective supply voltage of the circuit-under-control. The circuit resistance $R_{\text{circuit}}$ is inverse proportional to the circuit activity. As an example, an increase in activity will result in a decrease of $R_{\text{circuit}}$ and vice versa. In order to maintain constant the effective supply voltage, the series resistance $R_{\text{series}}$ of the actuator should change proportionally with $R_{\text{circuit}}$. In this way, the required value of $R_{\text{series}}$ can be determined for each different value of the circuit activity. Figure 32 shows the circuit activity as function of the series resistance of the actuator for the case of a constant operating frequency.

The total series resistance of the actuator can be expressed as:

$$R_i = \frac{K_R}{a_i \cdot C \cdot f_{CK}} = \frac{1}{\sum_{j=0}^{i-1} R_{Sj}}$$  \hspace{1cm} (35)

where $i$ is an integer between 0 and $M-1$ representing a particular discrete value of the circuit activity $a$, $K_R$ represents the ratio $R_{\text{series}}/R_{\text{circuit}}$ for the lowest circuit activity value $a_0$ and $R_{Sj}$ represents the resistance value of one individual transistor segment.
The actuator series resistance represents the equivalent resistance of a parallel resistance network. Using (35), the resistance value of each individual transistor segment can be calculated by the following expression:

\[
R_{Si} = \frac{K_R}{\Delta a_i \cdot C \cdot f_{CK}}
\]  

(36)

where \(i\) is an integer between 1 and \(M-1\) representing a particular value of the circuit activity, and \(\Delta a\) represents the activity step. The value of \(R_{Si}\) represents the sum of the resistance as introduced by a single header and footer transistor segment. Due to the symmetric implementation of the actuator, the header and footer segment resistance equals half the value as calculated in (36).

Two cases can now be considered: (i) \(f_{CK}\) is constant and (ii) \(f_{CK}\) is not constant. A constant \(f_{CK}\) reflects to the case when transistor segmentation is done individually for each major frequency. For each major frequency, all transistor segments have the same size when \(\Delta a\) is considered to be constant. Another approach would be to consider \(f_{CK}\) to be not constant. For this case, the transistor segmentation needs to be done between over the full range of \(f_{CK}\) and \(a\) values.

### 6.2.2 Smart segments

A segment decoder is present in order to reduce the control complexity of the transistor segments. The decoder converts the binary-coded control signals to the equivalent control signals for the transistor segments. When transistor segmentation is done per major frequency, the number of segment decoders required will be the same as the number of major frequencies. For this case, the segment decoders are similar to those of the \(\mu\)-supply control loop. When transistor segmentation is done over the full range of \(f_{CK}\) and \(a\), no addressing will be required for the segment decoders, which reduces the decoder complexity.

The segment decoder is derived from the \(\mu\)-supply equivalent (see section 5.2.2) and has been implemented in VHDL code using combinatorial logic only.
6.3 $\sigma$-supply sensor

Since the proposed power supply actuator is placed in series with the circuit-under-control, it is sensitive to variations in the average circuit activity, e.g. load changes. The non-switching circuit capacitance of the circuit-under-control should be sized sufficiently large to cope with the variations of the circuit activity at a clock cycle basis. The $\sigma$-supply sensor is used to detect changes in the average circuit activity. Figure 33 shows the circuit implementation of this performance sensor.

$$\text{Fig. 33} \quad \text{Block diagram of the } \sigma\text{-supply sensor.}$$

The $\sigma$-supply sensor consists of a delay line and a phase detector. The delay line's power supply is the same supply as for the circuit-under-control. The delay is equal to the critical path delay of the circuit. The delay line can be implemented by a critical path replica, or by any other circuit that models the critical path delay. One can also use an inverter chain for this purpose, but one should incorporate delay margins to guarantee operation of the full supply voltage range as has been shown in section 3.2.

A phase detector has been used that consists of two bang-bang type of phase detectors and a few extra logic gates [10]. A bang-bang phase detector uses a symmetrical flip-flop implementation to measure the phase difference. The detector contains only digital CMOS gates.

$$\text{Fig. 34} \quad \text{Left: Bang-bang phase detector. Right: Full circuit of the phase detector used [10].}$$

At every clock cycle, a comparison is done between the CGU clock edge and its delayed version. When the delay is less than one CGU clock cycle, the $\text{DN}$ signal of the phase detector becomes active indicating that the supply voltage of the circuit can be lowered. When the delay is more than one clock cycle, the $\text{UP}$ signal becomes active indicating that the supply voltage of the circuit must be increased. When the delay is exactly one CGU clock cycle, there is no phase difference between the input signals and the $\text{Just}$ signal becomes active. The phase detector outputs $\text{UP}$, $\text{Just}$, and $\text{DN}$ are propagated to the $\sigma$-supply controller, which in turn decides on the necessary control actions. The $\text{Just}$ signal will disable the $\sigma$-supply controller such that an unstable oscillatory behaviour is eliminated for small phase differences between the input signals.
6.4 \( \sigma \)-supply controller

Similar to the \( \mu \)-supply control, the \( \sigma \)-supply control is also done using a simple integral controller. Basically, the controller consists only of a counter. A simplified block diagram is shown in Figure 35.

For closed-loop operation, the input to the controller are the \( UP, Just \) and \( DN \) signals (provided by the \( \sigma \)-supply sensor) and the outputs are the binary-coded control signals for the power supply actuator. When the \( UP \) signal becomes active, the counter value is decreased by one to reduce the series resistance of the power supply actuator, thus, increasing the supply voltage of the circuit. When the \( DN \) signal becomes active, the counter value is increased by one to increase the series resistance of the power supply actuator, thus, decreasing the supply voltage of the circuit. The \( Just \) signal indicates that the circuit is powered off the desired supply voltage, and it disables the counter. The counter provides the control signals to the transistor segments of the actuator. There are \( 2^M \) counter values of which each represents an unique discrete activity level \( a_r \). As an example, the lowest activity value \( a_0 \) corresponds to \( \text{counter}=0 \), while the maximum activity value \( a_{M-1} \) corresponds to \( \text{counter}=2^{M-1} \).

The implementation of the \( \sigma \)-supply controller has been done in behavioural VHDL code.

6.5 Loop stability analysis

A delay locked loop (DLL) is used for \( \sigma \)-supply control. In the previous sections, it has been shown that the DLL consists of four components, namely (i) a voltage-controlled delay line, i.e. the critical path replica, (ii) a bang-bang phase detector, (iii) an integrator-based controller, (iv) a decoder unit. Ideally, when the DLL is near lock, the phase detector produces pulses with a quasi regular periodicity. This behaviour can be approximated by a sampled time model \([1][9]\). Furthermore, it is assumed that the phase detector only works on one of the CGU clock edges and using the CGU clock period \( T_{CK} \) as sampling period. As the control signals should only change during the time when the phase detector input waves are out-of-phase, their value can also be approximated by a sampled value. The block diagram of the \( \sigma \)-supply control loop is shown in Figure 36.
The input to this system is the reference phase of the CGU clock \( \phi_{\text{REF}} \). \( \phi_{\text{REF}} \) is supplied to the phase detector and the voltage-controlled delay line \( DL(z) \). \( K_{PD} \) represents the phase detector gain in \([1/s]\), \( K' \) represents the \( \sigma \)-supply controller gain and \( K_{DEC} \) represents the \( \sigma \)-supply segment decoder gain in \([V]\).

Every sampling period, the phase detector will create an impulse \((UP, \text{Just}, \text{or} \ DN)\) based on the phase difference \( \Delta \phi \). As these are digital signals, their difference will be either 0, or ±1, and they are supplied to the controller. When the loop is near lock, the gain coefficient of the phase detector \( K_{PD} \) can be expressed as:

\[
K_{PD} = \text{sign}(\Delta \phi)
\]  

(37)

where the \( \text{sign}(\Delta \phi) \) is a function that can be either 0, or ±1 depending on the phase difference between the reference and feedback clock signal.

The \( \sigma \)-supply controller is implemented by a simple (discrete) integrator that performs integration every clock cycle. Therefore, the controller gain \( K' \) equals unity.

The decoder gain coefficient \( K_{DEC} \) translates the controller output to a voltage representation. In this analysis, the decoder enables 25 activity steps over the whole data activity range between 0 and 0.5. Therefore, \( K_{DEC} \) can be calculated as:

\[
K_{DEC} = \frac{a_{\text{max}} - a_{\text{min}}}{M} \cdot V_{DDC}(a) = \frac{0.5}{25} \cdot V_{DDC}(a)
\]  

(38)

where \( a_{\text{max}} \) and \( a_{\text{min}} \) represent the maximum and minimum data activity of the circuit respectively, \( M \) represents the total number of activity steps over the circuit data activity range, \( a \) is the actual circuit data activity and \( V_{DDC}(a) \) expresses the relation between effective supply voltage and the actual circuit activity \( a \). This relationship can be calculated by using expression (11).

The gain coefficient \( K_{DL} \) (in \([s/V]\)) of the voltage-controlled delay line represents the relationship between its delay and its effective supply voltage. Its value can be determined by:

\[
K_{DL} = \frac{T_{CK}}{V_{DDC}}
\]  

(39)

The approach described in [1] has been used to determine the loop gain of the DLL. The final sampled time expression of the \( \sigma \)-supply control loop can be determined from Figure 36. This yields the following expression:

\[
\phi_{\text{OUT}}(n) = \phi_{\text{REF}}(n - \delta) - K_T [\phi_{\text{REF}}(n - 1) - \phi_{\text{OUT}}(n - 1)]
\]  

(40)

where \( K_T = K_{PD} K' K_{DEC} K_{DL} \) and \( \delta \geq 1 \) is the total delay of the voltage-controlled delay line in number of clock cycles.

The phase transfer function can be determined by taking the discrete z-transform of (40):
The voltage-controlled delay line is designed such that it models the critical path delay of the circuit-under-control. For this case, (41) becomes:

\[
\text{Loop gain} = \frac{\phi_{\text{OUT}}(z)}{\phi_{\text{REF}}(z)} = \frac{\frac{z^{-\delta} - K_T \cdot z^{-1}}{1 - K_T \cdot z^{-1}}}{\frac{1}{z^{\delta} - K_T \cdot z^{\delta-1}}}
\]

The overall phase transfer function will present a single pole. From (42), the stability condition for the \(\sigma\)-supply control loop can easily be derived: \(K_T < 1\). \(K_T\) is much smaller than 1 in typical integrated circuits for clock related functions [1]. This is also the case for the \(\sigma\)-supply control loop, and thereby, ensuring system stability.
7 Circuit implementation

The individual components of the adaptive power supply control scheme have been implemented in a 0.13µm CMOS technology using the system specification as presented in section 7.2. The implementation concerns circuit level schematics, which are obtained either through logic synthesis or directly on circuit schematic level.

This chapter gives an overview of the design tools and libraries used, the circuit details and the corresponding simulation results.

7.1 Design tools and libraries

The design tools used for designing the components are part of the Philips IC-CAD environment. An overview of the most important design tools and their version is given in Table 1. Circuit schematics and synthesized gate-level netlists have been obtained using the Cadence Framework. Transistor-level circuit simulations have been performed using the in-house PSTAR circuit simulator using Mos-Model 11 (MM11) transistor models.

<table>
<thead>
<tr>
<th>Tool</th>
<th>Version</th>
</tr>
</thead>
<tbody>
<tr>
<td>QDF</td>
<td>3.2</td>
</tr>
<tr>
<td>Cadence_assura</td>
<td>3.0.446.4</td>
</tr>
<tr>
<td>Cadence_ic</td>
<td>5.0.33.500.0.6</td>
</tr>
<tr>
<td>Cadence_philips</td>
<td>2003.2</td>
</tr>
<tr>
<td>Cadence_sedsm</td>
<td>05.40-S130</td>
</tr>
<tr>
<td>PSTAR</td>
<td>01.03.00</td>
</tr>
<tr>
<td>PSstar</td>
<td>4.6</td>
</tr>
<tr>
<td>SimKit</td>
<td>1.1.1.4.4.6</td>
</tr>
</tbody>
</table>

The tools and libraries are part of the design flow developed for Philips' 0.13µm CMOS technology (CMOS12). The nominal supply voltage for this technology is 1.2 volts. CMOS12 is a general purpose process containing six metal interconnect layers. An overview of the used libraries is given in Table 2.

<table>
<thead>
<tr>
<th>Library</th>
<th>Version</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCCL013HGPTP</td>
<td>2.1.1</td>
</tr>
<tr>
<td>Pccmos12corelib</td>
<td>2.1.1</td>
</tr>
</tbody>
</table>

The PCCL013HGPTP package includes the technology related data such as e.g. device models and CAD support for layout design and extraction. The Pccmos12corelib package contains the standard cell libraries and the related characterization files.

7.2 System specification

The proposed power supply control scheme has been implemented according the specifications that are shown in Table 3. The counter of the µ-supply sensor is 9-bit wide (up to 512 counts) due to the maximum clock frequency of 500 MHz and a count frequency, fc, of 1 MHz. There are five major frequencies with a value of 500 MHz, 400 MHz, 300 MHz, 200 MHz and 100 MHz respectively. As a result, there are five entries in the island look-up-table. To obtain the required
frequency resolution, there are 25 minor frequencies per major frequency step. The \( \mu \)-counter and the \( \Omega \)-counter of the \( \mu \)-supply controller are 3-bits and 5-bit wide respectively. In total there are 100 minor frequencies available. The \( \mu \)-supply power actuator contains 4 segment decoders and 100 header and footer transistor segments.

Table 3 System requirements of the proposed power supply control scheme.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of flip-flops/logic gates</td>
<td>1K/24K</td>
</tr>
<tr>
<td>Estimated IP area (no power switches included)</td>
<td>0.36mm²</td>
</tr>
<tr>
<td>IP operating frequency range ( f_{ck} )</td>
<td>100-500 MHz</td>
</tr>
<tr>
<td>IP data activity range ( a )</td>
<td>0-0.5</td>
</tr>
<tr>
<td>Equivalent circuit resistance range ( a=0 )</td>
<td>19.95 ( \Omega )</td>
</tr>
<tr>
<td>Equivalent circuit resistance range ( a=0.5 )</td>
<td>2-10 ( \Omega )</td>
</tr>
<tr>
<td>Frequency resolution ( \Delta f_{minor} )</td>
<td>4 MHz</td>
</tr>
<tr>
<td>Number of major frequencies ( K )</td>
<td>5</td>
</tr>
<tr>
<td>Number of activity steps over full ( f_{ck}, a )  range ( M )</td>
<td>25</td>
</tr>
</tbody>
</table>

The delay line of the \( \sigma \)-supply sensor represents the critical path of the circuit. It can be implemented using the ring-oscillator instance of the CGU. The up/down counter of the \( \sigma \)-supply controller is 5-bit wide (up to 32 counts) as a result of the 25 activity steps. The \( \sigma \)-supply power actuator contains 25 header and footer transistor segments.

### 7.3 The \( \mu \)-supply control logic

#### 7.3.1 \( \mu \)-supply sensor

The \( \mu \)-supply sensor converts the CGU clock frequency into a digital representation. The flow diagrams of this module can be found in appendix A. After logic synthesis, the following results have been obtained for the module on cell count and area:

Table 4 Cell count and area results of the \( \mu \)-supply sensor.

<table>
<thead>
<tr>
<th></th>
<th>Cell count</th>
<th>Area in [( \mu m^2 )]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Combinatorial instances</td>
<td>96</td>
<td>764.52</td>
</tr>
<tr>
<td>Noncombinatorial instances</td>
<td>31</td>
<td>1135.68</td>
</tr>
<tr>
<td>Total instances</td>
<td>127</td>
<td>1900.20</td>
</tr>
</tbody>
</table>

Figure 37 shows the simulations results of the module as obtained by logic simulation. The module contains three input signals (reset, slowck, and \( ck \)) and a 9-bit wide output bus (measent). The signal start and cnt are internal signals.

![Figure 37](image_url)

Figure 37 \( \mu \)-supply sensor simulation results.

The number of clock pulses found at input \( ck \) are counted during the clock period of slowck (~1\( \mu \)s). The counting is started at the rising edge of slowck, which is indicated by the start signal.
The output \textit{meascnt} is updated every rising edge of \textit{slowck}. A clock frequency of 100MHz has been used for \textit{ck}, and 1MHz for \textit{slowck} in this simulation. Therefore, \textit{meascnt} should be equal to 100 after counting pulses for a whole clock period of \textit{slowck}, which can be observed at a time of \textasciitilde1500\text{ns}.

### 7.3.2 The island look-up table

Reference performance values, i.e. the digital representation of the \textit{major} frequencies, are stored in the island look-up table. A LUT contains a number of memory elements, which can be anything ranging from basic flip-flops to fully-custom designed cells. In this implementation, a LUT is required that contains 5 words each of 9-bits wide. The following results are obtained when using flip-flops for the LUT without any encoding scheme:

<table>
<thead>
<tr>
<th>Table 5 Cell count and area results for the memory part of a flip-flop based LUT.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Noncombinatorial instances</td>
</tr>
<tr>
<td>----------------------------</td>
</tr>
<tr>
<td></td>
</tr>
</tbody>
</table>

Please note that the figures presented in the previous table are estimated worst-case figures for the LUT memory portion. The LUT area can be compressed by using fully-custom designed memory cells and by means of data-compression (e.g. by storing difference values). Furthermore, the LUT control logic has not been taken into account in the presented cell count and area figure.

### 7.3.3 \textit{\mu}-supply controller

The \textit{\mu}-supply controller sets required binary-coded control signals to properly bias the circuit-under-control as explained in section 5.4. The corresponding flow diagrams can be found in appendix B. Table 6 shows the results on cell count and area after logic synthesis.

<table>
<thead>
<tr>
<th>Table 6 Cell count and area results for the \textit{\mu}-supply controller.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Combinatorial instances</td>
</tr>
<tr>
<td>--------------------------</td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td>Noncombinatorial instances</td>
</tr>
<tr>
<td>Total instances</td>
</tr>
</tbody>
</table>

Figure 38, Figure 39, and Figure 40 show the \textit{\mu}-supply controller simulation results as obtained by logic simulation. The module contains seven input signals (\textit{reset, slowck, ck, refcntID, chfreq, refcnt, meascnt}) and four output signals (\textit{ucntr, ocntr, FreqError, FreqReady}). All other signals are internal signals. The \textit{refcntID} (e.g. LUT index value of \textit{refcnt}) and \textit{chfreq} signals enable setting a new performance through open-loop control. The 9-bit wide \textit{refcnt} and \textit{meascnt} signals are provided by the LUT and \textit{\mu}-supply sensor respectively. The 3-bit \textit{ucntr} and 5-bit \textit{ocntr} outputs represent binary-coded control signals that are provided to the transistor segments of the power supply actuator. In this implementation, the \textit{ucntr} can have a value in the range of 1 and 5, while the \textit{ocntr} can have a value in the range of 0 and 24. An overflow (underflow) of \textit{ocntr} will increase (decrease) the value of \textit{ucntr}. Basically, higher count values mean that the power supply actuator is less resistive, resulting in a higher effective supply voltage of the circuit.
Figure 38 Controlling from a operating frequency of 100MHz to a desired frequency of 200MHz.

Figure 38 shows an example when the circuit operates at a clock of 100MHz (measent@1500ns). A new reference performance is set by providing a refentID value followed by a request signal chfreq. The refentID corresponds to a reference performance value, e.g. refentID=2 corresponds to refcnt =200. As a result, the reference performance is set to 200MHz (refent@1500ns) and an acknowledge can be found at FreqReady. Now, the control procedure starts as explained in section 5.4. The error count nerr equals 100, which represents refent-measent. The shifted error count nerr_s equals a value of 25 (e.g. here nerr/4). The ocntr is updated by this value. Since this counter can only contain values in the range of 0 and 24, an overflow occurs which increments the ucntr (=refentID+1). As a result, the ucntr value becomes 3, while the value of ocntr remains zero. In the third clock cycle of slowck (~2500ns), a clock frequency of 175MHz has been measured. Nerr equals 100 (200-175) and nerr_s becomes 6 (integer of 100/4). The ocntr is updated by a value of 6, while the ucntr will remain at a value of 3. In the fourth clock cycle of slowck (~3500ns), a clock frequency of 190MHz has been measured. Nerr equals 10 (200-190) and nerr_s becomes 2 (integer of 10/4). The ocntr becomes equal to a value of 8 and the ucntr will remain at a value of 3. In the fifth cycle of slowck the desired operating of 200MHz has been reached, because refent equals measent. Therefore, the ucntr and ocntr will remain at their values.

Figure 39 Controlling from a operating frequency of 300MHz to a desired frequency of 200MHz.

Figure 39 shows an example when the circuit operates at a clock of 400MHz (measent@1500ns). The new reference performance is set to 300MHz (refent@1500ns) by providing a refentID value of 3 and raising the request signal chfreq. Nerr becomes equal to -100 (here represented by an unsigned decimal value of 412) and nerr_s becomes equal to -25. The ocntr is updated by this value, resulting in an underflow that decrements the ucntr (=refentID-1). As a result, the ucntr
value becomes equal to 2, while the value of \( ocntr \) remains zero. In the third clock cycle of \( slowck \) (~2500ns), a clock frequency of 325MHz has been measured. \( Nerr \) becomes equal to a value of -25 (300-325) and \( nerr_s \) becomes -7 (integer of -25/4). The \( ocntr \) is updated by a value of -7 (\( ocntr=18 \)), and the \( ucntr \) will decrease to a value of 1. In the fourth clock cycle of \( slowck \) (~3500ns), a clock frequency of 310MHz has been measured. \( Nerr \) equals -10 (300-310) and \( nerr_s \) becomes -32 (integer of -10/4). The \( ocntr \) becomes equal to a value of 15 and the \( ucntr \) will remain at a value of 1. In the fifth cycle of \( slowck \) the desired operating of 300MHz has been reached, because \( refcnt \) equals \( meascnt \) and the \( ucntr \) and \( ocntr \) remain at their values.

**Figure 40** Simulated saturation condition at the \( ucntr \) and \( ocntr \).

Figure 40 shows a special condition where saturation occurs of the \( ucntr \) and \( ocntr \) counters. The circuit operates at a clock frequency of 400MHz and a new reference performance of 200MHz is set. The \( ucntr \) and \( ocntr \) become zero, e.g. saturation occurs, and the \( FreqError \) signal becomes active every clock cycle of the \( slowck \).

### 7.3.4 µ-supply segment decoder

The µ-supply segment decoder sets the required control signals at the transistor segments of the power supply actuator as explained in section 5.2.2. Table 6 shows the results on cell count and area after logic synthesis.

**Table 7** Cell count and area results for the µ-supply segment decoder.

<table>
<thead>
<tr>
<th></th>
<th>Cell count</th>
<th>Area in [( \mu m^2 )]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Combinatorial instances</td>
<td>80</td>
<td>566.83</td>
</tr>
<tr>
<td>Noncombinatorial instances</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Total instances</td>
<td>80</td>
<td>566.83</td>
</tr>
</tbody>
</table>

Figure 41 and Figure 42 show simulation results of the µ-supply segment decoder as obtained by logic simulation. The module contains five inputs (\( bypass, standby, addressID, address, control \)) and two outputs (\( petri, nctrl \)). \( Bypass \) sets all transistor segments of the actuator to be conducting, while the \( standby \) sets all transistor segments to be non-conducting. The 3-bit wide \( addressID \) specifies the segment range (see section 5.2.2) and its value is unique for each segment decoder. The 3-bit \( address \) and the 5-bit \( control \) are the values of \( ucntr \) and \( ocntr \) respectively as they are provided by the µ-supply controller. The 25-bit outputs \( petri \) and \( nctrl \) are the control signals that are provided to the PMOS header and NMOS footer transistor segments respectively. Basically, \( petri \) and \( nctrl \) are complementary signals.
Figure 41 Simulated results on a segment decoder for a selected segment range.

Figure 41 shows an example of a segment decoder for a selected segment range. The segment range is selected when addressID and address are equal. Priorities have been set for the remaining input for the case that they become active at the same time. The priority of bypass is set to be highest, standby has a medium priority, and the lowest priority is set to control. When bypass is at high-level, all bits of pctrl are set to 0 and all bits of nctrl are set to 1, which results that, all transistor segments of the actuator are conducting. When standby is at high-level and bypass is at low-level, all bits of pctrl are set to 1 and all bits of nctrl are set to 0, which results that all transistor segments are non-conducting. The value of control is decoded and propagated to the outputs in case both bypass and standby are inactive, i.e. at low-level.

Figure 42 Simulated results on a segment decoder for a non-selected segment range.

Figure 42 shows an example of a segment decoder for a non-selected segment range, i.e. when addressID and address are not equal. In this case, the output values of pctrl and nctrl are not dependent on control anymore, but are dependent on the remaining inputs as explained earlier. The only difference can be found by the fact that the value of address impacts the output values in case bypass and standby are not active. If address<addressID, all bits of pctrl are set to 0 and all bits of nctrl are set to 1 which results that all transistor segments of this particular segment range are conducting. If address>addressID, all bits of pctrl are set to 1 and all bits of nctrl are set to 0 which results that all transistor segments of this particular segment range are conducting.

7.3.5 Complete µ-supply control logic

The µ-supply control has been build in behavioural VHDL code and it consists of the sensor, the controller and four segment decoders. After logic synthesis, the following results has been obtained for the module on cell count and area:

<table>
<thead>
<tr>
<th>Combination instances</th>
<th>Cell count</th>
<th>Area in [\mu m^2]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Combinatorial instances</td>
<td>729</td>
<td>5991.07</td>
</tr>
<tr>
<td>Noncombinatorial instances</td>
<td>96</td>
<td>3570.44</td>
</tr>
<tr>
<td>Total instances</td>
<td>825</td>
<td>9561.51</td>
</tr>
</tbody>
</table>

Table 8 Cell count and area results of the µ-supply control logic excluding the LUT.

Please note that in the previous table, the cell count and area figures of the LUT have not been taken into account. Figure 43 shows the area comparison of the individual components of the µ-
supply control logic. Here, the area of the total μ-supply control logic includes the LUT area, which results in a value of $10832.35\mu\text{m}^2$. In this figure it can be noticed that the area of the μ-supply control logic is dominated by the area of the controller.

![Figure 43 Area comparison of the different components in the μ-supply control logic.](image)

The μ-supply control loop has been verified as well by means of circuit simulation. A stripped version of the loop has been used to reduce simulation time. This stripped version contains the μ-supply sensor, controller and one segment decoder. The transistor segment sizes have been calculated using expression (23). The circuit-under-control is implemented by a CGU and an IP core. The CGU generates an operating frequency of about 220MHz at nominal supply. The IP core contains a total circuit capacitance of 2nF, a circuit activity of 0.3, and an additional decoupling capacitance of 6nF.

![Figure 44 Circuit simulation results of the μ-supply control loop for the case that the operating clock is lowered from 200MHz to 100MHz.](image)

Figure 44 shows the simulations results for the μ-supply control loop when the operating clock frequency (CK) is lowered from a value of 200MHz to 100MHz by means of supply voltage.
scaling. In this simulation, a count frequency (SLOWCK) of 5MHz has been used. From this example, it can be observed that the μ-supply control loop reducing supply voltage to just meet the required performance of 100MHz.

7.4 The σ-supply control logic

7.4.1 σ-supply sensor

The σ-supply sensor consists of a delay line and a phase-detector as has been explained in section 6.3. Its purpose is to translate phase difference between the clock edge and its delayed version into control signals for the σ-supply controller. The delay line models the critical path delay of the circuit-under-control, and therefore, its delay and size depends on the circuit. The results of the delay line presented in the next table are based on the circuit of which the characteristics are presented in section 7.2.

<table>
<thead>
<tr>
<th></th>
<th>Cell count</th>
<th>Area in [μm²]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Delay line</td>
<td>74</td>
<td>600</td>
</tr>
<tr>
<td>Phase detector</td>
<td>15</td>
<td>103</td>
</tr>
<tr>
<td>Total instances</td>
<td>89</td>
<td>703</td>
</tr>
</tbody>
</table>

The input of the σ-supply sensor is the CGU clock, and the outputs are the UP, Just, and DN signals. The delay line must be powered off the same power supply as the circuit-under-control.

Figure 45 shows the phase detector output signals as function of the phase difference between a CGU clock edge and its delayed version. This comparison is done every clock cycle. When the delay is less than one clock cycle, the DN signal becomes active. When the delay is more than a clock cycle, the UP signal becomes active. The Just signal becomes active for small phase differences (within ~10ps) between the clock edge and delayed clock edge. In case the Just signal window of ±10ps is too small, the phase detector circuit can be adapted to increase the window size as is shown in [10].

Figure 45 σ-supply sensor outputs as function of phase difference between clock and delayed clock.
7.4.2 $\sigma$-supply controller

The $\sigma$-supply controller sets required binary-coded control signals to properly bias the circuit-under-control to compensate for activity changes as explained in section 6.4. Table 10 shows the results on cell count and area after logic synthesis.

Table 10 Cell count and area results for the $\sigma$-supply controller.

<table>
<thead>
<tr>
<th></th>
<th>Cell count</th>
<th>Area in [(\mu m^2])</th>
</tr>
</thead>
<tbody>
<tr>
<td>Combinatorial instances</td>
<td>58</td>
<td>480.09</td>
</tr>
<tr>
<td>Noncombinatorial instances</td>
<td>16</td>
<td>589.02</td>
</tr>
<tr>
<td>Total instances</td>
<td>74</td>
<td>1069.12</td>
</tr>
</tbody>
</table>

Figure 46 shows the simulation results of the $\sigma$-supply controller as obtained by logic simulation. The module has five inputs (reset, ck, up, just, dn) and one output (ctrl). The 5-bit wide ctrl signal represents the binary-coded control signals that are provided to the $\sigma$-supply transistor segments of the power supply actuator.

Figure 47 shows an example of the operation of the $\sigma$-supply controller when the UP signal is active. The UP input signal indicates that the effective supply voltage should be increased. As a result, the counter value starts decreasing and turning on more transistor segments to increase the supply voltage.

Figure 48 shows an example of the $\sigma$-supply controller when the Just signal is active.
Figure 48 shows an example of the σ-supply controller when the Just signal is active. The Just signal indicates that the required supply voltage has been reached. For an active Just signal, the counter remains at its count value.

7.4.3 σ-supply segment decoder

The σ-supply segment decoder sets the required control signals at the transistor segments of the power supply actuator as explained in section 6.2.2. Table 11 shows the results on cell count and area after logic synthesis.

<table>
<thead>
<tr>
<th></th>
<th>Cell count</th>
<th>Area in [μm²]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Combinatorial instances</td>
<td>71</td>
<td>496.23</td>
</tr>
<tr>
<td>Noncombinatorial instances</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Total instances</td>
<td>71</td>
<td>496.23</td>
</tr>
</tbody>
</table>

Figure 49 shows simulation results of the σ-supply segment decoder as obtained by logic simulation. The module contains three inputs (bypass, standby, control) and two outputs (pctrl, nctrl). Bypass sets all transistor segments of the actuator to be conducting, while the standby sets all transistor segments to be non-conducting. The 5-bit control are the values of ctrl as they are provided by the σ-supply controller. The 25-bit outputs pctrl and nctrl are the control signals that are provided to the PMOS header and NMOS footer transistor segments respectively. Basically, pctrl and nctrl are complementary signals.

Figure 49 Simulated results on a σ-supply segment decoder.

Figure 49 shows simulation results of a σ-supply segment decoder. Priorities have been set for the remaining input for the case that they become active at the same time. The priority of bypass is set to be highest, standby has a medium priority, and the lowest priority is set to control. When bypass is at high-level, all bits of pctrl are set to 0 and all bits of nctrl are set to 1, which results that all transistor segments of the actuator are conducting. When standby is at high-level and bypass is at low-level, all bits of pctrl are set to 1 and all bits of nctrl are set to 0, which results that all transistor segments are non-conducting. The value of control is decoded and propagated to the outputs in case both bypass and standby are inactive, i.e. at low-level.

7.4.4 Complete σ-supply control logic

The σ-supply control has been build partly on the level of circuit schematics and partly in behav­ioural VHDL code. It consists of the sensor, the controller and a segment decoder. The following results have been obtained for the module on cell count and area:
Table 12 Cell count and area results of the \( \sigma \)-supply control logic.

<table>
<thead>
<tr>
<th></th>
<th>Cell count</th>
<th>Area in [( \mu \text{m}^2 )]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Combinatorial instances</td>
<td>218</td>
<td>1679.31</td>
</tr>
<tr>
<td>Noncombinatorial instances</td>
<td>16</td>
<td>589.02</td>
</tr>
<tr>
<td>Total instances</td>
<td>234</td>
<td>2268.33</td>
</tr>
</tbody>
</table>

Figure 43 shows the area comparison of the individual components of the \( \sigma \)-supply control logic. In this figure it can be noticed that the largest part of \( \sigma \)-supply control logic area is consumed by the controller.

![Figure 43 Area comparison of the individual components of the \( \sigma \)-supply control logic.](image)

The \( \sigma \)-supply control loop has been simulated by means of circuit simulation. The circuit-under-control is implemented by an IP core, which contains a total circuit capacitance of 2\( \text{nF} \), a circuit activity of 0.3, and an additional decoupling capacitance of 6\( \text{nF} \).

![Figure 50 Area comparison of the different components in the \( \sigma \)-supply control logic.](image)

![Figure 51 Circuit simulation results of the \( \sigma \)-supply control loop demonstrating tracking of the operating frequency by supply voltage control.](image)
Figure 51 shows the simulations results for the \( \sigma \)-supply control loop demonstrating the tracking of the operating clock by means of supply voltage scaling. When the Just signal becomes active, the desired supply voltage \((VDDC)\) has been reached such that the reference and delayed clock \((fCK)\) are synchronized.

### 7.5 Area estimation of the complete power supply control loop

The area of the complete power supply control loop has been estimated. The following results have been obtained on cell count and area:

<table>
<thead>
<tr>
<th></th>
<th>Cell count</th>
<th>Area in [(\mu m^2)]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Combinatorial instances</td>
<td>947</td>
<td>7670.63</td>
</tr>
<tr>
<td>Non-combinatorial instances</td>
<td>157</td>
<td>5430.30</td>
</tr>
<tr>
<td>Transistor segments</td>
<td>854.65</td>
<td></td>
</tr>
<tr>
<td>Total instances</td>
<td>1104</td>
<td>98565.68</td>
</tr>
</tbody>
</table>

Table 14 Cell count and estimated area results of the power supply control loop.

<table>
<thead>
<tr>
<th></th>
<th>Cell count</th>
<th>Area in [(\mu m^2)]</th>
</tr>
</thead>
<tbody>
<tr>
<td>(\mu)-supply control loop</td>
<td>870</td>
<td>10832.35</td>
</tr>
<tr>
<td>(\sigma)-supply control loop</td>
<td>234</td>
<td>2268.33</td>
</tr>
<tr>
<td>(\mu)-supply transistor segments</td>
<td>---</td>
<td>18082.0</td>
</tr>
<tr>
<td>(\sigma)-supply transistor segments</td>
<td>---</td>
<td>67383.0</td>
</tr>
<tr>
<td>Total power supply control loop</td>
<td>1104</td>
<td>98565.68</td>
</tr>
</tbody>
</table>

The area of the power supply control logic is taken from the synthesis results as presented in the previous sections. These results exclude the area consumed by the segmented transistors. The transistor segment size has been determined for the system as specified in section 7.2. The transistor segments are of the high-\(V_t\) type with a maximum transistor width of 10\(\mu m\) and a minimum channel length of 0.13\(\mu m\). The size of the \(\mu\)-supply transistor segments has been determined using expression (23). The segment sizing is done such that the voltage drop across the segments has a maximum value of 2.5\% of the nominal power supply voltage when all segments are turned-on. The \(\sigma\)-supply transistor segments has been determined using expression (36). The area results of the transistor segments include the drain-source junction areas and a double-sided poly-gate contact.

Figure 52 shows the relative area of the complete power supply control loop as normalised to its total estimated area value. From this figure it can be noticed that about 2/5 of the area (~41\%) is consumed by non-combinatorial instances, e.g. the LUT, registers, counters, etc. There is a balance between the use of non-combinatorial and combinatorial instances. Furthermore, it can be observed that the segmented transistors consume up to 87\% of the total control loop area. The \(\mu\)-supply controller consumes about 11\% of the total control loop area. In absolute numbers, the power supply control loop has been estimated to consume about 0.1 \(mm^2\) of silicon area of which ~0.0131 \(mm^2\) is consumed by the control logic.

For the small logic-dominated IP core as specified in section 7.2, the control loop increases the IP area by 28\% of which about 4\% is due to the control logic. The large area increase in mainly due to the segmented transistors of the \(\sigma\)-supply control loop. However, please note that this represents a worst-case area estimation, because it is done on cell area only. A layout implementation.
is required to obtain accurate area results that include the impact of parameters such as row utilization, power routing, clock distribution, I/O cells, bondpads, etc. As an example, the largest area consumer of the control loop is the power supply actuator. If the power supply actuator can be placed just beneath the IP power rings, it will not increase the IP area. Therefore, the area results presented in this section can only be used as an worst-case estimate.

![Figure 52 Relative area estimate of the complete control loop.](image)

- Left: Relative area estimate of the control logic as function of instance type.
- Right: Relative area estimate as function of the control loop components.

When using an external DC/DC converter to control the power supply of such small IP core, the overhead would be even larger as the one of the proposed solution. Therefore, work has to be performed to determine the optimal size of an island as well as the number of islands to be power supply controlled. The trade-offs between island size, the number of islands and area of the proposed solution should further investigated.
8 Conclusions

The problem of performing adaptive control of the power supply for island-based System-on-Chip type of applications has been investigated. An on-chip fully-digital solution has been provided that enables adaptive performance control for each individual island while maintaining system performance requirements. It is driven by performance requirements as provided by a performance scheduler, e.g. a PMU or directed through software.

The proposed solution consists of two independent negative feedback control loops. New performance request are handled in an open-loop control. Feedback control enables compensation of global process variations, temperature drifts and changes in the circuit activity. The behaviour of the loop control has been analysed and the proof of loop stability has been provided.

Analytical circuit models have been developed on power consumption, energy per operation, power conversion efficiency and transient response when using the proposed solution. Furthermore, area consumption of the solution has been estimated and simulation results have been provided.

In contrast to prior art, a fully-integrated fully-digital solution has been provided. This offers the advantage that no external components are needed for the power conversion, which is cheaper with respect to system integration. Next to that, the digital nature makes the solution more robust against digital supply noise, it avoids static biasing currents, and it is easily portable to next process generations as compared to analog counterparts. The proposed solution is especially useful in those applications where the IC is subdivided into various functional regions. The solution enables local performance optimisation of the IC and offers an integrated standby (or inactive) mode for each region. Another advantage over prior art is the fact that the IC's global power distribution network is not affected, which simplifies chip implementation significantly. The proposed solution offers fast dynamic response, i.e. low transition times, at the cost of reduced power conversion efficiency as compared to off-chip DC/DC conversion.

8.1 Consequences for the design

If the solution is used it has several consequences for the design of an island-based SoC. The consequences that are known at this point of the research are:

- Before the SoC can be operational, a calibration period is required to store the design-time performance values in the look-up-table of the solution.

- A performance scheduler is required to provide a reference performance to the solution. This performance scheduler can be implemented by e.g. a power management unit or in software. The reference performance should set the mode of operation (i.e. active or standby mode) and a required frequency of operation.

- For each island, the solution requires a circuit that models the critical path delay of the circuit-under-control. This circuit should be implemented as part of the solution.

- A low-frequency reference clock of 1MHz needs to be provided to the solution. This clock signal should be generated by an off-chip reference oscillator, i.e. a crystal oscillator.
• Level converters are required at the island boundary to avoid short-circuit currents.

• The size of the segmented transistors of the power supply actuator should be re-calculated for every different circuit-under-control.

8.2 Future work

More work can be done in improving the current solution and investigating its impact at system level. The following future work can be considered:

• Investigating the system level aspects of the solution. The question that should be addressed is how to implement the performance handling in case of a single or multiple islands. Related work would be the interfacing to the look-up table.

• Adding structural and functional test to the solution.

• Investigate the trade-offs between the application of on-chip linear DC/DC converters and off-chip switching DC/DC converters as function of the number of islands to be adaptively power supply controlled.

• Investigate the optimum size of an island and the number of islands that need to be power supply controlled.
References

Modelling Charge-Pump Delay Locked Loops

A dynamic voltage scaled microprocessor system.

Energy-efficient processor system design
University of California, Berkeley, 2001
Ph.D. dissertation

A completely on-chip voltage regulation technique for low power digital circuits.

[5] Chapiro, D.
Globally-Asynchronous Locally-Synchronous Systems.
Stanford University, Oct. 1984
Ph.D. dissertation

An adaptive on-chip voltage regulation technique for low-power applications.

Feedback Control of Dynamic Systems

[8] Gutnik, V. and A. Chandrakasan
An efficient controller for variable supply-voltage low power processing.
In: Symposium on VLSI Circuits, Digest of Technical Papers, June 1996, p. 158-159

z-Domain Model for Discrete-Time PLLs.
A 1 GHz Single-Issue 64b PowerPC Processor

A 2 V clock synchronizer using digital delay-locked loop.
In: Proc. of IEEE Asia Pacific Conference, Cheju, South Korea, 28-30 Aug. 2000, p. 91-94

Variable supply-voltage scheme for low-power high-speed CMOS digital design.

Managing power and performance for system-on-chip designs using Voltage Islands.

A voltage reduction technique for digital systems.

Adaptive Voltage Scaling Circuit Implementations and Islands-of-Voltage for System-on-Chip applications; Literature search.

Technology Exploration for Adaptive Power and Frequency Scaling in 90nm CMOS.

[17] Nowack, E.
Maintaining the Benefits of CMOS scaling when Scaling Bogs down.

[18] Nielsen, L., C. Niessen, J. Sparso and K. van Berkel
Low-power operation using self-timed circuits and adaptive scaling of the supply voltage.

Leakage current mechanisms and leakage reduction techniques in deep-submicrometer CMOS circuits.

[20] Sakurai, T.
A Simple MOSFET Model for Circuit Analysis.

© Koninklijke Philips Electronics N.V. 2004
[21] Sonh, S., I. Yang, J. Lee and M. Lee
ASIC Design of a Microcontroller with Power Management Unit

[22] Stratakos, A., S. Sanders and R. Brodersen
A low-voltage CMOS DC-DC converter for a portable battery-operated system.

[23] Veendrick, H.
Short-circuit dissipation of static CMOS circuitry and its impact on the design of buffer circuits.

A low power switching power supply for self-clocked systems.

[25] Zhang, H. and J. Rabaey
Low-swing interconnect interface circuits.

© Koninklijke Philips Electronics N.V. 2004
A Flow diagrams of the $\mu$-supply sensor

Three processes can be identified in the behavioural description of the $\mu$-supply sensor: (i) main, (ii) update count and (iii) restart count. The purpose of the main process is to update the sensor output ($\text{meascnt}$) with the value of the internal counter ($\text{CNT}$). Next to that, it increases the internal counter every CGU clock cycle ($\text{CLK}$) in cooperation with the update count process. The purpose of the restart count process is to send a trigger signal every rising edge of the count frequency to restart the counting process. Figure 53, Figure 54 and Figure 55 show the flow diagrams of the main, update count and restart count process respectively.

Figure 53 Main process of the $\mu$-supply sensor.

Figure 54 Update count process of the $\mu$-supply sensor.
Figure 55 Restart count process of the $\mu$-supply sensor.
B Flow diagrams of the \( \mu \)-supply controller

Three processes can be identified in the behavioural description of the \( \mu \)-supply controller: (i) \( \mu \)-count, (ii) O-count and (iii) restart count. The main purpose of the \( \mu \)-count process is to update the internal \( \mu \)-counter (UCNT) as a result of an open-loop frequency change (chfreq and refcntid signals) or as indicated by the O-count process (overflow and underflow signals) in case of a closed-loop operation. The main purpose of the O-count process is to update the internal o-counter (OCNT) in closed-loop operation. The restarted process determines the error count (NERR) and it implements the shifted value (NERR_S). Both process are operating at the CGU clock frequency. The restart count process relates the start of the \( \mu \)-count and O-count process to the count frequency. Figure 56, Figure 57 and Figure 58 show the flow diagrams of the \( \mu \)-count, O-count and restart count process respectively.

![Flow diagram of \( \mu \)-count process](image)

Figure 56 \( \mu \)-count process of the \( \mu \)-supply controller.
Figure 57 O-count process of the µ-supply controller.
Figure 58 Restart count process of the μ-supply controller.