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Coach: Prof.dr.ir. R.J. van de Plassche

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Distortion Analysis of Differential Amplifiers

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Abstract

In an attempt to create a digital receiver it became clear that an analog frontend was necessary. This analog frontend should condition the antenna signal so that an AD converter can be fed. A final part in this analog frontend is an amplifier that amplifies the signal's amplitude to a level close to the full scale of the AD converter.

The specification for the analog frontend, and thus the fixed gain amplifier, are mainly determined by the choice of the analog to digital converter. A ten bits AD converter implies a signal to noise ratio of -62 dB.

Several principles of differential amplifiers implemented using bipolar transistors are discussed.

In the first part the circuits are discussed theoretically. Here equations for the gain and the level of third order harmonic distortion are derived.

In the second part a comparison of the theoretical behaviour with the results from computer simulation is made. The simulation results show that the theoretical analysis can be used to do coarse calculations of the circuit, provided that all boundary conditions are met. Using the simulation results the circuits can be adjusted to maximum performance.

A simple differential pair amplifier proved to get the best gain-distortion ratio, but lacked a low output impedance. Buffering a simple differential pair amplifier with two emitter followers caused the gain to decrease.

The transresistance amplifier caused as much third order distortion as was gained by the increment of voltage space. At higher output signal amplitudes the transresistance amplifier seemed to get a better result.

For the desired output signal amplitude of 1 Volt a distortion level of -65 dB is the best result realized. While for a distortion level of -80 dB an output signal amplitude of only 450 milliVolt could be achieved. Overall can be concluded that the level of third order harmonic distortion is mainly dependent on the amplitude of the output signal.
1 Introduction

Over the last years the application of digital techniques has made enormous steps forward. Even in traditionally analog systems digital components marched in. The main advantages of this takeover are increasing performance and a simple means of implementing new features. The increase in performance is a direct result of the lack of loss of performance throughout the digital system. This is caused by the discrete levels which are maintained throughout the system. The variation of the signal, in well designed digital systems, never results in a wrong level. New features can easily be implemented because calculation with digital data can be done very fast and this area of research is widely covered.

One of these traditional analog fields is the world of wireless communication. Digitalization of the equipment in this field of research is still minimal. The receivers that are used nowadays are still mainly analog. To completely digitalize this area is not possible with today's analog to digital converters. The reasons for this are the high frequencies and the low amplitudes of the antenna signal. These restrictions show the necessity of an analog frontend. The demands imposed upon the analog system are mainly determined by the specifications of the AD converter. A basic architecture of a receiver is shown in figure 1.1.

![Basic digital receiver architecture.](image)

The main task of the analog frontend is to clean up the antenna signal to a level desired by the analog to digital converter. This cleanup mainly consists of filtering, mixing, amplification and dynamic compression of the antenna signal. The filtering limits the spectrum of the incoming signal decreasing the noise power. The mixing lowers the frequency of the desired signal to a frequency that can be handled by the AD converter. Amplification and dynamic compression of the signal should stabilize the output signal amplitude to a level close to the dynamic range of the AD converter. This takes full advantage of the AD converter's resolution, and thus results in the best performance of the system.
Introduction

A schematic view of the analog frontend is presented in figure 1.2. In this figure AGC stands for 'automatic gain control' meaning that the gain of these amplifiers is controllable. These AGC's are used for the dynamic compression of the signal.

The RF-AGC amplifies the desired signal to a minimum required level. This RF-AGC also performs some filtering, thus limiting the signal power of the signal passed to the mixer. The mixer then reduces the signal's frequency to an intermediate frequency. The filter then limits the signal spectrum even more before passing it to the IF-AGC who amplifies the signal to a specified level. A fixed gain amplifier amplifies the IF-AGC signal to a level close to the full scale of the following AD converter.

To make full use of the dynamic range of the AD converter the specifications for the analog frontend are highly related to the resolution of the AD converter. For the AD converter a signal to quantization noise can be derived of:

\[ S/N = n \times 6.02 + 1.76\ dB \]  

(1.1)

Where n is the resolution of the AD converter in bits. This signal to noise level should not be tackled by the analog frontend. Therefore this value sets the minimum performance of the analog frontend with respect to noise ratio and distortion level.

In this report various solutions for the fixed gain amplifier are discussed with respect to their distortion performance.
2 Deriving The Specifications

In this section the specifications for the fixed gain amplifier will be derived. This is done with consideration of signal levels and frequencies at various points in the analog frontend. For this sake figure 1.2 is redrawn here with the various signals numbered. This eases reference to signals.

Figure 2.1 Analog frontend of a digital receiver

2.1 Signal levels

The incoming antenna signal level can vary due to external factors. These external factors can be weather influences, mobility of the receiver or interference of transmitters. The signal is assumed to vary from 1.5 microVolt to 190 milliVolt. The RF-AGC compresses this range from 34 microVolt to 190 milliVolt. The mixer has no influence on the signal level but the filter causes a loss. The IF-AGC amplifies the signal amplitude to a value of approximately 100 milliVolt. The AD converter that is used has a full scale range of 1 Volt. This implies a gain of 10 for the fixed gain amplifier. Further does the AD converter have a resolution of ten bits. This implies a signal to noise level of approximately -62 dB. With a safety margin this implies a maximum noise and distortion level of -80 dB. This margin also prevents crosstalk to neighbouring channels which have less signal power.
2 Deriving The Specifications

These ranges are plotted in figure 2.2. This figure gives an idea of how each block affects the

signal levels.

2.2 Signal frequencies

The bandwidth of the signal presented to each block is graphically shown in figure 2.3. The frequency on which the desired signal is modulated is shown with a solid line. The other frequencies that are present in the signals are shown with the gray area’s.
The frequencies that are picked up and passed through by the antenna vary from 47 Megahertz up to 855 Megahertz. The RF-AGC limits this band and the mixer lowers the frequencies to the intermediate frequency of approximately 40 Megahertz. The filter then narrows the band even more. The final channel selection is done in the digital part of the receiver.

From these considerations it can be concluded that the fixed gain amplifier is operated with signal frequencies of approximately 40 Megahertz.
3 Theory Of Operation

3.1 The Bipolar NPN Transistor

In any amplifying circuit there is a need for an active element. A basic active element is a transistor. In this study only bipolar NPN transistors are considered because of their better high speed performance.

In figure 3.1 the symbol for the bipolar NPN transistor is drawn together with its naming conventions. Also the definitions of voltage polarities and current directions are shown here.

![Figure 3.1 Bipolar NPN transistor model](image)

For calculations on the large signal behaviour with this bipolar NPN transistor the Ebers-Moll model is commonly used. This model is depicted in figure 3.2.

![Figure 3.2 Bipolar NPN Transistor Ebers-Moll model](image)

From this model some basic equations can be observed using Kirchhoff’s law.

\[ I_e = I_b + I_c \]  \hspace{1cm} (3.1)

\[ I_e = I_F - \alpha_R I_R \]  \hspace{1cm} (3.2)
The currents can be described by using the transfer functions of the diodes in the model. This results in:

$$I_C = \alpha_F I_F - I_R$$  \hspace{1cm} (3.3)

In these equations the thermal voltage is described with $V_t$. This voltage equals $kT/q$ and approximates 25.5 milliVolt at room temperature. The parameters $\alpha_F$ and $\alpha_R$ are device dependent and are related to the current gain of the transistor. The current gain can be described as:

$$\beta_F = \frac{I_C}{I_b}$$  \hspace{1cm} (3.6)

$$\beta_R = \frac{I_C}{I_b}$$  \hspace{1cm} (3.7)

Together with the basic equations the current gains can be expressed in $\alpha_F$ and $\alpha_R$ as:

$$\beta_F = \frac{\alpha_F}{1 - \alpha_F}$$  \hspace{1cm} (3.8)

$$\beta_R = \frac{\alpha_R}{1 - \alpha_R}$$  \hspace{1cm} (3.9)

As can be seen from the model it consists of two diodes. Therefore four modes of operation can be determined for this bipolar transistor. These modes are distinguished as the direction of biasing the two pn-junctions.

First mode is the active mode where the base-emitter junction is forward biased and the base collector junction is reverse biased. In this case the reverse currents can be neglected resulting in a simple set of equations describing the transistor. This is the most commonly used mode because in this region the transistor acts as an amplifying device.

The two modes in which both junctions are biased in the same direction the transistor can be used as a switch. If both junctions are forward biased the impedance is low and the transistor can be considered as a closed switch. When both junctions are reverse biased the impedance is high and the transistor acts as an open switch.

At last there is the reverse mode in which the base emitter junction is reverse biased and the base collector junction is forward biased. This mode corresponds to a transistor used in reverse. In this mode the gain of the device is consistently lower than in the active mode. This is a result of design properties that are not optimized for this mode of operation.

From the Ebers-Moll model we can derive the basic equations of the transistor, applicable to all four modes of operation.

$$I_e = I_{ce}(e^{V_t/V_T} - 1) - \alpha_F I_{ce}(e^{V_t/V_T} - 1)$$  \hspace{1cm} (3.10)
3 Theory Of Operation

Because here the transistors are only used as an amplifying device, we can simplify these equations. First the reverse currents are neglected. This is valid if the base collector junction is reverse biased. In the active mode the base emitter junction is forward biased so the leakage current can be neglected with respect to the collector current. With these simplifications we get:

\[ I_e = \alpha p I_e \left( e^{v_{bc}/\eta T} - 1 \right) - I_{ce} \left( e^{v_{be}/\eta T} - 1 \right) \]  \hspace{1cm} (3.11)

For the validity of these equation the following conditions are to be met:

\[ V_{bc} > 0 \]  \hspace{1cm} (3.14)

\[ V_{be} > 0.7 \text{Volt} \]  \hspace{1cm} (3.15)

These simple equations applicable to the active mode of the transistor are used in further calculations in this report.

3.2 The Differential Pair

Because the design has to meet the very low distortion specifications, a complete differential design is suggested. The benefit of a differential design is its symmetry. This symmetry cancels any even order terms and thus has no even order harmonic distortion. This implicates that the third order harmonic distortion will determine the quality of the design. The design will be concentrated on the reduction of this third order harmonic distortion.

Transfer equation

A basic building block of a differential system is a differential pair. A schematic view of a bipolar differential pair is shown in figure 3.3.

![Bipolar differential pair](image)
The differential pair basically acts as a current distributor. The currents flowing through the collector of the transistors is dependent on the voltage difference between the base contacts. If there is no voltage applied, that is $V_{ip} = V_{in}$, the currents that flow through the transistors will be equal. As $V_{ip}$ is increased and $V_{in}$ is decreased in the same way, $I_{c1}$ will increase and $I_{c2}$ will decrease in the same order.

Now the transfer function of the bipolar differential pair will be derived using the transistor design model equations (3.12) and (3.13) for the active mode as described in section 3.1

First the input and output signals are defined as:

$$V_{ip} = V_{cm} + V_i/2$$
$$V_{in} = V_{cm} - V_i/2$$

$$I_{c1} = \alpha_F I_{bias}^2 / 2 + I_o$$
$$I_{c2} = \alpha_F I_{bias}^2 / 2 - I_o$$

In these definitions the input voltages and output currents are split in their differential and quiescent terms. With equations (3.12) and (3.13) the collector currents can be related with the input voltages.

$$I_{c1} = \alpha_F I_{es} e^{(V_{o}-V_o)/V_T}$$
$$I_{c2} = \alpha_F I_{es} e^{(V_{o}-V_o)/V_T}$$

With the definitions in equation (3.16) the output current $I_o$ can be expressed as:

$$I_o = \frac{I_{c1} - I_{c2}}{2}$$

$$= \frac{I_{es}}{2} e^{(V_{o}-V_o)/V_T} e^{-(V_{o}-V_o)/V_T}$$

$$= \frac{I_{es}}{2} e^{(V_{cm}-V_o+V_i/2)/V_T} e^{-(V_{cm}-V_o-V_i/2)/V_T}$$

$$= \frac{I_{es}}{2} e^{(V_{cm}-V_o)/V_T} e^{V_i/2V_T} e^{-V_i/2V_T}$$

By considering the quiescent currents an expression for the first term can be found:

$$I_{bias} = \frac{I_{c1} + I_{c2}}{\alpha_F}$$

$$= \frac{I_{es}}{\alpha_F} e^{(V_{cm}-V_o)/V_T} e^{V_i/2V_T} e^{V_i/2V_T}$$

Rewriting this expression leads to:

$$\frac{I_{es}}{2} e^{(V_{cm}-V_o)/V_T} = \frac{\alpha_F I_{bias}}{2(e^{V_i/2V_T} + e^{V_i/2V_T})}$$
Substitution in equation (3.19) results in:

\[
I_o = \frac{\alpha_p I_{bias}}{2} \left( \frac{e^{V_i/2V_T} - e^{-V_i/2V_T}}{2(e^{V_i/2V_T} + e^{-V_i/2V_T})} \right)
\]

This results in the general transfer function of the bipolar differential pair. This transfer function is drawn in figure 3.4. From this transfer function can be concluded that the distortion is caused by the hyperbolic tangent function. The magnitude of distortion that is caused by this function increases with increasing argument.

![Figure 3.4 The transfer function of a bipolar differential pair](image)

**Distortion**

Distortion is caused by nonlinearities in the system. It is obvious from the transfer function that the differential pair does not have a linear behaviour. The third order harmonic distortion caused by a differential pair will now be derived using the transfer function and the theory of Taylor McLaurin. This way of distortion calculus is more thoroughly explained in appendix B.

For the distortion calculus the transfer function is written in a Taylor McLaurin Series. For the coefficients the derivatives of the transfer function are needed.
3 Theory Of Operation

\[ I_0 = \frac{\alpha_{p\text{bias}}}{2} \tanh \frac{V_i}{2V_T} \]

\[ \frac{dI_0}{dV_i} = \frac{\alpha_{p\text{bias}}}{4V_T} \text{sech} \left( \frac{V_i}{2V_T} \right) \]

\[ \frac{d^2 I_0}{dV_i^2} = \frac{\alpha_{p\text{bias}}^2 \text{sech} \left( \frac{V_i}{2V_T} \right)^2 \tanh \left( \frac{V_i}{2V_T} \right)}{4V_T^2} \]

\[ \frac{d^3 I_0}{dV_i^3} = \frac{\alpha_{p\text{bias}}^3 \left( -2 + \cosh \frac{V_i}{V_T} \right) \text{sech} \left( \frac{V_i}{2V_T} \right)^4}{8V_T^3} \] (3.23)

With these derivatives the Taylor-McLaurin coefficients can be calculated.

\[ a_n = \frac{1}{n!} \frac{d^n I_0}{dV_i^n} (x) \bigg|_{V_i = 0} \] (3.24)

Leading to:

\[ a_0 = 0 \]
\[ a_1 = \frac{\alpha_{p\text{bias}}}{4V_T} \]
\[ a_2 = 0 \]
\[ a_3 = \frac{\alpha_{p\text{bias}}}{48V_T^3} \] (3.25)

With these coefficients the harmonic distortion can be calculated.

\[ HD_2 = \left| \frac{a_2A}{2a_1} \right| = 0 \]
\[ HD_3 = \left| \frac{a_3A^2}{4a_1} \right| = \frac{A^2}{48V_T^2} \] (3.26)

In these equations \( A \) represents the input signal amplitude.

From these equations can be concluded that the second order harmonic distortion is zero. About the third order harmonic distortion can be concluded that it is mainly dependent on the amplitude of input signal.

3.3 A Differential Pair Amplifier

A differential pair amplifier consists of a differential pair and a pair of resistors. These resistors convert the signal current from the differential pair into a differential output voltage. The schematic for this type of amplifier is depicted in figure 3.5.
The transfer function of this amplifier can easily be derived with the transfer function of the differential pair. The signal current flows through the resistors where the output voltage is generated. The transfer function is formulated in equation (3.27).

\[
V_u = -\alpha_p I_{bias} R_i \tanh \frac{V_i}{2V_T}
\]

**Gain**

The gain of this system can be found by the second Taylor-McLaurin coefficient. This coefficient gives the linear transfer function from input to output signal. This coefficient equals:

\[
G = \frac{dV_u}{dV_i}\bigg|_{V_i=0} = \frac{\alpha_p I_{bias} R_i}{2V_T}
\]

The common mode level of the output voltage equals the supply voltage minus the voltage generated over the load resistors by the bias current. The bias current through the resistors equals the bias current through the collector of the transistor if we do not load the circuit. This bias current can be expressed as \(\alpha_p I_{bias}/2\). The common mode level of the output signal can then be expressed with:

\[
V_{CMout} = V_{sup} - \frac{\alpha_p I_{bias} R_i}{2}
\]

This output common mode level limits the value of \(I_{bias} R_i\). Since this factor is also the main design property of the gain of the amplifier, the gain of this type is limited with respect to the voltage space. This maximum gain can be expressed as:
3 Theory Of Operation

\[ G_{\text{max}} = \frac{V_{\text{sup}} - V_{\text{CMout}}}{V_T} \]  

(3.30)

Distortion

With the transfer function the third order harmonic distortion can be calculated as described in appendix B. This results in:

\[ HD_3 = \frac{A^2}{48V_T^2} \]  

(3.31)

This is the same as for the differential pair because the load resistors are linear and thus do not contribute to any distortion.

From equation (3.31) can be seen that the third order harmonic distortion is mainly dependent on the input signal amplitude. For a specified maximum of third order harmonic distortion a maximum amplitude for the input signal can be calculated. Combining this with the limit on the gain we can conclude that for this type of amplifier a maximum level of third order harmonic distortion leads to a maximum in the amplitude of the output signal.

3.4 A Differential Pair Amplifier With Feedback

A commonly used method to reduce distortion is the use of feedback. With feedback the output signal is fed back and subtracted from the input signal. In the feedback loop the output signal can be processed to reach an optimum for the system.
In the differential pair amplifier described in the previous section feedback can be realised by putting resistors between the emitters of the transistor and the common point \( V_o \). This common method of feedback is shown in figure 3.6.

The transfer function for this type of amplifier can be derived using the same signal definitions as stated in equation (3.16). The base emitter voltage of transistor \( T_1 \) can be expressed with:

\[
V_{be1} = V_{ip} - V_0 - V_{R_e}
\]  

(3.32)

The voltage \( V_{R_e} \) can be expressed in a common mode term and a signal term. This also shows a flaw in the way the emitter resistors are connected. The bias current also flows through these emitter resistors generating an extra common mode voltage which decreases the voltage space for the load resistors. This does not benefit the system as concluded in the previous section. An improvement to this would be to directly connect the bias current sources to the emitters of the transistors. This requires an extra current source. But in this way the bias current does not flow through the emitter resistors which saves some precious voltage space. The principal of the circuit is not affected by this change.
The resulting circuit diagram is depicted in figure 3.7

![Reconstructed differential amplifier](image)

Figure 3.7 Reconstructed differential amplifier

Now the transfer equation of this system is derived. The signal current $I_s$ can be expressed using the transfer function of the differential pair. In this transfer function $V_i$ has to be changed. For the differential pair $V_i$ could be expressed as:

$$V_i = V_{be1} - V_{be2}$$
$$= (V_{ip} - V_o) - (V_{in} - V_o)$$

(3.33)

For this circuit $V_i$ can be expressed as:

$$V_i = (V_{be1} - V_{Rs} - V_o) - (V_{be2} + V_{Rs} - V_o)$$
$$= V_{be1} - V_{be2} - 2V_{Rs}$$
$$= V_{be1} - V_{be2} - 2I_s R_e$$

(3.34)

The effect of the extra current source can be taken care for by doubling the original bias current. This results in the following equation for $I_s$:

$$I_s = \alpha F I_{bias} \tanh \frac{V_i - 2R_s I_s}{2V_T}$$

(3.35)

With the relation between $V_u$ and $I_s$,

$$V_u = -2I_s R_1$$

(3.36)

this leads to:

$$V_u = -2\alpha F I_{bias} R_1 \tanh \frac{R_2 \frac{R_e}{R_1} V_u}{2V_T}$$

(3.37)
For various values of feedback a plot of the transfer function is shown in figure 3.8. From this it can be observed that an increasing feedback parameter results in an increment of the linear input range while the gain decreases.

**Gain**

The gain of the feedback differential pair amplifier can be found by:

\[
G = \left. \frac{dV_u}{dV_i} \right|_{V_i=0}
\]

\[
dV_u = -2\alpha_p I_{bias} R_i \left( \frac{V_i + \frac{R_e}{R_i} V_u}{2V_T} \right)^2 \left( \frac{1 + \frac{R_u}{R_i} dV_u}{2V_T} \right)
\]

Solving this equation and applying it for \(V_i=0\), the gain is found:

\[
G = \left. \frac{dV_u}{dV_i} \right|_{V_i=0}
= \left. \left( \frac{-\alpha_p I_{bias} R_i}{\alpha_p I_{bias} R_e + V_T + V_T} \right) \right|_{V_i=0}
= \frac{-\alpha_p I_{bias} R_i}{\alpha_p I_{bias} R_e + V_T}
\]

(3.38)
Again it can be observed from equation (3.39) that the gain of this type of amplifier is limited. This is caused by the common mode levels that should be kept above a minimum. Because of this maximum for the numerator in the expression, the gain is limited. The denominator has its minimum in the case where \( R_e \) is zero, resulting in the amplifier with no feedback discussed in section 3.3.

If the thermal voltage can be neglected with respect to \( \alpha_p I_{bias} R_e \), the gain equals:

\[
G = \frac{R_i}{R_e} \tag{3.40}
\]

**Distortion**

By calculating the derivatives of the transfer function the third order harmonic distortion can be found.

\[
\frac{d^3 V_u}{dV_i^3} \bigg|_{V_i=0} = \frac{\alpha_p I_{bias} R_i V_T}{2 (\alpha_p I_{bias} R_e + V_T)^4} \tag{3.41}
\]

Together with equations (B.7) and (B.2) from appendix B the third order harmonic distortion can be calculated as:

\[
HD_3 = \frac{V_T A^2}{48 (\alpha_p I_{bias} R_e + V_T)^3} \tag{3.42}
\]

From this equation it can be seen that the third order harmonic distortion is reduced with the third power of the feedback resistor \( R_e \). This is in case \( V_T \) can be neglected with respect to \( \alpha_p I_{bias} R_e \). For a fixed gain with optimal use of the available voltage space the minimal level of third order harmonic distortion can be calculated. If equation (3.42) is rewritten in terms of gain \( G \), supply voltage \( V_{sup} \) and the common mode output voltage \( V_{CMout} \), it follows:

\[
V_{CMout} = V_{sup} - \alpha_p I_{bias} R_i
\]

\[
HD_3 = \frac{V_T A^2 |G|^3}{48 (V_{sup} - V_{CMout})^3} \tag{3.43}
\]

Considering that the output signal amplitude equals the input signal amplitude times the gain, it can be concluded that the third order harmonic distortion increases with the output signal amplitude to the second power. Thus limiting the gain of the amplifier benefits the quality of the system with respect to the third order harmonic distortion level. The level of third order harmonic distortion is also dependent on the common mode level of the output signal. By choosing this common mode level as low as possible the amount of third order harmonic distortion can be kept to a minimum.
3.5 The Emitter Follower Output Stage

A disadvantage of the previous described amplifier is the lack of a low output resistance. If the amplifier is to drive a load, a part of the differential signal current is passed through the loading resistor $R_b$.

This causes a loss of gain. The gain then equals:

$$G = \frac{R_d R_b}{R_e (2R_1 + R_b)} \quad (3.44)$$

To solve this problem a buffering stage can be added to the amplifier. A simple solution can be found in the application of two emitter followers. A schematic view of this output stage is depicted in figure 3.10

The input impedance of this system can be found by considering the input current.

$$R_i = \frac{V_i}{I_i} \quad (3.45)$$

For the input current can be derived:
3 Theory Of Operation

I. Theory Of Operation

\[ I_i = I_{b,T} \]
\[ = I_{C,T} \]
\[ = \frac{I_u}{\beta_F} \]
\[ = \frac{V_u}{\beta_F R_b} \]  

(3.46)

With the unity gain this leads to an input impedance of \( \beta_F R_b \). Which is a factor \( \beta_F \) better.

The transfer function of this output stage can be derived using the basic transistor equations.

\[ V_i - V_{be1} - V_u + V_{be2} = 0 \]
\[ V_u = V_i + V_T \ln \left( \frac{I_{bias} R_b - V_u}{I_{bias} R_b + V_u} \right) \]  

(3.47)

By calculation of the derivative of this equation with respect to \( V_i \), and applying it for \( V_i \) is zero we find the gain of the circuit:

\[ G = \frac{dV_u}{dV_i} \bigg|_{V_i = 0} \]
\[ = \frac{I_{bias} R_b}{I_{bias} R_b + 2V_T} \]  

(3.48)

Which approximates unity when \( I_{bias} R_b \) dominates over \( 2V_T \).

With the theory of appendix B, for the third order harmonic distortion can be found:

\[ HD_3 = \frac{V_T A^2}{6 (I_{bias} R_b + 2V_T)^3} \]  

(3.49)

By maximizing the bias current the harmonic distortion minimizes and the gain approximates unity. With a given output signal amplitude the desired level of harmonic distortion can be reached by putting a demand on the input impedance of the following stage.

A disadvantage of this output stage is the loss of another base-emitter junction voltage. This loss limits the voltage space available to the previous stage. This results in loss of performance of the total system.

3.6 The Differential Pair Amplifier With Output Stage

To use a differential pair amplifier as described in section 3.4, it needs a buffering output stage as described in section 3.5. A system with cascaded amplifier stages which each a non linear behaviour can be described as one system with a total gain \( G_T \), and an overall third or-
der harmonic distortion level $\text{HD}_{3T}$. The performance of the total system can be derived using the theory of appendix C.

For the total gain can be found:

$$G_T = G_{DPA} G_{EF}$$

$$= \frac{-\alpha_F I_{bias, DPA} R_f}{\alpha_F I_{bias, DPA} R_f + V_T} \frac{I_{bias, EF} R_b}{I_{bias, EF} R_b + 2V_T}$$  \hspace{1cm} (3.50)

Where $G_{DPA}$ is the gain of the differential pair amplifier and $G_{EF}$ the gain of the emitter follower.

For the total distortion can be found:

$$\text{HD}_{3T} = \frac{V_T A_0^2}{48 (\alpha_F I_{bias, DPA} R_f + V_T)^3} + \frac{V_T (A_0 G_{DPA})^2}{6 (I_{bias, EF} R_b + 2V_T)^3}$$  \hspace{1cm} (3.51)

### 3.7 The Transresistance Amplifier

A resistor is a passive device to convert a current into a voltage. This principle is applied in the amplifier of section 3.3. In this system the bias current and the signal current were led through the same resistor. This causes a loss of voltage space that could be saved if the signal current could somehow be separated from the bias current.

A way of separating the signal current is to divert it through the feedback resistors of an amplifier. A schematic of this principle is shown in figure 3.11

![Figure 3.11 Transresistance amplifier](image)

The voltage at the input of the amplifier will be very small because of the feedback and the assumed high gain of the amplifier. Connecting this stage to a differential pair amplifier will almost completely divert the signal current through the feedback resistors. The output voltage $V_u$ will then become:
3 Theory Of Operation

\[ V_u = \frac{G}{G+1}2RI_s \]  

(3.52)

For the amplifier a differential pair amplifier can be used. This will be discussed in the next section.

3.7.1 Implementing A Differential Pair Amplifier.

A circuit diagram of the implementation of the transresistance amplifier utilizing a differential pair amplifier is shown in figure 3.12.

![Circuit Diagram of Transresistance Amplifier](image_url)

Figure 3.12 Implementation of a transresistance amplifier

The input current source is shown together as an ideal current source with its internal impedance. The current flowing through this resistor generates the input voltage of the differential pair. The main part of the input current will flow through the feedback resistors and thus generates the output voltage. The amplifier is built with a differential pair amplifier. This is not a linear amplifier and causes some distortion. Analysis of the level of third order harmonic distortion is done in the following sections.

The circuit equation

For the amplifier the circuit equation was derived in section 3.3. The buffering stage is loaded with the feedback resistors and the internal impedance of the signal current source. But this value is assumed to be large and the transfer equation of the output stage is assumed to be unity. Some considerations on the effect of loading the total circuit are made later.
The circuit equations of the amplifier then can be written as:

\[ V_u = \alpha_{p1} I_{bias1} R_i \tanh \frac{V_i}{2V_T} \]  

(3.53)

Summing the currents at the nodes \( V_{ip} \) and \( V_{in} \) leads to:

\[ I_s = \frac{V_{ip} - V_{in}}{R_i} + \frac{V_{ip} - V_{un}}{R_f} \]

(3.54)

\[ I_s = \frac{V_{ip} - V_{in}}{R_i} + \frac{V_{up} - V_{in}}{R_f} \]

Adding these equations leads to:

\[ 2I_s = 2 \frac{V_{ip} - V_{in}}{R_i} + \frac{V_{ip} - V_{in} + V_{up} - V_{un}}{R_f} \]

(3.55)

\[ 2I_s = 2 \frac{V_i}{R_i} + \frac{V_i + V_u}{R_f} \]

Combining this with equation (3.53) a general relation between the input current and the output voltage is obtained.

\[ V_u = \alpha_{p1} I_{bias1} R_i \tanh \frac{R_i (2R_f I_s - V_u)}{2V_T (2R_f + R_i)} \]

(3.56)

With this relation the transresistance and the third order harmonic distortion can be calculated using the theory of appendix B.

The transresistance equals the derivative of \( V_u \) with respect to \( I_s \).

\[ \frac{dV_u}{dI_s} = \frac{2R_i}{2R_f + R_i} \alpha_{p1} I_{bias1} R_i \]

(3.57)

\[ \frac{dV_u}{dI_s} = \frac{R_i}{2R_f + R_i} \alpha_{p1} I_{bias1} R_i + 2V_T \]

When in the denominator the term \( 2V_T \) can be neglected, the transresistance equals \( 2R_f \).

For the third order harmonic distortion can be derived:

\[ \frac{d^3 V_u}{dI_s^3} = \frac{4\alpha_{p1} I_{bias1} R_i V_T \left( \frac{2R_i}{2R_f + R_i} \right)^3}{\left( 2V_T + \alpha_{p1} I_{bias1} R_i \frac{R_i}{2R_f + R_i} \right)^4} \]

(3.58)

\[ HD_3 = \frac{V_T \left( \frac{2R_i}{2R_f + R_i} \right)^2 A_0^2}{6 \left( 2V_T + \alpha_{p1} I_{bias1} R_i \frac{R_i}{2R_f + R_i} \right)^3} \]
When again neglecting the $2V_T$ term in the denominator the equation simplifies to:

$$HD_3 = \frac{V_T (2R_f)^2 A_0^2}{6 (\alpha_f \beta_{bias} R_i)^3 \frac{R_i}{2R_f + R_i}} \quad (3.59)$$

From this can be concluded that the level of third order harmonic distortion is related to the square of the output signal amplitude $2R_f A_0$. The gain of the amplifying stage reduces the level of third order harmonic distortion with the third power. But this gain is limited because of common mode level considerations.

The output impedance of this circuit is built out of the parallel connection of the output impedance of the buffered differential pair amplifier and the serial connection of the two feedback resistors with the current source's internal resistance. Resulting in:

$$R_{out} = \frac{\frac{2R_i}{\beta_F} (2R_f + R_i)}{\frac{2R_i}{\beta_F} + 2R_f + R_i} \quad (3.60)$$

This value can be made low by choosing a low value of $R_i$. The value of this resistor can be made low when increasing the bias current of the amplifying stage. Because these factors only occur together in any gain or distortion equations.
3.8 A Three Stage Differential Amplifier

When combining the differential pair amplifier with the transresistance amplifier a complete differential amplifier can be made. This is shown in figure 3.13.

The first stage is a differential pair amplifier with feedback resistor between the emitters of the transistors. The second stage keeps the voltage $V_a$ low by feedback through the resistors $R_f$. This causes the signal current generated by the differential pair to be drawn into the second stage. The second stage is a transresistance amplifier. This second stage is buffered with an emitter follower output stage which also buffers the output of the total system. The distortion is minimized in the first stage by a local series feedback resistor. The second stage utilizes a shunt-shunt feedback to minimize distortion.

With the theory of cascading stages studied in appendix C the total gain and third order harmonic distortion can be found.

This leads to a total gain of:

$$G_{total} = \frac{\alpha_p I_{bias1}}{2(\alpha_p I_{bias1} R_f + V_T)} \frac{2R_f R_{11}}{R_f + R_{11}} \frac{\alpha_p I_{bias2} R_{12}}{R_f + R_{11}}$$

When neglecting the terms $V_T$, a simple equation is found by which an estimation on the total gain can be made.
For the total third harmonic distortion can be derived:

\[
G_{\text{total}} = \frac{R_f}{R_e}
\]  
(3.62)

The first term in this equation can be minimized resulting in a smaller value for the signal current passing into the second stage of the amplifier. The second term however mainly depends on the output signal amplitude and the voltage space available for the second stage differential pair amplifier. This will limit the performance of the circuit.

\[
HD_{3,\text{total}} = \frac{V_T A_0^2}{48 (\alpha_p I_{\text{bias1}} R_e + V_T)^3} + \frac{V_T \left( \frac{2R_f R_f + R_{11}}{R_{11}} \right)^2 \left( A_0 \frac{\alpha_p I_{\text{bias1}}}{2 (\alpha_p I_{\text{bias1}} R_e + V_T)} \right)^2}{6 \left( 2V_T + \alpha_p I_{\text{bias2}} R_{12} \frac{R_f + R_{11}}{R_f + R_{11}} \right)^3}
\]  
(3.63)

Simplifying this equation by neglecting \( V_T \) this leads to:

\[
HD_{3,\text{total}} = \frac{V_T A_0^2}{48 (\alpha_p I_{\text{bias1}} R_e)^3} + \frac{V_T \left( \frac{R_f A_0}{R_e} \right)^2}{6 (\alpha_p I_{\text{bias2}} R_{12})^3 \frac{R_{11}}{R_f + R_{11}}}
\]  
(3.64)

The first term in this equation can be minimized resulting in a smaller value for the signal current passing into the second stage of the amplifier. The second term however mainly depends on the output signal amplitude and the voltage space available for the second stage differential pair amplifier. This will limit the performance of the circuit.
4 Implementation And Simulation

In this chapter the previously discussed circuits are discussed with respect to the specifications derived in the Introduction. The circuits are optimized using simulation results and the pros and cons are discussed.

4.1 The Simulation Model Of The Bipolar NPN-Transistor

As a design is realized it has to be made sure that in practice it acts the same way as it was predicted to. One way of testing this is to simulate the circuit design with a circuit simulation program on a computer. In this computer simulation a more complex model of the transistor is used. With these computer simulations a more realistic picture of the circuit can be observed. The model of the transistor used by the simulator is depicted in figure 4.1.

![Simulation model of a NPN bipolar transistor](image)

In this model the parasitic components of the transistor are shown. The most important of these components are the resistors. These cause extra voltage drops resulting in losses of signal current and signal voltage. The effect of the capacitors will be noticed in a loss of bandwidth of the design. This does not limit the design because these effects are not of any importance at the intermediate frequencies that are applicable for this design.

For this design devices are used from Qubic1 library. From this library the B-series is discussed for their beneficiary specifications. For each transistor type of this series the most important parameters are specified in table 4.1.
Table 4.1 Transistor parameters of the Qubic1 library

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Transistor Type</th>
<th>Units</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>BNB2T</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I&lt;sub&gt;c,max&lt;/sub&gt;</td>
<td>400</td>
<td>750</td>
<td>900</td>
</tr>
<tr>
<td>β</td>
<td>180</td>
<td>155</td>
<td>146.7</td>
</tr>
<tr>
<td>R&lt;sub&gt;b&lt;/sub&gt;</td>
<td>50</td>
<td>25</td>
<td>16.67</td>
</tr>
<tr>
<td>R&lt;sub&gt;e&lt;/sub&gt;</td>
<td>30.8</td>
<td>20.85</td>
<td>18.4</td>
</tr>
<tr>
<td>R&lt;sub&gt;c&lt;/sub&gt;</td>
<td>115</td>
<td>57.5</td>
<td>38.33</td>
</tr>
</tbody>
</table>

4.2 The Differential Pair Amplifier

For the differential pair amplifier the gain and third order harmonic distortion were derived in section 3.3. For a maximum allowed third order harmonic distortion level of -80 dB, the maximum input signal amplitude can be calculated.

\[
A_{\text{max}} = V_r \sqrt{\frac{48HD_3}{G}}
\]

\[
= 1.77 \text{ milliVolt}
\]

(4.1)

For the calculation of the maximum gain with this maximum input signal amplitude expression (3.30) can be used. For use of this equation a value for the output signal common mode level is needed. The lower this common mode level the higher the gain.

A minimum value for this common mode level can be derived with some voltage level considerations. First, the bias current generation approximately needs 1 Volt. This includes the voltage space needed for a constant bias voltage generation and the voltage over a resistor where the bias current is generated. Second the base emitter junction needs to be forward biased to get the transistor in the active mode. This is necessary to justify the use of the active mode model equations, and for the device to be able to conduct the appropriate currents. This takes approximately 0.85 Volt. And last some voltage space is needed for the output voltage swing. The differential output signal of amplifier is the voltage difference between the two output nodes. With both the output nodes varying around the common mode level in counter phases, each output node swings half the output signal amplitude. Adding all of this the output signal common mode level can be specified as:

\[
V_{\text{CMout}} = 1 + 0.85 + A_{\text{out}}/2
\]

\[
= 1.85 + A_{\text{max}}|G_{\text{max}}|/2
\]

(4.2)
Putting this in equation (3.30) the maximum gain can be calculated.

\[
G_{\text{max}} = \frac{-2(V_{\text{sup}} - 1.85)}{A_{\text{max}} + 2V_T}
\]

\[
= -119.4
\]

(4.3)

With this maximum gain and the maximum for the input signal amplitude the maximum output signal amplitude can be calculated.

\[
A_{\text{out}} = A_{\text{max}} |G_{\text{max}}|
\]

\[
= 211 \text{ milliVolt}
\]

(4.4)

As can be seen from this result, the differential pair amplifier does not meet the specification of 1 Volt output amplitude level. To get an idea of the performance of this type of amplifier, the third order harmonic distortion can be calculated with all of the other specifications maintained.

\[
A_{\text{out}} = A |G|
\]

\[
= 1
\]

(4.5)

This leads to a common mode level for the output signal of 2.35 Volt. Resulting in a maximum gain of 104. Implying an input signal amplitude of 9.62 milliVolt. With equation (3.31) the distortion level can then be calculated as:

\[
HD_3 = -50.6 \text{ dB}
\]

(4.6)

From this can be concluded that an increase of the output signal amplitude increases the distortion level dramatically.

A plot of the gain calculated with equation (4.3) is shown in figure 4.2 together with the result of the simulation of this circuit. The simulation results are for various values of the bias current. For these various bias currents and input signal amplitude the value for \(R_1\) is calculated. This causes the gain to decrease with increasing input signal amplitudes.

The variation of the gain for the various values of the bias current is mainly caused by the parasitic emitter resistor in the differential pair's transistors. The effect of these emitter resistors is a loss of input signal because the signal current is passed through causing a voltage drop related to the input signal. This effect is used in the following section as a feedback.

In figure 4.3 the third order harmonic distortion is shown versus the input signal amplitude. In this plot the curves of the simulation are below the theoretical curves especially for larger input signal amplitudes. This is caused by the parasitic emitter resistors acting as a feedback. Further it can be concluded that with this feedback the bias current should be taken as high as possible to lower the distortion level. This is not according to the theoretical plot where the bias current doesn't have any effect on the distortion level. This implies that for the feedback
4 Implementation And Simulation

Theoretical
$I_{bias}$
- $500\mu A$
- $750\mu A$
- $1mA$

Figure 4.2  Gain versus input signal amplitude

amplifier large transistors should be used to allow these high currents. This is an extra possi-

Figure 4.3  Third order harmonic distortion versus input signal amplitude

bility to lower the level of third order harmonic distortion.
4.3 The Feedback Differential Pair Amplifier

The previous section showed the benefit of applying a series feedback to the differential pair amplifier. In the previous section the feedback was not intended and not controllable. Here the effect of the value of a feedback resistor applied is discussed.

When adding extra feedback resistors to the differential pair amplifier the gain can be expressed with equation (3.39). Assuming that the thermal voltage in the denominator can be neglected the gain can be calculated as the quotient of the load resistor and the emitter resistor. In this case the level of third order harmonic distortion can be calculated with:

\[ HD_3 = \frac{V_T^2}{48 (\alpha_p l_{bias} R_e)^3} \]  \hspace{1cm} (4.7)

For a given maximum value for the harmonic distortion and a given input signal amplitude, an equation for \(\alpha_p l_{bias} R_e\) can be obtained.

\[ \alpha_p l_{bias} R_e = \sqrt{\frac{V_T^2}{48 HD_3}} \]  \hspace{1cm} (4.8)

A minimum value for the output common mode level is defined in equation (4.2). While equation (3.43) specifies this common mode level. Combining these equation leads to:

\[ \alpha_p l_{bias} R_e = V_{sup} - 1.85 - \frac{A|G_{max}|}{2} \]  \hspace{1cm} (4.9)

For the maximum gain now can be derived:

\[ G_{max} = \frac{R_l}{R_e} = \frac{\alpha_p l_{bias} R_l}{\alpha_p l_{bias} R_e} \]  \hspace{1cm} (4.10)

Solving this equation for \(G_{max}\) with equations (4.8) and (4.9) leads to:

\[ G_{max} = \frac{V_{sup} - 1.85}{\frac{A}{2} + \sqrt{\frac{V_T^2}{48 HD_3}}} \]  \hspace{1cm} (4.11)

For a level of third order harmonic distortion of -80 dB and an input signal amplitude of 100 milliVolt a maximum gain of 7.40 is found. Resulting in an output signal amplitude of 740 milliVolt.

The level of third order harmonic distortion for a given input signal amplitude and output signal amplitude can be calculated using equation (3.43). A value of -71 dB is then found for the level of third order harmonic distortion.
In figure 4.4 a plot of the gain of the system versus the value for the emitter resistor is shown.

![Gain plots of the feedback differential pair amplifier](image)

Figure 4.4  Gain plots of the feedback differential pair amplifier

Various curves are plotted for different values of the output signal common mode level. These values are varied through variation of the resistor $R_e$. The theoretical plots are drawn with the solid line and the simulation results with a dashed line. It can be observed that the simple calculations with a theoretical model for the bipolar transistor approach the simulation results for the gain of the system.

A plot of the third order harmonic distortion is shown in figure 4.5. For this plot the same

![Distortion plots of the feedback differential pair amplifier](image)

Figure 4.5  Distortion plots of the feedback differential pair amplifier

properties are applicable as for the gain plots. Here it can be observed that the theoretical plot
is not affected by variation of the output common mode level. The simulation results however show, with increasing common mode level of the output signal, a lower value of third order harmonic distortion, nearer to the theoretical curve. Further it can be observed that with an increasing value of the emitter resistance, the simulated level of distortion tends to a curve with a stabilizing level of harmonic distortion where the theoretical slope is -3 (see figure 4.6). This stabilization occurs when the gain approaches unity. The voltage over the

![Figure 4.6 Logarithmic distortion plots of the feedback differential pair amplifier](image)

emitter resistors dominates the base-emitter junction voltages, causing the transistors to lose their functionality. The circuit loses its amplifying characteristic and is not functional anymore.

A plot of the third order harmonic distortion versus the gain is shown in figure 4.7. These are simulation results. From this plot a maximum gain can be found for a specified level of third
order harmonic distortion. For the -80 dB level a gain of approximately 5 is maximal. While

![Graph showing simulated distortion versus gain plot]

Figure 4.7  Simulated distortion versus gain plot

... a gain of 10 implies a level of third order harmonic distortion of minimal -64 dB.

### 4.4 The Emitter Follower Output Stage

In section 3.5 it was stated that an output stage was needed to buffer the output signal of the differential pair amplifier. This buffer was implemented using an emitter follower stage. The gain of this stage approached unity and the level of third order harmonic distortion was mainly dependent on the product of the bias current and the loading impedance.

For a given input signal amplitude and a maximum amount of third order harmonic distortion a minimum value for the loading impedance can be calculated with equation (3.49). Rewriting this equation results in:

\[
R_b = \frac{\sqrt{3V_T A^2} - 2V_T}{6H D_3 I_{bias}}
\]

(4.12)

For an input signal amplitude of 1 Volt and a maximum level of distortion of -80 dB we get a value of 3.44 kΩ.
In figure 4.8 a plot is shown of the gain versus the load resistor for various values of the input
signal amplitudes.

The third order harmonic distortion curves are plotted in figure 4.9. These curves are very
close to the theoretical curves calculated with the simple bipolar transistor model. Conclusive
it can be said that the distortion of the output stage can be calculated with equation (3.49),
but the gain is lower than calculated with equation (3.48). A negative aspect of this stage is
the voltage space it requires. This is one base emitter junction voltage.
The output stage was added to the system to lower the output impedance and to be able to drive higher currents. In figure 4.10 the output current is plotted versus the input current. The curves are generated by varying the load resistor \( R_b \). The direction of the arrow in figure 4.10 indicates an increasing value for this resistor from 1kΩ to 5kΩ. Various curves are plotted for different input signal amplitudes. Calculating the slope of the curves results in a value of 91. With a gain of approximately 1 an input impedance of 91 times \( R_b \) is obtained.

### 4.5 Differential Pair Amplifier With Output Stage

The addition of an output stage to the differential pair amplifier decreases the output impedance with a factor 91. But this extra stage also needs about 0.85 Volt of voltage space. This increases the common mode of the collectors of the differential pair with 0.85 Volt. The increment limits the gain that can be realized with the differential pair amplifier and thus limits the performance of the circuit. An extra loss is the addition of an extra source of third order harmonic distortion. This however can be minimized by demanding a higher input impedance of any following stage. This leaves the loss of voltage space to be the most important source for the loss in performance.
Simulation results are plotted together with the curves calculated with the equations from section 3.6 in figure 4.11 to figure 4.13.

Compared to figure 4.4 the gain decreased by approximately 10 percent. This is caused by the output stage, as found in the previous section, and as a result of the higher common mode level of the collectors of the differential pair.
For the third order harmonic distortion the effect of the distortion added by the output stage can be neglected. Further the effect of the increased common mode level of the differential pair’s collectors is opposed to the decrement of the gain. Resulting in an approximately equal level of third order harmonic distortion.

Concluding from the results in figure 4.13 it can be said that a gain of approximately 4.5 at a third order harmonic distortion level of -80 dB is the limit. If a gain of 10 is desired, this circuit has a third order harmonic distortion level of approximately -63 dB.

4.6 The Transresistance Amplifier

The transresistance amplifier was intended to divert the signal current from the bias current of a differential pair amplifier. In this way a higher gain can be realized in the differential pair amplifier because it gains some voltage space, and a higher gain can be realized in the conversion of the signal current into an output voltage. A solution to this is the transresistance amplifier. But it is another amplifying stage causing third order harmonic distortion. The level of third order harmonic distortion of this amplifying stage is derived in section 3.7.

The transresistance of the amplifier can be calculated by equation (3.57). The input signal current is generated by an differential pair as described in section 4.3. The input signal current amplitude varies hyperbolic with the emitter resistor, and ranges between 50 μA and 200 μA. To get an output amplitude signal of 1 Volt the appropriate value for the feedback resistor $R_f$ is calculated.

In figure 4.14 the transresistance is plotted for various values of the common mode level of the collectors of the differential pair. The effect of this common mode level becomes clearer.
in figure 4.15. This common mode level has no great influence on the transresistance because

\[ V_{cm,dpa} \]

it only affects the gain of the differential pair amplifier. This gain defines the output signal according to equation (3.52). From this equation it is obvious that if the gain is much higher than 1 the value of this gain only has a minor effect on the output signal's amplitude. With the equation (3.30) the gain for the various common mode levels is calculated as varying from 60 to 80.

The output signal amplitude is plotted in figure 4.15. The limited gain of the differential pair amplifier causes the output signal amplitude to be less than 1 Volt. The difference between
the theoretical curves and the simulation results can be explained with the fact that the input impedance of the differential pair is finite. This causes a part of the signal current to flow into the bases of the differential pair's transistors, resulting in a lower output signal amplitude.

The third order harmonic distortion levels are plotted in figure 4.16. It can be seen that lowering the common mode level of the differential pair's collectors causes a higher level of third order harmonic distortion. This is a result of the high output signal amplitude causing the collector base voltage to drop below a certain level. Below this voltage the collector current is mainly dependent on the collector emitter voltage. Thus the transistor is not in its active mode anymore.

The level of third order harmonic distortion for this output signal amplitude can not be lowered. This is conform equation (3.59) where the numerator consists of the output signal amplitude and the denominator mainly depends on the common mode level of the differential pair's collectors. From this can be concluded that the level of third order harmonic distortion

\[ \text{HD}_3 = \frac{I_x (\text{A})}{V_{cm, dpa}} \]

![Figure 4.16 Third order harmonic distortion of the transresistance amplifier](image-url)
is mainly dependent on the output signal amplitude. In figure 4.17 curves of simulation re-

\[ \text{HD}_3 (\text{dB}) \]

\[ \text{Parameter:} \quad I_s \]

\[ 50\mu A \]

\[ 100\mu A \]

\[ 150\mu A \]

\[ 200\mu A \]

Figure 4.17 Plots of the third order harmonic distortion versus the output signal amplitude

results are shown. These curves show the third order harmonic distortion versus the output signal amplitude for various values of the input signal amplitude. These curves show that a third order harmonic distortion level of less than -80 dB is not possible with this circuit. At least not for these high output signal amplitudes.

4.7 The Three Stage Differential Amplifier

As concluded from the previous section the third order harmonic distortion level of -80 dB can not be reached with the transresistance amplifier. In this section however the equations derived in section 3.8 will be compared with simulation results of the three stage differential amplifier.

A plot of the gain of the amplifier is shown in figure 4.18. These gain curves are calculated and simulated for different output signal amplitudes. That is, what the output signal ampli-
tude would be when calculated with equation (3.62). The circuit is designed with use of these simplified equations.

![Graph showing gain of three stage differential amplifier](image1)

**Figure 4.18** The gain of the three stage differential amplifier

The values of the load resistors and the bias currents determine the common mode levels in the circuit. These are to be chosen as low as possible but not too low to avoid clipping of any transistor. In figure 4.19 plots of the third order harmonic distortion are shown. It shows that the distortion level of the first stage is dominant for low values of the emitter resistor. For high values of this resistor the second stage dominates the level of third order harmonic.

![Graph showing third order harmonic distortion](image2)

**Figure 4.19** Third order harmonic distortion of the complete differential amplifier
distortion. It is also obvious that the first stage has a higher level of third order harmonic distortion than was obtained with the theoretical calculations. This is in accordance with the results found in section 4.3.

Equation (3.64) states that the third order harmonic distortion is the summation of the distortion levels of the separate stages. In figure 4.20 the calculated levels of third order harmonic distortion of both stages are plotted together with the total level of third order harmonic distortion.

![Graph](image)

**Figure 4.20** Calculation of the third order harmonic distortion per stage
To be able to find the optimum values for the emitter resistors, a plot of the total third order harmonic distortion versus the gain is presented in figure 4.21. In these plots the arrow indicates an increasing value for the emitter resistor in the first stage. The minima and their specific values for the emitter resistance, actual gain and level of third order harmonic distortion are listed in table 4.2.

![Figure 4.21 Simulated distortion versus gain](image)

Table 4.2 Performance at various output signal levels

<table>
<thead>
<tr>
<th>Calculated output signal Amplitude</th>
<th>Emitter resistance $R_e$ [Ω]</th>
<th>Actual gain $G$</th>
<th>Third order harmonic distortion level $HD_3$ [dB]</th>
</tr>
</thead>
<tbody>
<tr>
<td>$A_{V_{A}}$ [V]</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0.8</td>
<td>850</td>
<td>6.67</td>
<td>-72.0</td>
</tr>
<tr>
<td>0.9</td>
<td>785</td>
<td>7.43</td>
<td>-69.9</td>
</tr>
<tr>
<td>1.0</td>
<td>720</td>
<td>8.17</td>
<td>-68.1</td>
</tr>
</tbody>
</table>

The value of the actual gain found by simulation results is about eighty percent of the gain calculated with the theory described in chapter 3. This is caused by losses not catered for in the theory. Main contributions to these losses are the base currents. These currents cause loss of input voltage in the first stage because this base current flows through the emitter resistor. In the second stage the signal current flowing through the bases is not flowing through the feedback resistors hence does not contribute to the output signal. For this reason the second stage is biased with a smaller quiescent current. This results in a smaller signal current through the differential pair, limiting the signal current through the bases of the transistors.
Other loss factors are the parasitic resistors in the transistors causing extra voltage drops. The most important of these are the emitter resistance because these conduct larger currents.

The curves of the gain and third order harmonic distortion versus the operating frequency are plotted in figure 4.22. From these curves it can be observed that the gain is quite stable over a large frequency range. However for higher frequencies the level of third order harmonic distortion increases. This is caused by the parasitic capacitance in the transistor gaining importance. The bandwidth of the amplifier is about 3 Gigahertz. But the bandwidth with a low third order harmonic level is limited to about 100 Megahertz.
In figure 4.23 the levels of the other harmonic distortion are plotted. This plot shows that the third order harmonic distortion is dominant as stated previously.
5 Conclusions And Recommendations

From the simulation results it can be concluded that the theoretical analysis of the circuits can be used to do coarse calculations. The equations however can only be used if the transistor is kept in the active mode of operation. This implies some boundary conditions for the use of these equations.

Further it can be concluded that the circuits discussed in this report do not meet the specifications. For a distortion level as low as -80 dB the output signal amplitude of 1 volt can not be reached. For this output signal amplitude a distortion level of approximately -65 dB is minimal with the threestage amplifier discussed in section 4.7. With a distortion level of -80 dB an output signal amplitude of 450 millivolt is the best result. Conclusive it can be said that the distortion level is mainly dependent on the output signal amplitude.

The required bandwidth is not a limit on the circuits discussed.

Other amplifier principles could be tried. The following principles have been tested vaguely:

- An amplifier consisting of two buffered differential pair amplifiers with an overall feedback loop: This caused some instability at high frequencies.

- An equiripple design: This required a large number of differential pairs. To get a distortion level of -60 dB 25 differential pairs were needed!

Deeper analysis of these principles could lead to an amplifier with better performance.
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Eindhoven, May 1995,

L.P. de Goey.
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Appendix B  Distortion Calculus

Distortion is a result of any non-linearities in the system transfer function. Here the equations for the harmonic distortion will be derived.

The distortion of the system depicted in figure B.1 will be discussed.

\[ y = \sum_{n=0}^{\infty} a_n (x-x_0)^n \]  \hspace{1cm} (B.1)

Where the coefficients can be calculated with:

\[ a_n = \frac{1}{n!} \frac{d^n y}{dx^n} \bigg|_{x=x_0} \]  \hspace{1cm} (B.2)

For our nonlinear system the transfer function \( y=f(x) \) can be expressed as:

\[ y = a_0 + a_1 x + a_2 x^2 + a_3 x^3 + \ldots \]  \hspace{1cm} (B.3)

The higher order terms have been neglected because their contribution to the final expression is assumed minimal.

If a single tone signal is applied to this system with an amplitude \( A \) and a frequency \( f \) this results in:

\[
x = A \cos 2\pi ft
\]

\[
y = a_0 + a_1 A \cos 2\pi ft + a_2 (A \cos 2\pi ft)^2 + a_3 (A \cos 2\pi ft)^3 + \ldots
\]

\[
= \left( a_0 + a_2 A^2 /2 + \ldots \right) + \left( a_1 + \frac{3 a_3 A^3}{4} + \ldots \right) \cos 2\pi ft + \left( \frac{a_2 A^2}{2} + \ldots \right) \cos 4\pi ft + \left( \frac{a_3 A^3}{4} + \ldots \right) \cos 6\pi ft + \ldots
\]  \hspace{1cm} (B.4)

From equation (B.4) can be seen that a nonlinear system is fed with a tone signal it also generates tone signal with frequencies which are a multiples of the original tone frequency. These are called higher order harmonics. The harmonic distortion is defined as the amplitude
of this higher order harmonic relative to the amplitude of the first harmonic. The second order harmonic distortion can be expressed as:

\[
HD_2 = \left| \frac{a_2A^2}{2} + \ldots \right| \left| \frac{3a_1A^2}{4} + \ldots \right|
\]

The higher order terms can be neglected if the amplitudes are kept low. This simplifies the equation to:

\[
HD_2 = \frac{|a_2A|}{2a_1}
\]

(B.6)

In a similar way an expression for the third order harmonic distortion can be derived.

\[
HD_3 = \frac{|a_3A^3|}{4a_1}
\]

(B.7)
Appendix C Cascading Stages

To meet certain demands it is often necessary to put several amplifying stages in cascade. In this appendix only differential amplifying stages are considered. This causes the third order harmonic distortion to be dominant while the even order harmonic distortion is cancelled because of the differential design. To calculate the total third order harmonic distortion it is necessary to take a look at the effect of any other stage in the total system.

The third harmonic produced by the first stage for example is amplified by the second as if it was a base frequency of the input signal. This puts a high strain on the first stage.

Let's consider an amplifier consisting of n-stages as drawn in figure C.1.

Assuming a tone input signal and assuming that the amplifying stages only have third order harmonic distortion. Any higher order terms that are encountered are neglected. This is done to get a clear view and the higher order terms do not substantially add to the final result. Terms with the base frequency caused by third order terms are neglected also because their amplitudes are considered negligible with respect to the base term. This can be done for a low amplitude or low distortion levels (factors $a_{3n}$ are small compared to $a_{1n}$).

For the signals $x_n$ can then be found:

\[
\begin{align*}
    x_0 &= A_0 \cos (\omega t) \\
    x_1 &= a_{11}x_0 + a_{31}x_0^3 \\
    &= A_0a_{11}\cos (\omega t) + \frac{A_0^3a_{31}}{4}\cos (3\omega t) \\
    x_2 &= a_{12}x_1 + a_{32}x_1^3 \\
    &= A_0a_{12}\cos (\omega t) + \frac{A_0^3}{4}(a_{31}a_{12} + a_{11}a_{32})\cos (3\omega t)
\end{align*}
\] (C.1)

From this it can be observed that the distortion caused by the first stage will be amplified through system. While the last stage has a large input signal amplitude and thus causing high distortion. For stage $n$ the output signal can be derived as:
Appendix C Cascading Stages

\[ x_n = A_0 \cos(\omega t) \prod_{i=1}^{n} a_{i1} + \frac{A_0^3 \cos(3\omega t)}{4} \sum_{i=1}^{n} \left( \prod_{k=1}^{i-1} a_{i2} \prod_{k=i+1}^{n} a_{1k} \right) \]  \hspace{3cm} (C.2)

The last term is the sum of distortion added by each stage. This has to be multiplied with the gain of every latter stage. The input signal amplitude of every stage is found by multiplying the amplitude of the original input signal with the gain of each previous stage. This has to be taken to the third power for the third harmonic. The overall third order harmonic distortion of \( n \) stages is found by dividing the amplitude of the third harmonic by the amplitude of the base frequency. This leads to:

\[ HD_{3n} = \sum_{i=1}^{n} a_{2i} A_0^2 \prod_{k=1}^{i-1} a_{1k} \]  \hspace{3cm} (C.3)

The coefficients \( a_{2i} \) can be replaced by the gain of each stage. The third order harmonic distortion of each stage is defined as:

\[ HD_{3i} = \frac{|a_{2i}A_{i1}^2|}{a_{1i}^2} \]  \hspace{3cm} (C.4)

The amplitudes \( A_{i1} \) can be described by:

\[ A_{i1} = A_0 \prod_{k=1}^{i-1} G_k \]  \hspace{3cm} (C.5)

Resulting in:

\[ HD_{3n} = \sum_{i=1}^{n} HD_{3i} \]  \hspace{3cm} (C.6)

Thus the total third order harmonic distortion is the summation of the third order harmonic distortion of all stages. When calculating this value care should be taken to apply every stage with the appropriate input amplitude level.

Another point of attention are the common mode levels of input and output signals of each stage. Every stage should be biased with the proper voltage levels in order to make sure that the stage works as it was intended to work. This sometimes puts a restriction on any previous stage limiting its performance.

For example consider an amplifier consisting of three stages. Defining the input signal amplitudes of the stages as \( A_1, A_2 \) and \( A_3 \). The stages have a gain of \( G_1, G_2 \) and \( G_3 \) and third order harmonic distortion levels of \( HD_{3,1}, HD_{3,2} \) and \( HD_{3,3} \). These third order harmonic distortion levels are defined according to equation (C.4) as:

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Appendix C Cascading Stages

\[ HD_{3,1} = \frac{|a_{3,1}A_1^2|}{|d_{1,1}|^4} = H_1A_1^2 \]  
\[ HD_{3,2} = H_2A_2^2 \]  
\[ HD_{3,3} = H_3A_3^2 \]  

(C.7)

Where \( H_i \) is characteristic for the third order harmonic distortion of each stage.

The amplitude of the input signal is \( A_1 \), this results in an output signal amplitude of the first stage of \( A_1G_1 \). This equals the input signal amplitude of the second stage \( A_2 \). Similar the input signal amplitude of the third stage can be found as \( A_1G_1G_2 \), and the output signal amplitude as \( A_1G_1G_2G_3 \). This is in accordance with equation (C.5).

The third order harmonic distortion that is caused by each stage can be expressed as:

\[ HD_{3,1} = H_1A_1^2 \]  
\[ HD_{3,2} = H_2(A_1G_1)^2 \]  
\[ HD_{3,3} = H_3(A_1G_1G_2)^2 \]  

(C.8)

The third order harmonic distortion is the quotient of the amplitude of the third harmonic and the base frequency. This quotient is not affected by any following stage because the first and the third harmonic are amplified with the same gain. So the total level of third order harmonic distortion of the cascade is the addition of all contributions of each stage as described in equation (C.8).

\[ HD_{3,\text{total}} = H_1A_1^2 + H_2(A_1G_1)^2 + H_3(A_1G_1G_2)^2 \]  

(C.9)

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