MASTER

A low-power high-speed CMOS design method

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Eindhoven University of Technology
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A Low-Power High-Speed
CMOS design method

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at Philips Research Laboratories,

Professor: Prof.dr.ir. R.J. van de Plassche

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# Table of contents

Chapter 1 : Introduction ...................................................................................... 1

Chapter 2 : Low-power strategies ........................................................................ 2
  2.1 Introduction ......................................................................................... 2
  2.2 CMOS Power Dissipation .................................................................... 2
  2.3 Power Reduction Strategies .................................................................. 3

Chapter 3 : Possible methods ............................................................................... 4
  3.1 Introduction ......................................................................................... 4
  3.2 Mos Current Mode Logic (MCML) ...................................................... 4
  3.3 Source Coupled Logic (SCL) ............................................................... 5
  3.4 Folded Source Coupled logic (FSCL) .................................................. 6
  3.5 Complementary Pass-transistor Logic (CPL) ...................................... 7
  3.6 Swing Restored Pass-transistor Logic (SRPL) ..................................... 8
  3.7 Double Pass-transistor Logic (DPL) ................................................... 9

Chapter 4 : Why MCML? ................................................................................... 10

Chapter 5 : Mos Current Mode Logic ................................................................ 11
  5.1 Introduction ....................................................................................... 11
  5.2 Several MCML gates ......................................................................... 11
    5.2.1 2-input (N)AND gate ................................................................. 11
    5.2.2 2-input EX(N)OR gate ............................................................... 12
    5.2.3 2-input D-FLIPFLOP ................................................................. 12
    5.2.4 3-input FULL ADDER ............................................................... 14
  5.3 Differential input signals ................................................................... 15
    5.3.1 Advantage of differential input signals .............................................. 15
    5.3.2 Disadvantage of differential input signals .......................................... 15
  5.4 The effect of the wire-capacitance ..................................................... 15
  5.5 Replacing the load-devices ............................................................... 17
  5.6 Replacing the current-sources ........................................................... 17
  5.7 Input voltage-levels ........................................................................... 18

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Chapter 6: Theoretical debate

6.1 Introduction ................................................................. 19
6.2 Influence of offset on a (N)AND-gate ................................ 19
6.3 Influence of temperature on a (N)AND-gate ......................... 22
6.4 Leakage-current in cascoded differential-pairs ....................... 23
   6.4.1 Leakage-current in 2 cascoded differential-pairs ............... 23
   6.4.2 Leakage-current in 3 cascoded differential-pairs ............... 25
6.5 Power dissipation MCML vs. Standard CMOS ....................... 26
6.6 Testing a string of Standard CMOS inverters ....................... 29

Chapter 7: Designing and measuring

7.1 Introduction .................................................................. 33
7.2 Demands for the library ................................................... 33
7.3 Designing the cells ....................................................... 33
   7.3.1 2-input (N)AND-gate ..................................................... 34
   7.3.2 2-input EX(N)OR-gate ................................................. 35
   7.3.3 Master-Slave Flip Flop .................................................. 36
   7.3.4 The full adder .............................................................. 37
7.4 Specify the input signals .................................................. 39
7.5 Testing the designs ......................................................... 42
   7.5.1 DC-analysis of the (N)AND-gate ................................. 43
   7.5.2 Transient-analysis of the (N)AND-gate ......................... 43
   7.5.3 Monte Carlo analysis of the (N)AND-gate .................... 45
   7.5.4 DC-analysis of the EX(N)OR-gate ............................... 46
   7.5.5 Transient-analysis of the EX(N)OR-gate ........................ 47
   7.5.6 Monte Carlo analysis of the EX(N)OR-gate .................... 47
   7.5.7 DC-analysis of the Master-Slave Flipflop ...................... 47
   7.5.8 Transient-analysis of the Master-Slave Flipflop ............... 48
   7.5.9 Monte Carlo analysis of the M.S. Flipflop ...................... 49
   7.5.10 DC-analysis of the Full-adder .................................. 49
   7.5.11 Transient-analysis of the Full-adder ......................... 49
   7.5.12 Monte Carlo analysis of the Full-adder ...................... 50
7.6 MCML- vs. Standard CMOS power dissipation .................... 50
7.7 Delay-time of standard-CMOS-cells .................................. 53

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Chapter 8: Implementing the gates

8.1 Introduction
8.2 Theory of the Hilbert transformer
8.3 Designing the Hilbert transformer
8.4 Testing the Hilbert transformer

Chapter 9: Layouts

9.1 Introduction
9.2 Creating a layout
9.3 Used checksets

Chapter 10: Conclusions

Chapter 11: Acknowledgement

Chapter 12: References

Appendix I: The Full adder with two cascoded differential pairs
Appendix II: Standard CMOS designs
Appendix III: Cascading of the standard CMOS designs
Appendix IV: The 8-bit Hilbert-transformer
Appendix V: Created layouts

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**List of figures**

Figure 1: Sources of power dissipation in a CMOS inverter  
Figure 2: MCML 2-input (N)AND gate  
Figure 3: 2-input (N)AND SCL gate  
Figure 4: 2-input (N)AND FSCL gate  
Figure 5: CPL 2-input (N)AND gate  
Figure 6: SRPL 2-input (N)AND gate  
Figure 7: DPL 2-input (N)AND gate  
Figure 8: 2-input EX(N)OR-gate  
Figure 9: positive level triggered D-FLIPFLOP  
Figure 10: 3-input Full-adder  
Figure 11: current switching  
Figure 12: low impedance at V1 and V2  
Figure 13: replacing the load-devices (Rload)  
Figure 14: current-mirror replaces current-source  
Figure 15: Differential pair with offset  
Figure 16: Offset of a 2-input (N)AND  
Figure 17: Influence of temperature on a differential pair  
Figure 18: 2 cascoded differential-pairs  
Figure 19: three cascoded differential-pairs  
Figure 20: Current behaviour of an inverter without load  
Figure 21: inverter string of N inverters  
Figure 22: Inverter dissipation as function of the load capacitance  
Figure 23: Short-circuit current as function of different load capacitances  
Figure 24: specified 2-input (N)AND gate  
Figure 25: N cascaded inverters, build with 2-input (N)ANDs  
Figure 26: specified 2-input EX(N)OR gate  
Figure 27: N cascaded 2-input EX(N)OR-gates  
Figure 28: specified master-slave flip flop  
Figure 29: cascaded master-slave flip flop  
Figure 30: Circuit diagram of the full adder  
Figure 31: N cascaded full adders  
Figure 32: Temperature vs. differential input of NslowPfast-analysis

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Figure 33: Temperature vs. differential input of NtypPtyp-analysis
Figure 34: Input- and output signals after 10 cascaded full adders
Figure 35: Influence of temperature on a (N)AND
Figure 36: Determination of the delay-time of a cell
Figure 37: Power dissipation of one (N)AND-cell
Figure 38: Output signal after 9 (N)AND-gates
Figure 39: The flipflop as two-divider
Figure 40: Output signal after 9 cascaded full-adders
Figure 41: MCML full-adder vs. Standard CMOS full-adder
Figure 42: Output-voltage reduction due to increasing frequency
Figure 43: MCML (N)AND vs. Standard CMOS (N)AND
Figure 44: MCML flipflop vs. Standard CMOS flipflop
Figure 45: DSB to SSB conversion
Figure 46: Coarse schematic of the Hilbert transformer
Figure 47: Folded configuration of the Hilbert transformer
Figure 48: Output signals of the Hilbert-transformer

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Abstract

In digital circuits there are two aspects of major importance, namely low-power and high-speed. The standard CMOS design method contains both these aspects, it is fast and it dissipates little power. Although this last aspect depends very much on the operating frequency, because the power dissipation of a standard CMOS cell increases linear with the frequency. The standard CMOS design method dissipates little power for low frequencies, but what happens when this frequency goes above the 100 MHz. In this report we are interested in a minimum signal-frequency of 126 MHz, and the question if there are other design methods that dissipate less power than standard CMOS above this 126 MHz, will be answered in this report.

When digital circuits are combined with analog circuits on the same chip, a problem occurs. The standard CMOS digital cells create large spikes on the powersupply during switching, that will have a negative effect on the analog cells. These spikes can cause errors in the analog circuits, so these spikes have to be reduced, before they can reach the analog circuits. Normally the analog circuits are masked form the digital circuits, which results in a large space between the two circuits, resulting in a large chip-area. If we can find a new digital design method that produces only little spikes on the powersupply during switching, this masking will be unnecessary, resulting in a strong reduction of chip-area.

The new digital design method must

- be as fast, or faster, than standard CMOS,
- produce smaller spikes on the powersupply than standard CMOS
- dissipate less power than standard CMOS in the signal-frequency range above the 100 MHz

Before I started searching, I examined the power dissipation of a standard CMOS cell, and came to the conclusion that the power dissipation depends on the powersupply, voltage-swing, operating-frequency and the load-capacity. With these parameters in mind I found several design methods. After testing these design methods the MCML (Mos Current Mode Logic) came out best. This MCML design method will be discussed extensively in this report, and will be compared with the standard CMOS design method. The standard CMOS design method will therefore also discussed extensively in this report.

The MCML design method uses differential signals, which will also be discussed in this report. An important drawback of this MCML-method is the fact that the low-value of the input signal is not zero, but a value of x volt. If this low-value is applied to the gate of a MOS-transistor, this transistor will not be entirely off, as in standard CMOS, but a leakage-current will flow through that transistor. The minimum low-value of the input signal will also be determined in this report.

The cells which will be discussed in MCML and in standard CMOS are the “Full adder”, “Master Slave Flipflop”, “EX(N)OR” and the “(N)AND”. After the MCML-cells were extensively tested, it seemed that they dissipate approximately 20% - 60% less power than the standard CMOS-cells, measured in a signal frequency-range between 120 MHz and 400 MHz.

The spikes on the powersupply are 20 times smaller, than by the standard CMOS design method. The MCML method is 20% faster than the standard CMOS method, measured at a signal-frequency of 126 MHz.

The cells that are build in MCML are tested in a string of identical cells, and are implemented in an 8-bit Hilbert transformer. There are layouts of the cells given in this report.

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Chapter 1: Introduction

In this report a method for designing logic-gates, which will be used in a digital signal processing-environment, will be discussed. These logic-gates will be used in a high-speed low-power library.

The current high-speed low-power CMOS library that is currently used in Philips Nat.lab. consists of standard CMOS-gates. These standard CMOS gates have the property that they produce large spikes on the powersupply during switching. When these standard CMOS gates are used in a digital-circuit, this circuit produces a lot of switching noise on the powersupply. This switching noise becomes very important when we combine analog- and digital-circuits on the same chip. This switching noise has a negative effect on the analog-circuit. To reduce this switching noise the analog-circuit has to be masked from the digital-circuit, which is expensive and costs a lot of space on the chip.

When a new method can be found, that produces little spikes on the powersupply during switching, the analog- and digital-circuits can be placed beside each other on the same chip, which results in fewer costs (no masks) and smaller chip-area.

Another very important aspect for the new design-method is the power dissipation, this must be lower then the standard CMOS method. The standard CMOS design method has a power dissipation that increases linear with frequency. It is therefore almost impossible to find a design method that has a lower power dissipation over the entire frequency-range. This is also not necessary because the design method that we are looking for in this report must have a minimum signal-frequency of 126 MHz. So we are looking for a design method that dissipates less power than the standard CMOS design method for frequencies higher then 126 MHz (signal frequency).

The power dissipation of a cascaded standard CMOS-gate can not be easily calculated, because there are aspects as short-circuits (during switching), load-capacities and switching-speed that are of major importance in this power dissipation. In this report we will discuss this power dissipation of the standard CMOS-gates extensively, because we can retrieve several strategies for low-power design methods from these discussions. It is therefore a good start to examine the power dissipation of the standard CMOS cell, and check if there are parameters that can be influenced in such a way that the cell will dissipate less power. These parameters must be kept in mind when we are looking for other design methods.
Chapter 2: Low-power strategies

2.1 Introduction

Power dissipation is one of the most important design parameters for CMOS. This is not only true for battery-operated systems, but also for other systems like high-throughput digital communication and digital video processing in multimedia applications. After a short introduction of CMOS power dissipation, this chapter will present several strategies for low-power high-performance CMOS circuits. The equations that are stated in this chapter are quoted from [Nol 95].

2.2 CMOS Power Dissipation

For the calculation of the power dissipation of a CMOS gate, a CMOS inverter will be used, see figure 1.

The total power dissipation of this inverter can be split up into three different parts, namely

- The dynamic part $P_d$, which results from charging and discharging the output node capacitance $C_{eq}$ (figure 1). The output capacitance $C_{eq}$ will be charged when $V_{in} = \text{low}$.
and will be discharged when \( V_{in} = \text{high} \). When \( V_{in} = \text{high} \) the NMOS-transistor will conduct, while the PMOS-transistor is closed. When \( V_{in} = \text{low} \) the PMOS-transistor will conduct, while the NMOS-transistor is closed. The voltage swing \( \Delta V \) over the output node capacitance results in a charge difference of \( \Delta Q = \Delta V \cdot C_{eq} \) and leads, for the case of a periodic signal, to a DC supply current component of \( I_{dd} = f \cdot \Delta V \cdot C_{eq} \). With \( P = V \cdot I \) this results in \( P_c = f \cdot \Delta V \cdot C_{eq} \cdot V_{dd} \).

- The dynamic part \( P_{sc} = f \cdot V_{dd} \cdot Q_{sc} \) results from the short circuit current, which flows directly from \( V_{dd} \) to ground, while both p- and n-type transistors are conducting. \( Q_{sc} \) is the time integral of the short-circuit current over one signal period (figure 1). \( P_{sc} \) is less then ten percent of \( P_{tot} \). This ten percent results from tests, that were done by [Nol 95].

- The static part \( P_{leak} = V_{dd} \cdot I_{leak} \) results from leakage currents (\( I_{leak} \)) through diodes and sub-threshold transistor currents. \( P_{leak} \) is far less then one percent of \( P_{tot} \), see [Nol 95].

The total power dissipation of the CMOS inverter can be determined by adding these three parts, which results in

\[
P_{tot, gate} = \sigma \cdot f \cdot V_{dd} \cdot (\Delta V \cdot C_{eq} + Q_{sc}) + V_{dd} \cdot I_{leak} \tag{EQ 1}
\]

The factor \( \sigma \) represents the switching activity of the gate output node in relation to the clock frequency (i.e. \( \sigma = 1 \) for a clock signal, and \( \sigma = 0.5 \) for a maximum data rate featuring one transition per clock period).

Due to measurement [Nol 95], the first dynamic part seems to be the most important part, because the second dynamic part is less then ten percent of the total power dissipation and the static (third) part is far less then one percent of the total power dissipation.

### 2.3 Power Reduction Strategies

The dominating part of the total power dissipation is the first dynamic part \( P_c \). If we neglect \( P_{sc} \) and \( P_{leak} \), the total power dissipation will result in \( P_c = \sigma \cdot \Delta V \cdot f \cdot V_{dd} \cdot C_{eq} \). This equation shows that we have three parameters that can be influenced:

- The switching statistic \( \sigma \).
- The supply voltage \( V_{dd} \) and the voltage swing \( \Delta V \).
- The total nodal capacitance \( C_{eq} \).

One important drawback of reducing \( V_{dd} \) is the loss in maximum speed. Maximum speed is according to

\[
f_{\text{max, long}} \approx \frac{(V_{dd} - V_f)^2}{V_{dd}^2} = V_{dd} \tag{EQ 2}
\]

in the case of a long channel transistor and is according to

\[
f_{\text{max, short}} \approx \frac{(V_{dd} - V_f)}{V_{dd}} = 1 - V_f/V_{dd} \tag{EQ 3}
\]

in the case of sub-micrometer short channel transistors, respectively. The parameters that are of interest are the supply voltage and the voltage swing, the switching statistic and the total nodal capacitance are of less interest, because they are difficult to influence at transistor-level. In chapter 5.4 a method to reduce the influence of the nodal capacitance will be discussed.
Chapter 3 : Possible methods

3.1 Introduction
Several methods for designing low power CMOS-circuits will be discussed in this chapter. These circuits will be used in a DSP (Digital Signal Processing) environment, and have to full fill the following demands:

- The power-dissipation has to be low (preferable lower than standard CMOS)
- The signal-frequency has to be at least 126 MHz
- The spikes on the powersupply have to be minimum

Theoretical solutions for the first demand were discussed in chapter 2. During my library-research I kept these low-power-strategies in mind. The methods which were found after an extensive library-research will be briefly discussed in this chapter. These methods will be explained with the help of the schematic of a (N)AND-gate.

3.2 Mos Current Mode Logic (MCML)
A MCML circuit consists of an input-stage, an output-stage and one or more constant current sources. The input-stage consists of an NMOS-tree, and the output-stage consists of load-devices. A 2-input (N)AND MCML gate is stated in figure 2. When the inputs A and B are both high, the current $I_{ss}$ will flow through the transistors $M_{11}$ and $M_{21}$, resulting in a voltage-drop over the left load device. The output $Q'$ will contain the value $V_{dd} - V_{load device}$, where as the other output $Q$ contains the value $V_{dd}$, because a zero current flows through the right load device, resulting in a zero voltage drop. For any other input-combination the current $I_{ss}$ will flow through the right load device, and the zero current will flow through the left load device. The differential output ($Q - Q'$) will always be equal to the voltage drop over the load device.

The voltage-swing can be kept smaller than standard CMOS, because the low-level must be higher than 0 Volt. This is necessary because the MCML-cell is never 'off', the current $I_{ss}$ will always flow through the cell from $V_{dd}$ to $V_{ss}$. So a low-input-voltage must be high enough to let the cell operate. The high input-level is equal to $V_{dd}$. More about these input-signals will be discussed in chapter 5 and chapter 7.4.
An advantage of MCML is the use of current-routing instead of current-switching (standard CMOS), resulting in smaller spikes on the powersupply. Another advantage over standard CMOS is the use of differential signals, which makes the use of inverters superfluous.
3.3 Source Coupled Logic (SCL)

A 2-input (N)AND SCL gate which is build in SCL is shown in figure 3. A SCL-cell consists of an input-stage, an output-stage and several constant current-sources. The input-stage consists of an NMOS differential tree, which is biased with the current-source $I_{ss1}$. The output-stage consists of several load-devices, which are connected to the gates of NMOS-transistors, see figure 3. The NMOS differential tree is used to route the current $I_{ss1}$ from one of the load devices to $V_{ss}$ resulting in a differential voltage between the gates of the transistors $M_1$ and $M_2$. This differential voltage between the gates of the transistors $M_1$ and $M_2$ is retrieved in the same way as the differential output is retrieved by the MCML-gate of figure 2. The current $I_{ss2}$ will flow constant through the transistors $M_1$ and $M_2$, resulting in a nearly constant gate-source-voltage ($V_{gs}$) of the transistors $M_1$ and $M_2$. If the voltage at the gates of the transistors $M_1$ and $M_2$ changes, this will result in a similar change of voltage at the outputs $Q$ and $Q'$.

SCL has the same advantages over standard CMOS as MCML, however there is one drawback, namely SCL uses three current sources whereas MCML uses only one current source. This increasing of current sources will increase the power dissipation.

When we compare SCL with MCML, we can conclude that these two methods are almost equal, except for the source followers that are added to the system.

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3.4 Folded Source Coupled logic (FSCL)

A 2-input (N)AND gate which is build in FSCL is shown in figure 4. The input-stage consists of an NMOS differential tree, which is biased with the current-source $I_{ss1}$. The output stages are either PMOS or NMOS diode connected load devices, biased with the two current-sources $I_{ss2}$. The current $I_{ss1}$ will flow from node $Qc$ to $V_{ss}$ or from node $Q$ to $V_{ss}$, so that the currents through the two diode loads will be $I_{ss2}$ or $I_{ss2} - I_{ss1}$. The voltage at the nodes $Q$ and $Qc$ will be $I_{ss2} \cdot R$(diode load) and $(I_{ss2} - I_{ss1}) \cdot R$(diode load), resulting in a differential voltage between the two nodes of $I_{ss1} \cdot R$(diode load).

The FSCL-(N)AND has two transistors less than a SCL-(N)AND, but has the same disadvantage as the SCL-(N)AND, namely it uses three current-sources, where a MCML-(N)AND uses only one current-source. This high count of current-sources results in a higher power dissipation than MCML.

The spikes on the powersupply of FSCL are small compared to standard CMOS, which is an important feature of all the previous methods (values of spikes on the powersupply can be found in chapter 4.) The high- and low-level of the input signals are equivalent to those of the MCML-cell.
3.5 Complementary Pass-transistor Logic (CPL)

The main concept behind CPL is the use of an NMOS pass-transistor network for logic organisation, as shown in figure 5. CPL consists of complementary inputs/outputs, an NMOS pass-transistor logic network, and CMOS output inverters. These inverters can be replaced by PMOS latches, as shown in figure 5.

The high level of the pass-transistor outputs (nodes Q and Q') is a threshold voltage lower then the supply voltage. This loss in output voltage can be pulled up by PMOS latches or CMOS output inverters.

To maintain high speed switching and to make sure that the output signal has the same voltage swing as the input signal, it is necessary to use the PMOS latches or the output inverters. This has the disadvantage that spikes occur on the powersupply during switching.

The input voltage-levels are equivalent to those of standard CMOS, and this has the disadvantage that the voltage-swing is equal to V_{dd}.

Figure 4 : 2-input (N)AND FSCL gate
3.6 Swing Restored Pass-transistor Logic (SRPL)

SRPL is very similar to CPL, because it uses the same NMOS pass-transistor network. The two cross-coupled inverters are used for recovering the output signal, see figure 6.

An advantage of pass-transistor logic is its simplicity, but a disadvantage of SRPL is similar to a disadvantage of standard CMOS, namely the spikes on the power-supply that occur during switching. A SRPL-cell has the same (dis)advantages as a CPL-cell.
3.7 Double Pass-transistor Logic (DPL)

The switching tree of a DPL gate consists of both NMOS and PMOS pass-transistors, in contrast to the switching tree of a CPL gate, where only NMOS transistors are used. Full-swing operation is attained by simply adding PMOS transistors in parallel with the NMOS transistors. However, this addition will result in increasing input capacitance. The switching tree of a CPL gate consists only of NMOS transistors, which results in a lower input capacitance. The full-swing output-voltage restoration of a DPL-gate is done by the combination of an NMOS and a PMOS transistor, instead of the PMOS-latches or inverters which are used by CPL. A DPL 2-input (N)AND gate is given in figure 7.

![Figure 7: DPL 2-input (N)AND gate](image)

The input-signals of the DPL-cell are equal to the input-signals of the CPL-gate, which results in a voltage-swing of $V_{dd}$ Volt.
This chapter contains the arguments that I used when I decided that MCML is the most appropriate design method. The gates that are discussed in chapter 3 will be tested for delay-time, power dissipation and spike-currents.

There is an output capacitance of 30fF added to the outputs of the gates discussed in chapter 3. For testing these gates, the load-devices of these gates are replaced by ideal resistors of 50KΩ. The current sources are kept ideal, the powersupply is set to 2.5 Volt and the dimensions of the transistors are the same for all the gates. The input signals for the gates that use current-switching have a $V_{\text{low}}$ of 0 Volt and a $V_{\text{high}}$ of 2.5 Volt. The input signals for the gates that use current-routing have a $V_{\text{low}}$ of 1.25 Volt and a $V_{\text{high}}$ of 2.5 Volt. The current values of the current sources are kept as low as possible while maintaining an output voltage that has the same voltage-swing as the input signal.

The results of these tests are shown in table 1. Take into account that these results can only be used for a global overview, because this are worst-case values and there are different input-values used for different gates. The different input signals are used to create a practical situation for the different design-methods.

<table>
<thead>
<tr>
<th>Design Method</th>
<th>$I_{\text{peak}}$ ($\mu$A)</th>
<th>Power ($\mu$W)</th>
<th>Delay (nS)</th>
<th>$V_{\text{dd}}$ (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>DPL</td>
<td>~400</td>
<td>~60</td>
<td>~0.55</td>
<td>2.5</td>
</tr>
<tr>
<td>CPL</td>
<td>~400</td>
<td>~130</td>
<td>~0.50</td>
<td>2.5</td>
</tr>
<tr>
<td>SCL</td>
<td>~70</td>
<td>~140</td>
<td>~0.50</td>
<td>2.5</td>
</tr>
<tr>
<td>CMOS</td>
<td>~400</td>
<td>~50</td>
<td>~0.40</td>
<td>2.5</td>
</tr>
<tr>
<td>MCML</td>
<td>~20</td>
<td>~60</td>
<td>~0.40</td>
<td>2.5</td>
</tr>
<tr>
<td>SRPL</td>
<td>~400</td>
<td>~130</td>
<td>~0.40</td>
<td>2.5</td>
</tr>
<tr>
<td>FSCL</td>
<td>~20</td>
<td>~150</td>
<td>~0.50</td>
<td>2.5</td>
</tr>
</tbody>
</table>

The results show that the current spikes of a pass-transistor design are approximately 20 times larger than those of the MCML design method. These current spikes are measured by measuring the current that flows through the powersupply. This current is than plotted, and the spikes can be seen and measured. The pass-transistor design methods do not have a significantly advantage over MCML and CMOS due to power dissipation and delay time. Therefore the pass-transistor design methods are not interesting for me.

When we look at the design methods that use a current routing design technique, we come to the conclusion that MCML comes out best.

The MCML-design technique will be discussed extensively in the rest of this report. When we forget the spike-currents, the standard CMOS design technique comes out best, therefore I will relate the tests of the MCML-gates to the standard CMOS gates.
Chapter 5 : Mos Current Mode Logic

5.1 Introduction

Standard CMOS is used in the current standard cell library (StC100Corelib), which has two important drawbacks, namely spikes occur on the powersupply during switching, and the power dissipation increases linear with frequency (P=CV^2f, where C is the load capacitance, V is the supply voltage and f is the frequency, see chapter 2).

MCML uses current routing instead of current switching, so the current remains almost constant, resulting in very little spikes on the powersupply during switching, and the power dissipation is almost constant for increasing frequency, until a certain point (which will be discussed in chapter 7.6).

In this chapter the (N)AND, EX(N)OR, Master Slave flipflop and the Full-adder will be designed on transistor-level. The W/L-values of the MOS transistors, the input-values, etc. will be determined in chapter 7. The operation of these gates will be explained with the help of the schematics of these gates.

While discussing these gates, the input signals will have values as 'high' and 'low', instead of numerical values.

Because MCML uses differential signals, the (dis)advantages of differential signals will be discussed in this chapter.

5.2 Several MCML gates

The MCML-gates, that are discussed in this report are based on the CML library which is designed with bipolar transistors, see [Pra 90]. In this chapter the (N)AND-, EX(N)OR, Full adder- and the Master Slave Flipflop will be discussed, in terms of how they operate, and how the coarse schematics look like.

5.2.1 2-input (N)AND gate

Figure 2 shows a 2-input (N)AND gate in MCML, which contains two differential pairs (M_{11}, M_{12}) and (M_{21}, M_{22}). The current (I_{ss}) is routed through the gate by steering the two differential pairs, so that I_{ss} will flow through one of the load devices, resulting in a voltage loss over the load device. If I_{ss} flows through the right load device, the outputs Q and Q' will contain respectively the values V_{dd} - I_{ss} \cdot R_{(load device)}(low) and V_{dd}(high). The differential output is therefore equal to I_{ss} \cdot R_{(load device)}. When the input signals A and B contain a logic 'high', this will result in a 'low' value for output Q' and in a 'high' value for output Q. Output Q represents the AND operation for the input signals A and B. When A and B are 'high', the input signals A' and B' will be 'low'.
5.2.2 2-input EX(N)OR gate

There are three differential pairs \((M_{11}, M_{12}), (M_{21}, M_{22})\) and \((M_{31}, M_{32})\) in the EX(N)OR gate, which is shown in figure 8. The output \(Q\) represents the EXOR operation of the input signals \(A\) and \(B\), whereas the output \(Q'\) represents the EXNOR operation of the input signals \(A\) and \(B\). The high and low values of the outputs are equivalent to those of the NAND-gate. In the truth-table (next to figure 8) the 'L' represents a low-voltage and a 'H' represents a high-voltage. When the gate of a transistor contains a 'H' this transistor will conduct, when the gate contains a 'L' this transistor will not conduct.

When the input signals \(A\) and \(B\) are both high or low the current \(I_{ss}\) will flow through the left load device, when the input signals contain other values the current \(I_{ss}\) will flow through the left load device.

![Diagram of 2-input EX(N)OR gate]

Figure 8 : 2-input EX(N)OR-gate

5.2.3 2-input D-FLIPFLOP

The positive edge triggered D-FLIPFLOP contains six differential pairs, which can be seen in figure 9.
The routing of the current remains the same, because there is always one transistor of a differential pair that conducts, while the other transistor is closed in an ideal situation. Take into account that the clock-frequency is twice the signal-frequency (according to Nyquist is $f_{\text{clock}} \geq 2 \cdot f_{\text{signal}}$). When the clock is low (clock' is high), the current $I_{ss1}$ will flow through the transistors $M_{S1}$ and either $M_{11}$ or $M_{12}$. When $D$ is high transistor $M_{11}$ will conduct, when $D$ is low transistor $M_{12}$ will conduct. During the time that the clock is low, nothing will change. When the clock changes from low to high, the transistors $M_{S2}$ and $M_{61}$ will start to conduct, while the transistors $M_{S1}$ and $M_{62}$ will conduct no current. The current $I_{ss1}$ will now flow through the transistors $M_{S2}$ and either $M_{21}$ or $M_{22}$, which depends on the values of the input signals $D$ and $D'$ just before the clock-signal becomes high. When input $D$ is high, transistor $M_{22}$ will conduct, or else transistor $M_{21}$ will conduct. At the same time he current $I_{ss2}$ will flow through the transistors $M_{61}$ and $M_{31}$ if $D$ is high or $M_{32}$ if $D$ is low. If the clock becomes low again, the current $I_{ss2}$ will flow through transistor $M_{41}$ or $M_{42}$, keeping the output signals $Q$ and $Q'$ constant during the time that the clock remains low. The outputs $Q$ and $Q'$ are now independent of the input signals $D$ and $D'$. The high and low values of the outputs $Q$ and $Q'$ are $V_{dd}$ and $V_{dd} - I_{ss} \cdot R_{\text{load device}}$. 

Figure 9: positive level triggered D-FLIPFLOP
5.2.4 3-input FULL ADDER

The full adder is the largest cell that will be discussed in this report, it contains nine differential pairs, and is shown in figure 10.

The full adder contains three inputs, including the carry-input. There are two outputs, namely one for the least significant bit (F) and a carry-output for the most significant bit (C0). The truth table for the full-adder is shown below.

<table>
<thead>
<tr>
<th>A0</th>
<th>A1</th>
<th>C1</th>
<th>F</th>
<th>C0</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>L</td>
</tr>
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<td>L</td>
<td>H</td>
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<tr>
<td>H</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>H</td>
</tr>
</tbody>
</table>

The inputs C1, A1 and A0 control respectively the top, middle and bottom row of differential pairs. The logic table shows the outputs (F and C0) for all possible input-values. It will take quite some time to discuss which transistors will conduct and which are closed for every input-combination. When the gate of a transistor contains a logic 'high', this transistor will conduct, when the gate contains a logic 'low' it will not conduct. This assumption can easily be made because the full-adder contains only NMOS-transistors and load-resistors at this moment.
5.3 Differential input signals

In this chapter are some (dis)advantages of differential input signals summarized. Every (dis)advantage will be discussed extensively.

5.3.1 Advantage of differential input signals

- If the delay of a gate is determined by the output-capacitance (wiring and input capacitance), this delay will decrease according to the logic voltage swing $V_s$.

$$t_d = \frac{C_{het} \cdot V_s}{I_{het}} \quad \text{(EQ 4)}$$

By the use of differential signals instead of non-differential signals, it is possible to divide the logic swing by two, while maintaining the rate between the transistors which are 'on' and 'off'. This current-ratio is a measure for the robustness of the gate.

- The use of a reference voltage for MCML can be eliminated by the use of differential signals (with exception of the current-source reference). Non-differential MCML uses one reference voltage for every transistor layer, this would add three reference voltages for a full adder (figure 10). One important drawback of reference voltages is that they use a lot of static power, which we try to keep as low as possible.

- The small logic voltage swing, that is allowed by differential signals, makes sure that crosstalk between two metal-layers on a chip is minimum. The crosstalk between two 'wires' is compensated when both the differential signals flow parallel through the chip, the signals will only be slightly delayed.

- The gates are (within certain limits) independent of little variations on the powersupply.

- The cell output of MCML contains the output signals and the complementary signals.

5.3.2 Disadvantage of differential input signals

- To keep crosstalk as low as possible it is wise to keep signal and it's complementary signal close to each other, which is almost an impossible task for routing-programs. If these signals use wires of different length this can lead to a shifting in time of one of the signals. This results in a time-difference between the signals. Another disadvantage is that the wiring-channels will increase with a factor two in chip-area. The latter disadvantage will be compensated with the disappearance of the reference voltages.

5.4 The effect of the wire-capacitance

When we connect the outputs of a cell to the inputs of another cell, the wire-capacitance is of major importance. When these interconnect wires are small, the wire-capacitance will be small and won't cause much of a problem for low frequencies. But if the frequency is high and/or these wires are long a problem will occur. These wire capacities cause a delay-time which reduces the operating bandwidth. The length of these wires cannot be exactly
calculated, because a routing-program determines the length of these wires. When two cells that have to be connected to each other are neighbours, the interconnect-wires will be short (wire-capacitance is small), but if the next cell is on the other side of the chip, these wires are relatively long, resulting in a large wire-capacitance. The delay of the output signal strongly depends on this wire-capacitance.

This wire-problem can be solved by placing the load-devices close to the input signals of the next cell. The next step is to reduce the voltage-swing to a minimum, and control the cell with a current, instead of a voltage-swing. Figure 11 shows a schematic of this principle.

The basic principle behind this idea is that the differential voltage swing at the points A and B is reduced to a minimum, resulting in a circuit that can carry a big wire-capacitance, without getting a large delay-time. The current that flows through $M_1$ or $M_2$ will also flow through one of the load-devices, resulting in a voltage-loss. This will create a differential voltage over the outputs $Q$ and $Q'$. The differential voltage swing at the points A and B can be kept low by creating a low impedance at these points, which is done by the cross-coupled transistors $M_1$ and $M_2$.

The transistors $M_1$ and $M_2$ of figure 11 can be replaced by current sources, see figure 12. The voltage swing at the points $V_1$ and $V_2$ can be reduced to a minimum by using transistors with a $g_m$ that is equal to the inverted value of the load-resistance, which can be seen in the next calculation.

$$V_{41} = V_4 - V_1, \quad V_{32} = V_3 - V_2, \quad g_m \cdot V_{41} = -i \quad (1)$$

$$V_4 = -R \cdot i \quad (2)$$

Substituting (1) in (2) gives,

$$g_m \cdot i \cdot R + g_m \cdot V_1 = i \rightarrow$$

$$V_1 = (1 - g_m \cdot R) \cdot i / g_m \rightarrow$$

$$g_m = 1 / R$$

Figure 11: current switching

Figure 12: low impedance at $V_1$ and $V_2
When the cross-coupled transistors have a $g_m$ of $1/R_{load}$, the wire-capacitance has become of minor importance. When we test this method in practice it seems impossible to make the $g_m$ of the cross-coupled transistors equal to $R_{load}$, therefore a little voltage swing at the points A and B will remain. Still this method is very useful, even for this little voltage-swing that remains.

5.5 Replacing the load-devices

The load-device can be replaced by a PMOS-transistor, because this transistor can be used as a pull-up function, whereas the NMOS-transistor can be used as a pull-down function. Because the pull-down function is done by the NMOS tree, it is useful to replace the load-devices by PMOS-transistors which can fulfil the pull-up function.

To create a resistor of a PMOS-transistor, the PMOS-transistor has to operate in its triode-area. This can be accomplished by connecting the gate to a reference voltage. This reference-voltage must be chosen in such a manner that the PMOS-transistor operates in its triode-area.

There are several methods for designing a reference voltage, for instance with NMOS- or PMOS-transistors. The most logical choice is the use of a PMOS-transistor, because if the loads are changing under influence of temperature, the PMOS will change in a similar way. The load-structure is stated in figure 13.

![Figure 13: replacing the load-devices ($R_{load}$)](image)

5.6 Replacing the current-sources

MCML uses several current-sources (the full adder uses three current-sources, figure 10), these current-sources are not easy to implement in an IC-design. It is therefore useful to replace these current-sources by a single current-source, and create other current-sources by using a current-mirror. There are several designs for current-mirrors, see page 66 of [Was 91]. In this report the most simple current-mirror is used, see figure 14.

If we compare figure 14 with figure 13, it shows that they are almost identical, except for the transistors (NMOS or PMOS), they are both current-mirrors, only used for different purposes.
If we want to create a current-mirror with an almost constant bias-current, the channel shortage effect is a very important effect. If we choose the channel-length of the bias-transistors in figure 14 to short, the drain-current of the NMOS-transistor will show a variation when the drain-source voltage slightly changes. It is therefore important to choose the channel-length in such a manner that the changes due to channel shortage effect are minimum. Take into account that the channel-length can't be chosen to large, because the drain-source voltage is limited to a maximum.

5.7 Input voltage-levels

In the previous chapters, the input-values were called 'low' and 'high', but were never specified. We want to use the same input-levels for all the gates, therefore the low- and high-input-value must be determined in such a way that all the gates operate under all conditions. The full adder is the largest cell in this report and is therefore titled as the worst-case situation. If we want to determine the input voltage-levels, the best way of doing this is to take the worst-case situation, namely the full adder. If the input voltage-levels are correct for the three level logic cell (full adder), they will be correct for any other two level logic cell in this report.

If we take a look at the full adder (figure 10) there are three input-levels, namely $A_0$, $A_1$ and $C_1$. These differential input signals will create an almost constant voltage at the sources of each row of transistors. Assume that the voltage at the sources of the transistors $M_{11}$, $M_{12}$, $M_{21}$, $M_{22}$, $M_{31}$ and $M_{32}$ have value $x$. The voltage at the sources of the transistors $M_{41}$, $M_{42}$, $M_{71}$ and $M_{72}$ will be $V_{ds}$ lower than $x$, etc. When we know the voltage which will be needed to let the current-sources (NMOS-current-mirror) operate, and the voltage across the load-devises (output voltage) is known, we can determine the minimum value of the powersupply.

We do not want to use level-shifters for the different signals because of the extra power needed, therefore the three levels of input signals will all have the same low and high voltages. This will have the drawback that the low value of the input signals will be equal to the highest low-level, namely the low-level of input signal $C_1$. This low-level will be determined in chapter 7.4.
6.1 Introduction

This chapter contains several calculations concerning MCML-gates, such as calculating the offset of several cascoded differential-pairs, e.g. the full adder has three cascoded differential-pairs. Another important issue due to differential input signals is the fact that one transistor of a differential-pair is conducting, while the other transistor is not entirely switched off, because the gate of this transistor contains the low-level voltage instead of zero volt, and is therefore conducting a little. The current that flows through a transistor that is weakly conducting, is called the leakage-current. A relation between input signal and leakage-current will be determined in this chapter.

The influence of temperature is a very important parameter and is therefore discussed. The last detail which will be discussed in this chapter is the comparison of power-dissipation versus frequency for MCML and standard CMOS.

6.2 Influence of offset on a (N)AND-gate

The offset-current of a MOS differential-pair depends on the difference in threshold-values between the two transistors, and the slope ($\beta_Q$) of the transistors. Before the influence of the offset on a (N)AND gate will be discussed, we will first calculate the offset-voltage of a differential pair. For the calculation of the offset-voltage of a MOS differential pair, I will refer to figure 15 where the two voltage-sources are replaced by one voltage-source ($V_{in}$).

In this report I assume that the W/L of the transistors are constant.

$K = W \cdot \beta_Q / L$

From now on I will use K instead of $\beta_Q$, when the term "$\beta$-mismatch" occurs, I will use the K-factors instead of the $\beta$-factors.

By using the general quadratic equations, the difference between $V_{GS1}$ and $V_{GS2}$ can be found for a general case:

$$I_1 = \frac{K_1}{2} \left( V_{GS1} - V_{T1} \right)^2 \rightarrow V_{GS1} = V_{T1} + \frac{2 \cdot I_1}{K_1}$$

$$I_2 = \frac{K_2}{2} \left( V_{GS2} - V_{T2} \right)^2 \rightarrow V_{GS2} = V_{T2} + \frac{2 \cdot I_2}{K_2}$$

$$V_{in} = V_{GS1} - V_{GS2} = \left( V_{T1} - V_{T2} \right) + \frac{2 \cdot I_1}{K_1} - \frac{2 \cdot I_2}{K_2}$$

By substituting $I_1 = I_2 = I_d/2$ in the above equation, we can derive the $V_{in}$ that is needed to create two equal drain-currents. This $V_{in}$-value is called the offset-voltage ($V_{offset}$).

$$V_{offset} = \left( V_{T1} - V_{T2} \right) + \sqrt{\frac{\left[ \frac{K_2}{K_1} - \frac{K_1}{K_2} \right]}{2 \cdot I_d \cdot K_1 \cdot K_2}}$$

(EQ 5)
Chapter 6: Theoretical debate

Assume that $K_2 = K_1 + \Delta K$ and $V_{T2} = V_{T1} + \Delta V_T$

Substituting these two equations into equation 5 results in

$$V_{offset} = -\Delta V_T + \sqrt{\frac{1}{K_1}} \left( \frac{\Delta K}{1 + \frac{\Delta K}{K_1}} \right)$$

This can be rewritten, by using $\sqrt{1+\Delta} \equiv 1 + \frac{1}{2} \cdot \Delta$, into

$$V_{offset} \equiv -\Delta V_T + \frac{\sqrt{\frac{1}{K_1}} \cdot \Delta K}{\left( \frac{1}{K_1} \cdot (2 \cdot K_1 + \Delta K) \right)}$$

(EQ 6)

When using $\Delta K / K_1 << 2$ this will result in,

$$V_{offset} \equiv -\Delta V_T + \frac{\sqrt{\frac{1}{K_1}} \cdot \Delta K}{\left( \frac{1}{K_1} \cdot (2 + \Delta K) \right)} \equiv \frac{1}{2} \cdot \frac{\sqrt{\frac{1}{K_1}} \cdot \Delta K}{K_1}$$

The 2-input (N)AND gate consists of two differential pairs, so first we will discuss one differential pair and expand the calculation to two differential pairs, namely the (N)AND gate (see figure 8).

By analysing a differential pair, we take the view that the differential pair is completely symmetrical, $M_1 = M_2$, $V_{T1} = V_{T2} = V_T$. This assumption can be made, because the threshold-mismatch and the $\beta$-mismatch are already placed into the offset-voltage (equation 5). This offset-voltage will be used as a voltage-source ($\epsilon_1$) in the next calculation. Further we take the view that both transistors are in strong inversion and that they will operate in saturation. The body effect and the channel shortage effect will be neglected.

The input-voltage will consist of an $\epsilon$-source in series with a signal-source, see figure 15.

Assume $\epsilon_1 = V_{offset}$ (see equation 6)

To simplify the calculation the next thesis are made

$$V_{gs1} - V_{T1} = A$$

$$V_{gs2} - V_{T2} = B$$

Subtracting these thesis will result in,

$$V_{gs1} - V_{gs2} = A - B \quad (V_{T1} = V_{T2})$$

Substituting $V_{in} + \epsilon_1$ in $V_{gs1} - V_{gs2}$ results in,

$$V_{in} + \epsilon_1 = A - B$$

Figure 15 : Differential pair with offset
The drain-currents $I_1$ and $I_2$ can also be expressed in $A$ and $B$: 

$$I_1 = \frac{K}{2} \cdot A^2$$

$$I_2 = \frac{K}{2} \cdot B^2$$

The tail-current $I_s$ can now be expressed as:

$$I_s = I_1 + I_2 = \frac{K}{2} \cdot (A^2 + B^2)$$

For the differential-current $I_1 - I_2$, we can write the next equation,

$$I_1 - I_2 = \frac{K}{2} \cdot (A^2 - B^2) = \frac{K}{2} \cdot (A - B) \cdot (A + B)$$

(EQ 7)

Rewriting $A + B$ gives: $A + B = \sqrt{2 \cdot (A^2 + B^2) - (A - B)^2}$

(EQ 8)

Substituting equation 8 into equation 7 will result into,

$$I_1 - I_2 = \frac{K}{2} \cdot (A - B) \cdot \sqrt{2 \cdot (A^2 + B^2) - (A - B)^2}$$

Substituting $V_{in1}$, $\varepsilon_1$ and $I_s$ into equation 7 will result in,

$$I_1 - I_2 = \frac{K}{2} \cdot (V_{in1} + \varepsilon_1) \cdot \sqrt{\frac{4 \cdot I_s}{K} - (V_{in1} + \varepsilon_1)^2}$$

(EQ 9)

By substituting equation 5 into $\varepsilon_1$ of equation 9 an equation is retrieved were the $\beta$-mismatch and the threshold-mismatch of the MOS differential-pair can be seen.

In the next calculation the influence of the offset on a (N)AND-gate will be discussed. During this calculation the offset-voltage will be represented by the voltage-sources $\varepsilon_1$ and $\varepsilon_2$, see figure 16. This offset-voltage ($\varepsilon_2$) can be calculated in a similar way as the offset-voltage ($\varepsilon_1$), which was done in the beginning of this chapter. Because the calculation of $\varepsilon_2$ is almost similar to the calculation of $\varepsilon_1$, this calculation is not stated into this report.

The 2-input (N)AND gate can be built by cascoding 2 differential pairs, see figure 16.

![Figure 16: Offset of a 2-input (N)AND](image)
Chapter 6: Theoretical debate

For the differential pair $M_3$ and $M_4$, the above calculation can be repeated for the currents $I_3$ and $I_4$, resulting in,

$$I_3 - I_4 = \frac{K}{2} \cdot (V_{in2} + \varepsilon_2) \cdot \sqrt{\frac{4 \cdot I_s}{K} - (V_{in2} + \varepsilon_2)^2} \quad \text{(EQ 10)}$$

We can write for $I_1$,

$$I_1 = \frac{(I_1 + I_2)}{2} + \frac{(I_1 - I_2)}{2} \quad \text{(EQ 11)}$$

If we substitute equation 9 and $I_1 + I_2 = I_s$ into equation 11, this will result in,

$$I_1 = \frac{I_s}{2} + \left( K \cdot (V_{in1} + \varepsilon_1) \cdot \sqrt{\frac{4 \cdot I_s}{K} - (V_{in1} + \varepsilon_1)^2} \right) \quad \text{(EQ 12)}$$

$I_2$ can now be written in a similar way, because substituting $I_1 + I_2 = I_s$ into equation 12 will give an similar expression for $I_2$.

The equation for $I_3 - (I_2 + I_4)$ can be retrieved by subtracting $I_2$ from equation 10 which results in,

$$I_3 - (I_2 + I_4) = \frac{K}{2} \cdot (V_{in2} + \varepsilon_2) \cdot \sqrt{\frac{4 \cdot I_s}{K} - (V_{in2} + \varepsilon_2)^2} - \frac{I_s}{2} + K \cdot (V_{in1} + \varepsilon_1) \cdot \sqrt{\frac{4 \cdot I_s}{K} - (V_{in1} + \varepsilon_1)^2} \quad \text{(EQ 13)}$$

were the current $I_1$ can be found in equation 12.

6.3 Influence of temperature on a (N)AND-gate

The expression for the differential current $I_1 - I_2$ (see equation 9 with $\varepsilon = 0$) as function of $V_{in}$ (when we take into account that transistors of a differential pair are in strong inversion and in saturation) has only two parameters namely the factor $K$ and the tail-current $I_s$. Assume that the temperature for all the transistors is the same and remains constant, the K-factor remains constant, but when the temperature changes the K-factor will change as well. When the temperature increases, the transfer-curve will be ‘stretched’ in x-direction, see figure 17.

![Figure 17: Influence of temperature on a differential pair](image)

This ‘stretching’ along the x-as of the transfer-curve is caused by the K-factor, because the value of this K-factor decreases with increasing temperature. K can be written as,

$$K = \mu \cdot C_{ox} \cdot \frac{W}{L}, \text{ with } \mu = \mu_R \cdot \left( \frac{T}{T_R} \right)^{\gamma} \quad \text{(EQ 14)}$$
with 
\[ \mu = \text{mobility of the charge-carriers} \]
\[ \mu_R = \text{reference mobility} \]
\[ \beta = \text{temperature-exponent of } \mu \]
\[ C_{ox} = \text{specific oxide capacitance} \]
\[ T = \text{temperature} \]
\[ T_R = \text{reference temperature} \]

The most important parameter in this equation is the mobility \( \mu \), which is strongly temperature dependent.

When we substitute equation 14 into equation 13 this will result in an expression for the differential current where the offset-voltage and the temperature influence on the K-factor are variable.

### 6.4 Leakage-current in cascoded differential-pairs

The gates that are discussed in this report have a maximum of three cascoded differential-pairs, namely the full-adder, and a minimum of two cascoded differential-pairs. For the calculation of the leakage-current there are simplified versions of the two and three cascoded differential-pairs used, these figures are stated in figure 18 and figure 19. In these figures an ideal current-source is used, and the voltage-values after the load-devices are named \( V_{dd} \) and \( V_{low} \). Operational parameters of the MOS devices are obtained using the "Mosca" program.

#### 6.4.1 Leakage-current in 2 cascoded differential-pairs

Assume that the transistors \( M_1, M_2, M_3, M_5 \) and \( M_6 \) are operating in linear mode, and transistor \( M_4 \) is operating in saturation.

\[ M_2^* \text{ has a } W/L \text{ ratio with an } L \text{ that is twice the } L \text{ of } M_2 \]

\[ \text{ } = \text{ Voltage meter} \]

*Figure 18 : 2 cascoded differential-pairs*

In the following calculations the symbols A, B, ..., E are used instead of \( V_A, V_B, ... V_E \).
To simplify the next calculations, the following expressions concerning a MOS device are used:

\[
\begin{align*}
V_{DS} &= V_D - V_S \\
V_{GS} &= V_G - V_S \\
V_{GT} &= V_{GS} - V_T
\end{align*}
\]

By using transistor \( M_1 \) it is possible to determine the voltage at point A.

\[
I = \frac{K_1}{2} \cdot (2 \cdot V_{GT} \cdot V_{DS} - V_{DS}^2) = \frac{K_1}{2} \cdot (2 \cdot (V_{dd} - A - V_T) \cdot (V_{low} - A) - (V_{low} - A)^2)
\]

\[
\therefore = \frac{K_1}{2} \cdot (2 \cdot V_{dd} \cdot V_{low} - 2 \cdot A \cdot V_{dd} + A^2 - 2 \cdot V_T \cdot V_{low} + 2 \cdot A \cdot V_T - V_{low}^2)
\]

\[
\frac{2 \cdot I}{K_1} = 2 \cdot V_{dd} \cdot V_{low} - 2 \cdot V_T \cdot V_{low} - V_{low}^2 + A \cdot (2 \cdot V_T - 2 \cdot V_{dd}) + A^2
\]

\[
A_{1,2} = V_{dd} - V_T \pm \frac{1}{2} \sqrt{(2 \cdot V_T - 2 \cdot V_{dd})^2 - 8 \cdot V_{dd} \cdot V_{low} + 8 \cdot V_T \cdot V_{low} + 4 \cdot V_{low}^2 + \frac{8 \cdot I}{K_1}} \quad \text{(EQ 15)}
\]

The voltage at node D can be determined by using transistor \( M_4 \).

\[
I_{leak} = \frac{K_4 \cdot V_{DS}^2}{2} = \frac{K_4}{2} \cdot (V_{low} - D - V_T)^2 \quad \rightarrow \quad D = V_{low} - V_T - \sqrt{\frac{2 \cdot I_{leak}}{K_4}} \quad \text{(EQ 16)}
\]

The voltage at node E can be determined by using transistor \( M_5 \).

\[
I_{leak} = \frac{K_5}{2} \cdot (2 \cdot V_{GT} \cdot V_{DS} - V_{DS}^2) = \frac{K_5}{2} \cdot (2 \cdot (V_{dd} - E - V_T) \cdot (D - E) - (D - E)^2)
\]

Isolating parameter E will result in,

\[
E_{1,2} = V_{dd} - V_T \pm \frac{1}{2} \sqrt{(2 \cdot V_T - 2 \cdot V_{dd})^2 - 8 \cdot D \cdot V_{dd} + 8 \cdot D \cdot V_T + 8 \cdot D^2 + \frac{8 \cdot I_{leak}}{K_5}} \quad \text{(EQ 17)}
\]

The transistors \( M_2 \) and \( M_3 \) can be replaced by one transistor with a channel-length that is twice as long as the length of transistor \( M_2 \) and \( M_3 \) (taken into account that the channel-length and width of the transistors are the same), see figure 18. It is now possible to calculate the voltage at node C, by using the replaced transistor \( M_2^* \).

\[
I = \frac{K_2^*}{2} \cdot (2 \cdot (V_{dd} - C - V_T) \cdot (A - C) - (A - C)^2)
\]

Isolating parameter C will result in,

\[
C_{1,2} = V_{dd} - V_T \pm \frac{1}{2} \sqrt{(2 \cdot V_T - 2 \cdot V_{dd})^2 - 8 \cdot A \cdot V_{dd} + 8 \cdot A \cdot V_T + 8 \cdot A^2 + \frac{8 \cdot I_{leak}}{K_2^*}} \quad \text{(EQ 18)}
\]

Because all the voltage-nodes are known, it is now possible to create an expression for the voltage \( V_x \), with parameter \( I_{leak} \). Transistor \( M_6 \) is used to create this expression.

\[
I_{leak} = \frac{K_6}{2} \cdot (2 \cdot (V_T - C) \cdot (E - C) - (E - C)^2)
\]
Isolating $V_x$ will result in the next equation,
\[
V_x = \frac{\frac{2 \cdot I_{\text{leak}}}{K_6} + 2 \cdot E \cdot V_T - 2 \cdot C \cdot V_T - C^2 + E^2}{2 \cdot (E - C)}
\] (EQ 19)

This minimum voltage swing of a two level cell can now be calculated, with the help of equation 19. This voltage swing is determined by $V_{dd} \cdot V_x$, where $V_{dd} = 2.5$ Volt and $V_x$ is shown in equation 19. In this report I am interested in the low voltage ($V_x$) that is needed to retrieve a leakage-current of maximal 1% of the tail-current. If we calculate this low voltage, it will not be sufficient for the worst-case situation, because this $V_x$ is not calculated for a three level cell, which will be done in the next chapter.

### 6.4.2 Leakage-current in 3 cascoded differential-pairs

The conditions are similar to those in the previous chapter with 2 cascoded differential-pairs, see figure 19. A cascoding of three identical transistors can be replaced by a single transistor with an equal width and a three times larger channel-length, which can be seen in figure 19. First the voltages at the nodes A..E will be determined, so that they can be substituted in the equation for the voltage $V_x$, with the leakage-current as variable. These calculations are similar to the calculations of the previous chapter, so I only put the results down.

\[
A_{1,2} = V_{dd} \cdot V_T - \frac{1}{2} \sqrt{(2 \cdot V_T - 2 \cdot V_{dd})^2 - 8 \cdot V_{dd} \cdot V_{low} + 8 \cdot V_T \cdot V_{low} + 4 \cdot V_{low}^2 + \frac{8 \cdot l_{\text{leak}}}{K_1}}
\] (EQ 20)

\[
D = V_{low} - V_T - \frac{2 \cdot I_{\text{leak}}}{K_4}
\] (EQ 21)

\[
E_{1,2} = V_{dd} \cdot V_T - \frac{1}{2} \sqrt{(2 \cdot V_T - 2 \cdot V_{dd})^2 - 8 \cdot D \cdot V_{dd} + 8 \cdot D \cdot V_T + 8 \cdot D^2 + \frac{8 \cdot I_{\text{leak}}}{K_3}}
\] (EQ 22)

\[
C_{1,2} = V_{dd} \cdot V_T - \frac{1}{2} \sqrt{(2 \cdot V_T - 2 \cdot V_{dd})^2 - 8 \cdot A \cdot V_{dd} + 8 \cdot A \cdot V_T + 8 \cdot A^2 + \frac{8 \cdot I_{\text{leak}}}{K_2}}
\] (EQ 23)

\[
V_x = \frac{\frac{2 \cdot I_{\text{leak}}}{K_6} + 2 \cdot E \cdot V_T - 2 \cdot C \cdot V_T - C^2 + E^2}{2 \cdot (E - C)}
\] (EQ 24)

The minimum low input voltage ($V_x$) can now be determined for a three level cell, which is the worst-case cell in this report (full adder). If we calculate the minimum low voltage that is needed to obtain a leakage-current of 1% of the tail-current for the full adder, this will be a worst-case low voltage. Substituting $I_{\text{tail}} = 60 \mu\text{A}$, $I_{\text{leak}} = 0.6 \mu\text{A}$, $V_{dd} = 2.5$ Volt and the C100 parameters into equation 24 this will result in a worst-case value of $V_x = 1.1$ Volt, so the voltage swing is 1.4 Volt.
The transistors in the dotted areas are replaced by the transistors $M_2$ and $M_4$.

Transistor $M_2$ has a three times larger channel-length then the transistors in the large dotted areas, transistor $M_4$ has a two times larger channel-length then the transistors in the large dotted areas (the transistors outside the dotted areas all have the same width and length as the transistors in the large dotted areas).

Figure 19: three cascoded differential-pairs

6.5 Power dissipation MCML vs. Standard CMOS

In this chapter the power dissipation of MCML and standard CMOS will be compared. The power dissipation for MCML is quite simple, namely $I_{\text{tail}} V_{dd}$, where $I_{\text{tail}}$ is a constant value which will be routed through the gate.

The power dissipation for standard CMOS is not that easy to calculate, therefore an inverter will be discussed, because this is the most simple gate. This standard CMOS inverter cannot be compared with a MCML-inverter, because an inverter in MCML can be implemented by a simple wire (differential signals).

Still this detailed discussion will give a good view of the power dissipation of a standard CMOS-inverter, and other standard CMOS-cells, because a standard CMOS-cell always operates according to current-switching. This current-switching will be extensively discussed in this chapter.

Some calculations are too difficult and are therefore replaced by simulation values, see chapter 6.6. More information concerning this discussion on power dissipation of standard CMOS can be found in [Vee 84].
If we load a CMOS inverter with a capacitance, the power dissipation will consist of two components, namely a dynamic dissipation and a short-circuit dissipation. The first component can be expressed as 

\[ P_1 = C_L \cdot V^2 \cdot f \]

and the second as 

\[ P_2 = I_{mean} \cdot V \]

Since there is a difference in the short-circuit dissipation of an inverter without load and that of an inverter with load, we start this discussion on the basis of an inverter with zero load capacitance. For simplicity we assume that the inverter is symmetrical, which means that 

\[ K_n = K_p = K \text{ and } V_{T_n} = -V_{T_p} = V_T \]

During the period \( t_1 - t_2 \) (figure 20) the short-circuit current \( I \) increases from 0 to \( I_{max} \), the output voltage \( (V_{out}) \) will be larger than the input voltage \( (V_{in}) \) minus the threshold voltage \( (V_T) \) of the NMOST. As a consequence, the NMOS transistor will be in saturation during this period of time. Using the simple MOS formula, this leads to 

\[ I = \frac{K}{2} \cdot (V_{in} - V_T)^2 \quad \text{for} \quad 0 \leq I \leq I_{max}. \]

\[ \text{Figure 20: Current behaviour of an inverter without load} \]

This current will reach its maximum value when \( V_{in} \) equals half the supply voltage \( (V_{in} = V_{dd}/2) \), due to the assumption that the inverter was symmetrical. Another result of this assumption is that the current behaviour during the time period \( t_1 - t_3 \) will be symmetrical with respect to the time \( t_2 \).

The mean current during a time \( T \) (equal to one period of the input signal) can thus be written as

\[ I_{mean} = 2 \cdot \frac{2}{T} \cdot \int_{t_1}^{t_2} I(t) \, dt = \frac{4}{T} \cdot \int_{t_1}^{t_2} K \cdot (V_{in}(t) - V_T)^2 \, dt. \]  

(EQ 25)

Assuming equal rise and fall times \( (\tau_r = \tau_f = \tau) \) of the input signal (symmetrical) and a linear relation between the input voltage \( (V_{in}) \) and the time \( (t) \) during its transients it can be derived from figure 20 that 

\[ V_{in}(t) = \frac{V_{dd}}{\tau} \cdot t, \]  

(EQ 26)

and,
Chapter 6: Theoretical debate

\[ t_1 = \frac{V_R}{V_{dd}} \cdot \tau \quad \text{and} \quad t_2 = \frac{\tau}{2} \quad \text{(EQ 27)} \]

Substituting equations (26) and (27) into equation (25) results in

\[ I_{\text{mean}} = \frac{2 \cdot K}{T} \int_{\tau/2}^{\tau} \left( \frac{1}{\tau} \cdot t \cdot \frac{V_{dd}}{V_t} \right) \left( \frac{V_{dd}}{V_t} - t - V_t \right) dt \quad \text{(EQ 28)} \]

which has the solution

\[ I_{\text{mean}} = \frac{K}{12} \cdot \frac{V_{dd}}{V_t} \cdot (V_{dd} - 2 \cdot V_t)^3 \cdot \frac{\tau}{T} \quad \text{(EQ 29)} \]

From equation 29 and the expression for the short-circuit dissipation (\(P_2 = I_{\text{mean}} \cdot V\)) the following expression can be derived for the short-circuit dissipation of a CMOS inverter without load:

\[ P_2 = \frac{K}{12} \cdot (V_{dd} - 2 \cdot V_t)^3 \cdot \frac{\tau}{T} \quad \text{(EQ 30)} \]

As \(1/T = f\), equation 30 shows that this dissipation component is also proportional to the frequency of switching (\(\tau/T\)).

During the previous calculation several assumptions are made, namely that the rise-time is equal to the fall-time and the load capacitance equals zero. When we discuss a cascading of \(N\) inverter-cells, these assumptions are no longer valid, the load capacitance will be non-zero, and the rise- and fall-time will be different. When inverters are cascaded the rise-time of the second cell will depend on the fall-time of the first cell, on the switching speed of the second cell and on the value of the load-capacity. The above calculation satisfies a single inverter without load. The next step will be a cascading of \(N\) inverters, each with a load, see figure 21.

**Figure 21 : inverter string of \(N\) inverters**

For the next discussion the input signal \((V_{in})\) has the same shape as in figure 20, with a rise- and fall-time of 0.5 nSec, a high-time \((\tau_{\text{high}})\) of 3.4 nsec and a low-time \((\tau_{\text{low}})\) of 3.4 nsec, which is typical for all the tests in this report, and a powersupply \((V_{dd})\) of 2.5 Volt. The input signal of the second inverter has three possible shapes:

- The rise- and fall-time are equal to those of it's input signal \((V_{in})\).
- The rise- and fall-time are larger then those of it's input signal \((V_{in})\).
- The rise- and fall-time are smaller then those of it's input signal \((V_{in})\).

The voltage-swing remains the same for all the three possible shapes.

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These three possibilities strongly depend on the load-capacitance and the switching-speed of the inverters, which can be seen in chapter 6.6. The first situation is the most simple situation, because the previous calculation determines a worst-case power-dissipation for an inverter string, with the properties of the first situation. Figure 23 shows the short-circuit current versus load-capacitance of an inverter, which shows that the maximum short-circuit current occurs with a zero load-capacitance.

The next two situations (rise- and fall-time differ from the rise- and fall-time of $V_{in}$) are of more interest. I assume that the rise and fall time of the inverters are all equal, except the rise- and fall-time of the first inverter, these differ from the rest of the inverters. This assumption is tested in chapter 6.6. If we assume a zero load capacitance we take the worst-case short-circuit power dissipation. The short-circuit power dissipation of a string of inverters can be split up in two parts, namely for the first inverter and for the other inverters. The short-circuit power dissipation of the first inverter with zero load can be found in equation 30, with $\tau = 0.5 \text{ nSec}$. If we assume an ideal load, we can derive a worst-case short-circuit power dissipation for the string inverters. The power dissipation of each inverter can be calculated with a zero-load capacitance. For the other inverters the same equation for the short-circuit power dissipation can be used, only $\tau$ has a different value now, say $\tau'$. During tests with an inverter string it showed that the rise- and fall-time remain almost the same after the second inverter, therefore the total short-circuit power dissipation can be split up into two parts, namely the first inverter, and for the other inverters. The different values for $\tau$ can be found in chapter 6.6. For N inverters the total short-circuit power dissipation will result in

$$P_{\text{total}} = \frac{B}{12} \cdot (V_{dd}-2 \cdot V_T)^3 \cdot \tau' \cdot f + (N-1) \cdot \frac{B}{12} \cdot (V_{dd}-2 \cdot V_T)^3 \cdot \tau \cdot f$$  \hspace{1cm} (EQ 31)

For calculating the dynamic dissipation of N inverters, the load-capacitance is of major importance. For N cascaded inverters each with a load this would result in

$$P_{\text{total}} = N \cdot C_L \cdot f \cdot V^2$$  \hspace{1cm} (EQ 32)

Adding these two power-components up I would make an error, because $P_1$ is calculated with a string of N MOS devices with capacity loads, and $P_2$ is calculated with a string of N MOS devices without capacity loads. These two power-components give the maximum powerdissipation of an inverter string, numerical values are stated in chapter 6.6, where a similar inverter string is measured under similar circumstances.

6.6 Testing a string of Standard CMOS inverters

This chapter isn’t placed under chapter 7: Designing and measuring, because the tests of this chapter are strictly necessary for the theory in chapter 6.5. The inverter is not tested in MCML, because it seems a little odd to test a simple wire on it’s performance (an inverter can by made in MCML by switching the two wires, because MCML operates with differential-signals).

The inverter-string of figure 21 is build in cadence with the C100-library, where the PMOS and the NMOS parameters were retrieved from the StC100Corelib (standard CMOS-library). The length of the NMOS- and PMOS-transistor are both 0.5$\mu$m, the width of the NMOS-transistor is 0.8$\mu$m, and the width of the PMOS-transistor is 5.6$\mu$m.

First I will apply a signal (see figure 20, with the parameters as discussed in chapter 6.5) to the input of the first inverter, and measure the rise-time ($\tau_i$) of the next cell, and the rise-time after nine inverters, for several load-capacities. The results are stated below.
Chapter 6: Theoretical debate

Table 2: rise-time vs. load-capacitance

<table>
<thead>
<tr>
<th>load-capacitance</th>
<th>$\tau_r$ of input signal</th>
<th>$\tau_r$ after one cell</th>
<th>$\tau_r$ after nine cells</th>
</tr>
</thead>
<tbody>
<tr>
<td>2 fF</td>
<td>0.50 nsec</td>
<td>0.25 nsec</td>
<td>0.35 nsec</td>
</tr>
<tr>
<td>20 fF</td>
<td>0.50 nsec</td>
<td>0.40 nsec</td>
<td>0.45 nsec</td>
</tr>
<tr>
<td>50 fF</td>
<td>0.50 nsec</td>
<td>0.60 nsec</td>
<td>0.75 nsec</td>
</tr>
<tr>
<td>100 fF</td>
<td>0.50 nsec</td>
<td>1.10 nsec</td>
<td>1.20 nsec</td>
</tr>
</tbody>
</table>

From this test we can conclude that the first inverter determines the rise- and fall-time of the rest of the inverters (within certain margins).

For the next test I will measure the power dissipation, for different load-capacitance and different rise- and fall-time of the input signal, but other parameters (such as powersupply (2.5 Volt), signal-frequency (126 MHz) and temperature (25°C) are kept constant. The frequency of the input signal is kept constant, while the rise- and fall-time changes, by changing the high-, and low-time in such a way that the frequency of the input signal remains constant. The results of these tests are stated below.

$\tau_r = 0.25\text{ nsec}$:

<table>
<thead>
<tr>
<th>load-capacitance (fF)</th>
<th>power dissipation ($\mu$W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>7</td>
</tr>
<tr>
<td>2</td>
<td>8</td>
</tr>
<tr>
<td>20</td>
<td>24</td>
</tr>
<tr>
<td>50</td>
<td>54</td>
</tr>
<tr>
<td>100</td>
<td>101</td>
</tr>
</tbody>
</table>

$\tau_r = 0.5\text{ nsec}$:

<table>
<thead>
<tr>
<th>load-capacitance (fF)</th>
<th>power dissipation ($\mu$W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>24</td>
</tr>
<tr>
<td>2</td>
<td>24</td>
</tr>
<tr>
<td>20</td>
<td>45</td>
</tr>
<tr>
<td>50</td>
<td>67</td>
</tr>
<tr>
<td>100</td>
<td>112</td>
</tr>
</tbody>
</table>

The values for a rise-time of 1 nsec are not mentioned here, because the differences between the power dissipation by 1 nsec and 2 nsec are very small.
\( \tau_e = 2 \text{nsec} \):

<table>
<thead>
<tr>
<th>load-capacitance (fF)</th>
<th>power dissipation ((\mu\text{W}))</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>33</td>
</tr>
<tr>
<td>2</td>
<td>36</td>
</tr>
<tr>
<td>20</td>
<td>48</td>
</tr>
<tr>
<td>50</td>
<td>72</td>
</tr>
<tr>
<td>100</td>
<td>119</td>
</tr>
</tbody>
</table>

\( \tau_e = 3 \text{nsec} \):

<table>
<thead>
<tr>
<th>load-capacitance (fF)</th>
<th>power dissipation ((\mu\text{W}))</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>40</td>
</tr>
<tr>
<td>2</td>
<td>41</td>
</tr>
<tr>
<td>20</td>
<td>57</td>
</tr>
<tr>
<td>50</td>
<td>79</td>
</tr>
<tr>
<td>100</td>
<td>124</td>
</tr>
</tbody>
</table>

When we implement these values into one figure, this figure represents the power dissipation of the inverter as function of the inverter load capacitance, for several rise- and fall-times of the input signal, see figure 22.

\( \tau_e = 3 \text{nsec} \)
\( \tau_e = 2 \text{nsec} \)
\( \tau_e = 0.5 \text{nsec} \)
\( \tau_e = 0.25 \text{nsec} \)

\( \text{power dissipation (\(\mu\text{W}\))} \)

\( \text{100} \)
\( \text{10} \)
\( \text{1} \)

\( \text{1} \quad 10 \quad 100 \quad C_L \text{ (fF)} \)

\( \text{Figure 22 : Inverter dissipation as function of the load capacitance} \)
A third and last test will determine the spike-current through an inverter for several load-capacities (the rise- and fall-time are 0.5 nsec). The results are stated in figure 23.

Figure 23: Short-circuit current as function of different load capacitances
Chapter 7 : Designing and measuring

7.1 Introduction

The MCML-gates which are stated in chapter 5 have to be specified before they can be used in a test environment. In this chapter the transistors, input signals, current-sources etc. will be specified. When the gates are specified, they will be tested for several frequencies, load capacities, input signals, temperatures etc. A cell will be tested in a cascading of several equal cells. All this testing is necessary because these MCML-cells will be used in a library. So before we design these cells, the demands for these cells will be discussed. After these demands I will give the end versions of the specified cells first, and will then proceed with the testing of the cells, the discussions of the specifications of the cells and the input signals. This seems a somewhat odd order to give the final version of the cells before the cells are tested (which has a major influence on the specifications of the cells), and before the input signals are specified. Still it is done this way, to get an impression of the final version of the cells.

7.2 Demands for the library

Demands which are discussed earlier are low power, small spikes on the power supply and a signal-frequency of 126 MHz. But these are more general demands, instead of demands for a library. The demands for this library are,

- Operating temperature between -40 °C and +125 °C
- After a cascading of approximately 10 gates the output signal has the same shape as the input signal, without loss of voltage-swing
- Tolerance analysis methods have to be taken into account, such as worst-case analysis and non-worst-case analysis. These analyses are the “Slow-Nominal-Fast” analysis and the Monte Carlo analysis
- The input signal-sources and the powersupply have a tolerance of 10%
- Take the wire-capacity into account (~20 fF)

7.3 Designing the cells

In this chapter the cells will be designed and specified, during this designing several considerations have been made. The most fundamental consideration will be discussed in this chapter.

I started designing with transistors of minimum dimensions and a load-resistor of 50 KΩ. These load-resistors are replaced by PMOS-transistors, see chapter 5.5, which are biased at an approximately equal value of 50 KΩ. These PMOS-transistors are operating in their linear-region.

To determine the value of the powersupply and to specify the input signals I used the worst-case cell, namely the full-adder (figure 10). To keep the power-dissipation as low as possible we decided to use input signals without level-shifters, which has the consequence that the low-input-level is the same for all the input signals. It is important that the NMOS-tree still
Chapter 7: Designing and measuring

operates at this low-level, and contains the highest low-voltage-level in the full-adder, because the full-adder contains 3 cascoded differential-pairs which must all operate under all conditions. With the use of Mosca and measuring at worst-case situations (see chapter 7.4) a $V_{\text{low}}$ of 1.1 Volt seems acceptable (this 1.1 Volt is acceptable for a temperature of +125 °C, but can be higher for lower temperatures. This will be discussed in chapter 7.4). The powersupply is set to 2.5 Volt.

7.3.1 2-input (N)AND-gate

When we replace the load-devices and the current-source of figure 8 by PMOS-transistors, current mirrors and add the cross-coupled transistors (chapter 5.4), the cell can be tested. When I applied the transient input combination $A = B_c$ (and $A_c = B$) an error occurred. The output Q must be high while this input combination is applied, and output $Q_c$ must remain low. When the input signal changes from low to high (or high to low) there is a moment that the signals A and B are equal, and all transistors are conducting a little. Because the cell is not symmetrical, the left capacitor is discharged a little longer than the right capacitor. When this happens several times, the voltage over the left capacitor has dropped so far that the left cross-coupled transistor will conduct, which charges the left capacitor again. To prevent this voltage over the left capacitor from dropping, an extra transistor is added in the right branch, resulting in a symmetrical cell, see figure 24.

The channel-length and -width are determined after extensive testing of a string of these cells. This testing will be discussed in chapter 7.5.

Before this cell can be tested, a symbol of the dotted area will be made and the rest of the cell is biasing. A cascading of N cells is shown in figure 25.
Chapter 7: Designing and measuring

The biasing-circuit is equal for all cells that are discussed in this report, except for the bias-current, which has a different value for the master-slave flipflop and the full-adder.

7.3.2 2-input EX(N)OR-gate

By replacing the load-device and the current-source by mos-transistors and adding the cross-coupled mos-transistors to figure 8, the next cell is created (see figure 26).

This cell is tested in a string of N cells, where a symbol of the dotted area is made (a cell), and those symbols (cells) are then cascaded, which results in the next figure (figure 27).
Chapter 7: Designing and measuring

When we look at the truth table of figure 8 it shows that when holding input A at a constant high-level, the output is the inverted value of the input B, which is used in the cascading of these gates, see figure 27.

7.3.3 Master-Slave Flip Flop

The master-slave flip flop is tested in a different way than the other cells, which will be discussed extensively in chapter 7.5. After several tests (chapter 7.5) the specified cell is shown in figure 28.

Figure 27: N cascaded 2-input EX(N)OR-gates

Figure 28: specified master-slave flip flop
This cell was tested by transforming it into a divide by two stage. This is done by making a symbol of the dotted area and connecting the outputs to the inputs, where Q is connected to Dc, and Qc is connected to 0, see figure 29.

![Figure 29: cascaded master-slave flip flop](image)

The schematic as is shown in figure 29 doesn’t have any input signals. I put a pulse of x seconds on the output (also input, because connected) at the time t=0 to t=x (x << one clock-period), and after that time-period the flip flop will act as a divide by two stage (see chapter 7.5).

### 7.3.4 The full adder

The bias-current of the full adder is higher than the bias-current of the other cells, because it is the worst-case cell due to transistor count and it has three cascoded differential pairs, whereas the other cells only count two cascoded differential pairs. After extensive testing the full adder cell has the following circuit diagram, see figure 30.
Chapter 7: Designing and measuring

Figure 30: Circuit diagram of the full adder

Due to the three cascoded differential pairs, several problems occur, such as a higher low-voltage-level of the input signals, which results in a higher leakage-current and a higher bias current. The most important problem is the high leakage-current, which results in loss of voltage swing after several cascaded cells. One of the possible solutions was to find a way to build this full adder with only two cascoded differential pairs. The schematic for this full adder is stated in appendix I. During the tests of this full adder with two cascoded differential pairs other problems occurred, such as a higher power dissipation (due to 4 current sources, instead of only 3), and this cell was significantly slower. Taken these drawbacks into account I choose for the first method of three cascoded differential pairs.

Extensive testing of this full adder cell is done in chapter 7.S. This cell is tested in a similar way as the other cells, namely by making a symbol of the dotted area and making a string of these cells, shown in figure 31.
Figure 31: N cascaded full adders

7.4 Specify the input signals

The worst case cell is the full adder, as discussed in chapter 5.7, therefore this cell will be central in this chapter. The high input-level is equal to the power supply, because this is the highest level in the cell. The low input-level can’t be set to zero, because the cell wouldn’t operate any more, and is therefore set to a minimum value, see also chapter 5.7. If we choose this low input-level too high the leakage-current will be too high, see also chapter 6.4, which results in a reduced output-voltage after several cascaded full adders. It is impossible to make this leakage-current zero, because the transistors are always a little conducting due to this low input-level. In this chapter we try to find a suitable value for this leakage-current.

The leakage-current depends on several things, such as the low-level of the input signals, the temperature and the sort of analyses (NtypPtyp, NslowPslow, NslowPfast, etc.). Therefore we will take two full adder cells and connect them to each other as is done in figure 31, then we take two DC-signal-sources and connect them to the inputs A0 and A0'. Call these signal sources respectively A and A'. When we use the next Pstar-file, we can test the temperature vs. differential inputvoltage, with I_{ratio} = I_{leak}/I_{tail} as parameter. The tail-current is set to 60μA, see figure 31.

```
DC;
temp = -40, -20, 0, 20, 40, 60, 80, 100, 125;
E_C1 = 2.5;
E_C1c = 1.5;
E_A1 = 2.5;
E_A1c = 1.5;
E_A = 2.5;
E_A' = 2.0, 1.9, 1.8, 1.7, 1.6, 1.5, 1.4, 1.3, 1.2, 1.1, 1.0;
I_{ratio} = I_{leak}/I_{tail};
```
Chapter 7: Designing and measuring

\[ V_{\text{diff}} = E_A - E_{A'}; \]
\[ \text{file: Vdiff, Irate, Itail, Ileak;} \]
end;
run;

The current \( I_{\text{leak}} \) is measured in the first differential-pair, counted from the ground, and the tail-current (\( I_{\text{tail}} \)) flows through the current-mirror, see also figure 19. This test is done twice, namely for a typical analysis and for the worst-case analysis, namely the \( N_{\text{slowPfast}} \) analysis. Figure 32 shows a statistic temperature measurement of a full adder with an \( N_{\text{slowPfast}} \) analysis.

![Figure 32: Temperature vs. differential input of \( N_{\text{slowPfast}} \)-analysis](image)

Figure 33 shows the same test for an \( N_{\text{typPtyp}} \)-analysis.

Looking at the worst-case situation (figure 32), a current-ratio of 1% at 125°C is obtained with a differential input of 1.4 Volt. A ratio below this 1% is not acceptable, therefore I used a low-input voltage of 1.1 Volt (2.5V - 1.4V). This 1.4 Volt differential input-voltage will do fine for a typical analyse (see figure 33), because the current-ratio drops far below this 1% for a low-input of 1.1 Volt at 25°C.
Chapter 7: Designing and measuring

The gates (N(AND, EX(N)OR, Master Slave Flipflop and the Full adder) are designed in such a way that they produce a differential output-voltage of 1.4 Volt, while they retrieve a differential input-voltage of 1.4 Volt, while operating at an NslowPfast analysis at a temperature of 125°C. When we test the same gate at an NtypPtyp analysis at a temperature of 25°C, the output-voltage will drop to a differential voltage of 1 Volt. From chapter 6.3 we can see that the threshold-voltage of the NMOS- and PMOS-transistor increases when the temperature decreases. Beside this increasing threshold-voltage, the use of an NtypPtyp analysis instead of an NslowPfast analysis also has it's effect on the decreasing of the differential output voltage. A first intention would be, this 1 volt differential voltage is too small, but if we take a look at figure 33, and look 25°C and 1 Volt (differential) up we will find a current-ratio which is far below the 1%.

From this chapter we can conclude that the cells have to be dimensioned for a temperature of 125°C with a differential input-voltage of 1.4 Volt at an NslowPfast analysis, so that the output of each cascaded cell will be a differential voltage of 1.4 Volt.

To test this theory, I used a string of full adders (see figure 31) and did two tests, namely one at 125°C, NslowPfast, with a differential input-voltage of 1.4 Volt, while the other test is done at 25°C, NtypPtyp, with a differential input-voltage of 1 Volt. After 10 cascaded full adders, the output signals are shown in figure 34.
When we look at figure 34 it is obvious that the leakage-current is small enough for both the tests, so that the output voltage-swing isn't reduced after a string of ten gates, but has a voltage-swing that is almost equal to that of the input signal. This voltage-swing is 1 Volt for the second test (temp=25°C, NtypPtyp) and 1.4 Volt for the first test (temp=125°C, NslowPfast). From these tests we can conclude that the cells have to be specified for an 1.4 Volt differential input/output signal at a temperature of 125°C and tested for a NslowPfast-analysis.

7.5 Testing the designs

The cells, as discussed in previous chapters, will be tested in a string of identical cells. These tests will contain statistic-, dynamic-, worst-case-, temperature-, offset- and montecarlo-analysis. After these tests the cells will have the specifications as shown in chapter 7.3. In the beginning the gates were tested with ideal components, such as current-sources instead of current-mirrors and without wiring-capacity. This procedure of testing is discussed during the testing of the (N)AND-gate, but is not mentioned with the testing of the other gates, because this testing procedure is the same for all the gates.
7.5.1 DC-analysis of the (N)AND-gate

The first tests were done with ideal current-sources, instead of the current-mirror. In this test, I used a single cell as stated in figure 24 (without current-mirror) and measured the currents that flow through the cross-coupled transistors. This test was repeated for several differential input-voltages, several temperatures, for a typical analysis and a worst-case analysis. These results were put in a graphic with on the y-axe the difference of the two currents and on the x-axe the differential input-voltage, see figure 35.

\[ I_{diff}(\mu A) \]

\[ V_{diff}(V) \]

![Graph showing the influence of temperature on a (N)AND gate.](Image)

Not all the measured curves are drawn in figure 35, because none of the curves will be slower than the curve of a NslowPfast analysis at 125°C, therefore this situation is the worst-case situation. From this figure we can conclude that a differential voltage of 1.4 volt is sufficient to maintain a clear routing of the current through the gate under worst-case conditions. Another important issue of this test is that we can see if the gate is symmetrical, because when the differential input-voltage is zero, the same current will flow through the two cross-coupled transistors, resulting in zero differential current.

7.5.2 Transient-analysis of the (N)AND-gate

The first transient tests were done with a single (N)AND-gate with a current-source instead of a current-mirror without a load- or wiring- capacitor. After these tests the wiring-capacitor was added and the cell was tested again, which ended in the tests of a string of (N)AND-gates, with capacity and current-mirror, see figure 25.

When we change the temperature, this will effect the threshold-voltage of the mos-transistors. From chapter 6.3 we can retrieve that with an increasing temperature the threshold-voltage of a mos-transistor will decrease, so we will test this (N)AND-string also for several temperatures, between the -40°C and the +125°C. These tests will be done with typical and worst-case parameters, such as NtypPtyp, NslowPfast, etc.

transient;
\[
t = an(0, 100n, 200);
\]
\[
temp = -40, -20, 0, 20, 40, 60, 80, 100, 125;
\]

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Chapter 7: Designing and measuring

\[ E_X = \text{sinsq}(1.1, 2.5, 3.4n, 0.5n, 3.4n, 0.5n, 7.8n); \]
\[ E_{Xc} = \text{sinsq}(2.5, 1.1, 3.4n, 0.5n, 3.5n, 0.5n, 7.8n); \]

file: \( E_X, E_{Xc}, vn(y_1), vn(y_2), \ldots, vn(y_{N-1}) \);

\[
\text{pwr(cell 1), pwr(cell 2), pwr(cell N)}; \\
\text{end}; \\
\text{run};
\]

With this file we can measure the delay after each cell and we can measure the power-dissipation of each cell.

The delay of a cell can be measured by measuring the difference in time between the output- and the input signal (measured at 50% of the maximum voltage-level), see figure 36.

\[ V_{dd} = 2.5 \text{ Volt} \]

Figure 36: Determination of the delay-time of a cell

The signals as drawn in figure 36 are ideal, this is correct for the input signal of the first cell, because this signal comes directly from a signal-source (which is ideal). A more realistic output signal can be seen in figure 34, which represents an output signal of a full-adder after a string of 10 gates. For a string of (N)ANDs an almost equal wave-form will be measured. For these practical signals the delay-time is measured at exactly the same way as is stated in figure 36. When we take a look at the above figure it shows that there are two ways of measuring the delay-time, namely the rising edge and the falling edge of the signal, this is shown by the time-differences \( \tau_1 \) and \( \tau_2 \). In this case the cells are almost symmetric, and the input signal is symmetric, which results in just a slight difference of the delay-times. These differences are so small that they are of no interest to me. When we used a cell which is not symmetric \( (\tau_1 \neq \tau_2) \), both the delay-times should be taken into account.

For the string of (N)AND-gates, see figure 25, and an NtypPtyp-analysis with a temperature of 25°C and a \( V_{low} = 1.5 \text{ Volt} \) (see previous Pstar-file), the results are stated below.

- Delay between the input-signal and the signal after one gate : 0.28 nSec (rise-time)
- Delay between the input-signal and the signal after two gates : 0.72 nSec
- Delay between the input-signal and the signal after three gates : 1.18 nSec
- Delay between the input-signal and the signal after four gates : 1.65 nSec

The use of a \( V_{low} \) of 1.5Volt is correct for a typical analysis at a temperature of 25 °C, because this is discussed in chapter 7.4.

We can see that this delay increases linear with the number of cascaded gates, which is the reason that I didn't add more results to these four delay-times.
Chapter 7: Designing and measuring

When we change the temperature the low-voltage-level will change as well, which will result in a change in differential-output which results in different delay-times. The same thing will happen if we test the cells for a worst-case situation as an NslowPfast-analysis. These tests were done and they showed a similar wave-form as is stated in figure 34. The only difference between these tests are the low voltage-levels and the delay-times, but the tests were all successful for all the 10 cascaded (N)AND-gates and there are no voltage-drops measured.

With the command 'pwr(cell N)' the Pstar-file is the power dissipation of each cell is measured. The power dissipation is almost equal for all cascaded cells, figure 37 shows the power dissipation of one of the cells (the previous stated transient Pstar-file is used).

![Power dissipation of one (N)AND-cell](image)

**Figure 37**: power dissipation of one (N)AND-cell

The power dissipation can easy be calculated by, \( V_{dd} \cdot I_{bias} = 2.5 \cdot 45\mu = 112.5 \, \mu\text{Watt} \), which matches the measured power dissipation very well. The average value of this power dissipation can be calculated with the Cgap calculator, which results in an average power dissipation of approximately 112 \( \mu\text{Watt} \).

7.5.3 **Monte Carlo analysis of the (N)AND-gate**

In the Monte Carlo analysis the sample points are generated in a pseudo-random manner to simulate the actual manufacturing process. The Monte Carlo method generates values according to the component probability density functions. The MOS transistors which are placed close to each other on the chip are correlated with each other with a factor 0.8. This seems a suitable value for the C100 process. The Monte Carlo analysis is a 4\( \sigma \) analysis. More information about this Monte Carlo method can be found in [10 93].

In each cell of figure 25 we match the transistors that remain close to each other when they are placed on the chip, such as the PMOS-transistors, the cross-coupled transistors and the NMOS tree. In another test I matched every differential-pair separately, but that didn’t give other results then the matching of the entire NMOS tree. These groups of transistors are correlated to each other with a factor 0.8, which is done for every cell in the Pstar-file. In this test I used a transient-statistic test, which is shown in the next Pstar-file.
Chapter 7: Designing and measuring

statistics;
STATPROCES: C100DMA2 = 'C100DMA2';
c_1 (\text{PJEM1.CELL1, PJEM2.CELL1}) 0.8;
c_2 (\text{NJM2.CELL1, NJM3.CELL1}) 0.8;
c_3 (\text{NJM4.CELL1, NJM5.CELL1, NJM6.CELL1, NJM7.CELL1, NJM8.CELL1}) 0.8;
c_4 (\text{PJEM1.CELL2, PJEM2.CELL2}) 0.8;
..;
end;

trstat;
trials: 15;
seed: 1;
t = an(0, 100n, 200);
temp = -40, -20, 0, 20, 40, 60, 80, 100, 125;
E_X = \text{sinq (1.1, 2.5, 3.4n, 0.5n, 3.4n, 0.5n, 7.8n)};
E_{Xc} = \text{sinq (2.5, 1.1, 3.4n, 0.5n, 3.4n, 0.5n, 7.8n)};
file: \text{vn(Y1), vn(yz), .., vn(YN1), E_X, E_{Xc}};
end;
run;

The only transistors that I didn’t match are the current-mirror-transistors. The \text{NslowPfast-analysis} with temp = 125°C is the worst-case test, the output-signals after 9 gates are stated in figure 38.

The worst simulation has a \text{V_{high}} of 2.5 Volt and a \text{V_{low}} of 1.1 Volt, the other tests have a \text{V_{low}} which is slightly below the 1.1 Volt, and are therefore better. The signals have a \text{V_{high}} that has a little spike above the 2.5 Volt (overshoot).

![Figure 38: output signal after 9 (N)AND-gates](image)

7.5.4 DC-analysis of the EX(N)OR-gate
When we test the EX(N)OR-gate in the same way as the (N)AND-gate in chapter 7.5.1, the results will be similar to those of the (N)AND-gate. The EX(N)OR-gate is symmetrical, and has the same specifications as the (N)AND-gate. It was therefore predictable that the results would be similar to those of the (N)AND-gate. The single EX(N)OR-gate was tested for several temperatures and for several analysis, such as NtypPtyp and NslowPfast. The results are similar to those of figure 35, and are therefore not given.
7.5.5 Transient-analysis of the EX(N)OR-gate

The first transient tests were done with a single EX(N)OR-gate without load, with a current-source instead of a current-mirror and without a wiring-capacitor. After these tests the wiring-capacitor was added and the cell was tested again, which ended in the tests of a string of EX(N)OR-gates, with capacitor and current-mirror, see figure 27.

The transient tests were done with the same Pstar-file as discussed in chapter 7.5.2. The output signals have the same wave-forms as the wave-forms stated in figure 34. The delay time can be measured in the same way as was done in chapter 7.5.2, the results are stated below.

- delay between the input-signal and the signal after one gate: 0.29 nSec \( (\tau_1) \)
- delay between the input-signal and the signal after two gates: 0.77 nSec
- delay between the input-signal and the signal after three gates: 1.24 nSec
- delay between the input-signal and the signal after four gates: 1.74 nSec

When we compare these results with the delay-time results of the (N)AND-gate, we come to the conclusion that the EX(N)OR is a little slower then the (N)AND-gate. This slight difference can be explained by looking at the designs of the cells. The input signals of the (N)AND-gate only have to control one gate, where the input signals of the EX(N)OR-gate must control two gates, which can cause a little delay.

The power dissipation of the EX(N)OR-gates is equal to the power dissipation of the (N)AND-gates, and has the same wave-form, see figure 37.

7.5.6 Monte Carlo analysis of the EX(N)OR-gate

The transistors in the cells of figure 27 are matched in the same way as the transistors of the (N)AND-gate in chapter 7.5.3. The only difference is that the NMOS-tree now contains six transistors, instead of five in the case of the (N)AND-gate, therefore the fourth-line of the Pstar-file will correlate six transistors instead of five. The rest of the Pstar-file will remain the same.

It is not strange that the results are the same as those of the (N)AND-gates, because the two gates are almost identical due to specifications, and Pstar-file. The differences are so small, that I refer to figure 38 for the results.

7.5.7 DC-analysis of the Master-Slave Flipflop

The Maser Slave flipflop (figure 28) can be used perfectly for the recovery of a signal, because the clock-signal is always a signal-source and is therefore not deformed which will result in an optimal control of the lowest differential-pairs. The clock-frequency is minimum twice the value of the signal-frequency (Nyquist), which gives the flipflop enough time to create a reconstructed output-signal.

The outputs (gates of the left cross-coupled transistors) of the most left differential pair (controlled by D and D') are tested by offering several input signals to the inputs D and D', while keeping clock' at a high level. This test is done for several temperatures, and for typical as well as for worst-case situation. The results are even better than the DC-tests for the (N)AND-gate, see figure 35. These results are very predictable, because the (N)AND will switch two cascoded differential-pairs at the same time, whereas the flipflop switches in this
case only one differential-pair. When we hold the input signals \( D \) and \( D' \) at a constant value and offer several signals to the inputs clock and clock', still one differential-pair will switch, instead of two cascoded differential-pairs.

### 7.5.8 Transient-analysis of the Master-Slave Flipflop

The Master Slave Flipflop is tested in a different way than the other cells that are discussed in this report. This is done because of the simplicity of the way of testing, see figure 29. The test will represent a divide by two stage, which can be tested as N cascaded flipflops. The output will see an input, which is his own input in this case, instead of the input of the next cell. The next Pstar-file will be used for the tests.

```plaintext
circuit;
    vbr_1 (D, 0) 2.5;
    vbr_2 (D', 0) 1.5; /*where 1.5 Volt is used (typical), I used 1.1 Volt for a worst-case test*/
end;

transient;
    t = an(0, 100n, 200);
    temp = -40, -20, 0, 20, 40, 60, 80, 100, 125;
    E_clock = sinsq(1.5, 2.5, 1.5n, 0.5n, 1.5n, 0.5n, 4n);
    E_clock' = sinsq(2.5, 1.5, 1.5n, 0.5n, 1.5n, 0.5n, 4n);
    file: E_clock, E_clock', vn(y), pwr(cell);
end;
run;
```

The first part of this Pstar-file defines the values of the inputs \( D \) and \( D' \) (and outputs, because they are cross-coupled to the inputs) on \( t = 0 \) sec. After \( t = 0 \) this cell will act as a divide by two stage, see figure 39.
The rise-time is measured from the moment that the clock-signal reaches half its maximum value till the moment that the output-signal reaches half its maximum value. The fall-time is measured in a similar way, see figure 39. The results of the rise- and fall-time are stated in the above figure.

The power dissipation is measured with the command ‘pwr(cell)’ in the Pstar-file, which results in a similar figure as is stated in figure 37. The average power dissipation of the flipflop (measured with Cgap) is approximately 200 μWatt, which can also be calculated, 

\[
P = 2 \cdot I_{\text{bias}} \cdot V_{dd} \quad \text{(because there are two tail-currents)} = 200 \mu\text{Watt.}
\]

### 7.5.9 Monte Carlo analysis of the M.S. Flipflop

Because this cell produces a very steady signal (the best of all the gates in this report) it is not necessary to test this cell on matching-problems. When this cell is tested under worst-case conditions (NfastPslow, temp = 125°C) the output-signal remains very steady.

### 7.5.10 DC-analysis of the Full-adder

The best way to measure the leakage current is to apply a constant value to the inputs C1 and A1, see figure 30, and apply several input signals to the input A0. This is a worst-case test, because the low input-level will effect the lowest differential pairs the most which will result in a differential pair with one transistor conducting and the other will conduct a little (leakage current). This test will be done for several temperatures, NtypPtyp and the worst-case situation NslowPfast, the same Pstar-file will be used as in chapter 7.4. The figure that results from these tests is similar to that of figure 35, which confirms the tests of chapter 7.4, where the input signals are determined for the worst-case cell, namely the full-adder.

### 7.5.11 Transient-analysis of the Full-adder

The full-adder is tested in a similar way as the (N)AND- and the EX(N)OR-gate, namely in a string of cascaded full-adders, see figure 31. As input I used the same Pstar-file as used in the transient-tests of the (N)AND- and the EX(N)OR-gate. For a typical analysis (NtypPtyp) and at a temperature of 25°C, the delay-times are

- delay between the input-signal and the signal after one gate: 0.47 nSec (rise time)
- delay between the input-signal and the signal after two gates: 1.09 nSec
- delay between the input-signal and the signal after three gates: 1.82 nSec
- delay between the input-signal and the signal after four gates: 2.52 nSec.

When we increase the temperature, the output-voltage will decrease while the delay-time will increase. Under worst-case conditions (NslowPfast, temp = 125°C) the full-adder has an output-signal which has a voltage swing of 1.4 Volt (2.5V - 1.1V), see figure 34. Under typical conditions (NtypPtyp, temp = 25°C) the same full-adder has a voltage swing of 1 Volt (2.5V - 1.5V), see also figure 34.

The power dissipation is measured with the Pstar-command ‘pwr(cellN)’, and the average value is calculated with the Cgap calculator. When we calculate the power dissipation with Cgap or as follows \[V_{dd} \cdot 2 \cdot I_{\text{bias}}, \] both have the same result, namely 300 μWatt. The shape of the power dissipation is similar to that of figure 37.

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Monte Carlo analysis of the Full-adder

For this test I used the same Pstar-file as in chapter 7.5.3, with one difference, namely the statistics-block. The PMOS-load-transistors are correlated to each other with a factor 0.8, the cross-coupled transistors are also correlated with a factor 0.8 and the NMOS-tree is correlated with the same factor. An even more realistic test was the test were I correlated each differential pair of the NMOS-tree with a factor 0.8. After testing there were almost no differences between the two tests measurable. The output-signal after 9 gates is stated in the figure below.

![Figure 40: output signal after 9 cascaded full-adders](image)

From figure 40 we can see that all the different trails reach the 2.5 Volt and reach the 1.1 Volt or lower.

MCML- vs. Standard CMOS power dissipation

In this chapter the full-adder, the Master Slave flipflop and the (N)AND are tested on their power dissipation for several frequencies. After these tests, the same gates are copied from the StC100CoreLib (standard CMOS library) into an equivalent Cadence-design (built with C100-components) and tested in the same way. The results are plotted in a graph for every gate, which will result in graph where the power dissipation vs. frequency is plotted for the MCML- and the standard CMOS-version. The full-adder, Master Slave flipflop and the (N)AND which were build in standard CMOS are stated in appendix II. The EX(N)OR isn't used, because it is almost equivalent to the (N)AND. All these standard CMOS-cells are build in a similar way as was done for the MCML-gates, which are used to build a string of 10 cascaded cells, see appendix III. The power dissipation of a standard CMOS-cell is linear to the frequency, but is also linear to the number of branches which contain short-circuit currents. These aspects can be seen in the next graph. The power dissipation of the full-adder in MCML and Standard CMOS is stated in figure 41.
From chapter 6.5 we know that the power dissipation of standard CMOS is linear with the frequency, as can be seen in figure 41. The power dissipation of the MCML-cell remains constant for a period of time, but during increasing frequency, the output signal becomes less and less stable, and will finally decrease in voltage-swing, see figure 42. When this happens, W/L-rate of the PMOS-load-transistors has to be increased, which results in an increase of the bias-current to maintain the 1 Volt voltage-swing (typical circumstances). This adjustment of the PMOS-load-transistors happens at a signal-frequency of approximately 300 MHz.

Figure 41: MCML full-adder vs. Standard CMOS full-adder

Figure 42: output-voltage reduction due to increasing frequency
The same tests can be done for the MCML-inverter-string of figure 25, which will be compared with the tests of an equal inverter-string which is build with standard CMOS-(N)AND-gates. The standard CMOS 2-input (N)AND-gate is stated in appendix II and the schematic of the inverter-string is stated in appendix III. While using the same Pstar-file as is discussed in chapter 7.5.2, the next figure is achieved.

<table>
<thead>
<tr>
<th>Power/cell (µWatt)</th>
<th>NtypPtyp</th>
<th>Temp = 25°C</th>
</tr>
</thead>
<tbody>
<tr>
<td>Standard CMOS</td>
<td>MCML</td>
<td></td>
</tr>
</tbody>
</table>

Figure 43: MCML (N)AND vs. Standard CMOS (N)AND

The power dissipation of the EX(N)OR-gate shows an almost equal graph as the above graph of the power dissipation of the (N)AND-gate, and is therefore not shown.

A very important gate is the master slave flipflop, because the MCML-version is relatively small compared to the standard CMOS version (contains 9 branches), see appendix II, and therefore the difference in the power dissipation between the MCML-gate and the standard CMOS-gate will be larger compared to the other gates. The flipflop will be tested as a divide by two stage, as is shown in figure 39. For the standard CMOS master slave flipflop the test-schematic is shown in appendix III, and the cell-view is shown in appendix II. The cells are tested with the Pstar-file of chapter 7.5.8. The power dissipation vs. the frequency for the MCML- and the standard CMOS-master slave flipflop are shown in figure 44.

When we examine the three power dissipation-graphs it is obvious that the MCML master slave flipflop is superior in low power dissipation. The standard CMOS (N)AND-gate contains 2 branches and the standard CMOS full-adder contains 6 branches, but the standard CMOS master slave flipflop contains 9 branches, which results in the highest power dissipation. When we compare this to the MCML-versions, the master slave flipflop is smaller (power dissipation, and number of transistors) then the full adder.

It can also be seen that the power dissipation of the MCML-flipflop remains constant for a higher frequency then the other gates, this can be explained by the fact that the flipflop is controlled by an ideal clock-signal, whereas the other cells are controlled by the outputs of the previous cells (except the first cell, but this cell is ignored).
7.7 Delay-time of standard-CMOS-cells

In this chapter the delay-times of the standard-CMOS (N)AND and the full-adder are measured under typical conditions. These standard CMOS-cells are exactly the same as discussed in chapter 7.6, and are used in the same string of cascaded cells. The (N)AND and the full-adder are tested, because the (N)AND is the most simple cell in MCML, and the full-adder is the worst-case cell in MCML. The delay-times of the standard CMOS versions of the (N)AND and the Full-adder are stated below.

- Delay between input-signal and the signal after one NAND: 0.45 nSec (rise-time)
- Delay between input-signal and the signal after two NANDs: 0.96 nSec
- Delay between input-signal and the signal after three NANDs: 1.46 nSec
- Delay between input-signal and the signal after four NANDs: 1.95 nSec

- Delay between input-signal and the signal after one full-adder: 0.59 nSec (rise time)
- Delay between input-signal and the signal after two full-adders: 1.27 nSec
- Delay between input-signal and the signal after three full-adders: 1.94 nSec
- Delay between input-signal and the signal after four full-adders: 2.62 nSec

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Chapter 8 : Implementing the gates

8.1 Introduction

The gates are tested for all kinds of situations, but they were always tested in a string of identical gates. The next test will determine how the gates operate in a system application. For this test an 8-bit Hilbert transformer will be used. This Hilbert transformer will then be tested under typical circumstances, were I will put a certain bit-word on the inputs of the Hilbert transformer and check the output bit-words. When the output-words are correct, the second test will consist of offering a sampled sinus-wave to the Hilbert transformer.

8.2 Theory of the Hilbert transformer

The conversion of a DSB signal to a SSB signal can be accomplished by transforming the signal with a Hilbert transformer, see figure 45.

The frequency response of an ideal Hilbert transformer is given by

$$H_I(\omega) = e^{-j \frac{\pi}{2} \cdot \text{sgn}(\omega)}$$  \hspace{1cm} (EQ 33)

This is an allpass filter which imparts a phase delay of $\pi/2$ for positive frequency components, and a phase advantage of $\pi/2$ for the negative components. Thus, the output of the filter contains only the upper sideband of the input signal, which can be seen in the following expression

$$Y(\omega) = X(\omega) \cdot [1 + j \cdot H_I(\omega)] = \begin{cases} 2 \cdot X(\omega) & \omega > 0 \\ 0 & \omega < 0 \end{cases}$$  \hspace{1cm} (EQ 34)

The impulse response of the ideal Hilbert transformer can be retrieved by calculating the inverse Fourier transform of the frequency response (33), which will result in

$$h_I(n) = \begin{cases} 0 & n = 0 \\ \frac{\sin^2(\pi \cdot n/2)}{\pi \cdot n/2} & n \neq 0 \end{cases}$$  \hspace{1cm} (EQ 35)

Note that $h(n) = 0$ for all even n and $h(-n) = -h(n)$. It is some what dangerous to call this filter a Hilbert transformer, because page 70 of [Law 75] shows that a Hilbert transformer has the following frequency response

$$H(e^{j\omega}) = \begin{cases} -j & 0 \leq \omega < \pi \\ j & \pi \leq \omega < 2\pi \end{cases}$$  \hspace{1cm} (EQ 36)
Which shows that the filter in this chapter is shifted in phase, further it is the same filter as
the original Hilbert. For the convenience the filter in this chapter will be called a Hilbert
transformer.

8.3 Designing the Hilbert transformer

The Hilbert transformer that will be build with the MCML-gates is an 8-bit Hilbert
transformer. The schematic of the 8-bit Hilbert-transformer can be seen in figure 46.

When we implement the adders, substractors, registers and shifters into this coarse
schematic, a more detailed Hilbert transformer will be obtained. This more detailed Hilbert
transformer is a folded configuration, see figure 47.

The Hilbert transformer can be build in exactly the same way as is shown in figure 47,
because the components (adders and registers) are already in place. While building the
Hilbert we have to take into account that the Hilbert works according to the 2-complement bit
notation. The components A1 and A2 are full-adders and the components S1 and S2 are
substractors, which can be built with full-adders where the negative input (a + (-b)) has to be
presented in a 2-complement notation, which means that the bits are inverted and there is 1b
(LSB) added. A shifter of 0.5 can be created by shifting the MSB to the MSB-1 etc.

When I placed the cells (I used the cells as designed in chapter 7.3) in a schematic I made
sure that the clock-, ground-, powersupply- and the carry-lines are placed vertical, and placed
the signal-lines horizontal. When we take a look at the end design of the Hilbert transformer
in appendix IV, you can see that for every column of cells a bias-circuit is used, this can be
done because a column consists only of identical gates.
Chapter 8: Implementing the gates

8.4 Testing the Hilbert transformer

The Hilbert transformer (see appendix IV) will be tested in the following way,

- Put a bit-word at the input of the Hilbert, and check the output. As an input I used the bit-word \(01111111\)\(_{\text{b}}\), and after three clock-pulses the first word appears at the output, and after nine clock-pulses the last word will appear at the output. These words can be calculated with the help of figure 47, and can be easily verified with the output-words.

The next Pstar input-file is used for this test,

```
transient;
\[ t = \text{an}(0, 150n, 300); \]
\[ E_{\text{CLOCK}} = \text{sinsq}(1.5, 2.5, 3n, 0.5n, 3n, 0.5n, 7n); \]
\[ E_{\text{CLOCKe}} = \text{sinsq}(2.5, 1.5, 3n, 0.5n, 3n, 0.5n, 7n); \]
\[ E_{\text{b1}} = \text{sinsq}(1.5, 2.5, 25n, 0.5n, 10n, 0.5n); /*contains 2.5 Volt during 10nSec*/ \]
\[ E_{\text{b1e}} = \text{sinsq}(2.5, 1.5, 25n, 0.5n, 10n, 0.5n); /*contains 1.5 Volt during the same 10 nSec*/ \]
```
The output signals of the Hilbert transformer, while the above \texttt{Pstar-file} is applied, can be seen in figure 48.

![Figure 48: output signals of the Hilbert-transformer](image)

The output-words can also be determined from figure 47, which will result in the following bit-words,

- 000000111b
- 000000000b
- 001000110b
- 000000000b
- 110111000b
- 000000000b
- 111111000b

These words can also be found in figure 48, so we can conclude that the Hilbert-transformer is built correct, and operates correct.
Chapter 9 : Layouts

9.1 Introduction

In this chapter a layout of the cells (the dotted areas) as discussed in chapter 7.3 will be built. After there are layouts created of the cells, these layouts are tested with two checksets, namely with the Diva DRC check and the Diva LVS check. There are more checksets, but they are not used in this report, because I had too little time left to do these checks. The layouts of the (N)AND, EX(N)OR, Master Slave Flipflop and the Full adder are shown in appendix V. In this chapter I will discuss how the layouts were build and the two used checksets.

9.2 Creating a layout

For creating a layout of a schematic (the dotted area of a cell as shown in chapter 7.3) the Device-Level Editor (DLE) under Cadence is used. DLE is a layout program that lets you generate custom layouts from schematics. DLE compares the component connections in the layout with the connections in the schematic. DLE is used to show shorts, invalid connections, and incomplete nets, which helps to wire the design. By using DLE, the transistors and the input- and output-pins are given in a layout-window. DLE also shows which connections have to be wired to other connections, to create a layout of the used schematic. In the layouts I used metal1, metal2, metal3 and poly paths to wire the layout. The input-pins "load", "Vdd", "Vss" and "bias" are stretched vertically in the design and are made of metal3, where the rest of the input- and output-pins are placed as small pins below each other, and are made of metal1 (see appendix V). In this way identical cells can be placed above each other, because we can use the same bias-lines which can be placed through an entire column of cells. The other wiring is placed in a horizontal way through the design, and cannot interfere with the bias-lines, because the bias-lines are made of metal3, where the rest of the wiring is made of metal2, metal1 or poly. Beside the input-pins "Vdd", "Vss", "load" and "bias", metal3 isn’t used in the layouts.

When all wires are placed, the layout is tested with the Diva DRC check, which is discussed in chapter 9.3. When this DRC check is successful, the LVS check is applied. If this LVS check is successfully the connectivity of the layout and the schematic match. More information about this LVS check is given in chapter 9.3.

9.3 Used checksets

The first test that will be applied during the design of the layout (and when the layout is ready) is the Diva DRC check. The DRC checks a layout for design rule violations. When errors occur in the layout, these errors can be seen in the layout, because they are highlighted in the layout. I used a flat checking method, which means that all shapes, regardless of the hierarchy, in the layout are checked.

The next check is the Diva LVS check, which is not 100% save because it does not perform any device recognition. To guarantee a correct LVS check also Dracula LVS must be done. This is not done in this report because there wasn’t enough time available.
check can be done the layout must be extracted. This extraction step detects the connectivity. The LVS program runs on the extracted view. For running this LVS check several files have to be set, this information about the use of LVS and it's settings can be found in [C1095]. After successful extraction the actual LVS can be done. With Diva LVS the connectivity of the schematic is checked against the connectivity of the layout. For both views netlists are created and the netlists should match.
Chapter 10 : Conclusions

The MCML design method fulfils the demands that were stated in the beginning of this research. The spikes on the powersupply by MCML are approximately 20 times smaller than is the case with standard CMOS, measured for a 2-input (N)AND-gate. These spikes were also measured with the other gates, but are not mentioned in this report, because they are almost the same.

Another important issue is the power dissipation of the MCML-gates, which is lower than with standard CMOS designs. The MCML full adder dissipates less power than the standard CMOS full adder for the frequencies between 230 MHz and 420 MHz. The maximum power difference between the two full adders is 130 µW per full adder, at a clock frequency of 340 MHz. The MCML (N)AND dissipates less power than the standard CMOS version in the frequency range between 200 MHz and 420 MHz. The maximum difference is 90 µW per cell. The Master Slave Flipflop shows the largest difference, namely 500 µW per cell at 350 MHz. The MCML flipflop dissipates 200 µW at this frequency. The MCML flipflop dissipates less power than the standard CMOS version between the 130 MHz and the 450 MHz.

When we take a look at the delay-time of an MCML design and a standard CMOS design at a signal frequency of 126 MHz, the MCML design is approximately 30% faster than the standard CMOS design. This is an average value between the (N)AND and the full-adder.

The MCML design method uses differential signals whereas the standard CMOS design method does not. These differential signals have the advantage that inverters are no longer necessary. An inverter can be created by interchanging the two differential signals. When we take a look at the transistor-count of the MCML-gates and the standard CMOS gates, they have an approximately equal transistor count. A schematic which is build with MCML-gates has the advantage that there are no inverters needed. Therefore an MCML design will count less transistors than standard CMOS design. A disadvantage of an MCML design is the use of bias-circuits, which contain a current-source and three transistors. For every type of gate (M.S. flipflop or full adder etc.) a different bias-circuit can be used (except for the (N)AND and the EX(N)OR).

Another advantage of MCML is the calculation of the power dissipation, which can be calculated with a simple formula, whereas the calculation of the power dissipation of a standard CMOS design is very complex.
Chapter 11: Acknowledgement

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Chapter 12: References

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Appendix I: The Full adder with two cascoded differential pairs

This figure shows the full-adder when it is build with two cascoded differential pairs.
Appendix II: Standard CMOS designs

The next figure shows an inverter which is built with a (N)AND-gate, retrieved from the StCl100CoreLib. The inverter is added to retrieve an AND- and a NAND-gate, the MCML version also contains the AND and the NAND operation.

The next figure shows a Full-adder which is retrieved from the StCl100CoreLib.
Appendix II: Standard CMOS designs

The next figure shows a Master Slave Flipflop which is retrieved from the StC100CoreLib
Appendix III: Cascading of the standard CMOS designs

The standard CMOS full adder-cells are cascaded in the following way, which is identical to the cascading of the MCML-full-adder.

The standard CMOS (N)AND-cell is also cascaded in exactly the same way as the MCML-(N)AND-cell. The standard CMOS Master Slave Flipflop is also cascaded in the same way as the MCML-Master Slave Flipflop is cascaded.
Appendix IV: The 8-bit Hilbert-transformer

The Hilbert-transformer, build with the cells form chapter 7.3 is shown below.
Appendix V: Created layouts

The next figure shows the layout of an MCML 2-input (N)AND-gate, see the dotted area of figure 24.
The next figure shows the layout of an MCML 2-input EX(N)OR-gate, see the dotted area of figure 26.
The next figure shows the layout of an MCML Master Slave Flipflop-gate, see the dotted area of figure 28.
The next figure shows the layout of an MCML Full adder, see the dotted area of figure 30.