MASTER

Threshold voltage shift in amorphous organic field-effect transistors

Hendriks, R.H.

Award date:
2005

Link to publication
Final graduation report titled

Threshold voltage shift in amorphous organic field-effect transistors

by

Rutger H. Hendriks

23rd December 2004

Supervisors:
Dr. D. M. de Leeuw, Philips Research
Dr. P. A. Bobbert, Eindhoven University of Technology

Operational lifetime [h]

370 K

Organic semiconductor

a-Si

Philips Research Laboratories
High Tech Campus Eindhoven
Abstract

The operational stability of organic field-effect transistors has been investigated. The instability that is found, is due to a parallel shift in the threshold voltage. Similar to $a$-Si, the shift can be phenomenologically described by a stretched exponential. The parameters have been analysed and the intrinsic stability of organic semiconductors has been compared to that of $a$-Si. It was found that organic semiconductors are intrinsically more stable than $a$-Si. Moreover, in contrast to $a$-Si, the stress in organic semiconductors is also reversible.
# Contents

1 Introduction 1
   1.1 Historical perspective .................................. 1
   1.2 Semiconductors ......................................... 2
   1.3 Conjugated polymers .................................... 2
   1.4 Conduction ............................................. 3
      1.4.1 Energy bands in crystalline semiconductors ....... 3
      1.4.2 Hopping in polymeric semiconductors ............... 5
   1.5 The field effect transistor .............................. 5
   1.6 Energy band bending .................................... 6
      1.6.1 Flatband ........................................... 7
      1.6.2 Accumulation mode ................................ 8
      1.6.3 Depletion and inversion modes ..................... 8

2 Experimental details 9
   2.1 Transistor fabrication .................................. 9
      2.1.1 PTV ................................................. 9
      2.1.2 OC1OC10-PPV ..................................... 12
      2.1.3 P3HT .............................................. 12
      2.1.4 F8T2 .............................................. 13
   2.2 Experimental setup ..................................... 13
   2.3 Automating measurements ................................ 13

3 Measuring FET characteristics 15
   3.1 Transfer characteristics ................................. 15
      3.1.1 Linear region ..................................... 15
      3.1.2 Saturation region ................................ 18
   3.2 Mobility ................................................. 18
   3.3 Output characteristics ................................ 20
      3.3.1 Saturated region ................................ 20
      3.3.2 Linear region ...................................... 21
   3.4 Contacts ................................................ 21
      3.4.1 Ohmic contact ..................................... 21
      3.4.2 Schottky contact .................................. 21
   3.5 Threshold voltage shift ................................ 23

4 Theory 25
   4.1 Field-effect current in disordered systems .............. 25
   4.2 Stretched-exponential relaxation ........................ 27
5 Results

5.1 PTV stress
5.1.1 Transfer curves
5.1.2 Mobility curves
5.1.3 Output curves
5.1.4 Fitting transfer curves
5.1.5 Threshold voltage shift
5.1.6 Fitting threshold voltage shift

5.2 PTV stress recovery
5.2.1 Transfer curves
5.2.2 Output curves
5.2.3 Fitting transfer curves
5.2.4 Fitting threshold voltage shift

5.3 PTV stress temperature dependence
5.3.1 Relaxation time
5.3.2 Characteristic temperature

5.4 PTV stress recovery temperature dependence
5.4.1 Relaxation time
5.4.2 Characteristic temperature

5.5 Summary PTV
5.5.1 Sample 1
5.5.2 Sample 2
5.5.3 Sample 3

5.6 Other semiconductors

5.7 Overview
5.7.1 a-Si:H

6 Summary and conclusions

6.1 Goals
6.2 Methods
6.3 Conclusions
6.4 Technology assessment

Bibliography

A IBASIC program
B Solving differential equation
C Thermalisation energy
D Matlab transport model
Chapter 1

Introduction

This thesis deals with the instability of disordered organic field-effect transistors, i.e. transistors made of “plastic”, which are being operated continuously for large amounts of time and, as a result of this heavy use, no longer seem to exhibit their characteristic behaviour and stop working as intended. Here, measurements are performed that allow for comparing characteristic quantities of polymeric transistors with those of conventionally used transistors made of amorphous silicon (a-Si).

In this introductory chapter, some historical background is given on transistors, followed by a brief discussion of the concept of semiconductors. Next, conjugated polymers are introduced and their mechanism for conduction is explained by comparing it with that of crystalline semiconductors such as Si. Then the field effect transistor is introduced and its different operating modes are discussed.

In Chapter 2 the fabrication of the transistors is detailed, together with the experimental setup and the process of automating measurements.

Chapter 3 serves as an introduction to measuring field-effect transistors and details different operating modes and typical transistor behaviour.

A theoretical model for charge transport in organic transistors is given in Chapter 4, followed by a model copied from a-Si that describes the instability of continuously used field-effect transistors. This instability results in a shift of the device characteristics and is quantified by looking at the shift of the threshold voltage.

The stress and stress recovery measurements that were performed are explained extensively in Chapter 5 for a single organic field-effect transistor. Then the temperature dependence is investigated followed by an overview of the results obtained throughout this thesis. A comparison is made with other polymeric semiconductors found in literature and with a-Si.

In Chapter 6 a summary of the work done here is given together with the conclusions that were made.

1.1 Historical perspective

In 1947, three scientists named Bardeen, Brattain and Shockley, from Bell Laboratories, discovered how to make a point-contact transistor using some gold foil,
a triangular quartz crystal and a piece of germanium. Soon after, the germanium that was used as the semiconducting material was replaced by single-crystalline silicon and in 1960 the first integrated circuit was developed. Advancements in the field have been coming at a steady pace and this has accumulated in the fact that today, electronics, made of grains of sand, have found their place in almost all aspects of everyday life.

The same can be said for plastics, or organic materials. Their strength, low weight and processability make them very well suited as low-cost utensils or as a packaging and insulating material. In the 1960s, the photo-conductive properties of organic material were first looked at, but it wasn’t before chemically doped polyacetylene was investigated in 1977 that highly conductive polymers were discovered.

By combining materials with different properties, a wide range of new devices can be made such as polymer light-emitting diodes, solar cells and even flexible displays and flexible electronics. For these devices to be usable, the stability of polymer electronics has to be investigated and in particular the stability of polymer transistors, since they form the basic building block of most electronic devices. This thesis deals with measuring and quantifying this stability of polymer transistors.

1.2 Semiconductors

Solid-state materials can be categorised into three distinct groups based on their electrical conductivity $\sigma$ (expressed in units Siemens, where $1 \text{ S} \equiv 1 \text{ A/V}$), namely insulators, semiconductors and conductors. Insulators have very low conductivities on the order of $10^{-18} - 10^{-8} \text{ S cm}^{-1}$ (see e.g. [1]). Conductors have high conductivities ranging from $10^4$ to $10^6 \text{ S cm}^{-1}$. Semiconductors have conductivities in between those of conductors and insulators, and generally these conductivities are quite sensitive to temperature, impurity, electromagnetic field and illumination. It is this property that makes semiconductors invaluable in electronic applications.

The materials class of semiconductors can be divided into subclasses based on composition. Element semiconductors consist of a single species of atoms, such as silicon or germanium. These were the first materials to be investigated. In recent years, binary, ternary or even quaternary compounds were made, like e.g. GaAs, CdS, Al$_x$Ga$_{1-x}$As or Al$_x$Ga$_{1-x}$As$_y$Sb$_{1-y}$. Even more recently polymeric semiconductors were found. Examples are poly(p-phenylenevinylene) (PPV), poly(3-hexylthiophene) (P3HT) and poly(2,5-thienylene vinylene) (PTV).

1.3 Conjugated polymers

The polymeric semiconductors used in this thesis are all conjugated polymers, i.e. the backbone of the polymer chain consists of alternating double and single carbon-carbon bonds as shown in figure 1.1a. In the ground state, carbon has four electrons in the outer electronic level. Three electrons will form chemical bonds that have coplanar $sp^2$ hybridised orbitals which are at an angle of $120^\circ$. Note that a heavily doped metal can have a low conductivity, but this does not change the fact that it is a metal and not a semiconductor.
1.4. CONDUCTION

Figure 1.1: Schematic representation of the conjugated polymer polyacetylene. In (a) the molecular structure is shown. It consists of alternating single and double bonds, making polyacetylene a conjugated polymer. In (b) a schematic representation of the electronic bonds in polyacetylene is given. Three coplanar sp² hybridised orbitals form the chemical bonds and are called σ-bonds. The pₓ-orbitals form so-called π-bonds.

with each other. These bonds are called σ-bonds. The remaining electron will be in the pₓ orbital, perpendicular to the sp² hybridisation plane. Neighboring atoms will have overlapping pₓ orbitals and are said to be π-bonded, see figure 1.1b for a visualisation. The σ-bonds are associated with a highly localised electron density in the plane of the molecule and π-bonds establish a delocalised electron density above and below the plane of the molecule.

1.4 Conduction

As stated earlier, there is a large range in conductivity values for different materials. Since there is a large difference in structure between organic and inorganic materials, the range in conductivity must be explained using different models. The concept of energy bands can be used to qualitatively explain the range for inorganic semiconductors (1.4.1). Conductivity in organic semiconductors can be accurately described using the concept of variable range hopping (1.4.2).

1.4.1 Energy bands in crystalline semiconductors

Consider two identical atoms that are far apart. Their energy levels will be the same, meaning they will have the exact same energy. When they are brought
closer together, the interaction between the atoms will split the doubly degenerate energy level into two new levels. If \( N \) isolated atoms are brought together, the energy levels will likewise split into \( N \) separate, but closely spaced, energy levels. For large \( N \), this will essentially lead to a continuous band of energies, one for each subshell. When the distance between the atoms decreases further, these outer subshells will interact and overlap, causing their energy levels to join into a single energy band for that shell. If the interatomic distance is then brought to the equilibrium value, the energy band will split into a lower and an upper band, which are called the valence band and the conduction band respectively [1].

Take silicon as an example atom. Silicon has 14 electrons in total and these electrons are distributed over shells around the nucleus. The shells are labeled using the principal quantum number \( n \), which is a positive integer. The \( n = 1 \) and \( n = 2 \) shells contain 2 and 8 electrons respectively. They have an orbital radius much smaller than the interatomic separation in the crystal, i.e. the 10 electrons in those shells have deep-lying energy levels and are tightly bound to the nucleus. The four remaining electrons only partially fill the \( n = 3 \) shell, which causes them to be relatively weakly bound and allows them to be involved in chemical reactions. When silicon is in the crystal lattice, a valence and a conduction band will have formed and at \( T = 0 \) all four electrons in the outer shell of every silicon atom will be in the valence band because they will occupy the lowest energy states. The valence band will therefore be full and the conduction band will be empty.

The highest energy in the valence band is called \( E_V \) and the lowest energy in the conduction band is denoted by \( E_C \). The difference between them is called the band gap energy \( E_g \), so \( E_g = E_C - E_V \), and it is the energy required to move an electron to the conduction band, leaving a hole\(^2\) in the valence band. Because there are no energy states between \( E_V \) and \( E_C \), no electrons will have an energy in the bandgap. Therefore the bandgap is also referred to as the forbidden energy.

At elevated temperatures, some electrons can have enough thermal energy to cross the bandgap and occupy an energy level in the conduction band while leaving a hole behind in the valence band. Both the electron and the hole can then move through the semiconductor in opposite directions. They will transport charge and are therefore called charge carriers. Charge carriers can also be created by doping the semiconductor with impurities. The doping can be done using donors or acceptors. A donor has an excess electron and donates this electron to the conduction band, whereas an acceptor has an electron deficiency and takes an electron from the valence band, leaving behind a hole there. The electron in the conduction band and the hole in the valence band can then contribute to the transportation of charge.

Charge carriers moving through the semiconductor may encounter structural or chemical defects in the crystal. These defects introduce states in the forbidden energy gap and charge carriers may get trapped at such defect states. They will no longer contribute to the conductivity until they are released again from the trap site by absorbing a phonon.

\(^2\)When an electron is separated from the atom it belongs to, it leaves behind an electron deficiency. This deficiency can be filled by a neighboring electron and has then been moved in the direction opposite to the electron movement. The deficiency can therefore effectively be seen as a virtual particle with a positive instead of negative charge.
1.5. THE FIELD EFFECT TRANSISTOR

When the electronic wave functions of the defect states have sufficient overlap, then the charge carriers may also tunnel directly from one localised state to another, possibly by absorbing and emitting phonons. This phonon-assisted tunneling process is called “hopping” [2, 3]. Miller and Abrahams [4] calculated the tunneling transition rates at low temperatures. They found that the hopping from an occupied state \( j \) to an adjacent unoccupied state \( i \) takes place \( \nu_0 \) times per second, corrected for the tunneling probability and for the probability to absorb a phonon for hops upward in energy:

\[
\nu_{ij} = \nu_0 \exp \left( -2\gamma R_{ij} \right) \begin{cases} 
\exp \left( \frac{E_i - E_j}{kT} \right) & (E_i > E_j) \\
1 & (E_i < E_j)
\end{cases}
\]  

(1.1)

where \( \gamma^{-1} \) is a measure of the wave function overlap between the sites, \( R_{ij} \) is the distance between localised states, \( E_i \) is the energy at the state \( i \), \( k \) is the Boltzmann constant and \( T \) is the temperature. Here, \( \nu_0 \) is referred to as an attempt frequency and the exponent determines the amount of successful attempts, which are actually only very few. Although this model was developed to describe the hopping at very low temperatures, i.e. around \( T = 0 \), it is actually widely used at high temperatures too.

The variable range hopping model [5] is an extension to the Miller-Abrahams model and takes into account that, depending on the disorder of the system (energetic and structural), it can be favorable to hop over a longer distance with a low energy difference between sites, i.e. low activation energy, than over a shorter distance with a higher activation energy.

1.4.2 Hopping in polymeric semiconductors

As was explained in Section 1.3 on page 2, conjugated polymers consist of a chain of carbon atoms, that are alternatingly single or double bonded. Each carbon atom has one electron in the p\(_z\)-orbital that is \( \pi \)-bonded with its neighbors. On this atomic scale, the \( \pi \)-bonded electrons are delocalised. Typically the two energy bands, the highest occupied molecular orbital (HOMO) and the lowest unoccupied molecular orbital (LUMO), are narrow.

On a larger scale of around 5 nm, the conjugated polymer chains are interrupted by structural defects, such as chain kinks or twists out of coplanarity or by chemical defects, such as a nonconjugated sp\(^3\)-hybridised carbon atom on the polymer backbone. It is due to this disorder that the organic semiconductor can not simply be regarded as having two energy bands separated by an energy gap, like crystalline semiconductors can. Instead, a Gaussian distribution of energies applies to the charge transporting sites, i.e. to the individual polymer chains. This implies that all states are localised on one conjugated polymer chain. Charge transport is realised through a sequence of charge transfer steps between adjacent polymer chains in a manner similar to the hopping between defect states in inorganic semiconductors as explained in 1.4.1.

1.5 The field effect transistor

A field effect transistor (FET) is a device that can be switched between a conducting and a nonconducting state. It can then either transmit current or try
CHAPTER 1. INTRODUCTION

(a) (b)

Figure 1.2: Schematic representation of a Field Effect Transistor (FET) with (a) no voltages applied and (b) a negative voltage applied to the gate contact. Note they are not drawn to scale.

to resist current from passing through. These two states give rise to its name, which is an aggregation of the 'trans' of transmitter and the 'istor' of resistor. The capability to switch is why transistors are widely used as the basic building block of binary logic.

The FET can basically be viewed as a parallel plate capacitor, see figure 1.2a. One of the plates is called the gate electrode, or gate contact, and the other plate actually exists of two electrodes with a semiconductor in between. The electrodes are called the source and drain electrodes or contacts. An oxide layer electrically insulates the two "plates".

By applying a voltage $V_g$ to the gate electrode with respect to the voltages $V_s$ and $V_d$ applied to the source and the drain contact respectively, charge carriers are introduced in the semiconductor at the interface with the insulator, thereby forming a channel with excess positive or negative charge carriers, depending on the sign of the applied gate voltage, see figure 1.2b. This effect is called the field effect. The density of the charge carriers in the channel is a function of the applied gate voltage.

1.6 Energy band bending

Consider an isolated metal and an isolated p-type semiconductor. The energy band diagram for this situation can be seen in figure 1.3a. In this figure, the energy differences between the Fermi level and the vacuum level, called the work functions, are shown for the metal, $q\phi_m$, and for the semiconductor, $q\phi_s$. The energy difference between the conduction band edge of the semiconductor and the vacuum level is called the electron affinity $q\chi$.

When the metal and the semiconductor are brought together and an intimate contact is made, like is the case at the source and drain contacts of a FET (figure 1.2), the Fermi levels of the two materials will align and there will be a common Fermi level for both materials in the contact. Together with the continuous vacuum level, this gives a typical energy band diagram for a metal-semiconductor contact in thermal equilibrium as shown in figure 1.3b. The barrier that electrons and holes have to cross to move from metal to semiconductor or vice versa has a height $q\phi_{B_p}$ which equals the band gap minus
1.6. ENERGY BAND BENDING

Figure 1.3: Energy band diagram of a metal and a p-type semiconductor (a) not connected and not in thermal equilibrium, (b) connected and in thermal equilibrium.

Figure 1.4: Energy band level diagrams of an ideal metal-insulator-semiconductor structure at thermal equilibrium for a p-type semiconductor operated in the (a) flatband mode, (b) accumulation mode and (c) depletion mode.

the difference between the metal work function and the semiconductor electron affinity, i.e. \( q\phi_{B_p} = E_g - q(\phi_m - \chi) \).

Looking at the gate contact of a FET, a different type of structure is seen, namely a metal-insulator-semiconductor (MIS) configuration (figure 1.2). The insulator in this structure prohibits charge transport from the gate contact to the upper part where the source, drain and semiconductor are. As a result, the Fermi levels of these two parts are generally not equal.

For an ideal p-type semiconductor, the band bending diagrams corresponding to this configuration are given in 1.4 for the three possible operating regions: flatband, accumulation and depletion. These will be explained next.

1.6.1 Flatband

When a gate voltage is applied that is equal to the difference between the Fermi level of the gate metal and the semiconductor, no band bending will
occur at the semiconductor-insulator interface, meaning the energy bands in the semiconductor are flat. This gate voltage is called the flat band voltage, \( V_{FB} \), and the energy band diagram can be seen in figure 1.4a.

1.6.2 Accumulation mode

Applying a gate voltage below the flat band voltage, i.e. \( V_g < V_{FB} \), induces more positive charges, i.e. holes, in the semiconductor at the interface with the insulator and this mode of operation is therefore called the accumulation mode. The application of this voltage increases the Fermi level of the metal by \( qV_g \). Since the insulator does not permit charge to flow to the semiconductor, the Fermi level of the semiconductor does not change. The accumulation of holes at the semiconductor-insulator interface causes the energy bands to bend upward. The valence band then bends towards the Fermi level and the conduction band bends away from the Fermi level, see figure 1.4b.

1.6.3 Depletion and inversion modes

Application of a gate voltage above the flat band voltage, i.e. \( V_g > V_{FB} \), lowers the Fermi level of the metal. The Fermi level of the semiconductor doesn’t change. The energy bands now have to bend downward from the semiconductor bulk level to the interface level, figure 1.4c. Electrons are attracted by the applied gate voltage, filling up holes. The holes are therefore depleted and this mode is hence called depletion mode. For high \( V_g \), electrons, the minority charge carriers in a p-type semiconductor, are induced at the semiconductor-insulator interface and can become abundant over the holes (the majority charge carriers). This is called the inversion mode. Note that most organic semiconductors, especially the semiconductors that are used in this thesis, only operate in the accumulation mode, see e.g. [6].
Chapter 2

Experimental details

2.1 Transistor fabrication

The organic transistors that are investigated in this thesis are made using a standard process, where heavily doped \( \text{n}^{++} \) silicon wafers have an insulating \( \text{SiO}_2 \) layer, with a thickness of 200 nm, thermally grown on top. Gold source and drain contacts are then evaporated and photo-lithographically patterned on the insulating layer. The wafer itself is used as a common gate for all devices which results in a bottom gate, bottom contacts type device. The wafer is then cut into samples, that all have the same configuration of transistors with different types and sizes on them, see figure 2.1a. Ring transistors, figure 2.2, are present and also finger (interdigitated) transistors. The transistors used here, are all ring transistors, because in this type of transistors, the leakage current between drain and gate contact is minimal and any leakage between source and gate will have minimal effect on the current between source and drain. They are characterised by the dimensions \( L \) for length and \( W \) for width. \( L \) varies between 40 \( \mu \text{m} \) and 0.75 \( \mu \text{m} \) and \( W \) is the same for all ring transistors, namely 1000 \( \mu \text{m} \).

To minimise any effect of the contact resistance \( R_C \) on the measurements, transistors with a large channel length of 40 \( \mu \text{m} \) are used, figure 2.1b.

To complete the fabrication of the transistors, a thin semiconductor film is applied by spincoating a solution of the desired polymer on top of the sample. Standard spincoating conditions for all semiconductors are 5 seconds at 500 rpm, followed by 30 seconds at 2000 rpm. The resulting film thickness is around 200 nm. Most transistors need to be annealed in vacuum to remove any traces of the solvent or to convert the precursor (if one is used). After fabrication, the samples are handled in air. Storage is done under vacuum and shielded from light.

2.1.1 PTV

Transistors with PTV as the semiconductor are made using a 1 \% wt. solution of PTV in chloroform. The solution is spincoated on the sample using the standard procedure. The samples are then placed on a heating chuck and heated in vacuum to 190 °C for 5 minutes to convert the precursor to PTV, figure 2.3. Whenever the sample is exposed to air or when it has been stressed and it needs to recover, it is annealed in vacuum at 150 °C.
CHAPTER 2. EXPERIMENTAL DETAILS
2.1. TRANSISTOR FABRICATION

Figure 2.2: Schematic picture of a ring transistor, showing the channel width \( W \), which is the circumference of the active channel and the active channel length \( L \), which is the distance between source and drain.

Figure 2.3: Molecular structures of (a) the precursor used to make (b) poly(2,5-thienylene vinylene) (PTV).
2.1.2 \textit{OC}_{1}\textit{OC}_{10}\textit{-PPV}

A 0.4 % wt. solution of \textit{OC}_{1}\textit{OC}_{10}\textit{-PPV} in toluene or xylene is made using standard spincoating conditions. In figure 2.4 the molecular structure of \textit{OC}_{1}\textit{OC}_{10}\textit{-PPV} is shown.

2.1.3 \textit{P3HT}

Fabricating transistors with \textit{P3HT} as the semiconductor was done by spincoating a 2 % wt. solution of \textit{P3HT} in chloroform on the sample. The standard spincoating procedure was used. The \textit{P3HT} molecular structure is shown in figure 2.5. Annealing is done in vacuum at 160 °C.
2.1.4 F8T2

For transistors using F8T2, a solution of 0.2 % wt. F8T2 in xylene is made and spincoated on the sample using the standard procedure for spincoating. The molecular structure for F8T2 is shown in figure 2.6. Annealing the sample is done in vacuum at 120 °C.

2.2 Experimental setup

The samples with the FETs are placed on a heating plate inside a box where three probe needles are available to make contact to the source, drain and gate of the FET. To prevent leakage currents between the gate contact of the sample and the heating plate, a thin sheet of mica is placed on the chuck. To improve the thermal contact between the sample and the chuck, heat conducting paste is applied.

The heating element in the chuck is controlled by an actively coupled current-voltage supply, which can accurately set and monitor the temperature of the heating plate. The maximum temperature the chuck can be heated to is 170 °C.

The probes are connected to the inside of the box and on the outside triax cables provide a connection to a HP/Agilent 4155C semiconductor parameter analyser. The analyser can measure the source, drain and gate currents simultaneously. A vacuum pump is connected to the box, allowing pressures as low as $10^{-6}$ mbar to be reached inside the box.

2.3 Automating measurements

In this thesis, two types of measurements have to be alternated for exponentially increasing time intervals. This process is automated using a HP/Agilent semiconductor parameter analyser. The analyser can be programmed using IBASIC and can thus perform unattended measurements.

The program that was used is shown in Appendix A on page 65. It reads three files with predefined measurement parameters from disk. One file defines a gate sweep, another file details a drain sweep and the last file describes how
to stress. These types of measurements are explained in more detail in Section 3.1 on the facing page, Section 3.3 on page 20 and Section 3.5 on page 23 respectively. In short, a gate sweep measures the current between source and drain contact as a function of the voltage on the gate contact while the source-drain voltage is kept constant. A drain sweep is similar, except that the gate voltage is kept constant and the source-drain voltage is changed and the last measurement simply applies a constant voltage to the gate contact and applies zero voltage to both source and drain contacts. The results of all measurements are automatically written to disk.
Chapter 3

Measuring FET characteristics

When a voltage is applied to the gate contact of a Field Effect Transistor (FET), see figure 3.1a, charge carriers are induced at the interface between semiconductor and insulator (figure 3.1b) and they will travel between the source and drain contact when a voltage is applied to these contacts (figures 3.1c and 3.1d). The direction of movement depends on the sign of the applied source-drain voltage and the sign of the applied gate voltage, i.e. the sign of the induced charge carriers.

By keeping the source-drain voltage constant and varying the gate voltage, the so-called transfer characteristics of a FET can be determined. By changing the role of source-drain and gate voltage, i.e. by keeping the gate voltage constant and varying the applied source-drain voltage, the output characteristics of a FET can be found. Both characteristics will be explained below.

3.1 Transfer characteristics

The transfer characteristics of a FET are determined by applying a constant source-drain voltage $V_{sd}$ and determining the source-drain current $I_{sd}$ as a function of the applied gate voltage. This type of measurement is therefore also referred to as a gate sweep. Depending on the value of the applied source-drain voltage, it can be done in the linear and in the saturated region.

3.1.1 Linear region

When the source-drain voltage is much smaller than the gate voltage, i.e. when $|V_{sd}| \ll |V_g|$, the drain-gate voltage is about the same as the source-gate voltage, meaning the number of induced charges at the drain contact is about the same as it is at the source contact. The FET is then said to be operated in the linear region. An example gate sweep in the linear region can be seen in the upper curve of figure 3.2a and in the lower curve of figure 3.2b.

From these curves the threshold voltage $V_{th}$ can be obtained. In inorganic FETs, the threshold voltage is defined as the onset of strong inversion [1]. However, for most organic transistors no current is observed in the inversion mode
Figure 3.1: (a) Schematics of a field effect transistor with no voltages applied. (b) Positive charges are induced at the semiconductor-insulator interface, due to the applied gate voltage. Positive charge is indicated by + and negative charge by −. (c) Application of a negative voltage to the drain such that \( V_g < V_d \), i.e. in the linear region, leads to a non-uniform charge distribution and a current will flow from source to drain. (d) For drain voltages below the gate voltage, \( V_d < V_g \), i.e. in the saturation region, all positive charges are removed at the drain contact, i.e. a depletion zone is created.
3.1. TRANSFER CHARACTERISTICS

Figure 3.2: Example transfer $I - V$ characteristics of a $L = 40 \mu m$, $W = 1$ mm PTV ring FET operated at 35 °C in $10^{-6}$ mbar air and dark. Shown are the transfer curve in the linear region, $V_d = -1$ V, and in the saturated region, $V_d = -20$ V, in (a) a linear scale and (b) a logarithmic scale. The applied gate voltage starts at $+20$ V and decreases with 0.2 V steps to $-20$ V and increases again with the same step size to $+20$ V. Hysteresis is such that less current flows (below the threshold voltage) in the reverse sweep.
and they only work in accumulation mode. Therefore the threshold voltage is often defined as the gate voltage for which there is no band bending in the semiconductor, i.e. the gate voltage corresponding to the flatband condition, \( V_g = V_{FB} \) (see 1.6.1 on page 7). Since the variation in the channel current with the gate voltage is zero above \( V_{FB} \) and the channel current increases below \( V_{FB} \), the flatband voltage is also referred to as the switch-on voltage \( V_{so} \) [6]. As will be explained in Section 3.5, the shift in the threshold voltage will be of primary interest in this thesis and the threshold voltage shift is not influenced by using a different definition for the threshold voltage, as long as the definition does not change throughout a measurement. Since the switch-on voltage can easily be found experimentally by looking at the gate sweep and determining at which gate voltage a current starts to flow in the forward sweep between the source and drain contacts (figure 3.2b), this definition is used here.

The low-current curves that can be seen in figure 3.2b, for \( V_g > 5 \) V, are measured in the forward sweep and are very noisy. The return sweeps show a higher and constant current for \( V_g > 0 \) V. Both are caused by parasitic leakage.

The amount of current that flows between the source and drain contact, for a constant drain voltage, can be varied over orders of magnitude, by appropriately choosing the applied gate voltage.

The hysteresis in the curves is very small and such that less current flows on the reverse sweep below \( V_{th} \).

### 3.1.2 Saturation region

When the source-drain voltage is larger than the gate voltage, i.e. \( 0 < |V_g| < |V_{sd}| \), the drain-gate voltage is positive and no holes are induced at the drain contact. The FET is then said to be operated in the saturated region. An example gate sweep in the saturated region can be seen in the lower curve of figure 3.2a and in the upper curve of figure 3.2b.

### 3.2 Mobility

Mobility is the ease with which accumulated charge can move through a semiconductor under the influence of an electric field. In a FET it is the ease of moving from the source contact to the drain contact when a voltage is applied between them.

Consider a FET with an applied gate voltage \( V_g \). When the gate voltage is increased with a small incremental voltage \( \partial V_g \), this will give rise to an incremental increase in charge of \( C_i \partial V_g \), with \( C_i \) the capacitance per unit area [7]. The total incremental charge increase over the whole channel is then \( WLC_i \partial V_g \). If this charge increment has a mobility \( \mu \) and a small source-drain voltage is applied, then an incremental current \( \partial I_{sd} \) will flow according to

\[
\partial I_{sd} = \mu \frac{W}{L} C_i V_{sd} \partial V_g.
\]

Measuring the source-drain current as a function of the gate voltage at low drain biases provides the transconductance \( g_m \), using:

\[
g_m = \frac{\partial I_{sd}}{\partial V_g} \bigg|_{V_d \to 0} = \mu \frac{W}{L} C_i V_{sd}.
\]
3.2. MOBILITY

Figure 3.3: Example mobility curves determined from the transfer $I - V$ characteristics shown in figure 3.2. Both linear mobility (magenta circles) and saturated mobility (blue squares) are shown. The applied gate voltage starts at $+20$ V and decreases with 0.2 V steps to $-20$ V and increases again with the same step size to $+20$ V. Hysteresis is such that more current flows in the reverse sweep.

The field-effect mobility of the accumulated charge as a function of the gate bias can then be calculated using:

$$
\mu = \left( \frac{L}{WC_iV_d} \right) \frac{\partial I_{sd}}{\partial V_g} \bigg|_{V_g \rightarrow 0}.
$$

(3.3)

For disordered organic FETs it is demonstrated in [8] that, in spite of the strong variations in the local mobility in the active channel, the field-effect mobility from equation (3.3) is a relatively good estimate for the local mobility of the charge carriers at the interface.

To describe the mobility in the saturated region, the following equation is used:

$$
\mu_s = \frac{L}{WC_i} \frac{\partial^2 I_{sd}}{\partial V_g^2}.
$$

(3.4)

The mobility as a function of gate voltage corresponding to the gate sweep shown in figure 3.2 can be seen in figure 3.3. Shown are the mobility in the linear region and in the saturated region, calculated using equations (3.3) and (3.4) respectively.
3.3 Output characteristics

The output characteristics of a FET are determined by applying a constant gate voltage \( V_g \) and determining the source-drain current \( I_{sd} \) as a function of the applied source-drain voltage \( V_{sd} \). This type of measurement is therefore also referred to as a drain sweep. In figure 3.4 an example of an output curve can be seen. The hysteresis in the curves is very small and such that less current flows on the reverse sweep.

In the figure both the saturated and the linear region can easily be identified and they will be discussed next.

3.3.1 Saturated region

With increasing source-drain voltage, i.e. decreasing drain-gate voltage, the amount of induced holes at the drain contact decreases and at \( V_{sd_{sat}} \) no holes are induced at the drain contact anymore, i.e. the accumulation channel does not reach from source to drain. The point where the accumulation channel ends is called the pinch-off point. No holes are induced beyond the pinch-off point and there is therefore no contribution, beyond that point, to \( I_{sd} \). As \( V_{sd} \) increases beyond \( V_{sd_{sat}} \), the pinch-off point moves towards the source contact. The voltage at the pinch-off point never goes beyond \( V_{sd_{sat}} \), which means that
$I_{sd}$ stays essentially the same, see the leftmost part of figure 3.4. The current is then saturated.

### 3.3.2 Linear region

In the linear region, the rightmost part of figure 3.4, the curves leave the origin in straight lines. From the slopes of these lines, the mobility can be calculated and for this particular FET, a value of $\mu = 2 \cdot 10^{-3}$ cm$^2$/Vs is found. This value is consistent with what is shown in figure 3.3.

### 3.4 Contacts

The resistance of a FET equals the resistance of the active region of the device, i.e. the channel resistance $R_{ch}$, plus twice the resistance of the contacts, $R_C$. This results in a total resistance

$$R_{FET} = R_{ch}(L) + 2R_C = \frac{\partial V}{\partial I}. \quad (3.5)$$

The channel resistance depends on the semiconductor being used and it scales with the length of the channel, $L$, whereas the contact resistance does not scale with $L$, but depends on the difference in workfunction between the contact and the semiconductor.

Depending on the behaviour of a contact for low source-drain voltages, it is referred to either as an ohmic contact or as a Schottky contact.

#### 3.4.1 Ohmic contact

When a metal-semiconductor contact has a negligible contact resistance compared to the channel resistance, $R_C \ll R_{ch}$, the contact is said to be ohmic. Such a contact can pass the current with a minimal voltage drop compared to the total drop from source to drain. The output characteristics for such a contact show a curve that leaves the origin in a straight line under an angle with the drain current axis (figure 3.4).

#### 3.4.2 Schottky contact

In a Schottky contact, there is a large barrier at the metal-semiconductor interface that hinders charge carriers to move from one side to the other. At low drain voltages only few charge carriers can pass the barrier by thermionic emission or tunneling. This results in a lower current (for low drain voltages) compared to the ohmic contact where no such barrier exists. For higher drain voltages the charge carriers have higher energies and can therefore more easily pass the barrier. In figure 3.5 an example of a Schottky contact can be seen. Note the high slope (with respect to the drain current axis) at low voltages, which means there is a high contact resistance.

In the remainder of this thesis the source contact will be grounded, i.e. $V_s = 0$ and therefore, $V_{sd} = V_d$, $V_{sd, sat} = V_{d, sat}$ and $I_{sd} = I_d$. The semiconductor that is used in the FET will be of the p-type, meaning that holes are induced in the channel and not electrons.
CHAPTER 3. MEASURING FET CHARACTERISTICS

Figure 3.5: Example output $I - V$ characteristics of a $L = 40 \, \mu m$, $W = 1 \, mm$ poly-arylamine ring FET operated at $40 \, ^\circ C$ in $10^{-6}$ mbar air and dark. The FET has a Schottky contact, i.e. an S-shape curve can be seen at low drain voltages, caused by a Schottky barrier. Note this type of contact is not typical for this particular semiconductor.
3.5. **THRESHOLD VOLTAGE SHIFT**

![Graph showing transfer I - V characteristics](image)

Figure 3.6: The transfer $I - V$ characteristics are displayed for a $L = 40 \, \mu m$, $W = 1 \, mm$ PTV ring FET operated at $85 \, ^\circ C$ in $10^{-6} \, mbar$ air and in the dark. The FET is stressed at $-22.6 \, V$, i.e. 20 V below the starting threshold voltage. The threshold voltage clearly shifts towards the applied gate voltage. The total stress times for all measurements are displayed in the legend.

### 3.5 Threshold voltage shift

As was said earlier in Section 1.5 on page 5, FETs are the basic building blocks of binary logic and as such, their stability is very important. Organic FETs can usually not withstand high temperatures or even being brought into contact with air. Either act can degrade the organic material and permanently alter the characteristics of the FET. Unfortunately, shielding FETs from air and excessive heat will not ensure stability. Continuous usage of a FET, i.e. applying a constant voltage on the gate contact, also known as stressing the gate or simply stressing, will usually also change the characteristics of the device and reflects in a decreasing drain current $I_d$ as a function of time for a given gate voltage. Performing gate sweeps during the stressing results in transfer curves that are displaced with respect to the previous measurement while retaining the original shape of the curve. The size of this displacement or shift is dependent on the semiconductor that is being used, the voltage that is applied to the gate contact and the time between measurements. While some semiconductors are virtually stable, even after stressing the FET for several days, others exhibit large shifts even during a single gate sweep. An example of such a shift is shown in figure 3.6.

As was explained in 1.6.2 on page 8, applying a negative voltage to the gate increases the Fermi level of the metal, while the semiconductor Fermi level remains constant. The energy bands bend upward and holes are introduced at the interface with the insulator. Applying a negative drain voltage makes these
holes travel from source to drain. Along their path the holes, or rather the electrons that travel the other direction, can interact with the semiconductor, the insulator, any defects they encounter or with themselves. When they do, they can get trapped at the location where this happens (this location is called a trapsite) and will no longer contribute to the charge transport. The shift of the curve can then be explained by saying that more and more mobile charges are trapped at these trapsites, meaning that there is a decreasing number of charges flowing between source and drain and thus the current between source and drain will go down. A higher gate voltage must then be applied to obtain a similar source-drain current as before. In the figure this results in a shift towards the applied gate voltage.

By shifting the measured transfer curves on top of each other, the threshold voltage shift can be determined as a function of the stress time. The relative threshold voltage shift corresponding to figure 3.6 is shown in figure 3.7. By looking at this curve characteristic constants of the charge trapping can be determined.

When the application of the gate voltage is stopped, the FET is able to recover, meaning that trapped charges are able to break free and the threshold voltage shift is therefore reduced. The description of the time dependence for stress recovery is identical to that for stressing, but the characteristic constants are different.

As will be shown later, changing the temperature also changes the rate at which charges are trapped and released. The threshold voltage will shift faster at higher temperatures.
Chapter 4

Theory

Two models are given in this chapter. The first model describes the current flowing between source and drain as a function of the applied gate voltage $V_g$ and temperature $T$. It provides a characteristic temperature $T_0$ which is a measure of the width of the exponential distribution of the density of states corresponding to the semiconductor. The second model to be discussed predicts the threshold voltage shift as a function of time and provides another characteristic temperature $T^*$ which is a measure of the exponential distribution of trapping sites.

4.1 Field-effect current in disordered systems

To describe the charge transport in disordered semiconductors, the variable range hopping model proposed by Vissenberg and Matters [9] is used. They argue that the charge transport in disordered semiconductors is governed by the thermally activated tunneling (hopping) of charge carriers between localised states around the Fermi level. The charge carriers may either hop over a small distance with a high activation energy or over a long distance with a low activation energy. The density of states (DOS) in a disordered semiconducting polymer is described by a Gaussian distribution. At low temperature, $T$, and low charge carrier density, the tail of the DOS determines the transport properties. The Gaussian distribution can then be approximated by an exponential DOS

$$g(E) = \begin{cases} \frac{N_t}{kT_0} \exp \left( \frac{E}{kT_0} \right) & (-\infty < E \leq 0) \\ 0 & (E > 0) \end{cases}$$

(4.1)

where $N_t$ is the number of states per unit volume, $k$ is the Boltzmann constant and $T_0$ is a parameter that indicates the width of the exponential distribution.

In equilibrium, the energy distribution of the charge carriers is given by the Fermi-Dirac distribution $f(E, E_F)$, where $E_F$ is the Fermi energy. If a fraction $\delta \in [0, 1]$ of the localised states is occupied by charge carriers, such that the density of carriers is $\delta N_t$, then the position of the Fermi level is fixed by the condition

$$\delta = \exp \left( \frac{E_F}{kT_0} \right) \frac{\pi T}{T_0 \sin \left( \frac{\pi T}{T_0} \right)}.$$ 

(4.2)
CHAPTER 4. THEORY

Using a percolation model of variable range hopping, an expression for the conductivity as a function of the charge carrier occupation $\delta$ and the temperature $T$ can be derived [9]

$$\sigma(\delta, T) = \sigma_0 \left[ \delta \frac{N_i \left( \frac{T_0}{T} \right)^4 \sin \left( \frac{\pi T}{T_0} \right)}{(2\alpha)^3 B_c} \right]^{\frac{T_0}{T}} \cdot \frac{2^2}{b-1}, \quad (4.3)$$

where $\sigma_0$ is the prefactor of the conductivity, $B_c$ is a critical number for the onset of percolation, which is $B_c \approx 2.8$ for three-dimensional amorphous systems and $\alpha^{-1}$ is an effective overlap parameter between localised states.

In a field-effect transistor the charge density is not uniform. Hence, to calculate the field-effect current, the conductivity is integrated over the accumulation channel, i.e.

$$I_{ds} = \frac{W V_d}{L} \int_0^t \sigma(\delta(x), T), \quad (4.4)$$

where $L$, $W$ and $t$ are the length, width and thickness of the channel, respectively. Here the potential drop from source to drain electrode $V_d$ (the source electrode is grounded, $V_s = 0$) is neglected. This is only valid if the gate voltage $V_g$ is much greater than the drain voltage ($|V_g| \gg |V_d|$), i.e. in the linear region. In [6] the field-effect current is then shown to be

$$I_d = \frac{W V_d \varepsilon_s \varepsilon_0 \sigma_0}{L \varepsilon} \left( \frac{T}{2T_0 - T} \right) \sqrt{\frac{2kT_0}{\varepsilon_s \varepsilon_0}} \cdot \left[ \frac{(T_0)^4 \sin \left( \frac{\pi T}{T_0} \right)}{(2\alpha)^3 B_c} \right]^{\frac{T_0}{T}} \cdot \left\{ \frac{\varepsilon_s \varepsilon_0}{2kT_0 \left( \frac{C_i (V_g - V_{th})}{\varepsilon_s \varepsilon_0} \right)} \right\}^{\frac{2T_0}{T} - 1}, \quad (4.5)$$

where $e$ is the elementary charge, $\varepsilon_0$ is the permittivity of vacuum, $\varepsilon_s$ is the relative dielectric constant of the semiconductor, $C_i$ is the insulator capacitance per unit area and $V_{th}$ is the voltage at which current starts to flow, i.e. the threshold voltage. This can be rewritten to read

$$I_d = \frac{a W C_i V_d}{L} (V_g - V_{th})^{b+1}, \quad (4.6)$$

where

$$a = \frac{\sigma_0}{e} \frac{1}{b+1} C_i^b \cdot \left[ \frac{(T_0)^4 \sin \left( \frac{\pi T}{T_0} \right)}{(2\alpha)^3 B_c} \right]^{\frac{T_0}{T}} \cdot \left( \sqrt{2kT_0 \varepsilon_s \varepsilon_0} \right)^{-b}, \quad (4.7)$$

and

$$b = 2 \left( \frac{T_0 - T}{T} \right). \quad (4.8)$$
These equations are valid only in the linear region.

The drain current obtained from the transfer characteristics during the stress measurements was fitted using a Matlab routine (Appendix D on page 75) based on equation (4.6) and values for $a$, $b$ and $V_{th}$ are thus determined.

4.2 Stretched-exponential relaxation

As was explained in Section 3.5 on page 23, the shift of the threshold voltage can be explained by the trapping of charge carriers at defect sites in the material. The charges that are trapped can no longer contribute to the current flowing between source and drain contact and as a result, less current will flow for a given gate voltage. Increasing the applied gate voltage will induce more charges and result again in a higher current. Effectively the whole transfer curve will have shifted towards the applied stress voltage. The shift can be quantified by looking at the shift of the threshold voltage, $\Delta V_{th}$, which can be directly related to the amount of trapped charges, $\Delta Q_{\text{trapped}}$ using

$$\Delta Q_{\text{trapped}} = C_i \Delta V_{th},$$

with $C_i$ the insulator capacitance per unit area.

Previously, the threshold voltage shift in $a$-Si thin-film transistors (TFTs) has been studied and two major models have been developed [10, 11] to describe the density of defect states $\Delta N_D (x, t)$ and hence the threshold voltage shift. Using different underlying microscopic processes, both models explain the creation of defect states by a dispersive process, which is typical for amorphous materials. The differential equation for the density of defect states that follows from both models is

$$\frac{\partial \Delta N_D (x, t)}{\partial t} = -AD(t) \Delta N_D (x, t),$$

where $A$ is a constant of proportionality and $D(t)$ is a time-dependent diffusion coefficient. It is given by

$$D(t) = D_{00} (\nu t)^{-\alpha},$$

with $D_{00}$ a microscopic diffusion, $\nu$ an attempt frequency and $\alpha$ the temperature dependent dispersion parameter which is given by

$$\alpha = 1 - \beta = 1 - \frac{T}{T^*}.$$  

Here, $kT^*$ is the characteristic energy of the exponential distribution of trapping sites and $T$ is the temperature at which measurements are performed.

Solving eq. (4.10) using eq. (4.11), yields a stretched exponential [12] time dependence for $\Delta N_D (t)$ given by

$$\Delta N_D (t) = \Delta N_D (0) \exp \left[ - \left( \frac{t}{\tau} \right)^\beta \right],$$

where $\tau$ is the so-called relaxation time and $\beta = \frac{T}{T^*}$.

However, in this thesis, conjugated polymers are used as the semiconducting material and although the microscopic models derived for $a$-Si do not make sense
for polymer semiconductors it is found that in both materials the transport of charge is primarily due to diffusion. To describe the threshold voltage shift in amorphous polymer semiconductors, the amount of charge that is trapped at defect sites will be described with a differential equation similar to eq. (4.10), namely

$$\frac{\partial \Delta Q_{\text{trapped}}(x,t)}{\partial t} = -a (\nu t)^{-\alpha} \Delta Q_{\text{trapped}}(x,t),$$  \hspace{1cm} (4.14)

where $a$ is a constant of proportionality with unit s$^{-1}$, $\nu$ is again an attempt frequency and $\alpha$ again the temperature dependent dispersion parameter given by eq. (4.12). The amount of trapped charge is thus a function of time $t$ and distance $x$ from the insulator. To obtain the total trapped charge as a function of time, $\Delta Q_{\text{trapped}}(x,t)$ must be integrated over the thickness of the film, resulting in

$$\Delta Q_{\text{trapped}} = \Delta Q_{\text{trapped}}(t) \equiv \int_0^\infty \Delta Q_{\text{trapped}}(x,t) \, dx.$$  \hspace{1cm} (4.15)

This areal integral will be used in the remainder of this thesis. Using eq. (4.9), the differential equation can be written in terms of the threshold voltage shift, resulting in

$$\frac{d\Delta V_{\text{th}}}{dt} = -a (\nu t)^{-\alpha} \Delta V_{\text{th}}(t).$$  \hspace{1cm} (4.16)

Solving this equation (see Appendix B on page 71 for a more detailed deduction of all equations) yields a stretched exponential [12] time dependence for $\Delta V_{\text{th}}(t)$ given by

$$\Delta V_{\text{th}}(t) = \Delta V_{\text{th}}(0) \exp \left[- \left(\frac{t}{\tau}\right)^\beta \right],$$  \hspace{1cm} (4.17)

where $\tau$ is the so-called relaxation time and $\beta = \frac{T}{T^*}$. The threshold voltage will in principle not shift passed the applied gate voltage, therefore the threshold voltage after stressing infinitely long, $V_{\text{th}}(\infty)$, will equal the applied gate voltage. The relative threshold voltage shift then equals

$$\frac{V_{\text{th}}(t) - V_{\text{th}}(0)}{V_g - V_{\text{th}}(0)} = 1 - \exp \left[- \left(\frac{t}{\tau}\right)^\beta \right].$$  \hspace{1cm} (4.18)

The relaxation time $\tau$ is thermally activated and equals

$$\tau = \tau_0 \exp \left(\frac{E_r}{kT}\right),$$  \hspace{1cm} (4.19)

where $\tau_0$ is the inverted attempt to escape frequency $\tau_0 = \nu^{-1}$ and $E_r$ is the mean activation energy for trapping and is then equal to

$$E_r = kT^* \ln \left(\frac{\beta}{a\tau_0}\right).$$  \hspace{1cm} (4.20)

Note the logarithmic dependence on $\beta$ and hence on $T$. In this thesis a constant value for $E_r$ is found and the temperature dependence is not understood nor found experimentally.
Combining the temperature $T$ with the stress time $t$, the so-called thermalisation energy $E_{\text{therm}}$ can be defined (see Appendix C on page 73 for a more detailed derivation). It is given by

$$E_{\text{therm}} = kT \ln (\nu t).$$  \hspace{1cm} (4.21)

It can be seen as the energy below which all possible trap sites have been filled at temperature $T$ and time $t$. It can be used together with the relaxation time $\tau$ to rewrite the equation for the relative threshold voltage shift, eq. (4.18), so it reads

$$\frac{V_{th}(t) - V_{th}(0)}{V_g - V_{th}(0)} = 1 - \exp \left[ - \exp \left( \frac{E_{\text{therm}} - E_r}{kT^*} \right) \right].$$  \hspace{1cm} (4.22)

Note this equation has a linear temperature dependence in $E_{\text{therm}}$ and a logarithmic temperature dependence in $E_r$. 
Chapter 5

Results

In this chapter, results will be shown that are obtained from threshold voltage shift measurements using gate stressing on organic field-effect transistors. The semiconductor poly(2,5-thienylene vinylene) (PTV) will be discussed extensively for both stress and stress recovery on a single ring transistor at one specific temperature. Then the temperature dependence is investigated, again for both stress and stress recovery. The results are then summarised in Section 5.5 on page 51, together with the results of two additional samples.

5.1 PTV stress

Results obtained for a stress measurement on a single PTV ring transistor at a constant temperature are given in this section. First, the transfer characteristics obtained during the stress measurements are detailed and the mobility curves are shown. This is followed by the output characteristics that were measured. Then the results of fitting the transfer curves are given and the transport is investigated. Finally the threshold voltage shift is detailed.

5.1.1 Transfer curves

The transfer characteristics obtained during a stress measurement on a PTV FET are shown in figure 5.1. The threshold voltage shifted from -2.6 V at the start of the measurement to -12.2 V when the measurement was ended. The total duration of the measurement was 25 hours, during which 14 gate sweeps were performed, where each gate sweep started with a gate voltage of +5 V and ended with $V_g = -35$ V. The step size was -0.2 V and performing one gate sweep took around one minute. The measurement data was then saved to disk, taking another half a minute and immediately after, the stressing was resumed.

Shifting all the gate sweeps on top of the first gate sweep, see figure 5.2, it can be shown that indeed the transfer characteristics of a polymer FET that is stressed, do not change shape, but are merely shifted over the gate voltage. This proves that no structural changes are made to the components of the FET and that there is simply a trapping of charges in the FET so that less charges are left to contribute to the current between source and drain contact and hence there is a shift of the threshold voltage towards the applied gate voltage.
Figure 5.1: The transfer $I - V$ characteristics are displayed for a $L = 40 \, \mu m$, $W = 1 \, mm$ PTV ring FET operated at $85 \, ^\circ C$ in $10^{-6}$ mbar air and in the dark. The FET is stressed at $-22.6 \, V$, i.e. $20 \, V$ below the starting threshold voltage. The threshold voltage clearly shifts towards the applied gate voltage. The total stress times for all measurements are displayed in the legend.

Figure 5.2: Shown are all gate sweeps of figure 5.1, shifted over the gate voltage axis to position them exactly on top of the first gate sweep, proving that the shape of the transfer characteristics does not change during stressing.
5.1. **PTV STRESS**

5.1.2 Mobility curves

Using eq. (3.3) on page 19 to calculate the mobility from all transfer characteristics of the stress measurement, figure 5.3 is obtained. This curve can also be shifted on top of the first measurement, as shown in figure 5.4.

5.1.3 Output curves

To check for good contacts, the output characteristics of the FET are determined before and after the stress measurement, figures 5.5 and 5.6. Both figures show there was an ohmic contact and that the current saturates at high drain voltages. The maximum current at $V_g = -20 \text{ V}$ has been reduced from $-7.6 \cdot 10^{-8} \text{ A}$ before stressing to $-2.5 \cdot 10^{-9} \text{ A}$ after stressing, clearly showing the effects of a threshold voltage shift.

5.1.4 Fitting transfer curves

The transfer characteristics were then fitted using the model based on eq. (4.6) on page 26 and for each gate sweep a value for $a$, $b$ and $V_{th}$ was obtained. Figure 5.7a shows both data and fit on a linear scale, where no difference between data and fit can be seen. However, by using a logarithmic scale, figure 5.7b, it can clearly be seen the model doesn’t hold outside the linear region, which is as expected.

The values of $b$ obtained in the fit are not constant as expected, see figure 5.8, but seem to increase logarithmically with time, starting at 0.5 and ending at 0.8, with an average value of 0.69. For $T_0$ this means it also changes with
CHAPTER 5. RESULTS

Figure 5.4: Shown are all mobility curves of figure 5.3, shifted over the gate voltage axis to position them exactly on top of the first mobility curve, proving once again, that the shape of the transfer characteristics does not change during stressing.

Figure 5.5: Output characteristics obtained before the stress measurement.
5.1. PTV STRESS

Figure 5.6: Output characteristics obtained after the stress measurement.

time, from 450 K at the beginning to 501 K when the measurement is stopped. The average value is around $T_0 = 4.8 \cdot 10^2$ K, which is in fair agreement with literature, see [6]. The relative change in $T_0$ is thus smaller than in $b$.

Rewriting eq. (4.6) by taking the $(b + 1)$th root gives

$$I_d^{\frac{1}{b+1}} = \left( \frac{aWC_tV_d}{L} \right)^{\frac{1}{b+1}} (V_g - V_{th})$$

and the average value for $b$ can then be used to make figure 5.9, where $I_d^{\frac{1}{b+1}}$ is shown to be proportional to the applied gate voltage outside the linear region, even when using the average value of $b$. This means the model can be considered valid outside the linear region.

5.1.5 Threshold voltage shift

As was shown in the previous subsection, the $a$ and $b$ values obtained from the transport model are not constant during the stress measurements. This makes the extracted threshold voltage less accurate. Moreover, the threshold voltage is defined in the linear region, which is exactly where the transport model is not valid, making the exact value of the threshold voltage as determined by the model doubtful. However, it is the threshold voltage shift that needs to be determined and the transport model that is used might possibly still give accurate enough values for that.

To test this, a comparison is made with two additional methods of extracting the threshold voltage shift and the result can be seen in figure 5.10. All curves are normalised using the same normalisation constant which will be detailed in the next subsection.
CHAPTER 5. RESULTS

Figure 5.7: The transfer $I - V$ characteristics from the stress measurement are displayed for a $L = 40 \, \mu m$, $W = 1 \, mm$ PTV ring FET operated at $85 \, ^\circ C$ in $10^{-6}$ mbar air and in the dark, together with the fits based on eq. (4.6) on page 26. The FET is stressed at $-22.6 \, V$ and the total stress times for all measurements are displayed in the legend. In (a) the current is shown on a linear scale and in (b) a logarithmic scale is used.
5.1. PTV STRESS

Figure 5.8: The fit parameter $b = 2 \left( \frac{T_0 - T}{T} \right)$ is shown and it changes during the stress measurement.

Figure 5.9: Shown is the $(b + 1)$th root (here $b = 0.69$, i.e. $T_0 = 4.8 \cdot 10^2$ K) of the drain current as a function of the applied gate voltage.
Figure 5.10: Three different methods of determining the threshold voltage are compared. The curve labeled “Matlab shift” follows from the values found using the Matlab fit, “Curve shift” from shifting all curves on the first curve and “Switch-on shift” from looking at the voltage where current starts to flow.

The curve labeled “Curve shift” is determined by shifting the transfer curves on top of each other. This is done using a linear current scale and thus looking at high drain currents. The shifts were determined with 0.1 V accuracy. Since there is a large shift between the first sweep and the second sweep, i.e. between the 0 seconds sweep and the 10 seconds sweep (see figure 5.1), the method used was to shift the third, fourth and fifth sweeps on top of the second sweep and extrapolate the change in the curve shift to estimate the real shift between the first and the second sweep and then continue to shift all curves on the 10 seconds sweep. The bigger shift between the first and the second sweep might be caused by an unknown extra trapping mechanism with a much smaller timescale, but is not investigated here further. The third method to determine the threshold voltage shift is to simply look at the transfer curves on a logarithmic scale and determine the gate voltage for which a drain current starts to flow. This method has the disadvantage that very low currents are used and these can be sensitive to minimal changes inside or outside the sample.

Figure 5.10 shows there is less then a 10% difference between the methods. Here, the “Curve shift” method is used because it has sufficient accuracy and it is a straight forward approach.

5.1.6 Fitting threshold voltage shift

The threshold voltage shift as a function of the stress time is normalised so it can be fit using eq. (4.18) on page 28. The normalisation constant should equal
5.2 PTV STRESS RECOVERY

Figure 5.11: The relative threshold voltage shift (magenta circles) as a function of time. The parameters obtained from the stretched exponential fit (blue curve) are \( \tau = 3.6 \times 10^5 \) s and \( \beta = 0.30 \).

The maximum possible shift, i.e. the applied gate voltage minus the threshold voltage at the beginning of the measurement, \( V_{th}(0) \). This \( V_{th}(0) \) was found manually before the stress measurement was started, by determining the gate voltage for which current starts to flow. The gate voltage that was applied during the stress measurement was then set 20 V below this value. The normalisation constant was therefore 20 V and figure 5.11 shows the relative threshold voltage shift. The data was then fit using eq. (4.18) resulting in the blue curve. The parameters \( \tau \) and \( \beta \) at this temperature are found to be \( \tau = 3.6 \times 10^5 \) s and \( \beta = 0.30 \). Using eq. (4.12) the characteristic temperature of the exponential distribution of trapping sites is then \( T^* = 1.2 \times 10^3 \) K or \( 1.0 \times 10^2 \) meV.

Note that the total threshold voltage shift is only around 50% after measuring for 25 hours. Since the shift changes logarithmically with time, it is not practically feasible to fully shift this sample to the applied gate voltage.

5.2 PTV stress recovery

In this section the results are given that are obtained for a stress recovery measurement on a single PTV ring transistor at a constant temperature. First, the transfer characteristics obtained during the stress recovery measurements are detailed. This is followed by the output characteristics that were measured before and after the stress measurement. The results of fitting the transfer curves are given and the charge transport is characterised. Finally the threshold voltage shift is detailed and the best fit is determined using a stretched exponential
CHAPTER 5. RESULTS

Figure 5.12: The transfer $I - V$ characteristics are displayed for a $L = 40 \mu m$, $W = 1 \text{ mm}$ PTV ring FET operated at 85 $^\circ$C in $10^{-6}$ mbar air and in the dark. The FET is recovering from stress with the application of 0 V on the gate contact. The threshold voltage clearly shifts towards the applied gate voltage. The total stress times for all measurements are displayed in the legend.

as was done in Section 5.1. This results in values for the activation energy $E_r$ and the characteristic temperature of the exponential distribution of trapping sites $T^*$.  

5.2.1 Transfer curves

Immediately after the stress measurement is stopped, the stress recovery measurement is started on the same PTV ring transistor and at the same constant temperature as used during stressing in the previous section. The only difference between the stress measurement and the stress recovery measurement is the applied gate voltage, that is now 0 V.

Figure 5.12 shows the stress recovery measurement performed at 85 $^\circ$C. The measurement details are identical to the stress measurement detailed earlier. The threshold voltage shifted from -11.8 V at the start of the stress measurement to -6.2 V when the measurement was ended, which would result in a total shift of 5.6 V.

However, shifting all the gate sweeps on top of the last gate sweep by looking at high currents, see figure 5.13, results in a total shift of 3.8 V. The difference can be explained by looking at the logarithmic version of figure 5.13 that is shown in figure 5.14. This figure clearly shows that in the low-current part the transfer characteristics change over the measurement. Here, again the curve shift method is used since the high current behaviour of the transistor provides a more precise characterisation.
5.2. PTV STRESS RECOVERY

Figure 5.13: Shown on a linear scale are all gate sweeps of figure 5.12, shifted over the gate voltage axis to position them on top of the last gate sweep by looking at high drain currents.

Figure 5.14: Shown on a logarithmic scale are all gate sweeps of figure 5.12, shifted over the gate voltage axis to position them on top of the last gate sweep by looking at high drain currents.
5.2.2 Output curves

To check for good contacts, the output characteristics of the FET are determined before and after the stress recovery measurement, figures 5.15 and 5.16. Both figures show there was an ohmic contact and that the current saturates at high drain voltages. The maximum current at $V_g = -20$ V has been increased from $-2.55 \cdot 10^{-9}$ A to $-1.56 \cdot 10^{-8}$ A, clearly showing the effects of a recovery of the original characteristics of the device.

5.2.3 Fitting transfer curves

The transfer characteristics were then fitted using the model based on eq. (4.6) on page 26, giving values for $a$, $b$ and $V_{th}$ for each gate sweep. Figure 5.17a shows both data and fit on a linear scale, where no difference between data and fit can be seen. By using a logarithmic scale, figure 5.17b, however, it can be clearly seen the model doesn’t hold outside the linear region, which is as expected.

Contrary to the stress measurement, the values of $b$ obtained in the fit of the stress recovery measurement are constant at 0.80, meaning the characteristic transport temperature is $T_0 = 5 \cdot 10^2$ K.

5.2.4 Fitting threshold voltage shift

The curve shift obtained earlier gives the shift of the threshold voltage as a function of stress time. This shift can then be normalised with respect to the maximum possible shift, i.e. the applied gate voltage (0V for stress recovery)
5.3 PTV STRESS TEMPERATURE DEPENDENCE

The measurements detailed in the previous sections are repeated at different temperatures, ranging from 25 °C to 85 °C, and at each temperature the data is processed, giving \( \tau \) and \( \beta \) as a function of temperature. The temperature range was limited at room temperature because the setup does not support cooling and the higher temperature was chosen because the PTV was not found to be stable above 100 °C.

5.3.1 Relaxation time

In figure 5.19, extracted values for \( \tau \) are plot as a function of the inverted temperature for the same \( L = 40 \, \mu m, W = 1 \, \text{mm} \) PTV ring FET operated in \( 10^{-6} \) mbar air and in the dark. The data is fit using eq. (4.19) on page 28, i.e. by the Arrhenius type equation \( \tau = \tau_0 \exp \left( \frac{E_r}{kT} \right) \), and this gives \( \tau_0 = 10^{-3} \) s and \( \frac{E_r}{k} = 7.1 \times 10^3 \) K, resulting in an activation energy \( E_r = 0.61 \) eV for stressing for...
Figure 5.17: The transfer $I - V$ characteristics from the stress recovery measurement are displayed for a $L = 40 \, \mu m$, $W = 1 \, mm$ PTV ring FET operated at $85 \, ^\circ C$ in $10^{-6}$ mbar air and in the dark, together with the fits based on eq. (4.6) on page 26. The FET is stressed at $0 \, V$ and the total stress times for all measurements are displayed in the legend. In (a) the current is shown on a linear scale and in (b) a logarithmic scale is used.
5.3. PTV STRESS TEMPERATURE DEPENDENCE

The relative threshold voltage shift as a function of time corresponding to figure 5.17. The parameters obtained from the stretched exponential fit are $\tau = 5.0 \cdot 10^5$ s and $\beta = 0.48$.

The attempt frequency is then used to determine the thermalisation energy $E_{\text{therm}}$ as a function of time, eq. (4.21), with which several normalised threshold voltage shifts measured at different temperatures can be displayed in one single figure showing the normalised threshold voltage shift as a function of this thermalisation energy. Such a so-called thermal plot can be seen in figure 5.20. The dotted lines are calculated using eq. (4.22) and represent boundary values for $T^*$ of 1050 K and 1350 K, meaning there is an uncertainty in $T^*$ of around 13 %.

When the thermalisation energy equals the activation energy for $\tau$, i.e. when $E_{\text{therm}} = E_\tau$, then eq. (4.22) says that the normalised threshold voltage shift equals $1 - e^{-1}$, which equals about 0.63. All curves based on eq. (4.22) will cross at this point, independent of the characteristic temperature of the exponential distribution of trapping sites $T^*$ and independent of the measurement temperature $T$. The time it takes to shift $1 - e^{-1}$ is just the relaxation time $\tau$, i.e.

$$t = \tau = \tau_0 \exp \left( \frac{E_\tau}{kT} \right)$$

(5.2)

Note that for $\alpha$-Si an alternative to the stretched exponential is available that better describes the threshold voltage shift when the total shift approaches
Figure 5.19: The relaxation time $\tau$ as a function of the inverted temperature $T$ is shown and eq. (4.19) was used to fit the data (the blue curve). Fit coefficients found are $\tau_0 = 10^{-3}$ s and $\frac{E_a}{k} = 7.1 \cdot 10^3$ K.
5.3. PTV STRESS TEMPERATURE DEPENDENCE

Figure 5.20: The thermalisation plot for stressing a PTV ring FET, showing the normalised threshold voltage shifts obtained at different temperatures, as a function of the thermalisation energy $E_{\text{therm}}$. The dotted lines represent boundary values for the characteristic temperature of the exponential distribution of trapping sites $T^*$. The boundary lines cross at $E_{\text{therm}} = E_r = 0.61$ eV.

The applied gate voltage. This alternative is a hyperbole,

$$\frac{V_{th}(t) - V_{th}(0)}{V_g - V_{th}(0)} = 1 - \left[1 + \exp\left(\frac{E_{\text{therm}} - E_r}{kT^*}\right)^{-(\delta-1)^{-1}}\right], \quad (5.3)$$

but it has not been used here since the PTV FETs do not shift far enough to see if it better describes the data. The reason is because the time it would take to measure a complete shift at low temperatures is simply too long and increasing the temperature to quicken the stress effect does only work to a certain extent because temperatures above 85 °C result in deteriorated samples.

5.3.2 Characteristic temperature

The fit of the normalised threshold voltage shift detailed in 5.1.6 on page 38 not only provided a value for the relaxation time $\tau$, but also for $\beta$ and hence for the characteristic temperature of the exponential distribution of trapping sites $T^*$. Plotting $\beta$ as a function of temperature results in what can be seen in figure 5.21. The dotted lines represent the same boundary values for $T^*$, i.e. 1050 K for the upper line and 1350 K for the lower line as was found in 5.3.1. The values for $\beta$ all lie within the boundary lines. The uncertainty in $\beta$ is 13 % which is within the experimental uncertainty, since $\beta$ is rather sensitive to the initial and equilibrium values of the threshold voltage.
5.4 PTV stress recovery temperature dependence

5.4.1 Relaxation time

In figure 5.22, the relaxation time for stress recovery is shown for the same FET as before. The limited data set shows a large amount of scattering, especially at low temperatures. This can easily be understood by realising that the recovery measurements are always started immediately after a stress measurement at the same temperature to ensure the sample does not change in between the two measurements. This means that stress recovery measurements performed at low temperatures have also been stressed at low temperature and have therefore not shifted as much as samples stressed at high temperatures would, which means that the recovery threshold voltage shift \( \Delta V \) will be even smaller still. This means the data obtained for stress recovery are sensitive to e.g. the normalisation that has to be performed. From 5.22 it is obvious that an exact analysis is not possible with the current data set, i.e. it is not possible to extract values for the attempt frequency \( \nu \) and the activation energy \( E_r \) for stress recovery from this figure.

However, the thermal plot can still provide an estimate for the activation energy \( E_r \). For this, a value for the attempt frequency \( \nu \) is still needed and for lack of a more accurate value, the value found in the stress measurements was used, i.e. \( \nu = 10^3 \) Hz, which gives a fair agreement. This leaves two variables, \( T^* \) and \( E_r \), that are chosen to give the best fit. The result can be seen in figure 5.23, where \( 650 \text{ K} < T^* < 1100 \text{ K} \) and \( 0.61 \text{ eV} < E_r < 0.65 \text{ eV} \).
5.4. PTV STRESS RECOVERY TEMPERATURE DEPENDENCE

Figure 5.22: The relaxation time $\tau$ for recovery as a function of the inverted temperature $T$ is shown. The data could not be fit because there is too much spread.
Figure 5.23: The thermalisation plot for stress recovery of a PTV ring FET, showing the normalised threshold voltage shifts obtained at different temperatures, as a function of the thermalisation energy $E_{\text{therm}}$. The dotted lines represent boundary values for both the characteristic temperature of the exponential distribution of trapping sites $T^*$ and the activation energy $E_r$. 
5.5. SUMMARY PTV

The measurements of the threshold voltage shift observed on stressed FETs, as detailed in the previous sections, provided values for $\beta$ and for the relaxation time $\tau$ by using a stretched exponential to fit the shift as a function of time. By looking at their temperature dependence, values for the attempt frequency $\nu$, the characteristic temperature of the exponential distribution of trapping sites $T^*$ and the activation energy $E_r$ can be determined. At the same moment, the temperature of the exponential density of states $T_0$ could be obtained by fitting.

Figure 5.24: The values found for $\beta$ as a function of temperature. The dotted lines represent boundary values obtained from the thermalisation plot.

Again note that for $a$-Si the data is better described by a hyperbole, but as was explained earlier the measurements on the polymer FETs investigated here do not provide enough data to check that.

5.4.2 Characteristic temperature

The values for $\beta$, obtained from the threshold voltage shifts, are shown in figure 5.24. The boundary lines obtained from the thermalisation plot are also shown. It can be seen that the values at low temperature are not consistent with the boundary lines. As explained earlier, the reason is that the stress recovery threshold voltage shift is relatively small and thus sensitive to normalisation. Note that measurements performed on another device (as discussed later) show less spread.

5.5 Summary PTV

The measurements of the threshold voltage shift observed on stressed FETs, as detailed in the previous sections, provided values for $\beta$ and for the relaxation time $\tau$ by using a stretched exponential to fit the shift as a function of time. By looking at their temperature dependence, values for the attempt frequency $\nu$, the characteristic temperature of the exponential distribution of trapping sites $T^*$ and the activation energy $E_r$ can be determined. At the same moment, the temperature of the exponential density of states $T_0$ could be obtained by fitting.
Table 5.1: Values found for $\nu$, $T^*$ and $E_r$ from the threshold voltage shift and values for $T_0$ found by fitting the drain current in the stress measurements for PTV FET number 1 ($T_0^{Ref}$ is obtained from [6]).

<table>
<thead>
<tr>
<th></th>
<th>$\nu$ [Hz]</th>
<th>$T^*$ [K]</th>
<th>$T_0$ [K]</th>
<th>$T_0^{Ref}$ [K]</th>
<th>$E_r$ [eV]</th>
<th>$\tau$ [h]</th>
</tr>
</thead>
<tbody>
<tr>
<td>stress</td>
<td>$10^3$</td>
<td>$1200 \pm 150$</td>
<td>$468 \pm 20$</td>
<td>$382$</td>
<td>$0.61$</td>
<td>$56$</td>
</tr>
<tr>
<td>recovery</td>
<td>$-$</td>
<td>$875 \pm 225$</td>
<td>$492 \pm 20$</td>
<td>$-$</td>
<td>$0.63 \pm 0.02$</td>
<td>$104$</td>
</tr>
</tbody>
</table>

Table 5.2: Values found for $\nu$, $T^*$ and $E_r$ from the threshold voltage shift and values for $T_0$ found by fitting the drain current in the stress measurements for PTV FET number 2 ($T_0^{Ref}$ is obtained from [6]).

<table>
<thead>
<tr>
<th></th>
<th>$\nu$ [Hz]</th>
<th>$T^*$ [K]</th>
<th>$T_0$ [K]</th>
<th>$T_0^{Ref}$ [K]</th>
<th>$E_r$ [eV]</th>
<th>$\tau$ [h]</th>
</tr>
</thead>
<tbody>
<tr>
<td>stress</td>
<td>$\sim 20$</td>
<td>$1100 \pm 200$</td>
<td>$449 \pm 30$</td>
<td>$382$</td>
<td>$0.53$</td>
<td>$227$</td>
</tr>
<tr>
<td>recovery</td>
<td>$\sim 20$</td>
<td>$650 \pm 100$</td>
<td>$466 \pm 30$</td>
<td>$-$</td>
<td>$0.47$</td>
<td>$35$</td>
</tr>
</tbody>
</table>

the charge transport of each gate sweep with the model from [6]. All this has been performed on a single PTV FET which was the first of a series of three identical FETs. The same measurements have also been performed on the other two PTV FETs, where the third one had a top-coating of poly(4-vinylphenol) (in iso-propanol) applied, similar to what was done in [13]. The results will be summarised next.

5.5.1 Sample 1

The data obtained for the first sample are summarised in table 5.1 together with the temperature of the exponential density of states $T_0$ as obtained from literature (where available). It can be seen there is roughly a factor two difference between both temperatures $T^*$ and $T_0$. A comparison between $T_0$ as obtained here and $T_0^{Ref}$ as found in literature shows there is a fair agreement.

The activation energies $E_r$ for stress and stress recovery are similar and with an identical attempt frequency (assumed) this results in a characteristic time $\tau$ (in hours) that is about twice as high for recovery as it is for stress.

5.5.2 Sample 2

The second PTV sample was fabricated identical to and immediately after sample 1 and was stored in the dark and in vacuum before it was used. The measurements detailed for sample 1 were repeated on sample 2 and the results are shown in table 5.2. It can be seen that although the samples are prepared identical as much as possible, there is still quite some difference between values for sample 1 and values for sample 2. This confirms what was found earlier in this thesis, namely that the experimental accuracy is unfortunately rather low. Comparing $T_0$ with $T^*$ again shows roughly a factor of two difference. Again the value for $T_0$ found here is higher than values from literature.

The activation energies $E_r$ for stress and stress recovery are again similar and lower than values for sample 1. With an attempt frequency that was about similar for stress and stress recovery it is found that the characteristic time $\tau$ is about 7 times lower for stress recovery than it is for stress.
Table 5.3: Values found for $\nu$, $T^*$ and $E_r$ from the threshold voltage shift and values for $T_0$ found by fitting the drain current in the stress measurements for PTV FET number 3. ($T_{0\text{Ref}}$ is obtained from [6])

<table>
<thead>
<tr>
<th></th>
<th>$\nu$ [Hz]</th>
<th>$T^*$ [K]</th>
<th>$T_0$ [K]</th>
<th>$T_{0\text{Ref}}$ [K]</th>
<th>$E_r$ [eV]</th>
<th>$\tau$ [h]</th>
</tr>
</thead>
<tbody>
<tr>
<td>stress</td>
<td>$8 \times 10^4$</td>
<td>$1175 \pm 175$</td>
<td>$453 \pm 20$</td>
<td>$382$</td>
<td>$0.74$</td>
<td>$41$</td>
</tr>
<tr>
<td>recovery</td>
<td>$7 \times 10^5$</td>
<td>$875 \pm 175$</td>
<td>$469 \pm 20$</td>
<td>$-$</td>
<td>$0.80$</td>
<td>$31$</td>
</tr>
</tbody>
</table>

5.5.3 Sample 3

The third PTV sample was fabricated immediately after samples 1 and 2 and was also stored in the dark and in vacuum. Right before usage, a solution of poly(4-vinylphenol) (PVP) in iso-propanol was spincoated on top of the device, i.e. on top of the PTV layer, similar to what was done in [13], but using a standard device layout as was shown in figure 3.1a on page 16 and without annealing. In [13] the top-coating provided enhanced mobilities for F8T2 and it was investigated here whether this was also true for PTV and whether the stress behaviour of PTV was influenced by the top-coating.

Figure 5.25 shows obtained values of the relaxation time $\tau$ for both stress (magenta circles) and stress recovery (blue squares) as a function of temperature. It can be seen that the difference between both is within experimental uncertainty. Values extracted from the fit are given in table 5.3. It can be seen the activation energy for stress recovery is only slightly higher than it is for stressing, but this actually results in a factor 10 difference for the attempt frequency $\nu$. By looking at the equation that describes the relaxation time, eq. (4.19) on page 28, i.e. $\tau = \tau_0 \exp \left( \frac{E_r}{k_B T} \right)$ with $\tau_0 = \nu^{-1}$, it is obvious that a small change in $E_r$ has to be compensated with a large change in $\nu$ because of the exponential behaviour.

Figure 5.26 shows the $\beta$ values for stress (magenta) and stress recovery (blue) and the boundary values obtained from the thermal plot (not shown here). The data for both stress and stress recovery have boundary lines that are 350 K apart and all data points but one are consistent with these lines.

From the transfer curves of this device (not shown here), it can be concluded that, as opposed to what was found in [13], there is no influence on the mobility due to the top-coating that was applied. Testing the influence on stress behaviour resulted in increased values of the attempt frequency $\nu$ and activation energy $E_r$ when compared to samples 1 and 2 (see table 5.3). The relaxation time however has not changed significantly, i.e. changes are within experimental uncertainty.

Again there is slightly more than a factor of 2 difference between $T_0$ and $T^*$.

5.6 Other semiconductors

Before measurements on FETs made with PTV were performed, other semiconductors have been used. Most semiconductors were found to be unusable for performing stress measurements. A brief discussion on the different semiconductors follows here.

The first stress measurements were performed on poly(2-methoxy-5-(3',7'-dimethylocyloxy)-p-phenylene vinylene) (OC$_1$OC$_{10}$-PPV). Although this semi-
Figure 5.25: The relaxation time $\tau$ as a function of the inverted temperature $T$ is shown for stress (magenta circles) and stress recovery (blue squares) and eq. (4.19) was used to fit the data (magenta and blue curves). Fit coefficients found are $\tau_0 = 1.3 \cdot 10^{-5}$ s and $\frac{E_x}{k} = 8.5 \cdot 10^3$ K for stress and $\tau_0 = 1.4 \cdot 10^{-6}$ s and $\frac{E_x}{k} = 9.2 \cdot 10^3$ K for stress recovery.
Figure 5.26: The values found for $\beta$ from the sample with top-coating as a function of temperature for both stress and stress recovery. The dotted lines represent boundary values obtained from the thermal plot.
conductor is widely used in literature, it was found here that it was unsuitable for performing stress measurements. In order to see stress effects, i.e. see a shift of the threshold voltage within a reasonable amount of time, the device has to be heated too such high temperatures that it will deteriorate during the measurement. This happens already during the first stress measurement, meaning that stress recovery measurements can not be performed. Unfortunately, the precise characteristics of a device are very sensitive to preparation conditions and reproducibility is therefore low, meaning it is not possible to perform measurements on different samples and get accurate results.

From previous work it was known that poly(9,9-dioctyl fluorene-co-bithiophene) (F8T2) has the tendency to stress very easily. This was found to be true and measurements could be performed that showed a normalised threshold voltage shift equal to one, even at low temperatures. Unfortunately, again the samples were very unstable, meaning that there was almost no current left at the end of the stress measurement. The transport could therefore not be modeled and the polymer was thus unsuitable for this work. It was tried to improve the stability of the devices by applying a poly(4-vinylphenol) (PVP) in iso-propanol top-coating as was done in [13], but this did not improve the devices.

Another semiconductor that was tested was poly(3-hexylthiophene) (P3HT). It is widely used in literature and can withstand higher temperatures than PPV and F8T2. Unfortunately, to measure any stress influences the samples had to be heated to such high temperatures that these devices too deteriorated. The influence of a PVP top-coating was investigated on one of the devices and it was found there was a profound influence. The device had an initial threshold voltage of +5 V and when it was stressed at -20 V it showed a threshold voltage shift to 0 V during the first 15-30 minutes and then it stayed there during the rest of the stress measurement. Consecutive stress measurements at different temperatures did not show any threshold voltage shift anymore. This was not investigated here further.

5.7 Overview

The results obtained in this thesis are summarised in table 5.4. Additionally, data found in literature for PTV, poly(9,9'-dioctyl-fluorene-co-bithiophene) (F8T2), a-Si:H, poly([2-methoxy-5-(3',7'-dimethylocyloxy)]-p-phenylene viny lene) (OC1OC10-PPV), α-sexithiophene (T6), cadmium sulfide (Cds), pentacene and poly(3-hexyl thiophene) (P3HT) is also shown. The values found in literature will be used to compare orders of magnitude. Below is a brief discussion of literature on a-Si:H.

5.7.1 a-Si:H

Analysis of stress measurements on a-Si:H has shown there is a dependence on preparation conditions for $\nu$, $E_r$ and $T^*$. This dependence is used to optimise discrete TFTs. A typical example of a stress measurement on a-Si:H FETs is shown in [14]. Figure 5.27a shows the thermal plot as obtained there. The threshold voltage shift is fit using a stretched exponential (dotted line) and values found are $E_r = 0.99$ eV and $T^* = 450$ K. The stretched exponential can be seen to describe the data reasonably well for $E_{\text{therm}} < 0.95$ eV, but it exhibits
<table>
<thead>
<tr>
<th>Semiconductor</th>
<th>#</th>
<th>type</th>
<th>$\nu$ [Hz]</th>
<th>$T^*$ [K]</th>
<th>$T^*$ [meV]</th>
<th>$T_0$ [K]</th>
<th>$T_0$ [meV]</th>
<th>$E_r$ [eV]</th>
<th>Comment</th>
<th>Ref</th>
<th>$\tau$ [h]</th>
</tr>
</thead>
<tbody>
<tr>
<td>PTV</td>
<td>1</td>
<td>stress</td>
<td>$10^3$</td>
<td>$1200 \pm 150$</td>
<td>$103 \pm 13$</td>
<td>$468 \pm 20$</td>
<td>$40 \pm 2$</td>
<td>$0.61$</td>
<td>[6]: $T_0 = 382$ K</td>
<td>56</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>recovery</td>
<td></td>
<td>$875 \pm 225$</td>
<td>$75 \pm 20$</td>
<td>$492 \pm 20$</td>
<td>$42 \pm 2$</td>
<td>$0.63 \pm 0.02$</td>
<td></td>
<td>104</td>
<td></td>
</tr>
<tr>
<td>PTV</td>
<td>2</td>
<td>stress</td>
<td>$\sim 20$</td>
<td>$1100 \pm 200$</td>
<td>$95 \pm 17$</td>
<td>$449 \pm 30$</td>
<td>$39 \pm 3$</td>
<td>$0.53$</td>
<td>[6]: $T_0 = 382$ K</td>
<td>227</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>recovery</td>
<td></td>
<td>$650 \pm 100$</td>
<td>$56 \pm 9$</td>
<td>$466 \pm 30$</td>
<td>$40 \pm 3$</td>
<td>$0.47$</td>
<td></td>
<td>35</td>
<td></td>
</tr>
<tr>
<td>PTV coating</td>
<td>3</td>
<td>stress</td>
<td>$8 \cdot 10^4$</td>
<td>$1175 \pm 175$</td>
<td>$101 \pm 15$</td>
<td>$453 \pm 20$</td>
<td>$39 \pm 2$</td>
<td>$0.74$</td>
<td>[6]: $T_0 = 382$ K</td>
<td>41</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>recovery</td>
<td></td>
<td>$875 \pm 175$</td>
<td>$75 \pm 15$</td>
<td>$469 \pm 20$</td>
<td>$40 \pm 2$</td>
<td>$0.80$</td>
<td></td>
<td>31</td>
<td></td>
</tr>
<tr>
<td>a-Si:H</td>
<td></td>
<td>stress</td>
<td>$10^9$</td>
<td>720</td>
<td>62</td>
<td>band</td>
<td>band</td>
<td>0.975</td>
<td>[14]</td>
<td>5</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>recovery</td>
<td>$10^{13}$</td>
<td>720*</td>
<td>62*</td>
<td>band</td>
<td>band</td>
<td>1.1-1.5</td>
<td>[14]</td>
<td>313</td>
<td></td>
</tr>
<tr>
<td>T6</td>
<td></td>
<td>stress</td>
<td>$10^5$</td>
<td>382</td>
<td>33</td>
<td>417</td>
<td>36</td>
<td>0.52</td>
<td>[15]</td>
<td>0.033</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>recovery</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CdS</td>
<td></td>
<td>stress</td>
<td>$10^5$</td>
<td>522</td>
<td>45</td>
<td>522</td>
<td>45</td>
<td>0.67</td>
<td></td>
<td>3.6</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>recovery</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>OC$<em>1$OC$</em>{10}$-PPV</td>
<td></td>
<td>stress</td>
<td>$10^9$</td>
<td>580</td>
<td>50</td>
<td>568</td>
<td>49</td>
<td>0.96</td>
<td>[6]: $T_0 = 540$ K</td>
<td>3.2</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>recovery</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>F8T2</td>
<td></td>
<td>stress</td>
<td>$10^3$</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0.52</td>
</tr>
<tr>
<td></td>
<td></td>
<td>recovery</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Pentacene</td>
<td></td>
<td>stress</td>
<td></td>
<td></td>
<td></td>
<td>444</td>
<td>38</td>
<td></td>
<td>[6]: $T_0 = 385$ K</td>
<td>[17]</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>recovery</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>P3HT</td>
<td></td>
<td>stress</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>[6]: $T_0 = 425$ K</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>recovery</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 5.4: This table provides an overview of the results that were obtained in this thesis. No explicit data.

5.7. OVERVIEW
RESULTS

Figure 5.27: Threshold voltage shifts obtained in [14] by applying a gate voltage of $V_g = 30$ V for different times ($1 < t < 10^5$ s) and temperatures ($303 \, K < T < 403 \, K$) unified in terms of the thermalisation energy $E_{therm} = kT \ln (vt)$ are shown in (a). Both stretched exponential (dotted line) and stretched hyperbole (solid line) fits are shown. In (b) the probability distribution of activation energies for defect creation and defect removal is shown. Again the dotted line represents the stretched exponential fit and the solid line shows the stretched hyperbole fit.

A clear deviation for $E > 0.95$ eV. A stretched hyperbole is then introduced that much better describes the data for $E_{therm} > 0.95$ eV. Values found are then $E_r = 0.975$ eV and $T^* = 720$ K.

In figure 5.27b the probability distribution of activation energies for defect creation and defect removal are shown. The data have been obtained by taking the derivative of the threshold voltage shifts for defect creation (figure 5.27a) and defect relaxation. The attempt frequency for defect removal is found to be around $10^{13}$ Hz.
Chapter 6

Summary and conclusions

The operational stability of organic field-effect transistors is crucial for applications using polymer electronics. Any operational instability is reflected in a change of the electrical transport properties of the transistors upon application of a continuous gate bias.

The charge transport in organic field-effect transistors is typically described by the hopping of charge carriers in an exponential density of transport states. The source-drain current can be expressed as a function of gate bias and temperature using three parameters, namely a prefactor, a threshold voltage $V_{th}$ and the width of the exponential density of transport states, given by the characteristic temperature $T_0$. The main change in these transport parameters upon applying a continuous gate bias, i.e. by stressing the transistor, is a shift of the threshold voltage.

This threshold voltage shift is well-known in $a$-Si. There, the shift is related to the formation of defects. Charge carriers induced by the gate will first be trapped by the created defects. A higher gate bias is then needed to create free charge carriers. The result is a parallel shift of the transfer characteristics. The shift of the threshold voltage with time follows a stretched exponential. The characteristic time constant $\tau$ is thermally activated. The prefactor is an attempt frequency $\nu$ and the activation energy is $E_r$. The exponent $\beta$ in the stretched exponential is equal to the temperature divided by the width of the exponential distribution of defect sites, i.e. the temperature $T^*$. 

6.1 Goals

The aim of this thesis was threefold. Firstly, it was investigated whether the shift of the threshold voltage for organic semiconductors could be phenomenologically described in the same way as was done for $a$-Si. Secondly, a comparison was made between the two characteristic temperatures $T_0$ and $T^*$. Since the formation of defects in organic semiconductors is unlikely, it was expected that the shift of the threshold voltage is due to the space charge of the trapped charge carriers. This means that the same density of states is responsible for charge transport and charge trapping, meaning that $T_0$ and $T^*$ should be identical. Finally, the intrinsic stability of organic semiconductors was compared to that of $a$-Si by looking at the numerical values.
6.2 Methods

To this end, stress measurements were performed on several field-effect transistors using various organic semiconductors. Finally, poly(2,5-thienylene vinylene) (PTV) was taken as a model compound. In addition to the stress measurements on standard transistors, some transistors were measured with a poly(4-vinylphenol) (PVP) top-coating.

The transport characteristics of the transistors were measured as a function of stress time and temperature. A Matlab routine was written to obtain values of $V_{th}$ and $T_0$ from the transfer curves. The shift of the threshold voltage with time was then fitted by a stretched exponential.

6.3 Conclusions

Data analysis of the work done here can be summarised as follows:

- A gate bias stress causes a parallel shift of the transfer curves.
- The shift of the threshold voltage with time can be described by a stretched exponential, where the characteristic time constant $\tau$ is thermally activated. The attempt frequency $\nu$ is found to be extremely low. The physical origin of this is unknown.
- For most semiconductors $T_0$ is comparable to $T^*$. However, for PTV they are different.
- Organic semiconductors are intrinsically more stable than $a$-Si. This stability actually hampered the investigations. Application of a top coating may even increase the stability.
- Contrary to what is found for $a$-Si, stress effects in organic semiconductors are reversible. This has huge practical consequences.

In figure 6.1 the characteristic time constant $\tau$ for a PTV transistor and for an $a$-Si transistor, both are stressed at 370 K, are shown. The higher intrinsic stability of PTV is obvious.

6.4 Technology assessment

The results obtained in this thesis can have a far reaching impact on electronics as it can be seen today. It is shown here that the intrinsic stability of organic semiconductors is higher than that of $a$-Si when both are measured on a $SiO_2$ substrate. Moreover, reverse stressing organic semiconductors is much easier than reverse stressing $a$-Si, which is nearly impossible from a practical view. This means that the possibility of replacement of $a$-Si with organic semiconductors should be considered for certain applications.

The production of highly stable organic electronics might however not be trivial because of the different gate dielectric that has to be used to ensure flexibility. The replacements substrates usually have much bigger problems with respect to ion movement and the presence of water than $SiO_2$ substrates do. This might be the limiting factor for complete replacement of $a$-Si with organic semiconductors.
Figure 6.1: The characteristic time scale $\tau$ is shown here for PTV measured in this thesis and for $\alpha$-Si as mentioned in [14], both stressed at 370 K.
Bibliography


Appendix A

IBASIC program

As mentioned in Section 2.3, measurements are automated using an IBASIC program that can be run on a HP/Agilent semiconductor parameter analyser. The program that was used throughout this thesis is listed here.

```ibasic
90 !**************************************************************
91 ! Perform stress sweeps gate and drain
92 ! stress strvg.mes gate and drain sweep
93 ! long duration
94 !**************************************************************
98 ! Define a handler in the COM area so it can be used
99 ! in every context
100 COM ©Hp415x
107 !
108 ! Let the handler point to an I/O path (device), in this case 800 i.e. the built-in IBASIC controller
110 ASSIGN ©Hp415x TO 800
120 DISP "Loading setup files in memory"
135 !
140 !*** load files mes-files
141 ! Send 'command string' to the Hp415x
142 ! OUTPUT ©Hp415x;"command string"
148 ! Set the storage device to INTERNAL
149 ! (built-in floppy drive)
150 OUTPUT ©Hp415x;":MMEM:DEST INT"
159 ! Load a setup file into memory
160 OUTPUT ©Hp415x;":MMEM:LOAD:STAT 0, 'STRVG9.MES'"
164 ! Save setup file to MEM1.MES
165 OUTPUT ©Hp415x;":MMEM:STOR:STAT 0, 'MEM1.MES', 'MEMORY''
170 OUTPUT ©Hp415x;":MMEM:LOAD:STAT 0, 'SWEEP9G.MES'"
175 OUTPUT ©Hp415x;":MMEM:STOR:STAT 0, 'MEM2.MES', 'MEMORY''
180 OUTPUT ©Hp415x;":MMEM:LOAD:STAT 0, 'SWEEP9D.MES'"
185 OUTPUT ©Hp415x;":MMEM:STOR:STAT 0, 'MEM3.MES', 'MEMORY''
190 CALL Drain_sweeps("SWDA-")
200 CALL Gate_sweep("SW_",0)
```
APPENDIX A. IBASIC PROGRAM

210 Interval=0.
300 !
310 ! *** start loop ***
320 ! ****************************
400 FOR Tel=0 TO 20 STEP 1
420 DISP "THIS IS VG STRESS RUN NR";Tel
430 !
439 ! STRESS THE SAMPLE AT THIS VALUE
440 Vg=-22.6
500 ! **** STRESS ******
520 CALL Stress("STR_",Tel,Vg) ! 0 = nostress VG= ground
560 !
600 ! **** Gate SWEEP ****
650 CALL Gate_sweep("SW_",Tel+1)
800 NEXT Tel
910 ! ****************************
920 ! *** end loop ***
930 !
950 CALL Drain_sweeps("SWDB-")
970 DISP "THE PROGRAM HAS FINISHED"
980 BEEP
981 BEEP
982 BEEP
1000 END
9000 !
9010 !
9020 ! ****************************
9025 !
9030 ! **** Code of subprograms ****
9035 !
9040 ! ****************************
9050 !
9060 !
10000 ! ****************************
10005 SUB Measure_save(Filename$,Number)
10010 !***** execute measurement ********
10020 !
10030 COM @Hp
10040 ASSIGN @Hp TO 800
10048 ! Execute the measurement :PAGE:SCOntrol:SINGle
10050 OUTPUT @Hp;":PAGE:SCON:SING"
10055 ! Wait until measurement is completed.
10056 ! Check OPeration Completed bit
10060 OUTPUT @Hp;"*OPC?"
10070 ENTER @Hp;Complete
10080 !**** save data of measurement
10085 DISP "Saving data"
10090 OUTPUT @Hp;":MMEM:DEST INT"
10110 OUTPUT @Hp;":MMEM:STOR:SSH:DEL TAB"
10120 OUTPUT @Hp;":MMEM:STOR:SSH:LIND 1,MAX"
10130 OUTPUT @Hp;"":MEM:STOR:SSH:SMARK NONE"
10140 OUTPUT @Hp;":MEM:STOR:SSH:UNIT OFF"
10150 OUTPUT @Hp;":MEM:STOR:SSH '';Filename$;VAL$(Number);''"
10151 ! the name of the file is between ' '
10152 ! ; appends several variables
10160 OUTPUT @Hp;"*OPC?"
10170 ENTER @Hp;Complete
10180 SUBEND !*** END Measure_Save ***
10190 !
10200 !
10500 !**********************************************************************
10505 SUB Measure(Filename$,Number)
10510
10520 !***** execute measurement ***********
10530 COM @Hp
10540 ASSIGN @Hp TO 800
10548 ! Execute the measurement :PAGE:SCONtrol:SINGle
10550 OUTPUT @Hp;":PAGE:SCON:SING"
10555 ! Wait until measurement is completed.
10556 ! Check Operation Completed bit
10560 OUTPUT @Hp;"*OPC?"
10570 ENTER @Hp;Complete
10580 SUBEND !*** END Measure ***
10590 !
11000 !************************************************************************
11010 SUB Drain_sweeps(File$)
11020 !****** drain sweeps **********
11030 !
11040 COM @Hp415x
11110 ASSIGN @Hp415x TO 800
11120 OUTPUT @Hp415x;":MEM:LOAD:STAT 0,'MEM3.MES','MEMORY''"
11121 ! load .mes in memory
11130 OUTPUT @Hp415x;":PAGE:MEAS:MSET:ITIM MED"
11131 ! set MEDium integration time
11140 OUTPUT @Hp415x;":PAGE:DISP:SET:MODE GRAP"
11141 ! selects graph mode instead of spread sheet
11150 !
11160 DISP "Performing DRAIN sweeps"
11170 !** start drain sweep
11180 CALL Measure_save(File$,@)
11181 ! subprogram measurement & saving data
11190 !
11500 SUBEND !*** END Drain_Sweeps ***
11510 !
11520 !
12000 !************************************************************************
12010 SUB Gate_sweep(File$,Rn)
12020 !***** gate sweep ***********
12030 !
12100 COM @Hp415x
APPENDIX A. IBASIC PROGRAM

12110 ASSIGN @Hp415x TO 800
12120 OUTPUT @Hp415x;":\MMEM\:LOAD\:STAT 0, 'MEM2\,MES', 'MEMORY'"
12121 ! load .mes in memory
12130 OUTPUT @Hp415x;":\PAGE\:MEAS\:MSET\:ITIM MED"
12131 ! set MEDium integration time
12140 OUTPUT @Hp415x;":\PAGE\:DISP\:SET\:MODE GRAP"
12141 ! selects graph mode instead of spread sheet
12150 !
12160 DISP "Performing GATE sweep"
12170 !*** start gate sweep
12180 CALL Measure_save(File$,Rn)
12181 !*** subprogram measurement & saving data
12190 !
12500 SUBEND !*** END Gate_Sweep ***
12510 !
12520 !
13000 !***************************
13010 SUB Stress(File$,Rn,Volt) !** ground
13020 !****** gate sweep *********
13050 COM @Hp415x
13060 ASSIGN @Hp415x TO 800
13100 OUTPUT @Hp415x;":\MMEM\:LOAD\:STAT 0, 'MEM1\,MES', 'MEMORY'"
13101 ! load .mes in memory
13110 ! *** set values for stress
13120 Interval=.009*EXP(Rn/1.3)
13121 ! LRR: times duration of stress div. by 1.5 [min]?
13125 Points=1000
13126 ! No. of sampling points
13129 Value=1000*Interval
13130 ! Time to stress
13131 IF Interval>65 THEN ! Interval too large
13132 Interval=65 ! Adjusting parameters
13133 Points=DROUND(Value/Interval,2)
13134 Ipoints=INT(Points)
13135 IF Ipoints>10001 THEN
13136 BEEP
13137 DISP "CANNOT MEASURE THIS..
13138 Ipoints=10001
13139 END IF
13140 END IF
13145 OUTPUT @Hp415x;":\PAGE\:MEAS\:SAMP\:INT";Interval
13146 ! set Initial INTerval range:
13147 ! 6E-05 to 65.534E+00 (=65 seconds!!)
13150 OUTPUT @Hp415x;":\PAGE\:DISP\:GRAP\:X\:MAX";Value
13151 ! set maximum X axis value
13160 OUTPUT @Hp415x;":\PAGE\:MEAS\:MSET\:ITIM SHOR"
13161 ! set SHORT integration time
13170 OUTPUT @Hp415x;":\PAGE\:MEAS\:SAMP\:POIN";Points
13171 ! No. of sampling points
13200 IF Volt=0 THEN
13210 OUTPUT @Hp415x;"::PAGE:CHAN:CDEF:SMU2:MODE COMM"
13211 ! p. 5-89
13220 ELSE
13230 OUTPUT @Hp415x;"::PAGE:MEAS:SAMP:CONS:SMU2:SOUR ";Volt
13231 ! Stress with Vg=Volt   p. 5-181
13240 END IF
13300 OUTPUT @Hp415x;"::PAGE:DISP:SET:MODE GRAP"
13301 ! selects graph mode instead of spread sheet
13305 DISP "Stressing";Value;"secs at ";Volt;"Volt run";Rn
13310 !*** start stress
13320 CALL Measure(File$,Rn)
13321 !*** subprogram measurement & saving data
13330 !
13500 SUBEND !*** END Gate_Sweep ***
13510 !
13520 !
Appendix B

Solving differential equation

The differential equation for the threshold voltage shift, eq. (4.16) on page 28, i.e.

\[ \frac{d\Delta V_{th}}{dt} = -a(\nu t)^{-\alpha} \Delta V_{th}(t), \tag{B.1} \]

can be solved by rewriting it to

\[ \frac{1}{\Delta V_{th}} \frac{d\Delta V_{th}}{dt} = -a(\nu t)^{-\alpha} \tag{B.2} \]

and integrating. This gives

\[ \ln(\Delta V_{th}) = -a \left( \frac{1}{\alpha + 1} \right) (\nu t)^{-\alpha+1} + c_1 \tag{B.3} \]

with \( c_1 \) a constant of integration. For the threshold voltage shift this then results in

\[ \Delta V_{th} = \exp \left[ -a \left( \frac{1}{\alpha + 1} \right) (\nu t)^{-\alpha+1} \right] \cdot \exp(c_1). \tag{B.4} \]

For \( a\)-Si the threshold voltage shift was shown to be

\[ \Delta V_{th}(t) = \Delta V_{th}(0) \exp \left[ -\left( \frac{t}{\tau} \right)^{\beta} \right] \tag{B.5} \]

and by setting this equal to what was derived from the differential equation it is found that \( \alpha = 1 - \beta \) and

\[ \tau = \left( \frac{a}{\beta \nu^{-\alpha}} \right)^{-\frac{1}{\beta}}. \tag{B.6} \]

Using \( x^\nu = \exp[\ln(x^\nu)] \) this can be rewritten as

\[ \tau = \frac{1}{\nu} \exp \left[ \frac{1}{\beta} \ln \left( \frac{\nu \beta}{a} \right) \right]. \tag{B.7} \]

Using \( \beta = \frac{T}{T_f} \) and defining \( \tau_0 = \nu^{-1} \) this gives an Arrhenius equation for \( \tau \), namely

\[ \tau = \tau_0 \exp \left( \frac{E_r}{kT} \right) \tag{B.8} \]
where the activation energy $E_r$ is found to be $E_r = kT^* \ln \left( \frac{\beta}{\alpha T_0} \right)$. With $\beta = \frac{T}{k}$, the activation energy is a function of temperature, but varies only slowly with $T$ because of the logarithmic dependency. It is unclear what the origin of this dependency is and here, only a single value for $E_r$ is extracted from the stress data.
Appendix C

Thermalisation energy

The equation for the normalised threshold voltage as a function of time, eq. (4.18) on page 28, i.e.

\[
\frac{V_{th}(t) - V_{th}(0)}{V_g - V_{th}(0)} = 1 - \exp \left[ - \left( \frac{t}{\tau} \right)^\beta \right]
\]  

(C.1)

can be rewritten using \( x^y = \exp[\ln(x^y)] \) to read

\[
\frac{V_{th}(t) - V_{th}(0)}{V_g - V_{th}(0)} = 1 - \exp \left[ - \exp \left( \beta \ln \left( \frac{t}{\tau} \right) \right) \right].
\]  

(C.2)

Inserting the Arrhenius behaviour for the relaxation time \( \tau \), eq. (4.19) on page 28, i.e. \( \tau = \tau_0 \exp \left( \frac{E_r}{kT} \right) \), this gives

\[
\frac{V_{th}(t) - V_{th}(0)}{V_g - V_{th}(0)} = 1 - \exp \left[ - \exp \left\{ \beta \ln \left( \frac{t}{\tau_0} \right) - \beta \frac{E_r}{kT} \right\} \right]
\]  

(C.3)

or reduced to the same denominator

\[
\frac{V_{th}(t) - V_{th}(0)}{V_g - V_{th}(0)} = 1 - \exp \left[ - \exp \left\{ \frac{kT \beta \ln \left( \frac{t}{\tau_0} \right) - \beta E_r}{kT} \right\} \right].
\]  

(C.4)

Replacing \( \beta \) with \( \frac{T}{T^*} \) this equals

\[
\frac{V_{th}(t) - V_{th}(0)}{V_g - V_{th}(0)} = 1 - \exp \left[ - \exp \left\{ \frac{E_{therm} - E_r}{kT^*} \right\} \right]
\]  

(C.5)

with \( E_{therm} = kT \ln \left( \frac{t}{\tau_0} \right) \).
Appendix D

Matlab transport model

The model used to fit the drain current in Matlab is based on eq. (4.6), i.e.

\[ I_d = \frac{aWC_iV_d}{L} (V_g - V_{th})^{b+1}, \]  

(D.1)

with

\[ a = \frac{\sigma_0}{e} \frac{1}{b + 1} \frac{C_i^b}{b} \]

\[ \cdot \left[ \left( \frac{T_o}{T} \right)^4 \sin\left( \pi \frac{T}{T_0} \right) \right]^{T_o/T} \]

\[ \cdot \left( \sqrt{2kT_0 \varepsilon \varepsilon_0} \right)^{-b} \]  

(D.2)

and

\[ b = 2 \left( \frac{T_o - T}{T} \right). \]  

(D.3)

It was rewritten to

\[ I_d = \frac{aWC_i}{L(b+2)} \cdot \left\{ \left[ \frac{1}{2} (V_d + V_{th} - V_g) + \frac{1}{2} |V_d + V_{th} - V_g| \right]^{b+2} \right. \]

\[ - \left. \left[ \frac{1}{2} (V_{th} - V_g) + \frac{1}{2} |V_{th} - V_g| \right]^{b+2} \right\} \]  

(D.4)

in order to block current at \( V_g > V_{th} \) and using the Matlab function "fmins" a least squares fitting procedure is used to determine values for \( a, b \) and \( V_{th} \).
Index

acceptor, 4
accumulation, 7, 8, 18, 20
anneal, 9, 12, 13
Arrhenius, 43
attempt frequency, 27
automation, 13

barrier, 6
Boltzmann constant, 5
bonds
\( \pi \)-bonds, 3, 5
\( \sigma \)-bonds, 3
box, 13
bulk, 8

capacitance, 18, 27
capacitor, 6
carbon, 2, 5
channel, 6
current, 18
length, 9, 21
width, 9
characteristic temperature, 25

characteristics
output, 20, 31
transfer, 15, 31
charge carriers, 4, 15, 21
majority, 8
minority, 8
trapping, 27

charge density, 26
conduction band, 4
conductivity, 2, 26
conductor, 2
contact, 21
drain, 6, 9, 14
gate, 6, 9, 14, 15
ohmic, 21, 33
resistance, 9
Schottky, 21
source, 6, 9, 14

thermal, 13
crystal, 4
current
drain, 18
defects, 4, 5, 27
degenerate, 4
depletion, 7, 8
diffusion, 27
distribution
exponential, 25
trap sites, 25, 27
Fermi-Dirac, 25
Gaussian, 5, 25
donor, 4
doped, 2, 9
electron, 2, 4
affinity, 6
deficiency, 4

energy
activation, 5, 25, 28
band, 3, 4, 6
bending, 7
gap, 4
Fermi level, 6, 7, 23, 25
forbidden, 4
level, 3
thermal, 4
thermalisation, 29

FET, 15
flatband, 7, 18

hole, 4, 8, 20
HOMO, 5
hopping, 5
variable range, 3, 5, 25
hysteresis, 18

IBASIC, 13
impurity, 2, 4
<table>
<thead>
<tr>
<th>Word</th>
<th>Page Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>insulator</td>
<td>2, 7</td>
</tr>
<tr>
<td>inversion</td>
<td>8</td>
</tr>
<tr>
<td></td>
<td>strong, 15</td>
</tr>
<tr>
<td>leakage</td>
<td>18</td>
</tr>
<tr>
<td>LUMO</td>
<td>5</td>
</tr>
<tr>
<td>mica</td>
<td>13</td>
</tr>
<tr>
<td>MIS</td>
<td>7</td>
</tr>
<tr>
<td>mobility</td>
<td>18, 21, 33</td>
</tr>
<tr>
<td>molecular structure</td>
<td>12, 13</td>
</tr>
<tr>
<td>needle</td>
<td>13</td>
</tr>
<tr>
<td>normalisation</td>
<td>35, 38</td>
</tr>
<tr>
<td>nucleus</td>
<td>4</td>
</tr>
<tr>
<td>orbital</td>
<td>2</td>
</tr>
<tr>
<td>organic</td>
<td></td>
</tr>
<tr>
<td>material</td>
<td>2</td>
</tr>
<tr>
<td>paste</td>
<td>13</td>
</tr>
<tr>
<td>percolation</td>
<td>26</td>
</tr>
<tr>
<td>phonon</td>
<td>4</td>
</tr>
<tr>
<td>pinch-off</td>
<td>20</td>
</tr>
<tr>
<td>polymer</td>
<td>2</td>
</tr>
<tr>
<td></td>
<td>conjugated, 2, 5, 27</td>
</tr>
<tr>
<td>precursor</td>
<td>9</td>
</tr>
<tr>
<td>pump</td>
<td>13</td>
</tr>
<tr>
<td>quantum number</td>
<td>4</td>
</tr>
<tr>
<td>region</td>
<td></td>
</tr>
<tr>
<td></td>
<td>linear, 15, 21</td>
</tr>
<tr>
<td></td>
<td>saturation, 18, 20</td>
</tr>
<tr>
<td>relaxation time</td>
<td>28</td>
</tr>
<tr>
<td>resistance</td>
<td></td>
</tr>
<tr>
<td></td>
<td>channel, 21</td>
</tr>
<tr>
<td></td>
<td>contact, 21</td>
</tr>
<tr>
<td>semiconductor</td>
<td>2</td>
</tr>
<tr>
<td></td>
<td>p-type, 6, 8, 21</td>
</tr>
<tr>
<td></td>
<td>parameter analyser, 13</td>
</tr>
<tr>
<td>shell</td>
<td>4</td>
</tr>
<tr>
<td></td>
<td>subshell, 4</td>
</tr>
<tr>
<td>solvent</td>
<td>9</td>
</tr>
<tr>
<td>spincoating</td>
<td>9, 12, 13</td>
</tr>
<tr>
<td>stress</td>
<td>14, 23</td>
</tr>
<tr>
<td></td>
<td>recovery, 24</td>
</tr>
<tr>
<td>sweep</td>
<td></td>
</tr>
<tr>
<td></td>
<td>drain, 13, 20</td>
</tr>
<tr>
<td></td>
<td>gate, 13, 15</td>
</tr>
<tr>
<td>switch-on voltage</td>
<td>18</td>
</tr>
<tr>
<td>threshold voltage</td>
<td>15, 27</td>
</tr>
<tr>
<td></td>
<td>shift, 18, 23, 24</td>
</tr>
<tr>
<td>transconductance</td>
<td>18</td>
</tr>
<tr>
<td>transistor</td>
<td></td>
</tr>
<tr>
<td></td>
<td>field effect, 5, 15</td>
</tr>
<tr>
<td></td>
<td>finger, 9</td>
</tr>
<tr>
<td></td>
<td>ring, 9</td>
</tr>
<tr>
<td>trap</td>
<td>4</td>
</tr>
<tr>
<td></td>
<td>site, 24</td>
</tr>
<tr>
<td>tunneling</td>
<td>5, 21, 25</td>
</tr>
<tr>
<td>valence band</td>
<td>4</td>
</tr>
<tr>
<td>wafer</td>
<td>9</td>
</tr>
<tr>
<td>workfunction</td>
<td>6, 21</td>
</tr>
</tbody>
</table>