Characterization of hafnium oxide thin films for applications in high efficiency c-Si solar cells

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Characterization of Hafnium Oxide Thin Films for Applications in High Efficiency c-Si Solar Cells

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Abstract

In this work, HfO$_2$ was proposed as a passivation material for n-type and n$^+$ surfaces of high efficiency crystalline silicon solar cells. The potential for passivation is evaluated through extensive characterization of HfO$_2$ layers, using a variety of methods, which have provided insight into the physical, chemical, and electrical properties of the material.

HfO$_2$ layers were deposited via an atomic layer deposition (ALD) process, using two main precursors, the first being HyALD, a metal-organic precursor, containing a cyclopentadienyl ring, which improves the stability of the molecule, and the second being HfCl$_4$, a metal-halide precursor, used extensively for deposition of HfO$_2$. The HyALD precursor was used to deposit films using a plasma enhanced ALD process, at 250$^\circ$C, whereas HfCl$_4$ was used in a thermal ALD process, at 200$^\circ$C and 300$^\circ$C.

Initial simulations, using a Monte Carlo algorithm were used to compare the optical properties of HfO$_2$ with the standard passivation materials, Al$_2$O$_3$ and SiO$_2$, showing that similar performance can be expected from the three oxides. Transmission electron microscopy (TEM) was used to reveal the internal structure of HfO$_2$ under different annealing conditions, and chemical analysis, via energy-dispersive X-ray spectroscopy (EDS) and elastic recoil detection (ERD) have provided information regarding the foreign atomic species contained in the deposited layers, such as Cl and H.

Electrical characterization was done via capacitance-voltage (C-V) and conductance-voltage (G-V) measurements of metal-oxide-semiconductor (MOS) structures, using HfO$_2$ as the dielectric. The oxide fixed charge ($Q_f$) and the density of interface traps ($D_{it}$) were extracted, revealing the potential of HfO$_2$ for field effect and chemical passivation, respectively. Layer analysis was carried out for as-deposited samples, as well as after 30 minute anneals, at 300$^\circ$C, 400$^\circ$C, and 500$^\circ$C. The HyALD precursor showed very high $D_{it}$ for as-deposited layers, which was gradually reduced with annealing. The HfCl$_4$ precursor produced structures with a lower $D_{it}$, which contained either negative or positive fixed charge, depending on the deposition and annealing temperatures. The negative charge was attributed to the segregation of Cl impurities towards the interface between the HfO$_2$ layer and the silicon wafer.

Effective lifetime measurements via photocurrent decay in silicon wafers passivated with HfO$_2$ were used to calculate the surface recombination velocity ($S_{eff}$), in order to directly evaluate the overall passivation quality. High quality, n-doped, high resistivity (15.5 Ω cm) Cz silicon wafers with a mirror-polished surface were used for initial lifetime measurements. Good passivation was achieved after annealing at 300$^\circ$C and 400$^\circ$C with the HfCl$_4$ precursor, due to the presence of sufficient negative fixed charge to create an inversion layer and the low $D_{it}$ which ensured good chemical passivation. The very high $D_{it}$ obtained with the HyALD precursor resulted in very high $S_{eff}$ values as-deposited and after annealing at 300$^\circ$C. Higher temperature anneals provided some improvement, but overall passivation quality remained low. Lifetime measurements were also carried out for PV-grade, lower resistivity (4 Ω cm), n-type Cz silicon, textured wafers, with a 120 Ω/sq n$^+$ front surface field (FSF) in order to evaluate oxide performance in...
situations corresponding to solar cell applications.

The investigation results have led to the conclusion that HfO₂ is a material which can provide a wide range of properties, depending on deposition and post-processing conditions, showing potential for passivation of n-type and n⁺ silicon surfaces. Further research into this topic is proposed, in order to optimize the performance of HfO₂ as a passivation material for high efficiency solar cell applications.
Preface

The work presented in this thesis was carried out in fulfillment of the requirements for obtaining the Master of Science degree in Applied Physics, on the topic of Functional (Nano) Materials, at the Eindhoven University of Technology. The research project was part of a collaboration between IMEC, in Leuven, where most of the work took place over the ten months of the project, and SoLayTec, based in Eindhoven. Part of the work was also done at the TU/e Nanolab. This thesis constitutes my first foray into research in the field of photovoltaics.

First of all I would like to thank my thesis advisor, Professor Erwin Kessels, for his guidance throughout the year. It is with his help that I have managed to create what is, in my opinion, a well-structured and detailed thesis. His periodic input has kept me from straying from the path of meaningful research.

Of my colleagues at IMEC, I must thank my daily supervisor, Emanuele Cornagliotti. Due to his constant input and approachable nature, I have gained a wealth of knowledge, both within my research topic, and on general practices for reporting results in the academic environment. I believe that the experience gathered during the months spent under his wing will constitute a first step on my way towards becoming a successful, independent researcher. I would like to give special thanks to Laura Nyns, who was my go-to person for ALD depositions at IMEC. Significant gratitude is also owed to Barry O’Sullivan. His input regarding the electrical characterization of thin films has helped clarify what was, in my opinion, the most difficult part of my thesis. Finally, I must mention my colleagues Aashish Sharma and Shruti Jambaldinni, whom I consider to be my closest friends within the company.

To my second supervisor, Bas Dielissen of SoLayTec, I must express my gratitude for his very practical input, which has often provided a view of things from an outside perspective. I must also thank Huib Heezen and Ronald van Dijk of SoLayTec, for being my initial link to the entire project. Truly, without meeting them, this past academic year would have been completely different.

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Lastly, I would like to thank my family, without whom, nothing like this would be possible. The constant support from my parents has allowed me to always aim higher, and their confidence in me is most of the time greater than my own. My older brother has always echoed their feelings, while also challenging me to better myself through friendly competition, and for this I am eternally grateful. In hopes of continuing to make my family proud, I would like to close this section with a message to them in my own language:

Vă mulțumesc pentru tot sprijinul acordat de-a lungul anilor. Fără voi nu aș fi ajuns aici. Vă iubesc enorm!

Eindhoven, September 2015

Characterization of Hafnium Oxide Thin Films for Applications in High Efficiency c-Si Solar Cells
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Chapter 1

Introduction

1.1 The necessary rise of photovoltaic devices

The sun is a virtually unlimited source of energy for the entire planet. The emitted radiation from our nearest star provides the conditions for life and it is directly or indirectly involved in almost all processes that take place on Earth. It is because of the accessibility and inexhaustible nature of solar radiation, that the idea of harvesting it for humanity’s everyday energy requirements has attracted researchers throughout the 20th century and, increasingly, in the 21st century.

French physicist Edmond Becquerel is credited with the discovery of the photovoltaic effect, in 1839. While working in his father’s laboratory, at age 19, he had managed to generate electricity by illuminating platinum and silver electrodes with light of different wavelengths[1]. The first photovoltaic devices were developed using materials such as selenium[2, 3], and later copper-copper oxide[4] and thallium sulphide[5]. The structure of such devices is shown in fig. 1.1:

![Figure 1.1: Structure of the most efficient photovoltaic devices developed during the 1930s. Incident photons would generate electron-hole pairs in the Cu$_2$O, Tl$_2$S or Se layer stacked between the two metal contacts[6].](image)

Development of silicon solar cells began around the mid-20th century, along with the development and understanding of the first p-n junctions. The first modern silicon solar cell was developed in 1954[7]. The device, shown in fig. 1.2, had considerably higher efficiency compared to earlier ones. Although this advancement provided increased interest in photovoltaic technology, the difficulties of silicon preparation at the time meant that high production costs would limit solar cells to providing energy for space applications, where costs are not an issue.

Nowadays, economic and environmental constraints have led to a shift away from fossil fuels as the main energy source for everyday applications. The effects of CO$_2$ and other greenhouse gases have become increasingly apparent. The onset of global warming has been signaled by...
steadily increasing global average temperatures, causing visible climate shift and environmental changes. Improvements in efficiency and reductions in material costs for solar energy solutions have led to an ever-increasing presence of solar cells and solar thermal collectors on the global energy market. As a result, in 2013, the global added renewable electricity capacity (143 GW) surpassed that for fossil fuels (141 GW), signaling a worldwide trend towards clean energy, as mentioned by Bloomberg[8].

The predicted trend from fig. 1.3 suggests that investments into solar energy will continue to grow, whereas those for fossil fuels will decrease over the next few decades. The International Energy Agency has also predicted that, by 2050, "the sun could be the world’s largest source of electricity"[6]. This optimistic view is further supported by the decreasing price of solar energy solutions, due to recent technological advancements, which have reduced production times and material costs.

1.2 Current generation in solar cells

In this section, the basic principle of solar cell operation is described and the notion of passivation is introduced, as a means of increasing the energy conversion efficiency. The explanations and figures are based on those of Honsberg and Bowden[6].

Figure 1.2: Structure of an early Si solar cell, developed in 1954[6].

Figure 1.3: Worldwide power generation capacity additions (GW). A decline in investments for fossil fuels is projected in the coming years, while clean energy is expected to expand at an increasing rate. Solar technology will provide the largest contribution to clean energy expansion by 2030[8].
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Nearly all photovoltaic devices use semiconductor materials, such as silicon, to convert solar radiation into usable energy. Their design is built around a p-n junction. Incident sunlight generates an excess of carriers in the semiconductor bulk. The electrons and holes are spatially separated by the electric field present at the junction and produce a voltage across the device, called the open-circuit voltage ($V_{oc}$). This is the maximum voltage which can be extracted from the device. By connecting the n and p regions of the solar cell to a closed circuit, a current can be extracted. The maximum extractable current is called the short-circuit current ($I_{sc}$), and it occurs when the applied voltage is zero. $V_{oc}$ and $I_{sc}$ are used to describe the maximum output capabilities of a solar cell and they are represented in fig. 1.4. Since a solar cell generates no power at these operating points, the maximum power is achieved at a different point on the curve, called the maximum power point (MPP). The ratio between the maximum power and the product of $I_{sc}$ and $V_{oc}$ is a value called the fill factor (FF). It can be used to determine the maximum power when the values of $I_{sc}$ and $V_{oc}$ are known.

![IV curve of a solar cell, showing $I_{sc}$ and $V_{oc}$. The fill factor is calculated as the ratio between the power generated at the MPP and the product of $I_{sc}$ and $V_{oc}$. Graph re-plotted after Honsberg and Bowden[6]](image)

By applying a load to the solar cell, the carriers generate a current in the external circuit. However, minority carriers must cross the p-n junction, in order to contribute to the current. Light-generated carriers only survive in the semiconductor for a period of time equal to the minority carrier lifetime, before recombining. This means that, depending on its distance from the junction compared to its diffusion length, each carrier will have a certain collection probability. The variation of this probability across the section of a solar cell is shown in fig. 1.5. Carriers generated in the space charge area of the junction all contribute to the photocurrent, whereas outside of this area the probability starts to decrease. If carriers are more than one diffusion length away from the junction, they are not likely to reach it before recombining. Therefore, the collection probability for this situation is low. Moreover, surfaces typically have a higher recombination rate than the semiconductor bulk. As a result, carriers generated close to the...
surface are also collected by the junction with a much lower probability, due to their reduced lifetime. To correct this, a surface can be passivated, in order to lower the recombination rate. The impact of diffusion length and surface passivation are also illustrated in fig. 1.5.

![Figure 1.5: Carrier collection probability across the section of a solar cell. Surface passivation and the carrier diffusion length play a significant role in photocurrent generation. Graph recreated after Honsberg and Bowden[6].](image)

Due to the absorption of light in the silicon wafer, larger numbers of carriers are generated close to the front surface of the solar cell than anywhere else in the device. Photons of higher energies are absorbed over shorter distances than those of lower energies, such that the contribution of the higher frequency part of the spectrum is confined close to the front surface of the cell. If the recombination rate in this region is too high, part of the solar spectrum does not contribute to energy conversion within the device. Therefore, it is important to ensure low recombination at the surface, via passivation, to increase the energy conversion efficiency of a photovoltaic device. It is important to note that, by reducing carrier losses, surface passivation also affects the distribution of the electric field generated by the p-n junction. This leads to higher $V_{oc}$ values, which can also influence the maximum output of the solar cell.

A good way to describe recombination losses is via the recombination currents at the front, rear and in the bulk of a cell ($J_0_{front}$, $J_0_{rear}$, $J_0_{bulk}$). In the International Technology Roadmap for Photovoltaic (ITRPV) the predicted trend for surface recombination currents shows an expected 50% reduction by 2025, as shown in fig. 1.6[10]. In order for this to occur, research into surface passivation must produce continually better results.

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Figure 1.6: Projected trend for recombination currents for p-type and n-type cell concepts. Front and rear side recombination current should be reduced by 50% by 2025. Graph recreated after ITRPV[10].

1.3 Passivating the Si surface

As described in the previous section, the efficient collection of light-generated carriers provides increased solar cell energy conversion efficiency. In order to ensure high collection efficiency, the carriers must avoid recombination for sufficiently long times. There are three main recombination mechanisms, which are of varying importance, depending on the properties of the material used. They are depicted in fig. 1.7.

Radiative recombination occurs when an electron and hole recombine by emitting a photon of a frequency corresponding to the bandgap energy. This effect is prevalent in semiconductors which have a direct bandgap. In this case the energy of the electron=hole pair is at a minimum when the carriers are at the same \( k \) value within the crystal lattice and they can freely recombine once they reach this state. Silicon is an indirect-bandgap semiconductor, such that the conduction band minimum and the valence band maximum are located at different \( k \) values. In this case, the recombination of an electron-hole pair can only take place with the assistance of a phonon, which can provide the required crystal momentum. This means that recombination in silicon is

Figure 1.7: The main recombination mechanisms in semiconductors: (a) radiative, (b) Auger, and (c) SRH recombination.
A three-particle effect, with a significantly reduced probability. Therefore, silicon solar cells do not suffer significant losses due to radiative recombination.

The second recombination mechanism is due to the Auger effect. In this case, an electron and hole recombine, with the excess energy being transferred to a separate carrier (either an electron or a hole), which is sent into an excited state as a result. This is again a three-particle process, which means that it has a low occurrence probability. However, the probability of Auger recombination increases at high carrier concentrations. Therefore, if the number of carriers is sufficiently high, such as in high injection, or for highly doped semiconductors, this effect can become important, leading to significant carrier losses and reduced cell efficiency. Although high injection is avoidable, depending on the intensity of the incident radiation, for highly-doped semiconductors, the high number of extrinsic carriers means that the effect cannot be circumvented. In this case, it is necessary to provide good passivation by reducing the effectiveness of the last, and most important, carrier loss mechanism, Shockley-Read-Hall (SRH) recombination.

The SRH mechanism consists of the recombination of an electron-hole pair via a transition to an empty energy state within the bandgap energy range. These bandgap states can be introduced by any deviations in the crystal lattice, such as the presence of impurities or defects in the crystal bulk. The most important source of bandgap states is the large discontinuity in the crystal represented by its surface. This is due to the tetrahedral nature of Si atoms: within the crystal, each atom is covalently bound with its four neighbors, leaving no unsaturated bonds. At the surface, however, there are missing atoms which leave dangling bonds. These bonds play the role of recombination centers for the light-generated carriers. At high densities, the surface state energies shift due to the influence of all neighboring dangling bonds, forming a continuum of recombination centers.

The three mechanisms are characterized by specific lifetimes. We can define an effective carrier lifetime, by combining them, along with a separate term related to recombination at the surface:\[^{11}\]

\[
\frac{1}{\tau_{\text{eff}}} = \frac{1}{\tau_{\text{rad}}} + \frac{1}{\tau_{\text{Auger}}} + \frac{1}{\tau_{\text{SRH}}} + \frac{1}{\tau_{\text{surf}}} \quad (1.1)
\]

The effective lifetime of a wafer, \(\tau_{\text{eff}}\), can be determined from photoconductance measurements and can be used as a measure of passivation quality. In eq. (1.1), the first three terms on the right side are bulk recombination terms. The two final terms are introduced by trap-assisted recombination, and throughout this thesis we will be focusing on increasing the surface recombination lifetime, \(\tau_{\text{surf}}\).

By grouping the bulk terms together, and considering a symmetrically passivated wafer, with sufficiently low surface recombination velocity, we can write:

\[
\frac{1}{\tau_{\text{eff}}} = \frac{1}{\tau_{\text{bulk}}} + \frac{1}{\tau_{\text{surf}}} = \frac{1}{\tau_{\text{bulk}}} + \frac{2S_{\text{eff}}}{W} \quad (1.2)
\]

where \(S_{\text{eff}}\) is the effective surface recombination velocity and \(W\) is the wafer thickness[11]. If the bulk lifetime is sufficiently high, the bulk term can be neglected and an upper limit for \(S_{\text{eff}}\) can be deduced. This provides a conservative measure for surface passivation, a maximum expectable value of the surface recombination velocity, independent of the bulk properties. The calculated value is a good approximation for the effective surface recombination when bulk lifetimes are much larger than 1 ms[11].

\[
S_{\text{eff}} < \frac{W}{2\tau_{\text{eff}}} \quad (1.3)
\]

To reduce recombination and effectively passivate a Si surface, there are two major possibilities. First, the elimination of the surface dangling bonds reduces the number of recombination
centers. This can be achieved by growing an oxide layer at the surface. Each O atom, being bivalent, can bond covalently with a Si atom, satisfying the dangling bonds, passivating the surface.

A popular method of metal oxide growth is atomic layer deposition (ALD). This technique consists of using the surface reactions of a metal precursor and co-reactant to grow different materials one sub-monomolayer at a time. ALD offers very good thickness control and the possibility of high-throughput processing, via recent advancements in spatial ALD technology\cite{12, 13, 14}. Layer growth by ALD does not always produce a perfect interface with the silicon wafer. This can be due to a number of factors, such as a lack of reactive sites or larger molecules obstructing the bonding of others to the surface, an effect known as steric hindrance. To improve the interface and provide better passivation, the wafers can be subjected to a post-deposition hydrogenation step. This can be achieved via a forming gas (H$_2$ + N$_2$) anneal, during which the highly mobile hydrogen atoms can passivate the remaining Si dangling bonds at the Si/oxide interface. Alternatively, if sufficient hydrogen is present in the oxide layer, a simple anneal in N$_2$ atmosphere can lead to hydrogenation of the surface\cite{40}. In order to evaluate chemical passivation quality, we can use electrical measurements to determine the density of interface traps, $D_{it}$, i.e. the number of states present in the bandgap. A measurement scheme for this will be shown in a later chapter.

![Figure 1.8: Schematic of chemical passivation: (a) unpassivated Si surface, showing dangling bonds which generate high $D_{it}$ (approximately 10$^{14}$ cm$^{-2}$eV$^{-1}$)\cite{15}; (b) Passivated and hydrogenated surface, showing reduced $D_{it}$ (approximately 10$^{12}$ and 10$^{10}$ cm$^{-2}$eV$^{-1}$, respectively\cite{15}).](image)

The density of carriers at the surface also affects recombination. Therefore, a second type of passivation is achieved when a significant reduction in the density of one type of carrier is induced at the surface\cite{11}. This is called field effect passivation. One possibility of providing field effect passivation is via the fixed charges present in the oxide layer. Additional types of charges are also present in the oxide. They do not aid surface passivation, but they have visible effects, which will be discussed later. The first of these are mobile charges. They are usually produced by alkaline ions and can move under electric fields. Second are interface charges, which have variable polarity, depending on the surface band bending and Fermi level position\cite{16}. The fixed charges induce an electric field at the semiconductor surface, which attracts or repels carriers.

In fig. 1.9, the effective surface recombination is plotted as a function of the charge induced in the silicon substrate by the oxide charge\cite{16}. 

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Figure 1.9: Effective surface recombination as a function of oxide charge for a p-type Si substrate, (a) in depletion/inversion (i.e. for positive oxide fixed charge)[16] and (b) in accumulation (i.e. for negative oxide fixed charge)[17]. The space charge created in the silicon substrate ($Q_{Si}$) in figure (a) is negative. The absolute value ($-Q_{Si}$) is used on the horizontal axis, for ease of comparison with figure (b). The case for n-type Si is similar to the one presented here, but the charge polarities are reversed.

In the case represented in fig. 1.9, the p-type silicon substrate is driven into depletion by the positive fixed charge of the oxide layer, equivalent to a negative substrate charge. At sufficiently high charge densities, an inversion layer can be created at the surface. This consists of an accumulation of minority carriers, while majority carriers are driven away from the surface, due to the bending of the energy bands. This can lead to lower recombination, for sufficiently high inversion charge values. We see a dependence of the recombination velocity on the carrier injection level, such that, especially at low values, $S_{eff}$ can be drastically increased around the charge value corresponding to the onset of inversion. This is due to the fact that, around the inversion threshold, there are high concentrations of both electrons and holes at the surface, enhancing recombination[16]. This injection level dependence is undesirable for solar cell operation, since variations in $S_{eff}$ between open circuit conditions and the maximum power point (MPP) can cause a reduction in the cell’s fill factor (FF)[18]. A negative fixed charge density induces a positive space charge region in the silicon, resulting in accumulation. In this case, we see that surface recombination values decrease monotonously with increasing charge content and the injection level dependency does not occur.

By analyzing the cases of accumulation, depletion and inversion, we can conclude that, while long lifetimes are achievable when the oxide fixed charge causes strong inversion at the surface, the best case scenario is that of accumulation. Moreover, inversion can cause parasitic shunting[16]. This induces an additional injection level dependence of the recombination velocity, which can cause a reduction of the fill factor and of the short-circuit current at low illumination intensity. Consequently, we can expect to achieve good field effect passivation in the following cases:

- An n or n$^+$ Si surface passivated by an oxide containing positive charges
- A p or p$^+$ Si surface passivated by an oxide containing negative charges

A schematic representation of a passivated n-type surface is given in fig. 1.10. It illustrates the above statement, by showing the effect of fixed charge polarity on the silicon band structure.
Figure 1.10: Schematic of field effect passivation for an n-type silicon surface. $Q_f$ is the oxide fixed charge density. Limiting the number of minority carriers reduces the maximum possible recombination rate.

The dopant concentration in the Si substrate also plays an important role in determining the achievable lifetimes for a passivated wafer. In this regard, passivation of highly-doped wafers is more difficult, due to increased recombination. First of all, high doping of the silicon wafer leads to the creation of more defects in the crystal lattice, reducing bulk lifetimes, due to SRH recombination. Additionally, high carrier concentrations lead to increased Auger recombination, which also lowers carrier lifetimes. In order to provide good field effect passivation, higher $Q_f$ is required, to successfully remove minority carriers from the surface. Moreover, the importance of achieving low $D_{it}$ is increased, since higher carrier concentrations increase the probability of recombination into surface bandgap states.

Evaluation via capacitance-voltage (C-V) measurements of a metal-oxide-semiconductor (MOS) structure can provide information regarding the polarity and magnitude of the oxide’s fixed charge content ($Q_f$). This way, we obtain $Q_f$ as a direct measure of field effect passivation. Additionally, $D_{it}$ can be extracted from the same electrical measurements, providing insight into the achievable chemical passivation. The methods for determining $Q_f$ and $D_{it}$ will be described in more detail in the following chapters. The overall passivation quality will be investigated via effective lifetime measurements and calculation of surface recombination velocities.

1.4 HfO$_2$ for Si passivation

Although surface passivation is an important part of solar cell functionality, the concept is present in a much wider area of applications. Most notably, passivation is required in electronic devices, such as metal-oxide-semiconductor field effect transistors (MOSFETs), like the one shown in fig. 1.11. In this case, the oxide plays the role of dielectric in the MOS capacitor used to induce a conductive channel at the gate terminal. To give good performance, the oxide must be an effective insulator, in order to prevent charge leakage to the metal contact.

Due to constraints imposed by miniaturization of electronic devices, researchers have started looking to novel materials, which can replace SiO$_2$ as gate dielectric. Hafnium oxide has been proposed, among others, in a study by Wilk et al [19], stating that it had shown encouraging electrical properties. Optimization of HfO$_2$ layers has resulted in significant improvements such that, in 2007, Intel Corporation introduced a Hf-based gate oxide with a metal gate[20] into production of its 45nm technology chips. Among the properties which make it a successful gate oxide is first of all its high $\kappa$-value, which is typically between 18 and 25. Compared to 3.8 for SiO$_2$, it can provide a sizeable improvement in achievable capacitance at the same oxide thickness. The wide bandgap of HfO$_2$[21] (> 5.5) make it an excellent insulator. The low $D_{it}$ value and
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Figure 1.11: Design schematic of a MOSFET. The gate oxide layer prevents charge leakage, while ensuring transistor functionality. Low values for $Q_f$ and $D_{it}$ are desired.

the possibility of achieving low $Q_f$ are also of crucial importance for gate oxide functionality.

Some of the same properties suggest that hafnium oxide could be used as passivation layer in photovoltaic devices. First of all, the wide bandgap prevents any absorption within the UV part of the solar spectrum. Also the refractive index value is approximately 2, similar to that of silicon nitride ($\text{SiN}_x$), which is a standard material used as anti-reflective capping layer. This ensures reduced losses due to reflection at the oxide-nitride interface. Low $D_{it}$ is important for passivation, as discussed in the previous section. Research has shown that a wide range of fixed charge densities are achievable, such as in the precursor comparison realized by Sreenivasan et al[22]. This indicates that the material can theoretically be used to passivate Si surfaces of various doping conditions. One last, very attractive property of HfO$_2$ is the fact that deposition is theoretically possible by a spatial ALD process. This technology has already been introduced for another well-studied high-$\kappa$ dielectric, Al$_2$O$_3$[12]. If integration of HfO$_2$ is possible, it can lead to greatly reduced processing times, both in research and at an industrial level, which are required for market penetration to be possible.

Previous research on HfO$_2$ passivation of silicon solar cells has produced promising results. A relevant study is that of Lin et al[23]. In their experiments, HfO$_2$ was deposited by thermal ALD at 300 °C and annealed at 440 °C. Float zone (FZ) silicon was used as a substrate. Results have shown that HfO$_2$ can provide good chemical and field-effect passivation for moderately doped n and p-type Si wafers, with surface recombination values of 24 cm/s and 55 cm/s respectively. Previously, in a 2012 master’s thesis, Morato had used p-type Czochralski (Cz) Si wafers, passivated with HfO$_2$ by a thermal ALD process at 200 °C[24]. Post-deposition forming gas anneals (FGA) at 300 °C and 500 °C were done. His studies revealed that annealing improves chemical passivation by reducing $D_{it}$. The formation of fixed charge is also annealing-dependent, as $Q_f$ values switched from negative to positive polarity after post deposition anneal (PDA). In 2014, symmetrical passivation capabilities (i.e. passivation of n and p-type surfaces at the same time) were demonstrated for stacks of HfO$_2$ and Al$_2$O$_3$, by Simon et al[25]. In the study, FZ silicon wafers were passivated by Al$_2$O$_3$ deposited over a very thin layer of HfO$_2$, grown during the first few ALD cycles. Depending on the thickness of the HfO$_2$ layer, the fixed charge content can be changed to very low values, allowing for good passivation, irrespective of majority carrier type. As a result, on n-type surfaces, the recombination velocity at low injection levels was reduced from 2 cm/s when passivation was done with Al$_2$O$_3$ alone, to about 0.8 cm/s with a HfO$_2$ interlayer. For p-type silicon, the surface recombination velocity was unaffected by the addition of the HfO$_2$ layer, remaining at very good value of 0.8 cm/s.
1.5 Thesis objectives and motivation

In light of the promising results produced by HfO$_2$ as a passivation layer for both electronic and PV devices, further research into this field is well justified. Currently, Al$_2$O$_3$ can provide excellent passivation for p and n-type solar cells at moderate doping levels[14]. However, in high efficiency cells, highly doped emitters and front surface fields (FSF) are utilized[26]. Consequently, p$^+$ and n$^+$ surfaces also require high performance passivation materials. In this regard, the negative fixed charge present in Al$_2$O$_3$ layers should provide good field effect passivation for low to highly-doped p-type wafers, and potentially on low-doped n-type wafers, due to inversion layer formation. However, on highly doped n-type surfaces, inversion is harder to achieve, due to the larger concentration of majority carriers than in the lower-doped case. Therefore, films with positive fixed charge are required, in order to obtain high effective lifetimes. This becomes apparent, when considering the behavior presented in fig. 1.9. Consequently, the negative charge of Al$_2$O$_3$ would not be beneficial for n$^+$ surface passivation.

HfO$_2$ could provide an alternative for n-type and n$^+$ surface passivation, since it has been shown to exhibit positive fixed charge. Moreover, the wide range of values reported for this parameter make it a versatile material, capable (in theory) of passivating a wider selection of doped surfaces. We may also envision a scenario where HfO$_2$ can be used to provide symmetric passivation, if sufficiently low fixed charge can be achieved, along with a low density of interface traps.

Figure 1.12: Design of n-PERT, IBC, PERC, and Al-BSF cells. Red highlights show areas where HfO$_2$ passivation might be applied.

Potential applications for HfO$_2$ can be found in current high efficiency n-type solar cells, such as the ones illustrated in fig. 1.12. For example, the n-PERT design utilizes an n$^+$, phosphorous-diffused FSF[27]. An IBC-type cell, utilizes a similar n$^+$ front surface, while also containing both n$^+$ and p$^+$ regions on the rear side, where the contacts are located[28]. A third type of solar

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cell, which utilizes an $n^+$ front side emitter is the passivated emitter rear cell (PERC) design, created from p-type silicon wafers[29]. Lastly, p-type large-area rear passivated cells, with an aluminium back surface field (Al-BSF) also possess an $n^+$-doped front surface[30]. In order for HfO$_2$ to replace current passivation solutions in the above solar cell designs, the achievable output should be increased by comparison. Alternatively, if similar performance is obtained, a reduction in production prices or processing time would also justify a change in the approach to surface passivation.

The ITRPV predicts that in the near future, n-PERT and IBC cells will encounter a slight increase in market share, as shown in Fig. 1.13. However, passivated emitter rear cell (PERC) technology will quickly become the dominant market presence, meaning that advances in $n^+$ surface passivation will become more important as researchers look to increase the overall efficiency of this design. Moreover, Al-BSF cells currently dominate the photovoltaic device market, due to their simplicity and low manufacturing costs. This serves to emphasize the importance of high quality $n^+$ surface passivation, in both present and future solar cell designs.

![Figure 1.13: Projected market share of different solar cell technologies. PERT and IBC will see a gradual increase, whereas PERC technology will quickly become the dominant market presence[10].](image)

The experiments carried out in this thesis have served to investigate utility of HfO$_2$ as a passivating oxide for n-type and $n^+$ surfaces. Electrical characterization of deposited layers was used to evaluate the quality of chemical and field effect passivation achievable. Lifetime measurements have revealed the overall passivation quality, providing a term for comparison with standard materials. Different precursors and deposition conditions were used for the ALD oxide layers, which were deposited on Cz Si wafers, with various resistivities, thicknesses and surface types. Moreover, physical characterization via transmission electron microscopy (TEM) and chemical analysis via energy-dispersive X-ray spectroscopy (EDS) and elastic recoil detection (ERD) were used to link passivation quality to the observable film characteristics. By establishing the applicability of HfO$_2$ for solar cell passivation, this thesis represents a very early step towards industrial integration. Deposition via a high-throughput passivation solution, such as spatial ALD may ensure fast, cheap production of high efficiency solar cells.
1.6 Thesis outline

In this section, the structure of this thesis is briefly described. The first chapter served as an introduction to the field of photovoltaics, from both a technological and a physical standpoint. The problem of carrier recombination at the silicon surface was introduced and passivation methods via oxide deposition were described. HfO$_2$ was proposed as a candidate material for n-type and n$^+$ surface passivation and its importance in future solar cell designs was stated.

The second chapter describes the deposition method used to grow the passivating HfO$_2$ layers, specifically atomic layer deposition (ALD). The ALD reaction cycle is described, and a comparison of reactor configurations and deposition schemes is given. Next, experimental details are given, including a description of the metal precursors used for HfO$_2$ deposition. A description of the sample preparation process is also given.

In the third chapter, a detailed characterization of HfO$_2$ layers is shown, in order to establish its effectiveness as a passivating material. First its performance is compared to other standard oxides from an optical standpoint. To this end, a solar cell structure was simulated and a ray tracing Monte Carlo algorithm was used to calculate the maximum achievable photocurrent. Next, the physical and chemical structure of the ALD HfO$_2$ layers is described, using results obtained by transmission electron microscopy (TEM) analysis. A detailed description of the electrical properties of the oxide follows, after a presentation of the characterization methods which were used.

Chapter four covers the direct analysis of HfO$_2$ passivation quality, via wafer lifetime measurements. Surface recombination velocity is reported as a measure for surface passivation, independent of the bulk properties of the silicon wafers. Comparisons are made between HfO$_2$ and standard materials used for solar cell passivation, in order to ascertain its applicability.

The final chapter will present the conclusions of the research which was carried out during this thesis. The potential of HfO$_2$ for passivation of silicon solar cells is evaluated and suggestions are given for further improvement.
Chapter 2

Atomic layer deposition of HfO$_2$ for solar cells

2.1 Oxide growth by atomic layer deposition

In this section, deposition of oxide layers by ALD is described in detail. Two types of ALD processes were used in the experiments described in the following chapters: thermal ALD and plasma enhanced ALD. For the first category, both a temporal and a spatial reactor were available, depending on the deposited material. These ALD techniques are all compared here.

2.1.1 The ALD process

Atomic layer deposition is a self-limiting process allowing thin film growth with very precise thickness control. It provides excellent layer uniformity, achieved via a multi-step process, which is repeated in order to deposit metal oxides at a rate of up to one monolayer per cycle.

The technology for ALD depositions was developed and patented in the late 1970s in Finland, by Suntola and Antson[31]. The ALD cycle is also described in many recent works, such as the PhD theses of Dingemans[11], Niinistö[32], Vermang[14], or the MSc thesis of Morato[24]. In this section, the ALD process is briefly described, with an emphasis on thermal ALD, which uses the thermal energy of the reacting molecules to drive layer growth.

The ALD process takes place inside a reactor chamber. A cycle consists of alternating doses of a precursor and a co-reactant, or oxidizer, which participate in half-reactions, ultimately depositing the desired material. Each precursor and oxidizer dose must ensure optimal surface coverage, by careful selection of the deposition parameters. After exposure, a purge or pump step is used to remove any excess precursor molecules or reaction products. In fig. 2.1 we can see an illustration of an ALD cycle. The co-reactant is usually H$_2$O or O$_3$, but other molecules have also been used, such as O$_2$, N$_2$O and H$_2$O$_2$[32]. The process for each pulse step is self-limiting such that, beyond a certain point, the half-reaction can no longer take place. This occurs due to the limited number of favorable adsorption spots. The reactant can only bond to these spots, thereby driving ALD growth. After these spots are occupied, the precursor cannot react with its own surface reaction products, such that the film cannot grow further until the next step in the ALD cycle. Adsorption can also be inhibited by steric hindrance. This occurs when large size groups within the molecules which are already bound to the surface prevent the adsorption of remaining precursor ligands to an otherwise favorable location. As a result, saturation of surface...
reactions usually occurs before the entire surface has reacted with the precursor. Consequently, one ALD cycle usually cannot provide full coverage of the surface.

Figure 2.1: Schematic of one ALD cycle for a metal halide, such as HfCl$_4$, a widely used HfO$_2$ precursor[33].

A practical example of a relatively simple thermal ALD cycle is described in the following relations. They show the surface reactions that lead to HfO$_2$ growth from HfCl$_4$ and H$_2$O. Bonding of the HfCl$_4$ molecule to the surface occurs according to the following reaction:

\[(\text{surf}−\text{OH})_x + \text{HfCl}_4(\text{g}) \rightarrow (\text{surf}−\text{O})_x−\text{HfCl}_{4−x} + x\text{HCl}(\text{g})\]  

(2.1)

In the above equation, x is lower than 4 and represents the number of OH surface terminations which react with the precursor. The reaction results in the separation of the OH group, with the O atom remaining bound to the Hf atom. In the subsequent step, the water molecules react with the bonded precursor, breaking the bond between hafnium and chlorine, forming volatile HCl molecules, and OH groups bound to the surface Hf atom. The OH groups will react with the precursor at the start of the next cycle:

\[\text{surf}−\text{Hf}−\text{Cl} + \text{H}_2\text{O}(\text{g}) \rightarrow −\text{Hf}−\text{OH} + \text{HCl}(\text{g})\]  

(2.2)

The overall reaction for the deposition of HfO$_2$ is:

\[\text{HfCl}_4(\text{g}) + 2\text{H}_2\text{O}(\text{g}) \rightarrow \text{HfO}_2 + 4\text{HCl}(\text{g})\]  

(2.3)

ALD is suitable for the deposition of a large number of oxides, including HfO$_2$, Al$_2$O$_3$, SiO$_2$, and ZnO, but also nitrides, and noble metals such as platinum[11].

The most basic form of ALD uses the thermal energy of the reactants to drive the oxide growth. A metal precursor and an oxidizer are used as reactants, which are inserted into the
ALD reactor in the vapor phase, participating in surface reactions. In the following paragraphs, the influence of temperature on ALD growth is described in more detail.

The growth rate is influenced by the velocity of the reactions which take place at the surface and the time required to bring the reactants to the surface. These parameters depend on the pressure and temperature inside the reactor\cite{24}. In fig. 2.2, we can see the different behaviors that can occur during deposition\cite{32}:

![Figure 2.2: Dependence of ALD growth rate on the length of the precursor pulse (a) and the chamber temperature (b); a self-limiting process ensures controllable oxide thickness.](image)

When surface saturation is achieved, the growth per cycle is independent of pulse length. This occurs if the precursor dose and/or the exposure time are sufficiently high, and leads to the self-limiting growth case depicted in fig. 2.2a. If, in this scenario, the growth rate remains constant over a wide range of temperatures, then we can define an "ALD window". Operating in the ALD window enables the reproducible growth of thin films, due to the reduced influence of temperature fluctuations (fig. 2.2b). If the temperature lies outside the optimal range for controlled ALD growth, the reactions are inhibited. At too low temperatures, there is insufficient thermal energy to drive the surface reactions. In some cases, condensation of the precursor on the surface may occur, which can affect the stoichiometry of the deposited layers. On the other hand, if the temperature is too high, the thermal energy may lead to greater rates of desorption than adsorption. As a result, any further increase in temperature would lead to lower growth rates. It is also possible for the high thermal energy to lead to decomposition of the precursor in the vapor phase. This results in increased growth rates, due to additional film growth via pyrolytic chemical vapor deposition (CVD)\cite{34}.

Surface conditioning can influence film growth, by affecting the way the reactants bond to the surface in initial phases of the ALD process. The surface terminations can cause different adsorptive behavior of the precursor molecules, favoring or inhibiting film growth within the first few cycles. Two surface types can be distinguished in relation to their interaction with water molecules: hydrophobic or hydrophilic. The effect of each type on initial layer growth is illustrated in fig. 2.3. Hydrophobic and hydrophilic surface conditions are achieved through different wafer processing methods, prior to atomic layer deposition.

A hydrophobic surface can be obtained during wafer cleaning, via a final step meant to strip away any oxide, which can be either chemically grown, or formed due to exposure of the silicon to air. The oxide is stripped by shortly immersing the wafers in a diluted HF solution (1% HF in H\(_2\)O). This approximates a H-terminated surface, which repels water molecules. This was shown to hinder the ALD process in the first few cycles of HfO\(_2\) deposition, favoring island growth (Volmer-Weber) of oxide layers, which results in a nucleation and growth delay\cite{35}. After

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the initial deposition stage, a constant growth rate is achieved, due to the saturation of surface reactions by steric hindrance or full coverage of the available reaction sites.

To obtain a hydrophilic surface, the silicon wafers must be processed in such a way that they are coated with a very thin SiO$_2$ layer. This happens naturally during exposure of a bare silicon surface to air. However, such an oxide grows in an uncontrolled fashion and is of very low quality. To properly prepare a hydrophilic surface, one possibility is to subject the wafers to a bath in ozonated water, at the end of the pre-deposition cleaning process. This creates a chemical SiO$_2$ layer, with a thickness of approximately 1 nm on the wafer surface. The SiO$_2$ creates OH terminations at the surface, which favor oxide nucleation and growth. It has been shown that, for sufficiently thick chemical oxides (approximately 0.8 nm), the OH coverage of the surface is reached and optimal HfO$_2$ is achieved in the initial stages of ALD[35].

Pre-deposition surface conditioning for HfO$_2$ growth has been investigated in works such as those of Green et al.[36] and Nyns et al.[35]. In the first example, Rutherford back scattering (RBS) experiments were conducted in order to measure the Hf coverage as a function of the number of ALD cycles for a hydrophobic surface (HF last) and surfaces covered by chemical (SiO$_2$) or thermal (SiO$_2$ or Si-O-N) oxides. The results, seen in fig. 2.4 show a long transitional period for a H-terminated surface, whereas the chemical or thermal oxide coverage ensures a quick growth per cycle stabilization. Nyns et al. compared thermal and chemical oxide-covered surfaces and found that, while the deposition process is independent of oxide type, the electrical characteristics may vary. This is most likely due to the different physical properties of each oxide.

Figure 2.3: Comparison between differently-treated surfaces with regard to the first few cycles of ALD oxide growth: (a) hydrophobic surface, favoring nucleation and island formation; (b) hydrophilic surface, allowing epitaxial growth.

Pre-deposition surface conditioning for HfO$_2$ growth has been investigated in works such as those of Green et al.[36] and Nyns et al.[35]. In the first example, Rutherford back scattering (RBS) experiments were conducted in order to measure the Hf coverage as a function of the number of ALD cycles for a hydrophobic surface (HF last) and surfaces covered by chemical (SiO$_2$) or thermal (SiO$_2$ or Si-O-N) oxides. The results, seen in fig. 2.4 show a long transitional period for a H-terminated surface, whereas the chemical or thermal oxide coverage ensures a quick growth per cycle stabilization. Nyns et al. compared thermal and chemical oxide-covered surfaces and found that, while the deposition process is independent of oxide type, the electrical characteristics may vary. This is most likely due to the different physical properties of each oxide.
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Figure 2.4: Comparison of different surface treatments. Hf content was measured via RBS as a function of the number of deposition cycles. This provides a clear picture of nucleation and growth behavior. Graph re-plotted after Green et al[36].

2.1.2 Plasma-enhanced ALD

A simple schematic of an ALD reactor is shown in Fig. 2.5. This design permits one-sided deposition of oxide for one wafer at a time. Other designs are available, with batch processing or two-sided deposition capabilities, or spatial separation of ALD steps. These modifications provide greater functionality and higher throughput, if necessary[13].

Figure 2.5: A shower head design for an ALD reactor. After Delft et al[13].

A different type of reactor design can be used to provide high quality layer growth, by enhancing the reactivity of the oxidizing molecules. This is achieved by generating a plasma from the reactant gas during the second ALD half-cycle. The increased reactivity provides greater
freedom of selection for processing conditions, meaning a wider range of material properties are attainable, while potentially increasing the ALD window.

This type of deposition provides several advantages, which make it an attractive option for numerous applications, including deposition of HfO$_2$ passivation layers. These advantages are given below, as reviewed by Proft et al$[37]$:

- For some materials and applications, better material properties have been reported, such as film density, impurity content and improved electronic properties. Usually, these improvements arise due to the enhanced reactivity delivered by the plasma.

- Deposition is possible at lower temperatures. This is also a result of the improved reactivity, since less thermal energy is required to drive the reactions. This provides the possibility of using ALD on less thermally stable substrate materials, such as organics, with possible applications in, for instance, flexible solar cell technology. Lower temperatures also prevent the decomposition of less thermally stable precursors.

- It enables deposition of layers using a wider range of precursors and materials, compared to thermal ALD.

- Control of film stoichiometry and composition is improved, due to the extra process parameters introduced by the plasma, such as the operating pressure, the plasma power, exposure time, the biasing voltage and even by introducing additional species into the plasma.

- Higher growth rates are achievable due to several reasons. These include, (but not always applicable) a higher density of reactive surface states, due to the high plasma reactivity, a shorter nucleation delay compared to thermal ALD processes, and shorter plasma pulse and purge times, leading to shorter overall process times.

- More in-situ processing options are available, due to the introduction of a plasma source. As such, wafers can be subjected to pre-deposition treatments, such as oxidation, nitridation or cleaning, but also post-deposition processing and reactor maintenance and cleaning.

![Figure 2.6: Plasma-assisted ALD reactor configurations: (a) direct plasma; (b) remote plasma; (c) radical enhanced. After Proft et al$[37]$.](image)

Depending on the reactor configuration, there are three types of plasma ALD tools$[38, 37]$. First, there is direct plasma ALD, where the plasma is generated directly above the wafer, which is positioned at one of the plasma-generating electrodes. Second is remote plasma ALD, in which...
the plasma is generated away from the substrate, but it is still present above the deposition surface. This offers an advantage when compared to direct plasma ALD, because the substrate temperature and the properties of the plasma can be varied separately from one another. The third possibility is that the plasma is generated separately from the ALD chamber, such that it is not present at the wafer surface. The plasma must travel through the reactor tubing and, due to surface collisions, radicals are created which reach the wafer surface, where they take on the role of reactant. Consequently, this deposition scheme is also referred to as radical enhanced ALD. The three schemes are shown in fig. 2.6.

2.1.3 Spatial ALD

Recent advances in reactor design and precursor chemistry have led to the creation of tools capable of spatial ALD for high efficiency solar cells, such as that of SoLayTec [12, 14]. This type of reactor is capable of ultra-fast depositions, via the design shown in fig. 2.7[13]. The working principle consists of quickly passing the wafer underneath a set of inlets for each reactant, which are separated spatially by a curtain flow of nitrogen. This allows simultaneous, continuous dosing of precursors, at different positions in the reactor. The temporal separation of reactions in a certain location on the wafer is determined by the speed with which the wafer passes through the reactor. Thus, with each pass, a full ALD cycle is completed. Temporal limitations may arise from the reaction speed, which may restrict the speed at which the wafer is allowed to move through the reactor, in order for optimal deposition to take place. However, reaction time scales on the order of milliseconds are achievable, ensuring very high deposition rates[13], despite such restrictions. The precursor flow can also influence reaction speed, and this must be optimized in accordance with the wafer speed.

The SoLayTec spatial ALD reactor design has been used successfully for Al₂O₃ depositions, due to the material’s importance in passivating p-type surfaces. If HfO₂ can provide high quality passivation of n-type surfaces, one could envision a spatial ALD application in which it could be used for high-throughput solar cell production. One possibility would be for simultaneous...

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deposition on both surfaces of an n-PERT cell, with Al₂O₃ on the backside and HfO₂ at the front. This would greatly reduce processing times, as current solutions for n-PERT front side passivation materials, such as SiNₓ-capped SiO₂, require lengthy deposition processes. By replacing SiO₂ with HfO₂, a long thermal oxidation or PECVD step would be eliminated. SiNₓ capping of the front side of the cell would still be required, due to the anti-reflective properties of the material, which cannot be replicated with only a thin HfO₂ layer. Thicker HfO₂ layers may also have good anti-reflective properties on their own, but investigations into this type of application are outside the scope of this thesis. Nevertheless, a reduction in processing times can be achieved by implementation of spatial ALD for solar cell passivation.

There are, however, a few restrictions with spatial ALD. First of all, the reactor is not kept under a vacuum. This means that preventing the release of harmful chemicals into the work environment may lead to increased cost, from a design safety standpoint. Otherwise, special attention can be given to choosing precursors which generate more easily-disposable reaction products. Also, the reaction products must not damage or clog the reactor, to ensure tool functionality for sufficiently long periods. An example of an unsuitable precursor is the widely used HFCl₄. The surface reactions produce molecules of HCl. This is a highly corrosive acid, which can lead to tool failure, by damaging the interior walls of the reactor. This also increases the risk towards the safety of the operators. Larger, more complex organic precursors may provide an alternative, but passivation for solar cell applications must first be demonstrated, in order to ensure a worthwhile investment.

2.2 Sample preparation

The experiments carried out in this thesis required the creation of two types of samples: some for lifetime measurements and others for electrical characterization of the HfO₂ layers. The exact silicon wafer specifications may vary with each conducted experiment, but we can distinguish between two main categories:

- First, 200 mm diameter, n-type, round Cz Si wafers, with an approximate thickness of 700 μm were used. These wafers are of a high quality, with a mirror-polished surface. They are used in CMOS applications. They have very high bulk lifetimes due to low defect densities. The doping levels for this type of wafer are generally low. All our samples had values between 2.9 · 10¹⁴ cm⁻³ (or a resistivity of 15.5 Ωcm) and 2.8 · 10¹⁵ cm⁻³ (1.7 Ωcm). All electrical measurement samples were created using this type of substrate. Some lifetime samples were also created using such substrates, with a more precisely determined resistivity value of 15.5 Ωcm. In this way, we managed to significantly reduce any bulk effects and determine the effective surface recombination velocity with increased accuracy.

- A second type of wafer was used to investigate the passivation quality achievable in solar cells. These wafers consist of n-type Cz silicon, in an 156 mm x 156 mm, semi-square shape, which was cut from a cylinder with a 200 mm diameter. The doping level is approximately 1.15 · 10¹⁵ cm⁻³, for a resistivity of 4 Ωcm. The wafer surface in this case resembles the front side of a standard n-PERT solar cell, with an upright pyramid texture. The general characteristics of both wafer types are shown in table 2.1

Prior to HfO₂ deposition via ALD, each wafer was prepared according to the type of investigation to which it would be subjected. For electrical characterization, samples were created from CMOS-type wafers, as illustrated in fig. 2.8. The preparation process consists of a single cleaning step before deposition. The clean serves both to remove contamination and to functionalize
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Table 2.1: General wafer characteristics

<table>
<thead>
<tr>
<th>Wafer type</th>
<th>1.CMOS</th>
<th>2.PV</th>
</tr>
</thead>
<tbody>
<tr>
<td>Doping type</td>
<td>n-type</td>
<td>n-type</td>
</tr>
<tr>
<td>Resistivity</td>
<td>1.7-15.5 Ωcm</td>
<td>4 Ωcm</td>
</tr>
<tr>
<td>Silicon</td>
<td>Cz</td>
<td>Cz</td>
</tr>
<tr>
<td>Approximate thickness</td>
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<td>180 µm</td>
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<td>Surface finishing</td>
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<td>Upright pyramids</td>
</tr>
<tr>
<td>Shape</td>
<td>Round</td>
<td>Semi-square</td>
</tr>
</tbody>
</table>

the surface, as will be explained later in this chapter. Electrical measurements require a metal-oxide-semiconductor (MOS) structure to be created on the sample, such that after a one-sided ALD growth step, the samples undergo a metal contact deposition step. This is achieved via thermal evaporation of 500nm of aluminium, using metallic masks. This creates round contacts of varying diameter (between 50 µm and 500 µm), upon which capacitance-voltage (C-V) and conductance-voltage (G-V) measurements can be carried out. An annealing step is used before contact deposition, to produce thermally treated samples, at various temperatures.

![Process flow for fabrication of MOS structures](image)

Figure 2.8: Process flow for fabrication of MOS structures for electrical measurements.

Depending on the type of wafer used, lifetime samples undergo slightly different process steps. CMOS-type wafers are cleaned, after which two-sided ALD oxide deposition takes place. After thermal annealing, lifetime/photoluminescence measurements can be carried out to assess the quality of passivation achieved. For PV-type wafers, the process flow is shown in Fig. 2.9. The front surface of a solar cell is mimicked by creating an n$^+$ FSF, through a POCl$_3$ diffusion at high temperature. Next, the wafer undergoes thermal oxidation in an O$_2$ atmosphere, to drive the created n$^+$ region further into the silicon while also creating a thermal oxide (SiO$_2$) layer at the surface. The oxide is removed via a dip in a diluted hydrofluoric acid (HF) solution (1% HF in H$_2$O, at room temperature). At this stage, the wafers are ready for oxide deposition, thermal annealing, and measurements, respectively.

All anneals consisted of a temperature ramp-up stage, followed by a 30 minute step at the set temperature and a ramp-down. The process is carried out in a nitrogen atmosphere, such that any hydrogenation of defects which takes place is due to the hydrogen content of the oxide layers.
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2.3 Experimental details

Figure 2.10: Precursors used to grow the HfO₂ thin films: (a) HfCl₄, a simple and widely used metal halide precursor for thermal ALD (b) HyALD, an organic precursor, used here for plasma-enhanced ALD.

Atomic layer deposition of HfO₂ was carried out via two separate systems with different precursors, shown in Fig. 2.10. Thermal ALD using HfCl₄ and H₂O was available on the ASM Polygon 8200 system, capable of processing 200mm CMOS wafers and 156 mm x 156 mm semi-square PV wafers, with the use of pocket wafers. This system is capable of one-sided depositions, at 200 °C and 300 °C. Al₂O₃ can also be deposited, in a thermal process, using the well-known precursor trimethylaluminium (TMA - Al(CH₃)₃) and H₂O.

The second available system was the Oxford Instruments FlexAL, remote plasma ALD reactor, capable of processing wafers up to 200 mm diameter and also PV-type, 156 mm x 156 mm semi-square wafers with the use of a 200 mm, round, pocket wafer. The reactor was equipped with a more complex, organic precursor containing a cyclopentadienyl (Cp) ring, called HyALD, supplied by Air Liquide (CpHf(NMe₂)₃). Cyclopentadienyl complexes are generally thermally stable, thus ensuring high quality depositions, by avoiding precursor decomposition. The ALD
process uses O$_2$ plasma as an oxidizer and one-sided depositions are possible. The process temperature was 250 $^\circ$C. This equipment is also capable of depositing Al$_2$O$_3$ films, from TMA and H$_2$O or O$_2$ plasma, at variable temperatures.

Some depositions of Al$_2$O$_3$ were necessary for reference purposes. For passivation of PV-type wafers, the depositions were carried out via spatial ALD, in the SoLayTec InPassion LAB reactor, at 200 $^\circ$C. For CMOS-type wafers, the ASM Polygon 8200 system was used, at the same temperature. Other reference wafers were passivated using SiN$_x$ or SiO$_2$, deposited in the Tempress PECVD reactor, using an optimized, proprietary recipe.
Chapter 3

Characterization of HfO$_2$ layers

In this chapter we present the characterization results of the deposited HfO$_2$ films, while briefly describing the methodology. The investigations have provided an understanding of the potential of the two hafnium precursors for passivation. Simulations were used to compare the optical performance of HfO$_2$ with other standard oxides, such as Al$_2$O$_3$ and SiO$_2$. Physical and chemical characterization revealed the crystal structure and impurity content of the investigated samples and electrical investigations were carried out, in order to measure the fixed charge content and density of interface traps.

3.1 Optical simulations

In order to assess the effectiveness of HfO$_2$ as a passivation layer from an optical point of view, simulations were carried out. We determined the maximum achievable photocurrent from a solar cell structure, not accounting for any, non-optical losses. Wafer ray tracer, an online simulation software package, developed by PV lighthouse, was used for the simulations. The software uses a Monte Carlo ray tracing algorithm which is described as follows[39]:

- A given number of light rays are generated above the simulated structure.
- At each interface, the reflectance, transmittance and absorptance are calculated and the values are used in a weighted, random decision on whether to transmit or reflect each ray.
- Propagation of a ray through absorbing media leads to a reduction in its intensity. Absorption in the silicon substrate equates to photogeneration of carriers, constituting gains for the current.
- If a ray’s intensity falls beneath a given threshold, it is considered to be completely absorbed.
- Calculations are carried out until all the rays are either absorbed or leave the structure by transmission or reflection.
- Each ray is only allowed to be reflected or transmitted a given maximum number of times. After this number is reached, no further calculations are done for the respective ray.
- The output of the simulation is produced by calculating the total photogeneration gains, and losses by reflection, transmission, and parasitic absorption, integrated over the simulated spectrum. The value of the achievable photocurrent which is calculated equates to
the short-circuit current achievable in a solar cell with the simulated configuration, without taking into account any non-optical losses.

The simulation algorithm takes into account the real part of the refractive index, and the extinction coefficient of each material, providing an estimate for the achievable current from a simulated solar cell structure. While a more detailed analysis could be achieved by accounting for, as an example, the complex nature of the refractive index, the results shown here should provide a starting point for our discussion around HfO$_2$ as a viable passivation material. Certain approximations had to be made, due to gaps in the available data and the structure of the ray tracing algorithm, as will become apparent later in this section. These approximations limit the impact of the results presented here, but a deep understanding of the optical properties of HfO$_2$ is outside the scope of this thesis, and the actual photocurrent values are not of crucial importance. The goal of this investigation is to provide a comparison between HfO$_2$ and other, standard passivation layers.

The AM1.5g solar spectrum was used for the simulations, with wavelengths varying from 300 nm to 1200 nm. Incidence of light was perpendicular to the surface. We considered an n-PERT-type structure for the solar cell, with passivation and anti-reflective (AR) SiN$_x$ capping at the front side, as shown in fig. 3.1. The 170 µm thick silicon wafer had a textured front surface, with random upright pyramids, which improves light trapping. On the rear, non-textured surface, ALD Al$_2$O$_3$ capped with PECVD SiO$_x$ was used as passivation and a 2 µm aluminium layer was used as a back contact. The simulation variable was the SiN$_x$ thickness which was used to optimize the photocurrent for each type of oxide used at the front side of the structure (HfO$_2$, Al$_2$O$_3$, SiO$_2$). A reasonable and practical value of thickness was considered for each oxide. In the case of SiO$_2$, 25 nm is the thickness obtained after the dry oxidation step, in which the n+ FSF is driven into the wafer surface. This is usually capped with PECVD SiN$_x$, providing good passivation for the n-PERT cell’s front side. For Al$_2$O$_3$ 10 nm was considered a standard thickness, for the purposes of the simulations. Finally, 15 nm was the thickness used for HfO$_2$, for reasons that will become apparent later on. This value was used because it is achievable via ALD, although thinner layers are preferred in practice, due to the long duration of ALD depositions and the high costs related to long processing times.

![Figure 3.1: n-PERT structure considered for the optical performance comparison of HfO$_2$, Al$_2$O$_3$ and SiO$_2$. Perpendicular illumination was considered. A Monte Carlo simulation is used to trace a large number of light rays.](image)
The thickness of the SiN\textsubscript{x} layer was varied between 20 nm and 100 nm and the maximum photocurrent is shown in fig. 3.2. All oxides showed increased performance at mid-range capping layer thicknesses. HfO\textsubscript{2} and Al\textsubscript{2}O\textsubscript{3} produce very similar results, with a slightly higher maximum current value for HfO\textsubscript{2}. Since the difference between the two materials is smaller than the simulation errors, it is only possible to conclude that both oxides should show similar optical performance in their respective best case scenario.

SiO\textsubscript{2} layers are less optically efficient, producing a slightly lower current value at the optimal nitride thickness, although the calculation errors lead to a certain amount of overlap with HfO\textsubscript{2} and Al\textsubscript{2}O\textsubscript{3}. The explanation can be found by looking at the amount of absorption taking place in the silicon wafer for each oxide and the amount of reflected light. The absorption and reflection spectra are shown in fig. 3.3. There is a net difference in the ultraviolet (UV) range between SiO\textsubscript{2} and the other two materials. This is due to the differences in refractive index (RI) between the materials, in conjunction with the different layer thicknesses.

The RI range for each material is shown in table 3.1. An asterisk indicates a value corresponding to a wavelength other than 300 nm, due to lack of data within the software library. In simulations, the RI is considered constant between the last available wavelength and the end of the simulated spectrum, at 300 nm. The wavelengths at which the respective refractive index values were given are relatively close to 300 nm (365 nm for HfO\textsubscript{2} and 400 nm for Al\textsubscript{2}O\textsubscript{3}). As such, an assumption is made in the algorithm, that the values used in the simulation differ only slightly from the real ones. We see that the HfO\textsubscript{2} layer matches relatively well with the SiN\textsubscript{x}, whereas the Al\textsubscript{2}O\textsubscript{3} and SiO\textsubscript{2} have significantly lower RI values. A refractive index mismatch allows total internal reflection (TIR) to occur at the oxide/nitride interface. A larger mismatch lowers the critical angle at which TIR occurs, allowing a greater amount of light to be reflected from the solar cell.

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Figure 3.3: Optical simulation results for HfO$_2$, Al$_2$O$_3$ and SiO$_2$: (a) fraction of incident light absorbed in the silicon wafer, which contributes to carrier generation; (b) fraction of incident light reflected off the front surface of the simulated structure. In both cases, SiO$_2$ performs worse than the other materials in the UV part of the spectrum.

Table 3.1: Refractive index values for oxides and the AR capping layer, taken from the software library. For HfO$_2$ and Al$_2$O$_3$, the wavelength closest to 300 nm at which data was available is given. The refractive index is considered constant between 300 nm and the respective wavelength. The database values of the extinction coefficient for all three oxides is zero within the simulated spectrum.

<table>
<thead>
<tr>
<th>Material</th>
<th>Refractive index at 300 nm</th>
<th>Refractive index at 1200 nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>HfO$_2$</td>
<td>2.18$^a$ (at 365 nm)</td>
<td>2.08</td>
</tr>
<tr>
<td>Al$_2$O$_3$</td>
<td>1.66$^a$ (at 400 nm)</td>
<td>1.63</td>
</tr>
<tr>
<td>SiO$_2$</td>
<td>1.49</td>
<td>1.45</td>
</tr>
<tr>
<td>SiN$_x$</td>
<td>2.29</td>
<td>1.98</td>
</tr>
</tbody>
</table>

The large difference between the reflection spectrum of Al$_2$O$_3$ (or HfO$_2$) and SiO$_2$ is most likely due to the difference in layer thickness. This is corroborated by the data shown in fig. 3.4, where oxide layers of identical thickness were used in the same type of simulation. The 25 nm thick films show very similar performance for both Al$_2$O$_3$ and SiO$_2$. Taking into account the parameters of the simulation algorithm, the divergence of the curves at higher SiN$_x$ thicknesses is most likely due to the difference in refractive index of the two oxides. Since Al$_2$O$_3$ has a slightly higher refractive index, it is better matched with the anti-reflective SiN$_x$, resulting in a slightly higher photocurrent than in the case of SiO$_2$, due to the larger angle of total internal reflection. Conversely, the optimal SiN$_x$ thickness and the better superposition of the curves in the respective region is a result of the identical thickness of the two oxides.

In conclusion, the simulations show that HfO$_2$ is a viable passivation material, from an optical point of view, particularly as front side material, in conjunction with a SiN$_x$ layer. The refractive index, being close to that of the nitride, does not disrupt its anti-reflective functionality, thereby reducing losses in comparison with the other oxides. This and the totally negligible absorption within the layer itself, which is due to a null extinction coefficient (within the software library), and the low layer thickness, work to ensure a value for the maximum photocurrent on par with the other two materials investigated.

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Figure 3.4: Optical simulation results for Al₂O₃ and SiO₂ layers of the same thickness (25 nm). The similar behavior between the two oxides suggests that the difference in performance from fig. 3.2 is due in large part to the difference in film thickness. A table containing the simulation results is available in appendix A.

3.2 Physical characterization of HfO₂ layers via TEM

Transmission electron microscopy (TEM) was used to investigate the structure of the deposited films, before and after annealing. It has been reported that a thin interfacial SiO₂ layer is formed during atomic layer deposition of HfO₂[23]. To confirm this, films deposited on a hydrophobic surface were investigated. This way, the oxide layer is not present before deposition and is probably a result of the HfO₂ growth process. Layers were grown using both the HyALD and HfCl₄ precursor. HfCl₄ was used to deposit layers at both 200°C and 300°C. High resolution TEM was used to determine the crystallinity of the oxide at different annealing conditions. A chemical analysis was carried out, using the energy-dispersive X-ray spectroscopy (EDS) capabilities of the TEM, in order to identify any impurities in the oxide layer that may result from the ALD reactions. It has been reported by Sreenivasan et al. that Cl impurities may create negative fixed charge in HfO₂ layers grown from HfCl₄[22]. EDS was used to confirm the validity of this statement for our samples, providing a better understanding of the fixed charge creation mechanism, necessary for electrical analysis. The investigated samples for each precursor and growth condition consisted of as-deposited layers of HfO₂, as well as layers annealed at 400°C and 500°C. Additionally, chemical analysis via elastic recoil detection (ERD) was used to determine the concentration of hydrogen atoms present in the deposited layers. Large amounts of H found in, for example, SiNx can lead to hydrogenation of the Si substrate via annealing at high temperatures, which leads to the passivation of defects at the Si surface and in the Si bulk[40]. Another example of a material with high H content, which can contribute to surface passivation via hydrogenation, is Al₂O₃. The optimal annealing temperature was found to be around 400°C[11], suggesting that hydrogenation from the layer occurs at this point. Al₂O₃ constituted a reference for our measurements. A 10 nm thick Al₂O₃ layer was deposited at a temperature...
of 300°C, from TMA and H₂O. The resulting concentration of H was 6.1 at.%, which is indeed a large value. As-deposited samples of HfO₂ grown from the two precursors were measured for comparison, providing further insight into the passivation capabilities of the material.

3.2.1 HyALD precursor

The first HfO₂ layers were grown from the metal-organic HyALD metal precursor, at 200°C, on a hydrophobic surface. Depositions were done via a plasma enhanced ALD process, as described in section 2.3. TEM images of the samples are shown in fig. 3.5. We can distinguish the interfacial layer, with an average thickness of slightly over 1 nm, which is present in the as-deposited sample, and therefore must be formed either during sample manipulation in air, or during HfO₂ deposition. Annealing to 400°C does not considerably affect the thickness of the interface layer. The 500°C-annealed sample did not allow high resolution images to be taken, due to its increased cross-section thickness, which leads to more electron scattering events. As a result, the thickness of the interface layer is probably underestimated, due to the roughness of the SiO₂-HfO₂ interface. The reason for this is the very high depth of field of the TEM, which means that the same focus is obtained throughout the entire thickness of the sample[41]. It follows that any overlap between structures leads to a darker area of contrast. The thicker sample, seen in fig. 3.5c, shows more overlap between the two oxide layers, increasing the darkness in the interface region. Therefore, the bright SiO₂ layer is probably thicker than can be precisely determined, while the HfO₂ layer is slightly thinner.

Figure 3.5: TEM images of HfO₂ layers deposited using the HyALD precursor. An interfacial SiO₂ layer is formed during deposition. Onset of crystallization seems to be around 400°C.

One possibility is that the interfacial layer is grown, at least partially, during the first part of the ALD process, when the hydrophobic surface favors island growth of HfO₂. During this period, the Si surface is exposed to the oxidizing plasma, which leads to SiO₂ formation. Chemical analysis via EDS, shown in fig. 3.6 reveals that the layer indeed contains both Si and O atoms. The presence of such an interfacial layer reduces the overall relative electrical permittivity of the HfO₂ layer, which in turn decreases its miniaturization potential for electronic device applications. This isn’t a concern for photovoltaic devices, since the permittivity does not influence passivation quality. This does, however, affect the quality of the interface and may even influence the oxide fixed charge density, as will be explained later in this section.

The structure of the HfO₂ layer is amorphous in the as-deposited state. The onset of crystallization is known to be around 450-500°C[42]. However, in our investigation, we observe crystalline formation in the samples annealed at the lower temperature of 400°C. The lower resolution for the 500°C-annealed sample prevents the identification of crystallites, but it is more than sensible to assume that the layer is polycrystalline, since crystallization already occurs at a lower
CHAPTER 3. CHARACTERIZATION OF HfO$_2$ LAYERS

Temperature. A possible explanation for the quicker onset of crystallization may be linked to the roughness of the SiO$_2$-HfO$_2$ interface. This, combined with steric hindrance leads to the formation of interface defects. Here the potential barrier for nucleation of crystals may be lower than in the rest of the material, due to the structural difference, thus allowing crystal formation at a lower temperature than expected. Crystallization of HfO$_2$ also occurs due to exposure to the high energy electron beam during measurement, but the amorphous nature of the as-deposited sample suggests that the process is sufficiently slow to allow the analysis of a relatively unaffected layer.

Chemical analysis of the deposited layers is shown in fig. 3.6, in the form of EDS maps. The green map reveals the presence of Hf atoms in the interfacial layer and in the Si substrate, which is most likely due to the ion milling process used to decrease sample thickness. The incident ion beam sputters atoms from the top to the bottom of the structure, such that a certain amount of Hf is displaced towards the substrate. Due to the metal-organic nature of the Hf precursor, impurities containing C and N were expected in the layers. The chemical maps for these elements are available in appendix C. Only a very small signal was detected for these elements, which suggests that their concentration is close to the detection limit of 1 at.%. We can therefore conclude that relatively low quantities of impurities are incorporated in the layer during the ALD process.

The analysis of the H content of the layers revealed a concentration of 1.7 at.%, with an approximate uncertainty of 0.5 at%. The presence of H, albeit in a lower concentration than for the Al$_2$O$_3$ reference sample, suggests that passivation of any interface defects may be improved by high temperature annealing.

![Figure 3.6: Energy-dispersive X-ray spectroscopy (EDS) maps of the Hf (green), O (red) and Si (cyan) content of the HfO$_2$-passivated Si surface imaged in fig. 3.5. Hf presence in the substrate is due to the ion beam milling of the sample in a top to bottom direction. The interfacial layer is marked with a yellow box. It is most likely a SiO$_2$ layer, formed during the first cycles of the ALD process. The maps correspond to the as-deposited sample. Hf, O and Si content is similarly distributed after 400°C and 500°C anneals. Enlarged images are available in appendix C.](image)

3.2.2 HfCl$_4$ precursor

Similar investigations as with the HyALD precursor were carried out for samples deposited using HfCl$_4$. A thermal ALD process was used for these depositions, as opposed to the plasma-enhanced ALD in the previous case. Depositions were carried out at 200°C and 300°C. It has previously been shown that the two deposition conditions produce quite different layers, with regard to film structure and composition[42]. Similar to the HyALD-derived films, the depositions were done on a hydrophobic surface, to allow for the identification of any interfacial oxide layer grown during the ALD process. Samples of as-deposited, 400°C-annealed and 500°C-annealed layers were once again investigated.
High resolution TEM images of the 200°C-deposited layers are shown in fig. 3.7. An interface layer can be distinguished, similar to the case for the previous precursor. The average thickness of the interface layer appears to be slightly lower than that grown with the HyALD. One possible explanation for this is related to the size of the two precursor molecules. The much larger organic molecule leads to more steric hindrance, which limits surface reactions. As a result, the binding of Hf is inhibited after a lower fraction of the surface has been covered than in the case of the smaller HfCl$_4$ molecule. This leaves more of the Si surface exposed to the oxidant, such that a thicker interface layer is then formed with the HyALD precursor.

![Figure 3.7: TEM images of HfO$_2$ layers deposited using the HfCl$_4$ precursor at 200°C. An interfacial SiO$_2$ layer is formed during deposition. The interface layer is thinner than the one grown during deposition using HyALD. Onset of crystallization seems to be around 400°C, similar to the HyALD-deposited HfO$_2$ layers.](image)

Crystallization of the HfO$_2$ layers already occurs at 400°C, similar to the situation for the HyALD precursor. The high resolution image for the 500°C-annealed sample enables the visualization of the crystal grains. We determine that their size is comparable to the thickness of the oxide layer. The layer is completely polycrystalline in this situation, whereas after a 400°C anneal, it is still possible to distinguish areas where the film has an amorphous structure.

Chemical analysis reveals a distribution of Hf, O, and Si atoms identical to the one seen with the HyALD precursor in fig. 3.6. Consequently, we do not show the EDS maps here, but only mention that Hf and O are mainly found in the deposited layer, with some traces in the Si substrate, due to the ion milling direction. The interface layer is composed mainly of Si and O. However, a search for Cl impurities reveals a preferential distribution of this species at the interface. This was also found by Sreenivasan et al., via secondary ion mass spectroscopy (SIMS) investigations[22]. The Cl distribution is shown in the EDS maps from appendix C. While Cl atoms are detected throughout the HfO$_2$, there is a clear peak in the SiO$_2$ interface layer.

While differences in Cl signal are registered between the three annealing cases, it is not directly clear that the actual concentrations vary in a similar way. More precisely, the differences in signal strength may be due to the detection method, rather than the actual Cl content of the imaged structures. This is because Cl is a highly volatile atomic species, and may be displaced by the incident electron beam, which is used for both imaging and chemical analysis of the samples. It is therefore possible that a stronger signal actually points to a more stable bonding of the Cl atoms within the layer, rather than a higher concentration. Consequently, we cannot draw any firm conclusions from the Cl EDS signal intensity, but only confirm the preferential distribution of this species towards the interface. The reason for this arrangement was proposed by Sreenivasan et al.[22], and it is explained in detail, further on in this section.

ERD analysis revealed a very high concentration of H (8.7 at.\% ± 1 at.\%) in the layers deposited from HfCl$_4$, at 200°C. This will most likely lead to hydrogenation of the interface when samples are annealed, resulting in increased lifetimes, due to reduced interface trap densities.
CHAPTER 3. CHARACTERIZATION OF HFO\textsubscript{2} LAYERS

Investigations of samples deposited using HfCl\textsubscript{4} at 200°C and 300°C revealed a relatively significant influence of the deposition temperature on the physical and chemical properties of the HfO\textsubscript{2} layers. Similarly to the case for 200°C deposition, there is a thin interfacial oxide at 300°C, of a lower thickness than that observed for the HyALD precursor. However, a difference in the structure of the as-deposited film is immediately evident. Films grown at 300°C possess a partly polycrystalline structure immediately after deposition, as shown in fig. 3.8. This leads us to assume that lifetimes measured for wafers passivated at this deposition condition will be lower than those for the 200°C case. The crystallization in the as-deposited condition may be a result of the increased thermal budget provided during the 300°C deposition. The deposition would then function as a much longer anneal at 300°C than our post-deposition processes.

Figure 3.8: TEM images of Hfo\textsubscript{2} layers deposited using the HfCl\textsubscript{4} precursor at 300°C. An interfacial SiO\textsubscript{2} layer is formed during deposition, similar to samples deposited at 200°C. As-deposited, layers show a mixed, amorphous-polycrystalline structure. The grain sizes are marked with red arrows. Annealing produces an increase their in lateral dimensions.

The size of the crystal grains is comparable to the layer thickness for the as-deposited sample, whereas annealing at 400°C doubles their lateral dimensions. The sample cross-section for the 500°C annealing case was thicker than the others, leading once more to a lower resolution, which did not permit visualization of the crystal structure of the HfO\textsubscript{2} layer. However, since annealing was shown to increase grain size, it is safe to assume that the film is also crystalline in this situation.

ERD analysis revealed a high concentration of H in the HfO\textsubscript{2} layers deposited at 300°C. At 3.7\% ± 0.5 at.\%, the hydrogen content is less than half that of the layers deposited at 200°C. This is most likely a direct result of the higher temperature, which causes a greater rate of desorption of the H-containing species at the surface. Nonetheless, the measured concentration is relatively high, such that we can again expect low interface trap densities, due to hydrogenation of the Si surface.

Chemical analysis via EDS was not carried out for the 300°C-deposited layers, since previous research has shown that increased deposition temperature leads to lower Cl impurity concentration\cite{sreenivasan2006}. Due to the very weak Cl signal in the 200°C deposition case, we did not expect any valuable information to be extracted from Cl mapping in the 300°C situation. The absence of a chemical analysis is not crucial in this case, since the Cl impurity concentration can already be linked to the fixed charge density of the deposited layers. This charge creation mechanism is presented in the following paragraphs.

3.2.3 Mechanism for fixed charge formation in Hfo\textsubscript{2} layers

The source of positive and negative fixed charge in Hfo\textsubscript{2} layers deposited from metal-organic precursors (such as HyALD) and metal-halide precursors (such as HfCl\textsubscript{4}) respectively has been proposed by Sreenivasan and his colleagues in 2006\cite{sreenivasan2006}. Hfo\textsubscript{2} layers were grown on p-type Si...
wafers, passivated by a 1.5 nm-thick, chemical SiO$_2$ layer. In our experiments, such a layer is intrinsically grown, but is probably of much lower quality than the one grown via a controlled process.

SIMS measurements were used to construct the impurity depth profile of the deposited stacks. A local peak in Cl concentration was found in the HfCl$_4$-derived films, similar to our EDS characterization results. Electrical measurements revealed a flat band voltage shift, corresponding to a negative fixed charge density. The films deposited using a metal-organic precursor contained positive fixed charge, in absence of any Cl impurities. Annealing such films in HCl lead to Cl segregation to the SiO$_2$ interface. This induced a $V_{FB}$ shift in the measured capacitance-voltage curve, pointing to the addition of negative charge, revealing the Cl impurities to be a contributing factor.

Segregation of Cl to the SiO$_2$-HfO$_2$ interface can be explained by considering the difference in coordination number between the two materials. Whereas Si has a fourfold coordination to O in SiO$_2$, Hf has a higher coordination number of 7 or 8 in HfO$_2$, depending on its crystal structure. This leads to unsatisfied Hf bonds at the interface, producing a local positive fixed charge. Segregation of electronegative species, such as Cl, to this location works towards the compensation of the positive charge, while excessive segregation, above that required to passivate the Hf bonds, leads to the formation of negative fixed charge.

In conclusion, the presence of both positive and negative fixed charge can be explained for HfO$_2$ layers, as a result of the chemical structure of the SiO$_2$-HfO$_2$ interface and the chemical composition of the metal precursors. This explanation is further sustained by our electrical measurement results, as will be shown further on in this chapter.

### 3.3 Extraction of $Q_f$ and $D_{it}$ via electrical measurements

In order to determine the values of fixed charge and interface trap density for the deposited HfO$_2$ films, capacitance-voltage (C-V) and conductance-voltage (G-V) measurements were carried out, respectively. Both types of measurements were done simultaneously, using the Agilent HP4156c Precision Semiconductor Parameter Analyzer.

Sample preparation consisted of creating MOS capacitor structures on a CMOS-type Si wafer. This was done by first depositing a HfO$_2$ layer on a preconditioned surface and annealing at the desired temperature. Next, circular aluminium contacts were deposited via thermal evaporation. No post-deposition contact anneal was done, in order to ensure that no extra treatment of the deposited layers took place, other than the initial thermal processing. In this way, we ensure a similar thermal budget for both electrical and lifetime samples, when annealed at the same temperature, making it possible to accurately link electrical and lifetime results. The structure and measurement setup for an electrical sample are depicted in fig. 3.9.

To measure a sample, it is placed on a metal chuck, which constitutes the back contact in the measurement scheme, and a probe needle is placed on top of an Al front contact. Although contacts of various diameters were deposited, only a small range of sizes were used for the actual measurements. This was done to avoid unwanted effects such as leakage, which can occur when carrying out measurements on larger dots, due to large capacitance values and a larger absolute number of defects in the layer. The smallest-sized contacts were also avoided, due to the large relative variations in area given by even small imperfections in their circular shape. These would lead to large relative errors when calculating the densities of the desired parameters. Consequently, we only considered contacts with diameters between 120 $\mu$m and 150 $\mu$m, which generally registered capacitance values under 200 pF, while retaining a regular, circular shape of relatively consistent area.
3.3.1 The ideal MOS capacitor

For an ideal MOS capacitor there should be no oxide charge, and the metal and semiconductor work functions should be equal\cite{43}. This means that at no applied bias, all energy levels should be flat and the electric field across the whole structure should be zero. The band structure is illustrated in fig. 3.10.

The equivalent circuit of an ideal MOS capacitor is shown in fig. 3.11, as described by Nicollian and Brews. The capacitor acts as the series combination of the oxide capacitance and that of the silicon. The capacitance of the silicon is dependent on bias, since it is generated by the charge

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induced at the substrate/oxide interface. As a result, the total capacitance will be the one given in eq. (3.1), where $\psi_s$ is the silicon band bending, induced by the applied bias:[44].

\[
\frac{1}{C} = \frac{1}{C_s(\psi_s)} + \frac{1}{C_{ox}}
\]  

(3.1)

Figure 3.11: Electrical and physical model for an ideal MOS capacitor [44].

A C-V measurement consists of applying a high, variable bias voltage to one terminal and a small, alternating, probing voltage to the other. This way, the capacitance value of the MOS structure can be measured in different charging regimes. In most literature reports on the subject of MOS capacitors, the bias is applied to the gate, defined in our experiments by the front side Al contact dots. The measurement voltage is then applied to the Si substrate. However, due to technical disadvantages given by this measurement scheme, in our experiments we applied the bias voltage to the Si substrate. This had the benefit of reduced measurement noise, the only difference to the standard case being that the bias is reversed, such that all measured curves are mirrored with respect to the applied voltage. A detailed description of C-V measurements for MOS capacitors is available in several different works [45, 44, 43].

Depending on the measurement parameters, such as the frequency and bias sweeping rate, the registered C-V curves can vary, as shown in fig. 3.12 (in which the bias voltage is applied in the typical way (i.e. to the metal gate). We can distinguish three regions: accumulation, depletion and inversion. The band diagram for these situations is shown in fig. 3.13.

The behavior of an ideal MOS capacitor with an n-type substrate can be explained as follows. If a bias sweep is started at a positive value, the capacitor is in accumulation. In this situation, electrons are attracted to the surface, and the silicon bands bend downwards, as shown in fig. 3.13a. For a very strong positive bias, the electron density at the surface will be much larger than that of the bulk. As a result, the silicon capacitance term in eq. (3.1) becomes negligible ($\frac{1}{C_s(\psi_s)} \rightarrow 0$), and the total capacitance is equal to that of the oxide, $C_{ox}$. As the positive bias is decreased, the electron concentration at the surface decreases, which translates to a lower silicon capacitance, $C_s$. This results in the total capacitance becoming lower than $C_{ox}$. When the flat band voltage is reached, at zero applied bias, electrons start to be repelled
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Figure 3.12: Measurable C-V characteristics for an ideal MOS capacitor with an n-type substrate. Capacitance measured in inversion depends on the measurement conditions[45].

![Figure 3.12](image)

Figure 3.13: Band structure of an ideal MOS capacitor with an n-type Si substrate, in accumulation (a), depletion (b) and inversion (c).

![Figure 3.13](image)

from the surface and the silicon bands begin to bend upwards, as in fig. 3.13b. A depletion layer is formed, which widens as the bias is swept to more negative voltages, further decreasing $C_s$ and the total capacitance. When the Fermi level at the silicon surface crosses the intrinsic level at the middle of the bandgap, the electron and hole densities become equal. Past this point, holes start to dominate, as the capacitor enters the inversion regime. In this case, the measured capacitance depends on the measurement frequency and the speed at which the bias voltage is varied[45]. As such, three types of response can be achieved, as shown in fig. 3.12.

- First, if the bias voltage is swept sufficiently slowly, such that the inversion layer has time to form, and if the frequency of the measurement voltage is low enough to allow the inversion charge to respond to the applied electric field, we obtain the low frequency curve, $C_{lf}$, where the capacitance approaches $C_{ox}$ asymptotically[44].

- Second, if the bias voltage sweep is sufficiently slow, but the probing frequency is too high for the charge to respond, we obtain the high frequency response, $C_{hf}$.

- Finally, if the sweep rate is too high, we obtain the deep depletion curve, $C_{dd}$, regardless of
the measurement frequency, since the structure does not reach equilibrium and the inversion layer does not have time to form.

3.3.2 The real MOS capacitor

In the case of a non-ideal MOS capacitor, the metal and silicon work functions can differ. Additionally, charges are present both in the oxide and at the oxide-silicon interface. They generate an intrinsic electric field, which leads to deformations of the energy levels close to the interface. This phenomenon is known as band bending and the potential difference between the semiconductor bulk and the interface is known as the flat band voltage ($V_{FB}$), which is linked to the amount of charge present in the oxide. An illustration of the band structure for a non-ideal MOS capacitor is shown in fig. 3.14.

![Figure 3.14: The band structure for a non-ideal MOS capacitor, at zero applied bias.](image)

The deviations from the ideal case result in modifications of the measured C-V curve for a real MOS capacitor. First of all, the difference between the metal and semiconductor work functions generates a Fermi level offset between the two, which is compensated at equilibrium, resulting in band bending. For zero oxide charge, the flat band voltage is equal to the work function difference:

$$V_{FB} = \Phi_{MS} - \Phi_{Si}$$

(3.2)

The metal work function represents the minimum energy required for an electron to escape. It is equal to the difference between the vacuum energy and the Fermi energy in the metal. The semiconductor work function is a bit more complicated to interpret. If we consider an n-type semiconductor, the Fermi level will be higher than the intrinsic energy at mid-gap, by an amount equal to the bulk potential, $\Phi_b$:

$$\Phi_b = qV_t \ln \left( \frac{N_D}{n_i} \right),$$

(3.3)

where $V_t$ is the thermal voltage at room temperature and $N_D$ and $n_i$ represent the donor and intrinsic carrier concentration of the semiconductor, respectively. Therefore, we can deduce with
CHAPTER 3. CHARACTERIZATION OF HFO$_2$ LAYERS

the aid of fig. 3.14, that for an MOS capacitor, the metal-semiconductor work function is given by:

$$\Phi_{MS} = \Phi_M - \Phi_{Si} = \Phi_M - \chi_{Si} - \left(\frac{E_C - E_V}{2q}\right) + qV_t \ln \left(\frac{N_D}{n_i}\right), \quad (3.4)$$

where the semiconductor work function has been expressed in relation to the electron affinity, $\chi_{Si}$, the potential difference between the conduction band minimum and the intrinsic energy (i.e. half of the bandgap) and the bulk potential. We can now determine the flatband voltage in the absence of oxide charge, as long as the dopant concentration of the substrate is a known quantity.

Fixed charges present in the oxide generate an additional electric field, which modifies the flatband voltage from the quantity described in eq. (3.4). The oxide fixed charge expressed in Coulombs, $Q$, can be described as the cause of an additional flatband voltage shift, which is not due to the work function difference, as shown in eq. (3.5)[45]:

$$Q = \left(\frac{\Phi_{MS}}{q} - V_{FB}\right) \frac{C_{ox}}{[C]} \quad (3.5)$$

This relation provides a method of extracting the oxide fixed charge from a C-V curve, provided that the metal-semiconductor work function is known. As mentioned in section 1.3, oxide trapped charges produce the same effect and cannot be distinguished from fixed charges. Therefore, the measured quantity is actually the cumulative effect of both types of charges.

Mobile charges, present in the oxide mainly in the form of positive ionic impurities, can also induce a shift in flatband voltage. This can be visualized by performing a two-way voltage sweep during measurement. The mobile charges drift under the applied field, from one oxide interface to the other, causing hysteretic behavior. For example, in an MOS capacitor with an n-type substrate, the voltage sweep starting in accumulation transitions from positive to negative gate bias and back. If a high voltage is maintained for a sufficiently long time at the end of the first sweep, the mobile charges can transit the oxide from the gate to the semiconductor interface. This generates a surplus of positive charge at the silicon surface, which leads to a negative shift of the C-V curve for the return sweep. This produces a clockwise-oriented hysteresis loop, as shown in fig. 3.15. The effect of mobile charges is only important at high temperatures, which offer increased ion mobility[45]. Our measurements were done at room temperature, such that any observed hysteresis must be generated via a different mechanism. An example of a different mechanism is the injection of charges from the metal contacts or the silicon substrate into the oxide layer at high bias voltages. This modifies the fixed charge content of the oxide, leading to horizontal shifts in the C-V curves.

Interface trapped charges, measured as $D_{it}$, are also known to distort C-V curves from the ideal shape. In order to understand how this occurs, we must look into the nature of the traps. One model, backed by experimental evidence[45], developed for the SiO$_2$/Si interface, distinguishes between two categories of bandgap states introduced by interface traps:

- States in the lower half of the bandgap, exhibiting donor-like behavior;
- States in the upper half of the bandgap, with acceptor-like behavior.

As such, all donor traps are occupied by electrons when their energy is below the Fermi level and they are positively charged when their energy is between the Fermi level and the intrinsic level, at mid-gap. In contrast, acceptor states are considered neutral when their energy is above the Fermi level and they are negatively charged below the Fermi level. The model is illustrated in fig. 3.16a, b, and c. Figure 3.16a shows the effect of interface traps under flatband conditions, where acceptor-like traps below the Fermi level generate a net negative charge at the interface.
A more negative voltage shifts the bands upwards at the interface, inducing a net increase in positive charge, by lowering the number of acceptor states below the Fermi level (fig. 3.16b). At sufficiently low voltages, the Fermi level can cross the mid-gap level at the surface, leading to the additional positive charging of donor traps. Lastly, a voltage more positive than $V_{FB}$ produces a downward shift of the energy bands at the interface, increasing the number of charged acceptors, producing a net increase in negative charge (fig. 3.16c).

Figure 3.16: Donor-like (D) and acceptor-like (A) behavior of interface traps, as described by Schröder[45]. The n-type silicon surface is represented at a gate bias voltage $V_G=V_{FB}$ (a), $V_G<V_{FB}$ (b), and $V_G>V_{FB}$ (c). A uniform distribution for $D_{it}$ is considered and the +, −, and 0 signs denote the charge induced by the respective traps.

To understand the effect of interface traps on the shape of the measured conductance curve, we can consider an n-type MOS capacitor, for which the gate bias is swept from accumulation to depletion (positive to negative). Under flatband conditions ($V_{FB}$ is positive in this case), the $D_{it}$ contributes a net negative charge. Below $V_{FB}$ and towards negative values, there is a decrease in
negative charge, as fewer acceptors are occupied and donor occupation starts to decrease, when
the Fermi level is shifted below the intrinsic level. Conversely, for gate voltages above flatband
(i.e. higher positive voltages), extra negative charge is created at the interface. The distortions
to the C-V curve are schematically illustrated in fig. 3.17.

![Figure 3.17: Effect of $D_{it}$ on the C-V curve, for an n-type silicon substrate. At high frequency
(a), the traps do not contribute any capacitance, but the bias induces a charge which stretches
out the curve horizontally. For low frequencies (b), there is an interface trap contribution to
capacitance, in addition to the effect of biasing (after D.K. Schroder[45]).

When visualizing the effects of interface traps on measured C-V curves, we must consider the
frequency dependence of the added charge response. Consequently, we can observe two types of
trap-induced curve distortions:

- At high frequencies, the traps cannot contribute to the total capacitance, but they can
  follow the slowly sweeping gate voltage. Therefore, charging of interface traps in relation to
  the Fermi level position at the surface induces a positive horizontal shift in the conductance
curve for increasingly positive gate voltages and a negative shift for increasingly negative
  bias. This is shown in fig. 3.17a, as a stretching-out of the C-V curve in a horizontal
direction.

- If a low probing frequency is applied, the charges are able to follow the ac field, contributing
  to the total capacitance. This is seen as an increase in the depletion capacitance, in addition
to the horizontal stretching due to the gate voltage, as seen in fig. 3.17b.

3.3.3 Measurement interpretation

Sample measurements reproduce real MOS capacitor characteristics, which can differ strongly
from the ideal representation. As stated previously, in the chosen electrical configuration, the bias
is applied to the substrate and, for the n-type Si samples that were investigated, accumulation
occurred at negative applied voltages, while depletion and inversion occur at positive voltages.
However, for all calculations, the curves were considered mirrored with respect to voltage, to
avoid confusion.

The curves shown in fig. 3.18 better illustrate the differences between our measurement scheme
and the standard case, for an MOS capacitor with an n-type silicon substrate. In order to clarify
the situation, let us consider the voltage required for the structure to reach the flatband condition
(i.e. the flatband voltage).
Figure 3.18: Clarification of the differences between the standard C-V measurement configuration and the one used for our experiments. The resulting curves are horizontally mirrored and the interpretation of flatband voltage shifts is reversed. In the substrate biasing situation, positive $V_{FB}$ shifts indicate the presence of positive charge, while negative shifts point to negative charge.

As mentioned before, in the standard case, the gate is biased, while the measurement voltage is applied to the silicon substrate, via the metal chuck, on which it is placed. As a result, accumulation is achieved in the structure when a positive voltage is applied, crossing the flatband condition and bending the silicon energy bands downwards at the surface. A positive fixed charge in the oxide layer gives a more negative potential at the surface, inducing additional downwards band bending. Consequently, the flatband condition is achieved at more negative values of the gate voltage, which leads to a horizontal shift of the measured C-V curve in the negative direction. Conversely, negative oxide fixed charge induces upwards band bending at the surface, such that higher positive gate voltages are required, in order to achieve flatband conditions. This translates into a horizontal shift of the C-V curve in the positive direction.

When the bias voltage is applied to the sample with an n-type substrate, the situation is completely reversed. Accumulation is now achieved when a negative voltage is applied, repelling the majority carriers from the rear contact, towards the oxide-semiconductor interface. Positive oxide fixed charge still induces downwards band bending, which in this case is compensated by a positive substrate bias, such that a positive flatband voltage shift is observed. Conversely, the band bending induced by a negative oxide fixed charge is compensated by a negative substrate bias, such that we observe a negative horizontal shift in the C-V curve.

For the explanations regarding the theory of MOS capacitors from section 3.3.1 and section 3.3.2, the standard measurement scheme was considered. From this point on, all figures will contain curves measured with the alternative configuration we described, such that positive flatband voltage shifts will indicate positive oxide fixed charge, while negative shifts point to negative charge.
A typical measured curve is shown in Fig. 3.19a. From here, we can graphically extract the oxide capacitance and flatband voltage, which are required for the calculation of fixed charge density. By dividing Eq. (3.5) with the elementary charge, $q$, and the area of the capacitor, $S$, we can determine the surface density of point charges present in the oxide, close to the silicon interface, which will be referred to as $Q_f$ from this point on:

$$Q_f = -\frac{C_{ox}}{qS} \left( V_{FB} - \frac{\Phi_{MS}}{q} \right) \ [cm^{-2}] \ (3.6)$$

The determination of oxide fixed charge from the measured C-V curves requires the extraction of two parameters: $C_{ox}$ and $V_{FB}$. The oxide capacitance is determined as the value measured at the highest accumulation bias, since the silicon contribution to capacitance becomes negligible at this point. It is important to note that for sufficiently high voltages, charge leakage may occur, increasing the measured capacitance. Consequently, the bias voltage should be swept in a small enough range to prevent this, while still illustrating the capacitance response in accumulation, depletion and inversion.

Flatband voltage determination is a more complicated issue, due to the existence of several different methods, which can provide different levels of accuracy, depending on the situation. In our calculations, we used a quick method, in which the flatband voltage is considered approximately equal to the bias voltage at which an inflection point occurs in the measured C-V curve. The method was proposed by Winter et al. [46], and it is reported to provide an accurate approximation of the flatband voltage for sufficiently thin films and low enough interface trap densities [47]. The film thicknesses and $D_{it}$ values reported in this study fall within the limits of this approximation, such that the inflection point method may be applied.

More accurate techniques for flatband voltage extraction are available. A more thorough comparison of the inflection point method and two others is given in Appendix B, while the main characteristics and drawbacks of each of the methods considered are presented in this section. The most precise method consists of comparing the measured C-V curve with an ideal one, where the oxide is considered to have no fixed charge. The horizontal shift of the curve represents $V_{FB}$. This technique strongly depends on the accuracy with which the ideal curve can be modeled. The uncertainties in area, dielectric thickness, doping concentration and uniformity of the substrate, and also in the value of the metal work function prevent the proper implementation of this method.

Another widely used method consists of calculating the capacitance of the MOS structure under flatband conditions. The flatband voltage can be graphically determined from the C-V curve. A drawback for this method is its limited applicability: its accuracy is only guaranteed in the case of high frequency C-V measurements and the method requires prior knowledge of the sample parameters [46]. A comparison between this and the inflection point method for our samples revealed relatively insignificant differences in the resulting fixed charge values. Consequently, the quicker inflection point method was utilized for $V_{FB}$ determination in our experiments. More details regarding the choice of method are also given in Appendix B.

Further complications in the determination of fixed charge density arise from the non-ideal behavior of the MOS structures. This induces artifacts in the C-V curves, which can increase the difficulty of precisely calculating $Q_f$. Instances of non ideal behavior are shown in Fig. 3.19. As illustrated in Fig. 3.17b, at low enough frequencies, the interface trapped charges are able to respond to the probing signal and contribute to the measured capacitance. The model describing this (Eq. 3.16) assumes that the energy levels of the traps are distributed uniformly across the silicon bandgap. In practice, they have a peak distribution around the energy levels of the silicon dangling bonds, which the traps represent. This leads to the behavior observed in Fig. 3.19b, where trap contributions are only seen around a certain bias. The presence of interface traps...
also leads to an increase in conductance at the respective bias, as shown in fig. 3.19c. This is used in $D_t$ calculations, as will be described later in this section. Hysteresis, adds a level of uncertainty to our calculations, due to shifts in the flatband voltage. Depending on the source of the hysteresis, both the forward and the return curve can be horizontally shifted. In order to compensate for this, fixed charge calculations are done for both sweeping directions, using their respective flatband potentials. This provides a range within which we can expect the actual value of $Q_f$ to be found. Consequently, all our fixed charge graphs will show two values for each condition, $Q_f$ left and $Q_f$ right, derived from the two curves recorded in each measurement.

In order to investigate the density of interface traps, a simplified conductance method was used. The complete method was proposed by Nicollian and Goetzberger and is covered in works such as those of Schroder [45], Nicollian and Brews[44], and Sze[43]. A short overview is provided here, for the sake of completeness. The method consists of measuring the equivalent parallel conductance of an MOS capacitor as a function of bias voltage and frequency. The electrical model for the measured structure, used by the parameter analyzer, is shown in fig. 3.20c.
Figure 3.20: Circuit model of an MOS capacitor: (a) model which takes into account the effect of interface traps; $C_{it}$ and $R_{it}$ represent the conductance and resistance of interface traps, respectively; (b) simplified equivalent of (a); $C_p$ and $G_p$ are the equivalent parallel capacitance and conductance; (c) the measured circuit, which only considers a parallel capacitance and conductance, $C_p$ and $G_p$ (after D.K. Schroder [45]).

The model of an MOS capacitor with interface traps is shown in fig. 3.20a, and a more convenient representation is shown in fig. 3.20b, where the parallel conductance, $G_p$, and capacitance, $C_p$, can be derived [45]:

$$C_p = C_{Si} + \frac{C_{it}}{1 + (\omega \tau_{it})^2}$$

(3.7)

$$\frac{G_p}{\omega} = \frac{q \omega \tau_{it} D_{it}}{1 + (\omega \tau_{it})^2}$$

(3.8)

where $C_{it} = q^2 D_{it}$, $\omega = 2\pi f$, $f$ being the measurement frequency, and $\tau_{it} = R_{it} C_{it}$, the interface trap time constant. By plotting $G_p/\omega$ versus $\omega$ from eq. (3.8), we find that $G_p/\omega$ has a maximum at $\omega = 1/\tau_{it}$, resulting in a value for $D_{it}$:

$$D_{it} = \frac{2}{q} \left( \frac{G_p}{\omega} \right)_{max}$$

(3.9)

Capture and emission of charges primarily occurs for traps located within a few $kT/q$ above and below the Fermi level, leading to a time constant dispersion and modifying the normalized conductance. The dispersion is generally attributed to surface potential fluctuations due to non-uniformities in oxide charge, interface traps and doping density [45]. By taking such fluctuations into account, an approximate expression for the interface trap density can be given, related to the measured conductance:

$$D_{it} \approx \frac{2.5}{q} \left( \frac{G_p}{\omega} \right)_{max}$$

(3.10)

where $G_p$ and $\omega$ correspond to the measurement peak. Although the above equations all use the parallel conductance value $G_p$, fig. 3.20c reveals that the actual measured conductance, $G_m$, and capacitance, $C_m$, are different, since a simplified circuit is considered for the measured structure. For a more precise $D_{it}$ determination, this can be taken into account, via circuit comparison, and the resulting relations are given elsewhere [24]. For thin oxides, the measured devices may show considerable leakage current. Additionally, the MOS capacitor can be affected by series resistance which has so far been neglected. It is possible to determine its value, by biasing the device in accumulation and calculating:

$$r_s = \frac{G_m}{G_{max} + \omega^2 C_{max}^2}$$

(3.11)
where the index \( ma \) represents a value measured in accumulation. The accuracy of \( D_{it} \) calculations can be improved by applying a series resistance and tunneling (i.e. leakage) current correction, as described by Schröder [45].

The complete conductance method is one of the most sensitive techniques to measure \( D_{it} \) values, but it is also complicated and time-consuming, since it involves a large number of measurements. The simplified method we used is similar to that introduced by Hill and Coleman [48]. Instead of performing conductance measurements for a wide range of frequencies, they proposed using a single, high-frequency, C-V and G-V measurement to determine \( D_{it} \). The method is effective in probing only interface traps situated around the mid-gap region, and not the entire bandgap. Consequently, it tends to underestimate trap densities. However, for our purposes, it is sufficient to understand the trends in \( D_{it} \), since no quantitative post-calculations are required.

In light of the above reasoning, determination of \( Q_f \) and \( D_{it} \) was done as follows:

- A C-V and G-V measurement are performed simultaneously on a chosen device. This is done via a two-way voltage sweep, applied to the silicon substrate, starting in accumulation.
- A series resistance correction is applied to the measured curves.
- \( C_{ox} \) is extracted from the curve as the maximum capacitance value in accumulation.
- \( V_{FB} \) is extracted as the voltage where an inflection point occurs in the C-V curve. Two \( V_{FB} \) values are obtained, corresponding to the forward and return sweep.
- \( Q_f \) is calculated, using eq. (3.6); for both \( V_{FB} \) values. The real value of \( Q_f \) is expected to be situated between the two resulting extremes.
- The G-V curve shows a peak, also associated with a trap-induced distortion in the C-V curve. The maximum conductance value is used in eq. (3.10), to calculate \( D_{it} \).

Measurements were done at a relatively low frequency (1 kHz), in contrast to the method of Hill and Coleman. Furthermore, a low bias sweeping rate was used (0.05 V/step). This combination of measurement parameters ensured good charge response, such that the effects of interface traps become visible in the C-V curve. At the same time, measurements at frequencies above 500 Hz showed reduced noise for our samples, compared to lower frequencies. Further noise reduction was ensured by using long integration times. Thus, a smooth curve was extracted, by averaging a large number of measured values at each bias point.

### 3.4 Electrical measurement results

In this section, the results of C-V and G-V measurements are discussed in detail. The values for \( Q_f \) and \( D_{it} \) are averaged from up to 10 measurements per sample. All deposited films had a nominal thickness of 10 nm, to reduce the possibility of leakage, while maintaining low processing times. Measurements were done for as-deposited samples, as well as after annealing at 300°C, 400°C and 500°C. The observed trends are explained and conclusions are drawn on the applicability of HfO\(_2\) for passivation in each scenario. The results will be linked to those in the next chapter, to explain why a certain level of passivation quality is obtained and how it might be improved, if necessary. Films deposited from each precursor are investigated separately and a comparison is made at the end, citing the benefits and disadvantages of each one.
3.4.1 HyALD precursor

Films deposited by PEALD at 250°C, using the HyALD precursor, were the first to be investigated. HfO$_2$ deposition was done on a hydrophobic surface. A comparison of measured curves under all annealing conditions is shown in Fig. 3.21. We can distinguish a slight distortion in the as-deposited case, around 0.5 V applied bias. In the annealed samples, this effect becomes more visible. As illustrated in Fig. 3.19, this is due to the influence of interface traps on the measured capacitance. $D_{it}$ is reduced via post-deposition annealing, thus lowering the trap capacitance. As such, it is possible to visually distinguish between the oxide and the trap contributions. At high positive substrate bias, the capacitor should enter inversion. For the as-deposited and 300°C-annealed sample curves, the large flatband voltage shift moves the depletion region to higher positive voltages, such that the inversion region is shifted outside of the measurement range. The curve at 400°C shows a hump-like increase in capacitance around 1.25 V, pointing to a weak inversion layer response, whereas the 500°C-annealed sample shows a clear increase in capacitance due to inversion layer formation.

![Figure 3.21: C-V curve comparison between all annealing cases for the HyALD precursor (n-type silicon substrate). The inset illustrates the direction of hysteresis. $D_{it}$ contribution to capacitance decreases after thermal processing at higher temperatures. Inversion capacitance visible for 500°C anneal. The metal work function (corresponding to $V_{FB}$ in the absence of fixed charge) is equal to +0.053 V, with respect to the substrate.](image)

The $Q_f$ and $D_{it}$ results are shown in Fig. 3.22. Due to the high density of interface traps shown for the as-deposited and 300°C-annealed cases, the fixed charge cannot be determined without accounting for the interface trapped charge. This would require more precise knowledge of $D_{it}$ throughout the bandgap, which cannot be obtained with the measurement methods used. Low temperature measurements may provide a clearer picture of the effect of fixed charge, by eliminating the interface state contribution to the C-V characteristic, but they were not carried out for this work. As a result of the $D_{it}$ behavior, conclusions can only be drawn regarding the 400°C and 500°C-annealed samples, where very low negative charge was extracted (less than $10^{12}$ cm$^{-2}$). A slight trend is observed, towards more positive values at 500°C. Low oxide fixed charge may provide possibilities for symmetrical passivation schemes, if $D_{it}$ is sufficiently low, producing a significant reduction of SRH recombination at the surface.

The high $D_{it}$ values for the as-deposited and 300°C-annealed cases may be a result of the deposition process. Since the HfO$_2$ is grown via PEALD, it is possible to cause plasma damage...
to the films[37]. Moreover, the H-terminated surface favors island growth during ALD, decreasing the quality of the interface, since a stable growth per cycle is not immediately reached and variable surface coverage is obtained after each partial ALD reaction. $D_{it}$ values were greatly reduced by applying thermal treatment to the films, at temperatures higher than 300°C. We believe that this is due at least in part to the hydrogenation of the silicon surface, via effusion of atomic H from the HfO$_2$ layer. However, the onset of crystallization for HfO$_2$ also occurs in the range of 300°C to 400°C such that it is also possible for passivation quality to decrease at temperatures beyond this point.

The hysteresis of the C-V curves obtained from the HyALD-derived films consists of a negative flatband voltage shift for the return sweep, from depletion to accumulation (n.b. due to the measurement scheme, the value of $V_{FB}$ is the opposite of the inflection point voltage taken from each curve). This indicates a net positive charge increase, probably due to injection of holes to the oxide/silicon interface at high negative bias in the inversion region. The shift in $V_{FB}$
is small, indicating a possible compensation or inhibition of charge injection. Higher annealing temperatures lead to an increase in hysteresis, as illustrated in fig. 3.23. This may be explained by the low fixed charge present in the oxide after high temperature treatments, as opposed to the high positive charge produced by interface traps in the as-deposited and 300°C-annealed cases. The positive charge may work to repel any incoming holes from the oxide. After annealing above 400°C, the interface trapped charge is reduced, such that injection of holes is permitted, leading to a slightly larger hysteresis shift in $V_{FB}$.

### 3.4.2 HfCl$_4$ precursor at 200°C

ALD of HfO$_2$ using HfCl$_4$ as the metal precursor was carried out at both 200°C and 300°C. It has been shown by Sreenivasan et al. that, HfCl$_4$-derived films exhibit negative fixed charge [22]. This would make the precursor less suitable for passivation of n-type silicon than for p-type silicon. However, the variability of the fixed charge may allow for thermally treated layers to be used for such purposes.

HfO$_2$ films were grown at 200°C on both H-terminated and OH-terminated surfaces. In the first case, the measurement curves show a net negative shift with respect to substrate bias. This translates to a positive flat band voltage shift, which arises due to the presence of negative fixed charge in the oxide, in contrast to the films grown using the HyALD precursor. Example C-V curves for each annealed sample are shown in fig. 3.24. At 500°C annealing temperature, the flatband voltage is much closer to zero, such that we expect to see a much lower fixed charge density. High inversion capacitance was seen for all samples except those annealed at 300°C and 500°C. Due to the choice of frequency, which is slightly higher than what is normally used for low frequency measurements, the inversion response varies between curves, as can be seen for the curve corresponding to the 300°C-annealed sample, where the particular example shown reveals zero inversion capacitance, whereas other measurements for the same annealing temperature showed a non-zero value.

![C-V curve comparison for the HfCl$_4$ precursor, with depositions at 200°C on a hydrophobic surface (n-type silicon substrate). The inset illustrates the direction of hysteresis. $D_{it}$ contribution is much less pronounced than in the HyALD case. A shift to the left indicates negative oxide fixed charge. The metal work function (corresponding to $V_{FB}$ in the absence of fixed charge) is equal to +0.049 V, with respect to the substrate.](image)

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Fixed charge calculations confirm its negative polarity, as shown in fig. 3.25a. The temperature dependence can be explained by considering that Cl impurities are the source of the negative fixed charge, as discussed in section 3.2.3. It is possible that annealing at temperatures in the lower range provides sufficient energy for the Cl to segregate to the interface, where it produces a negative charge contribution. Higher temperatures provide more energy, possibly leading to effusion of Cl from the structure, reducing the negative charge, as seen for the sample annealed at 500°C. The interface trap density is very low even as-deposited, compared to the HyALD case. One reason for the large difference is the different ALD process used to deposit the layers. By using a thermal ALD process, damage to the layers from energetic charged particles is avoided, such that fewer defects are present at the interface. A second advantage may stem from the fact that HfCl4 is a much smaller molecule than that of the HyALD precursor. As a result, steric hindrance is reduced, meaning that better surface coverage can be achieved within one ALD cycle. This leads to better passivation of the dangling Si bonds at the interface, therefore reducing $D_{it}$. Moreover, the high concentration of H determined in section 3.2.2 most likely adds to passivation quality via hydrogenation of the silicon surface after annealing at sufficiently high temperatures. The H content should not be influenced by surface conditioning, since H should be present in the entire layer, not only at the interface. As such, we expect hydrogenation to also take place for samples which were prepared with hydrophilic surfaces.

![Figure 3.25: Fixed charge (a) and interface trap densities (b) for the HfCl4 precursor, with depositions at 200°C on a hydrophobic surface. High negative $Q_f$ contrasts with the organic precursor; low $D_{it}$ suggests much better chemical passivation is achieved by avoiding plasma damage due to the less energetic thermal ALD process.](image)

Hysteresis behavior is consistent with the interpretation from the previous precursor. The corresponding data is shown in fig. 3.26. As-deposited, the high negative charge favors the injection of holes at the interface, inducing a larger flatband voltage shift for the reverse sweep. The lower fixed charge at 500°C is comparable to the value achieved for the HyALD precursor, resulting in comparable hysteresis values.

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Figure 3.26: Average flatband voltage shift due to hysteresis for HfO$_2$ films deposited using the HfCl$_4$ precursor at 200°C, on a hydrophobic surface. The trend is consistent with the previous interpretation, of negative charge favoring $V_{FB}$ shifts.

Evaluation of films deposited on a hydrophilic surface revealed the annealing temperature dependence of the C-V curves shown in fig. 3.27. The range of flat band voltage is reduced in comparison to the hydrophobic surface case. Once more, $D_{it}$ capacitance contribution is low, compared to the HyALD precursor. Annealing further reduces the trap capacitance response. The trend of the fixed charge, shown in fig. 3.28a, is similar to the previous case. Between 400°C and 500°C, a relatively large amount of net positive charge is added, such that in this case the polarity is reversed. This is probably due to the effusion of negative Cl impurities from the structure, similar to the previous case, leading to the dominance of positive charge.

The interface trap density exhibits a temperature dependence similar to the one reported by Morato[24]. The as-deposited value is reduced by annealing at 300°C or 400°C, but for 500°C we register an increase, possibly due to high degree of film crystallization. This behavior and the overall lower $Q_f$ values may be explained by the quality of the interface, in relation to the findings of Sreenivasan et al.[22]. The Cl impurities are preferentially distributed close to the interface, where they are stably bonded with Hf atoms, up to 500°C. Here, they compensate any positive charges created by unsatisfied Hf bonds. An excess of Cl produces negative fixed charge. If the interface quality is increased, as should be the case for a hydrophilic surface, fewer Hf bonds remain unsatisfied, such that the number of Cl atoms also decreases, producing less negative charge.

In relation to the $D_{it}$ behavior, we can note that a net positive fixed charge points to an absence of Cl. This leaves unsatisfied Hf bonds at the HfO$_2$-SiO$_2$ interface, which may be sufficiently close to the Si surface to induce trap states. Therefore, the 500°C-annealed layer shows a larger $D_{it}$ in the positively charged hydrophilic case, than in the hydrophobic case, where $Q_f$ is close to zero.

C-V curve hysteresis values are comparable to those corresponding to low fixed charge in the previous cases. In this instance, shown in fig. 3.29, we register an increase of $\Delta V_{FB}$ with annealing temperature, which does not appear consistent with our previous interpretations. It is possible that the increasing trend is induced by a less prominent mechanism, which is different from the ones described until now.
Figure 3.27: C-V curve comparison for the HfCl$_4$ precursor, with depositions at 200°C on a hydrophilic surface (n-type silicon substrate). The inset illustrates the direction of hysteresis. Shifts in $V_{FB}$ are much lower than on an H-terminated surface. The metal work function (corresponding to $V_{FB}$ in the absence of fixed charge) is equal to $+0.006$ V, with respect to the substrate.

Figure 3.28: Fixed charge (a) and interface trap densities (b) for the HfCl$_4$ precursor, with depositions at 200°C on a hydrophilic surface. Lower $Q_f$ is measured, with respect to the hydrophobic case. $D_{it}$ improves after annealing at 300°C and 400°C, but crystallization leads to an increase at 500°C.
3.4.3 HfCl₄ precursor at 300°C

Sreenivasan et al. reported that increased temperatures lead to fewer impurities incorporated in HfCl₄-derived, ALD HfO₂ films [22]. The metal-halide precursor features Hf-Cl bonds, which are replaced by Hf-O bonds during the deposition process. A high activation potential barrier must be overcome for this to take place, such that fewer Cl impurities may be present in the 300°C-deposited layers than the 200°C case. Both hydrophobic and hydrophilic surfaces were passivated and a comparison of the two growth temperatures for each case improves our understanding of the $Q_f$ and $D_{it}$ behavior.

Figure 3.30: C-V curve comparison for the HfCl₄ precursor, with depositions at 300°C on a hydrophobic surface (n-type silicon substrate). The inset illustrates the direction of hysteresis. Annealing adds positive charge, inducing a positive horizontal shift in the higher temperature curves. The metal work function (corresponding to $V_{FB}$ in the absence of fixed charge) is equal to +0.0075 V, with respect to the substrate.
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The C-V curve comparison for a hydrophobic surface, shown in fig. 3.30, reveals a negative initial flatband shift, with respect to substrate bias. Annealing at 500°C shows a positive shift, and we expect the fixed charge polarity to change at a certain temperature. Once more, the influence of $D_{it}$ on the capacitance is minimal in the as-deposited case, and annealing leads to a further reduction.

![Figure 3.31: Fixed charge (a) and interface trap densities (b) for the HfCl$_4$ precursor, with depositions at 300°C on a hydrophobic surface. Lower $Q_f$ is probably a result of the reduction in Cl impurities due to the higher deposition temperature. $D_{it}$ behavior is similar to the 200°C-grown samples.](image)

The $Q_f$ and $D_{it}$ values are shown in fig. 3.31. Measurements of as-deposited samples revealed a lower fixed charge value, compared to the 200°C-grown samples with the same type of surface preparation, which is in agreement with expectations. Higher temperature anneals lead to increasingly positive charge, but an increase in $D_{it}$ must be avoided, to ensure good passivation of $n$ and $n^+$ surfaces. Our measurements indeed reveal low interface trap densities after annealing up to 500°C, but crystallization in the oxide layer may cause a reduction in carrier lifetimes at higher temperatures. Interestingly, the $D_{it}$ value at 500°C is the lowest registered. The results are consistent from one measurement to another, with low variation in between measured devices (standard deviation of ~ 6% of the average value). This would contradict the idea that a hydrophobic surface creates more interface traps. The reduction in $D_{it}$ may be due, in this case, to the crystal grain size in the HfO$_2$ films. In section 3.2.2, we noticed that crystal grains form in the as-deposited films and annealing leads to an increase in lateral grain size. It is possible that very large grains would lead to a reduction in the number of interface traps, due to the lateral spreading of their periodic structures, which would leave fewer interface irregularities. Alternatively, the relatively high H concentration may play a role, in conjunction with the crystallization of the layers. By restructuring the atoms within the film to form crystal grains, it is possible that atomic H is more easily released, thus aiding in surface passivation more than in the films showing lower crystallinity.

As-deposited, the samples show high hysteresis, which is reduced by annealing. Higher temperatures appear to be more suited for reducing charge trapping. There is also an apparent correlation between negative oxide charge and high $V_{FB}$ shifts, similar to the HyALD case and the one for HfCl$_4$ deposited at 200°C. This is illustrated in fig. 3.32.
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HfO$_2$ films deposited on a hydrophilic surface produced curves of the type shown in fig. 3.33. An annealing dependency very similar to the hydrophobic case is observed. Thermal treatment induces a shift which indicates a net addition of positive charge.

The $Q_f$ and $D_{it}$ values are presented in fig. 3.34. Fixed charge follows an identical trend to the hydrophobic scenario, but the numerical values are slightly lower. This is probably a result of the more uniform film growth within the first few ALD cycles, which leaves fewer unsatisfied Hf bonds. The interface trap density is relatively low for all annealing temperatures and shows a minimum at 400°C. This can be seen directly in the measured conductance curves of fig. 3.35, where the peak around 0.75 V vanishes.

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Figure 3.34: Fixed charge (a) and interface trap densities (b) for the HfCl$_4$ precursor, with depositions at 300°C on a hydrophilic surface. The OH-terminated surface ensures a more uniform oxide growth during the first few cycles, reducing the interface charge created by segregation of Cl impurities.

Figure 3.35: Conductance curve comparison, showing the difference between samples annealed at 300°C and at 400°C (n-type silicon substrate). The conductance peak generated by interface traps disappears at the higher temperature, indicating lower $D_{it}$. 

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Samples annealed at all other temperatures show this peak. $D_{it}$ is measured at the voltage corresponding to the peak, even at 400°C, where no such peak exists, to ensure consistency in the measurements. The hysteresis seen in the C-V curves is relatively constant, at around 90 mV, as seen in Fig. 3.36. Annealed samples show slightly lower values, but no significant trend can be identified.

![Figure 3.36: Average flatband voltage shift due to hysteresis for HfO$_2$ films deposited using the HfCl$_4$ precursor at 300°C on a hydrophilic surface. All values are around 90 mV, with no apparent trend corresponding to the different processing conditions.](image)

3.5 Measurement conclusions

As a quick conclusion to our layer characterization results, we can emphasize the large range of values achieved for both $Q_f$ and $D_{it}$. The organic, HyALD precursor produced layers with very high $D_{it}$, preventing proper fixed charge determination. The metal halide HfCl$_4$ produced negatively-charged films, with lower $D_{it}$. The negative charge was revealed to be a result of negative impurities (in this case Cl) segregating preferentially to the oxide-silicon interface. $D_{it}$ was generally reduced by annealing up to 400°C, with much lower values registered for the HfCl$_4$ precursor. The high $D_{it}$ measured for HyALD may be linked to plasma damage incurred during layer deposition via PEALD, which is not present in the case of thermal ALD using HfCl$_4$. We attribute the reduction in $D_{it}$ with higher temperature anneals, at least in part, to hydrogenation of the Si surface, which is ensured by the H contained in the as-deposited layers. Positive fixed charge was obtained for layers derived from HfCl$_4$, following high temperature anneals. However, annealing up to 500°C can also increase $D_{it}$, reducing passivation potential. In the next chapter, lifetime measurements are carried out, in order to determine the surface recombination velocity for each condition, which directly characterizes the quality of passivation that can be achieved.
Chapter 4

Investigation of passivation quality via lifetime measurements

4.1 Experimental methods for lifetime measurements

A direct evaluation of surface passivation quality is achieved by measuring the effective lifetime, described in section 1.3, of a passivated silicon wafer. Measurements can be done via a number of different methods, depending on the expected lifetimes. Techniques for recombination lifetime measurements include photoconductance decay (PCD), photoluminescence (PL) decay, surface photovoltage, free carrier absorption, electron beam induced current method and several others, which are all described in reference [45]. In our experiments, two methods based on photoconductance decay were used, which will be explained in the following paragraphs.

The photoconductance decay method is based on the optical generation of electron-hole pairs in the semiconductor sample and monitoring their recombination as a function of time. As the name of the method suggests, the excess carriers induce a change in the conductivity of the sample. The conductivity ($\sigma$) is defined in the following relation:

$$ \sigma = q(\mu_n n + \mu_p p) \tag{4.1} $$

where $\mu_n$ and $\mu_p$ are the mobilities of the electrons and holes, respectively, and $n$ and $p$ are their respective concentrations. If we assume that the average excess hole density is equal to that of electrons, $\Delta p = \Delta n$, the added conductance for the illuminated wafer can be expressed as [45]:

$$ \Delta \sigma = q \cdot \Delta n \cdot (\mu_n + \mu_p) \tag{4.2} $$

Long lifetimes are measured accurately using a Sinton Instruments WCT-100 lifetime tester, in the so-called transient mode. This measurement mode uses a very short light pulse to produce charge carriers, after which the decay of photoconductance in the silicon wafer is monitored, using a circular coil, which registers a proportional, induced voltage. The effective lifetime in this case is described by the following equation [49]:

$$ \tau_{eff} = \frac{\Delta n}{\Delta n dt} \tag{4.3} $$

Lifetimes are reported at an excess carrier density of $\Delta n = 10^{15}$ cm$^{-3}$. For lifetime values lower than 200 µs, the accuracy of the transient photoconductance decay method decreases, and measurements must be carried out differently [50]. We used the quasi-steady state photoconductance...
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(QSSPC) method, developed by Sinton et al in 1996\[51]\). Such measurements were carried out on the BT Imaging LIS-R1 system. The wafer is illuminated with a slowly decaying laser pulse, with a wavelength of 808 nm. The pulse decay must be long compared to the lifetime of the sample, in order to provide a slow variation in light intensity and recreate steady-state conditions. A comparison of the measured photoconductance in the transient mode and in the quasi-steady state mode is shown in fig. 4.1. In transient mode the illumination is quickly cut off, producing a very short light pulse. The carriers have a much longer decay than the illumination, determined by their effective lifetime. In contrast, during QSSPC measurements, the illumination is reduced much more slowly, leading to a photoconductance decay which is determined by the carrier generation rate.

![Figure 4.1: Comparison of the measured illumination and photoconductance, in the transient (a) and quasi-steady state (b) modes. The slower photoconductance decay for QSSPC measurements is due to the continued generation of carriers by the longer light pulse. Graphs re-plotted after Morato\[24].](image)

In steady-state conditions, carrier generation and recombination rates are equal. The quasi-steady state method recreates such conditions for a wider range of illumination intensities. In the quasi-steady state regime, the effective lifetime can be expressed as\[49\]:

$$\tau_{eff} = \frac{\Delta n}{G},$$  \hspace{1cm} (4.4)

where $G$ is the carrier generation rate (given in $m^2s^{-1}$). $G$ is illumination-dependent, such that absorption of light into the wafer needs to be determined. Its time-dependence is described by the following expression\[24\]:

$$G(t) = \frac{I(t)f_{abs}N}{W},$$  \hspace{1cm} (4.5)

where $I(t)$ is the illumination intensity, measured in suns, $f_{abs}$ is the fraction of absorbed light, $N$ is the flux of photons in solar light with an irradiance of 1 sun (in $m^2s^{-1}sun^{-1}$), and $W$ is the thickness of the wafer (in m). Since all required parameters can be determined through measurement, the effective lifetime can be calculated, using eq. (4.4).

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4.2 Comparing passivation quality via surface recombination velocity

As mentioned in section 1.3, the effective lifetime of a wafer includes contributions from both its bulk and its surface:

\[
\frac{1}{\tau_{\text{eff}}} = \frac{1}{\tau_{\text{bulk}}} + \frac{1}{\tau_{\text{surf}}} \tag{4.6}
\]

Therefore, in order to analyze the effect of passivating oxides at the silicon surface, we need to calculate the surface recombination velocity, \(S_{\text{eff}}\). In order to extract \(S_{\text{eff}}\) from an effective lifetime measurement, we must first determine the value of \(\tau_{\text{bulk}}\). A semi-empirical relation for n-type silicon was derived from lifetime measurements of float zone silicon with very low defect levels, as shown by Honsberg and Bowden[6]:

\[
\frac{1}{\tau_{\text{bulk}}} = (\Delta p + N_D)(1.8 \cdot 10^{-24}N_D^{0.65} + 3 \cdot 10^{-27} \Delta p^{0.8} + 9.5 \cdot 10^{-15}) \tag{4.7}
\]

This enables the determination of an approximate bulk lifetime value, given only the concentration of donors, \(N_D\) (\(\text{cm}^{-3}\)), and the concentration of excess carriers, \(\Delta p\) (\(\text{cm}^{-3}\)). In practice, the Cz silicon wafers used by us have higher defect densities than the FZ wafers used in the model, meaning eq. (4.7) provides an overestimation of the bulk lifetimes. This results in an underestimation of the surface lifetime, providing an upper limit to the surface recombination velocity. As a result, we can expect slightly more optimistic values than those calculated in this report.

A second equation is required to approximate the surface lifetime, in relation to the surface recombination velocity. The approximation

\[
\tau_{\text{surf}} = \frac{W}{2S_{\text{eff}}} \tag{4.8}
\]

was given in section 1.3. This expression is accurate to within 4%, for wafers with very high bulk lifetimes and/or a well-passivated surface[52]. For wafers with poorer surface passivation, a more general expression is required:

\[
\tau_{\text{surf}} = \frac{W}{2S_{\text{eff}}} + \frac{1}{D} \left( \frac{W}{\pi} \right)^2 \tag{4.9}
\]

Here, \(D\) represents the minority carrier diffusion coefficient, which we determined using the application provided by Honsberg and Bowden[6]. The expression provides better than 5% accuracy over the complete range of so-called normalized surface recombination velocities (\(S^*\)), defined in reference [52] as:

\[
S^* = \frac{S_{\text{eff}}W}{D} \tag{4.10}
\]

However, when surface recombination velocities are very high (\(S_{\text{eff}} \to \infty\)), the surface lifetime contribution depends only on the diffusion coefficient and wafer width, and \(S_{\text{eff}}\) determination is not possible via eq. (4.9).

By reporting surface recombination velocities in place of lifetimes, we are able to compare passivation quality on different types of wafer. In our experiments, the CMOS-type wafers have a much higher bulk quality than the PV-type ones, while also being much thicker and having a polished surface (as opposed to a textured one). Therefore, the bulk lifetime is much longer for CMOS-type samples and the wafer surface has a lower impact on the effective lifetime.
Consequently, much higher lifetimes are measured for CMOS-type wafers. The effective surface recombination velocity is independent of the wafer shape or bulk quality, only providing insight into the surface contribution to $\tau_{eff}$. In this case, the effect of Auger recombination at highly-doped surfaces is also included in the surface lifetime $\tau_{surf}$. A comparison of similarly passivated CMOS and PV wafers will therefore reveal how surface texturing and doping affect the final passivation quality achieved via ALD oxide deposition.

### 4.3 Lifetime measurement results

In this section we report the surface recombination velocities achieved through ALD HfO$_2$ deposition using the two precursors, on CMOS and PV-type wafers. This provides insight into the effect of fixed charge and interface trap densities measured in the previous chapter. While samples created from CMOS-type wafers provide a general understanding of the passivation capabilities of the HfO$_2$ layers, the PV wafer samples reveal the applicability of the material in solar cell structures with an n$^+$ FSF. Not all deposition conditions were used for PV-type samples, due to the difficulty of processing thin, semi-square wafers on the Polygon ALD system. In order to assess the passivation quality achieved with HfO$_2$, the results are compared with those extracted from reference samples, which use industry-standard materials.

#### 4.3.1 Reference samples

Both n-type CMOS samples and PV-type samples with an n$^+$ FSF were passivated using reference materials. For the low-doped, n-type, CMOS case, Al$_2$O$_3$ was chosen, since it has been shown to provide good passivation for both float zone and Cz silicon surfaces [53, 54]. Al$_2$O$_3$ was deposited on n-type CMOS wafers ($n \approx 2.9 \cdot 10^{14}$ cm$^{-3}$), using a thermal ALD process (TMA + H$_2$O), at 200°C, using the Polygon 8200 system. Both hydrophobic and hydrophilic surfaces were passivated and post-deposition anneals were carried out, in the same temperature range as for the HfO$_2$ samples. The results are shown in fig. 4.2.

Al$_2$O$_3$ is known to contain a large amount of negative fixed charge [53], which can lead to the creation of an inversion layer at the silicon surface. Additionally, high hydrogen content aids the passivation of interface traps, providing very good chemical passivation. As a result, surface recombination values lower than 20cm/s were recorded for all annealing temperatures, with the best case scenario of just under 0.5 cm/s achieved for samples annealed at 500°C. Consequently, we looked to achieve $S_{eff}$ values in the range of 0.5 cm/s to 20 cm/s for the low-doped CMOS wafers.

Good passivation of n$^+$ surfaces is achieved with SiO$_2$/SiNx stacks for high efficiency solar cell structures such as n-PERT and p-PERL [26]. This material stack was used as a reference in our experiments for textured PV-type wafers with an n$^+$ FSF (120 $\Omega$/sq). SiO$_2$ was grown during the dry oxidation process undergone by the wafers after the POCl$_3$ diffusion step which creates the n$^+$ region. The resulting SiO$_2$ layer is around 25 nm thick. SiNx was deposited via PECVD, to a thickness of approximately 65 nm, at a temperature of 440°C. This resulted in surface recombination velocities between 5 cm/s and 12 cm/s, with an average value of approximately 9 cm/s, which was set as the target value for HfO$_2$ layers grown for PV-type samples.
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Figure 4.2: Surface recombination velocities extracted for n-doped \( n \approx 2.9 \times 10^{14} \text{ cm}^{-3} \) CMOS-type silicon wafers passivated with 10 nm of Al\(_2\)O\(_3\). Both hydrophobic and hydrophilic surfaces were prepared. High temperature anneals lead to very low \( S_{\text{eff}} \) values (below 1 cm/s). \( S_{\text{eff}} \) values showed standard deviations lower than 0.1 cm/s.

4.3.2 HyALD precursor

Both CMOS and PV-type samples were prepared using the HyALD precursor. HfO\(_2\) layers were deposited on hydrophobic surfaces only. Electrical measurements, discussed in section 3.4.1, revealed very high \( D_{\text{it}} \) values as-deposited and after a 300°C anneal. Consequently, for the CMOS samples at these conditions, the effective lifetime is very low (below 20 µs). This translates to a very high value of \( S_{\text{eff}} \). As a result, the surface lifetime contribution becomes independent of the surface recombination velocity, as the \( \frac{W_{\text{eff}}}{2S_{\text{eff}}} \) term in eq. (4.9) goes towards zero. In this case, we can only assume that the surface recombination velocity tends towards infinity, as its precise determination becomes impossible with the relations presented in section 4.2. The \( S_{\text{eff}} \) values are shown in fig. 4.3.

At higher annealing temperatures, the decrease in \( D_{\text{it}} \), seen in fig. 3.22b, leads to a reduction in \( S_{\text{eff}} \), such that its contribution to the surface lifetime becomes non-negligible. The slight \( Q_f \) trend seen in fig. 3.22a suggests that higher annealing temperatures lead to an increase in positive fixed charge. This should lead to an improvement in \( S_{\text{eff}} \) provided that the chemical passivation is still reasonable at the higher annealing temperature.

The data for PV-type samples is shown in fig. 4.4. Due to the lower bulk lifetimes of the lower resistivity PV wafers and their lower thickness, the surface contribution to the effective lifetime becomes more important in this sample category. As a result, the value of \( S_{\text{eff}} \) can be calculated even in the high \( D_{\text{it}} \) cases, under as-deposited and 300°C annealing conditions. HfO\(_2\) layers of 5 nm, 10 nm, and 15 nm were deposited. The values are averaged from two samples per condition. Exceptions occurred for the 15 nm layers annealed at 400°C and 500°C, where one sample had similar \( S_{\text{eff}} \) values to all other conditions, while the other showed much lower passivation quality, leading to the increased result shown in the figure.

It is immediately apparent that surface passivation is of low quality, due to the high \( S_{\text{eff}} \) values, compared to those for SiO\(_2\)/SiNx. However, the recombination velocities are reduced, in comparison with the CMOS samples. This may be due to the degradation of the CMOS-type
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Figure 4.3: Surface recombination velocities extracted for n-doped (~ 2.9 · 10^{14} \text{cm}^{-3}) CMOS-type wafers passivated with 10 nm of HfO_2. The \( S_{ee} \) values for as-deposited and 300°C-annealed samples cannot be calculated using eq. (4.9), because the effective lifetime is practically independent of \( S_{ee} \). Therefore, \( S_{ee} \) is considered infinite, which is in accordance with the results from section 3.4.1. Reduction of \( D_{it} \) due to annealing at higher temperatures leads to lower \( S_{ee} \), but good passivation is still not achieved. The standard deviations for 400°C and 500°C are lower than 35 cm/s.

samples over time, as the annealing and measurements were carried out after a longer post-deposition period than for the PV-type samples. Additionally, the n-n^+ junction, present in the PV wafers, leads to a reduction in minority carriers at the surface. This ensures reduced recombination, despite the additional Auger contribution. Nevertheless, the passivation quality provided by the HyALD-derived ALD HfO_2 films is very poor. In agreement with our observations in section 3.4.1, a possible explanation for this is the presence of plasma damage, sustained by the layers during deposition. Moreover, a non-negligible Cu and K contamination of wafers was detected via total reflectance X-ray fluorescence (TXRF) studies. The metal particles can be detrimental to effective lifetimes, providing recombination centers at the wafer surface. Additionally, at high temperatures, the contaminants can diffuse within the wafer bulk, constituting defects, which reduce bulk lifetimes, increasing the impact of surface recombination on the effective lifetimes. This can be corroborated by controlled contamination studies. However, such extensive studies were not carried out, and our limited data can only point to contamination that occurred either during transport between the production and measurement facilities, or during surface preparation, prior to the ALD process.

4.3.3 HfCl_4 precursor at 200°C

The investigations of HfO_2 layers deposited using HfCl_4 at 200°C were carried out for both hydrophobic and hydrophilic surfaces, on CMOS-type samples. For PV samples, only hydrophobic surfaces were prepared. In fig. 4.5 we present the results for CMOS-type samples, giving a comparison between the two surface types. The standard deviation of the data shown is lower than 1 cm/s for all values, with a few exceptions. The standard deviation is slightly higher, more precisely 1.3 cm/s for the as-deposited samples, and almost 6 cm/s for the 500°C-annealed, hydrophobic case.
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Figure 4.4: Surface recombination velocities extracted for PV-type, textured samples with an n+ FSF, passivated with 5 nm, 10 nm, and 15 nm of HfO$_2$. $S_{\text{eff}}$ values are much higher than those of the reference samples, but lower than those of the CMOS samples, from fig. 4.3.

For the HfCl$_4$ precursor, much lower $S_{\text{eff}}$ values are extracted than in the HyALD case, for all annealing conditions. The values are comparable to those achieved with the reference Al$_2$O$_3$ samples. Both hydrophobic and hydrophilic surfaces are similarly well passivated, with slightly lower variation in the hydrophilic case. This is most likely connected to the lower variation of fixed charge, observed in fig. 3.28a, compared to fig. 3.25a.

Figure 4.5: Surface recombination velocities extracted for CMOS-type samples, passivated with 10 nm of HfO$_2$, using HfCl$_4$, at 200°C deposition temperature. A comparison is offered between layers grown on hydrophobic and hydrophilic surfaces. $S_{\text{eff}}$ values are comparable to those obtained with Al$_2$O$_3$.

The low $D_{it}$ values observed in fig. 3.25b and fig. 3.28b ensure good chemical passivation of the silicon surface, while the negative fixed charge favors the formation of an inversion layer, providing low recombination velocities. The relatively high $S_{\text{eff}}$ for as-deposited layers on hydrophilic surfaces is most likely a consequence of the somewhat higher $D_{it}$, which leads to increased
recombination at the created bandgap states. The fact that, for the hydrophobic case, the $D_{it}$ value is also higher before annealing, further supports this assumption. At 500°C annealing, in the hydrophobic case, we register a large increase in $S_{eff}$. This is most likely a result of the crystallization of the HfO$_2$ layer.

![Figure 4.6: Surface recombination velocities extracted for PV-type samples with an n$^+$ FSF, passivated with 5 nm, 10 nm, and 15 nm of HfO$_2$, using the HfCl$_4$ precursor, at 200°C deposition temperature. Layers were grown on hydrophobic wafers. A considerable decrease in $S_{eff}$ is registered at high annealing temperatures, possibly due to the addition positive fixed charge to the oxide layer.](image)

Similar to the HyALD case, PV wafers were passivated by 5nm, 10nm, and 15 nm thick HfO$_2$ layers using HfCl$_4$ at 200°C deposition temperature. The extracted recombination velocities are shown in fig. 4.6. As mentioned in section 4.2, our method of extraction for $S_{eff}$ does not correct for increased recombination due to the Auger effect in the n$^+$ FSF region. Moreover, we expect $D_{it}$ values to be higher than the ones measured from our electrical samples, due to the increased roughness of the textured wafer surfaces. As a result, very high surface recombination velocities were registered in as-deposited conditions. The data was once again extracted from two samples per condition, with the exception of 600°C annealing, where only one sample was available. Differences between samples at the same conditions were lower than 100 cm/s, with the exception of the 5 nm layers in the as-deposited state, where a difference of approximately 160 cm/s was registered.

The reduction of $S_{eff}$ after annealing at temperatures above 400°C indicates that the Auger contribution is of lower importance. The trend observed for $Q_f$ in fig. 3.25a suggests that annealing at temperatures outside our standard range (i.e. above 500°C) may further increase the positive fixed charge content of the HfO$_2$ layers. The lower recombination velocities achieved at 600°C further support this idea. The overall trend that we observe for $S_{eff}$ is probably due to the combined effect of reducing $D_{it}$ and shifting $Q_f$ towards higher positive values. We notice a decrease in $S_{eff}$ for thicker HfO$_2$ layers, especially after higher temperature anneals. This may be a consequence of the variable size of crystal grains in the films with increasing temperature. In very thin layers, the grain dimensions quickly become comparable to the layer thickness, creating recombination sites at the interface, wherever grain boundaries occur. In thicker layers, higher temperatures or longer annealing times would be required for the grain boundaries to reach the interface. As a result, interface traps are not created by the grain boundaries, such that lower recombination velocities are extracted.
4.3.4 HfCl$_4$ precursor at 300°C

For HfO$_2$ layers deposited at 300°C using HfCl$_4$, only hydrophobic surfaces were prepared for lifetime investigations. Since no significant or essential difference was registered between the two surface types in the electrical measurements from section 3.4.3, this investigation should provide sufficient insight into the expected trends for surface recombination for both scenarios. In other words, because the trend in fixed charge content is the same for layers deposited at 300°C on both hydrophobic and hydrophilic surfaces, and differences in $D_{it}$ are lower than for layers deposited at 200°C (see fig. 3.25, fig. 3.28, fig. 3.31, and fig. 3.34), we do not expect any significant differences between the samples prepared with H-terminated and OH-terminated surfaces. Moreover, only CMOS-type samples were prepared, due to processing restrictions on the ASM Polygon 8200 ALD system. The maximum standard deviation was 2.1 cm/s, while the values at 300°C and 400°C were closer, with only a 0.6 cm/s deviation.

![Figure 4.7: Surface recombination velocities extracted for CMOS-type samples, passivated with 10 nm of HfO$_2$, at 300°C deposition temperature. The observed trend is similar to the one for 200°C-deposited layers, but $S_{eff}$ values are somewhat higher.](image)

The surface recombination values are presented in fig. 4.7. We recognize a trend similar to the one seen for HfO$_2$ deposited at 200°C using HfCl$_4$, which suggests that the same mechanisms are responsible for changes in $S_{eff}$ with annealing temperature for both cases. Overall, recombination values are increased, compared to the 200°C case, probably due to the crystallization of the oxide layer even in the as-deposited state (see section 3.2.2). The shift in optimal annealing temperature is probably also a consequence of increasing layer crystallization at higher temperatures, coupled with a relatively low $D_{it}$ at 300°C. However, observations made from fig. 3.31 would suggest that a 500°C anneal should provide the best passivation, due to relatively high positive fixed charge and very low $D_{it}$. It is evident from fig. 4.7 that this is not the case. As a result, we may assume that an additional mechanism exists, which works to increase $S_{eff}$ values at 500°C.

Overall, passivation quality is similar to that achieved with Al$_2$O$_3$ on CMOS-type wafers, with $S_{eff}$ values between 10 cm/s and 22 cm/s, although better performance is achieved with layers deposited at 200°C.
CHAPTER 4. INVESTIGATION OF PASSIVATION QUALITY VIA LIFETIME MEASUREMENTS

4.3.5 Discussion

The surface passivation achieved with the two HfO$_2$ precursors is highly variable. Very high $D_{it}$ leads to high recombination at the silicon surface in the case of the HyALD metal-organic precursor, while depositions of HfO$_2$ from HfCl$_4$ result in much better performance, with 200$^\circ$C providing passivation on par with Al$_2$O$_3$ on the n-type CMOS samples. Passivation of PV-type samples on par with the standard SiO$_2$/SiN$_x$ layer stack was not achieved in our experiments, although an optimistic decrease in surface recombination was observed at high temperatures.

An important fact to note is that passivation layers containing negative fixed charge can lead to low surface recombination velocities on n-type and n$^+$ silicon substrates, through creation of an inversion layer. As explained in section 1.3, although long lifetimes are achieved, this is not the desired case for solar cell operation, since it induces injection level dependencies. Consequently, the ideal situation would be one in which the oxide fixed charge is positive, combined with a sufficiently low $D_{it}$, such as for the PV samples with 200$^\circ$C-deposited HfO$_2$, annealed at 500$^\circ$C and 600$^\circ$C (fig. 4.6). However, the achieved $S_{ef}$ is still significantly higher than the value achievable with the SiO$_2$/SiN$_x$ reference. Annealing at even higher temperatures may lead to lower recombination velocities, provided that the fixed positive charge continues to increase. Positive fixed charge was measured for HfCl$_4$-derived layers, deposited at both 200$^\circ$C and 300$^\circ$C, when annealed at 400$^\circ$C or 500$^\circ$C.

We have carried out limited experiments with a third hafnium precursor, specifically tetra-kis(ethylmethyldiamino)hafnium (TEMAH), with promising results. Depositions took place via a thermal process (TEMAH + H$_2$O, at 250$^\circ$C). Surface recombination velocities as low as 1.9 cm/s on n-type, 9.2 cm resistance PV-type wafers (chemically polished) were achieved. For n$^+$ surfaces, a value of 13.7 cm/s was obtained on wafers with a similar base resistance, after creation of the front surface field. Electrical measurements revealed a relatively high positive fixed charge for the deposited layers, which should ensure good field effect passivation, while also registering $D_{it}$ values comparable, if not lower than those measured for layers deposited using HfCl$_4$. These results are shown in fig. 4.8.

![Figure 4.8: Fixed charge (a) and interface trap densities (b) for the TEMAH precursor, with depositions at 250$^\circ$C on a hydrophobic surface. High positive $Q_f$ and low $D_{it}$ lead to promising surface passivation results.](image)

We experienced a setback for the TEMAH experiments due to the fact that the ALD process for this precursor was not fully optimized. This led to large non-uniformities over the sample surfaces and low thickness control. Nevertheless, the results provide an optimistic perspective towards passivation for both n and n$^+$ surfaces, provided that the deposition process and post-
deposition treatments can be optimized to produce higher quality layers.

An additional factor, which could potentially increase passivation quality, is the addition of a SiN_x capping layer. This is usually done for the front side of solar cells, due to the material's anti-reflective and passivation functionality. It has been shown that SiN_x capping can improve the quality of surface passivation for materials such as Ta_2O_5[55] and SiO_2[56]. It would be interesting to investigate the effects of SiN_x in the case of HfO_2 as well, since it is known to contain positive fixed charge and a large amount of hydrogen, which could help passivate any defects in the HfO_2 layer and/or any unsatisfied Si bonds at the wafer surface[57, 58], while also providing an additional contribution to field effect passivation.

Finally, the ALD deposition method may influence the structure of the deposited layers, as we have pointed out in section 3.4.1. Plasma processes increase the risk of damaging the surface during deposition, due to high energy particles colliding with the sample surface. This creates defects in the deposited film, which may lead to increased D_{it} and poor passivation. An alternative would be to utilize a less aggressive, thermal process for deposition and investigate whether D_{it} is reduced (which would support the plasma damage hypothesis), or not (in which case other deposition parameters can be modified in order to improve performance of the deposited HfO_2 passivating layers). Optimization of the plasma deposition process accordingly may lead to improved passivation, using the HyALD precursor.

In conclusion, although in our experiments HfO_2 passivation has led to surface recombination velocities ranging from very bad to very good, solar cell applications require a match between a chosen surface type and annealing temperature, and good surface passivation. Although very low recombination velocities were achieved with HfCl_4, the negative fixed charge is not optimal for solar cells with an n-type or n^+ surface. Improvements to passivation can be made through post-deposition anneal optimization and capping of the HfO_2 layers. Other options include optimization of the deposition process parameters or the use of different precursors. Overall, HfO_2 is a promising material for Si surface passivation due to its diverse range of achievable electrical and physical properties.
Chapter 5

Conclusions

5.1 HfO$_2$ as passivation material

HfO$_2$ has been proposed as a new material fit for solar cell passivation, due to its proven effectiveness in similar applications for MOSFET technology and its versatility, given by the large range of obtainable material properties. In this thesis, we have analyzed the passivation capabilities of this oxide, towards possible future integration in high efficiency solar cell designs, with n-type silicon surfaces.

HfO$_2$ was deposited via thermal and plasma enhanced ALD, from two main precursors. Post-deposition thermal treatments were applied, in an attempt to improve the characteristics of the oxide layers, and to investigate their adaptability for specific passivation situations.

The analysis of HfO$_2$ consisted of TEM studies for physical characterization, chemical characterization via both EDS and ERD, electrical characterization through C-V and G-V measurements, and direct analysis of surface passivation quality, via effective lifetime measurements and surface recombination velocity calculations. The quantities which formed the basis of our analysis were the oxide fixed charge density, $Q_f$, connected with field effect passivation, the density of interface traps, $D_{it}$, which determines chemical passivation potential, and the effective surface recombination velocity, $S_{ef}$, which describes the overall passivation quality resulting from the oxide deposition and post-processing. An investigation of the optical performance of HfO$_2$, in comparison with Al$_2$O$_3$ and SiO$_2$ was also carried out, via Monte Carlo simulations. This has further supported the suitability of HfO$_2$ as a passivating material, predicting good anti-reflective properties, on a similar level with the other oxides, if not better.

Investigations of the chemical composition of the HfO$_2$ layers revealed the presence of hydrogen in considerable quantities. This is known to lead to improved passivation, due to hydrogenation of the Si surface and passivation of defects in both the film and the wafer bulk. We believe that hydrogenation most likely occurs above 400°C, which is most evident in the case of layers deposited using the HyALD precursor.

Physical characterization revealed the presence of an interfacial SiO$_2$ layer, which may be a consequence of low surface coverage in the incipient phase of the ALD process, due to steric hindrance. An alternative explanation would be that the hydrophobic silicon surface is oxidized during manipulation in air, prior to HfO$_2$ deposition, or the layer can simply form spontaneously, due to diffusion of O and Si atoms at the interface. The presence of the layer affects the quality of the Si/HfO$_2$ interface, which is a determining factor for the electrical characteristics of the oxide. To ensure a high quality interface, the layer can be chemically grown, creating a hydrophilic surface, which also aids nucleation and growth during the initial stages of ALD deposition.
CHAPTER 5. CONCLUSIONS

Our measurement results show that deposition of HfO$_2$ using the HyALD precursor, via plasma enhanced ALD, leads to very high $D_{it}$ (up to $4.5 \cdot 10^{12}$ cm$^2$eV$^{-1}$), which has proven detrimental to surface passivation quality. Annealing aids in the reduction of $D_{it}$, but the low negative fixed charge is not optimal for this passivation scheme. However, a decrease in surface recombination velocity was registered due to the reduced $D_{it}$. One possibility is that damage incurred by the HfO$_2$ layer during deposition, due to high energy particles in the O$_2$ plasma, is a source of interface traps. At 400°C, the hydrogen contained in the layer passivates both interface and bulk defects, but ultimately the achievable $S_{eff}$ values remain high. If the plasma damage hypothesis is correct, then a further $S_{eff}$ reduction may be achieved if the plasma process can be optimized to reduce damage to the layer. Alternatively, HfO$_2$ layers can be deposited via a less aggressive, thermal process.

The HfCl$_4$ precursor was used to deposit HfO$_2$ layers at 200°C and 300°C. We found negative fixed charge in the layers, resulting from Cl impurities, which segregate preferentially towards the interface. Higher temperatures lead to lower Cl content, and consequently lower fixed charge. A hydrophobic surface also provides lower fixed charge, increasing the potential for symmetric passivation of n and p-type surfaces simultaneously. The lowest recombination values were extracted for 200°C-deposited layers, in which case surface passivation was aided by the creation of an inversion layer.

Throughout our analysis, we found that $D_{it}$ plays a very important role, constituting a limiting factor for surface passivation. As such, even in the case of relatively low-doped (CMOS) wafers, high $D_{it}$ such as in the as-deposited, HyALD-derived layers, leads to very high $S_{eff}$. Consequently, it is important to optimize the HfO$_2$ deposition process and post-deposition treatments, irrespective of precursor, such that the number of interface traps is reduced below $5 \cdot 10^{11}$ cm$^2$eV$^{-1}$, as we determined an apparent correlation between $D_{it}$ in this range and low surface recombination velocities. Hydrogenation of the interface can provide a further boost to passivation quality, either through forming gas anneals, or by release of atomic H from the oxide layer.

We described the mechanism of fixed charge formation in the HfO$_2$ layers, as a consequence of the difference in coordination numbers between silicon and hafnium (section 3.2.3). This creates unsatisfied bonds at the interface, which introduce a net positive charge. Segregation of Cl impurities, in the case of HfCl$_4$, serves as a compensating mechanism, and overcompensation gives a net negative charge. The absence of chlorine or other negative halide species from organic precursor molecules means that the positive charge should remain uncompensated.

Our results show the large range of HfO$_2$ properties, which can be achieved by applying a simple post-deposition thermal treatment, or by modifications in the deposition process. HfO$_2$ has thus proven to be a versatile candidate for silicon surface passivation and further investigations are well warranted, due to this optimistic outcome.

5.2 Open questions

There are an abundance of options for increasing passivation quality, one reason for this being the number of different metal precursors which are available. In this sense, we have seen that TEMAH can be used to provide excellent passivation, given its positive fixed charge and low obtainable $D_{it}$.

Further improvements may be brought on by SiNx capping, which can aid field effect passivation via addition of positive fixed charge, while also providing anti-reflective properties to the solar cell structure, improving efficiency by optical means. SiNx is also known to contain a large amount of hydrogen, which can aid in passivating interface and bulk defects in both the oxide layer and the silicon wafer.
A more thorough investigation of the variation of HfO$_2$ characteristics with annealing temperature is of great interest, since interesting effects were observed around 500°C, such as the addition of positive fixed charge in the HfCl$_4$-derived layers. Investigations at higher temperatures should provide valuable insight into the limitations of this process. A more precise variation in annealing temperature may also be interesting. One example of this was obtained during our brief study of the TEMAH precursor, where a very large decrease in recombination velocity occurred at 350°C, whereas none of our other studies included such intermediate temperatures. As a result, the optimal annealing temperature may have been omitted from our analysis.

Okamoto et al.\cite{59} managed to achieve flatband voltage control for HfO$_2$ films, by incorporating La atoms, to create La$_2$O$_3$ or HfLaO, effectively modifying the oxide fixed charge density. Such control over the oxide properties can dramatically improve the passivation capabilities of the material and its adaptability to a wider range of surface conditions. Similarly, incorporation of Al$_2$O$_3$ into the structure, in the form of HfAlO, was proven to increase the thermal stability of HfO$_2$, suppressing crystallization for 5 minute annealing up to 900°C\cite{60}. Such developments can be used to broaden the applicability of HfO$_2$ passivation to a wider range of solar cell technologies, including those requiring high temperature processing.

Once optimal passivation is achieved for a desired application, implementation of ALD HfO$_2$ in a working solar cell is a necessary step, in order to evaluate the real performance parameters achievable by replacement of standard passivation layers. Ultimately, the introduction of HfO$_2$ passivation into high efficiency solar cell technology at the industrial level is dependent on the availability of high-throughput deposition methods. Spatial ALD provides a solution for this, allowing up to thousands of wafers to be processed per hour\cite{61}. HfO$_2$ integration into spatial ALD solutions requires careful selection of precursors, and fine tuning of processing conditions, such that excellent passivation is achieved, while ensuring safe and efficient depositions. Reduction of costs is another important factor to take into account for industrial implementation.

As a closing remark, we must reiterate the general idea which one can surmise from the theoretical and experimental data presented in this thesis: HfO$_2$ is a very versatile material, capable in theory of providing surface passivation for a wide range of applications. Its implementation in MOSFET technology as gate oxide is a demonstration of its applicability. The somewhat different requirements of the photovoltaic industry will require further optimization of the material’s deposition and post-processing conditions, towards increased solar cell efficiencies. The research presented in this thesis is only a small step towards industrial implementation of HfO$_2$, in a future powered by renewable energy.
Bibliography


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## Optical simulation results

Table A.1: Results of the optical simulations from section 3.1. The maximum achievable photocurrent is highlighted in bold, in each situation.

<table>
<thead>
<tr>
<th>SiN&lt;sub&gt;x&lt;/sub&gt; thickness (nm)</th>
<th>HfO&lt;sub&gt;2&lt;/sub&gt; 15 nm</th>
<th>Al&lt;sub&gt;2&lt;/sub&gt;O&lt;sub&gt;3&lt;/sub&gt; 10 nm</th>
<th>Al&lt;sub&gt;2&lt;/sub&gt;O&lt;sub&gt;3&lt;/sub&gt; 25 nm</th>
<th>SiO&lt;sub&gt;2&lt;/sub&gt; 25 nm</th>
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<td></td>
<td>Photocurrent (mA/cm&lt;sup&gt;2&lt;/sup&gt;)</td>
<td>Error (mA/cm&lt;sup&gt;2&lt;/sup&gt;)</td>
<td>Photocurrent (mA/cm&lt;sup&gt;2&lt;/sup&gt;)</td>
<td>Error (mA/cm&lt;sup&gt;2&lt;/sup&gt;)</td>
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Appendix B

Methods of flatband voltage determination

The most precise way to extract $V_{FB}$ is to compare the measured curve with an ideal curve, where no fixed charge is present. In order to do this, precise knowledge of all MOS capacitor parameters must be available, to be able to simulate the corresponding C-V curve. There are many ways to introduce errors given this restriction, but one clear example is that of the difficulty in determining the oxide permittivity. First of all, the growth of HfO$_2$ is linked to the presence of a SiO$_2$ interfacial layer, as described in section 3.2.2. Since the SiO$_2$ interlayer is not always grown in a controlled fashion, this leads to variations in the equivalent permittivity of the experimental oxide stack. Moreover, the permittivity of HfO$_2$ also varies with respect to annealing temperature, due to changes in the film structure. Another parameter which can introduce uncertainties in calculations is the device area. The precision with which this value can be determined is greatly dependent on the contact deposition method. The thickness of the dielectric layer is also an uncertain quantity. Annealing can cause changes in the layer density, such that the thickness must be determined for each separate situation. Moreover, non-uniformities in the layer thickness may further increase the difficulty of its precise determination. As a result, the calculated flatband voltage is a very uncertain value, unless the MOS structure parameters can be very precisely controlled.

Another widely used method involves calculating the flatband capacitance and graphically determining the corresponding voltage from the measured C-V curve. This requires knowledge of the substrate doping density, which can easily be determined via wafer resistivity measurements. The relations used to calculate the flatband capacitance, considering an n-type substrate are the ones shown in eq. (B.1) and eq. (B.2), similar to those given by Winter et al for p-type silicon[46].

First, the Debye length is calculated for the substrate:

$$\lambda_D = \sqrt{\frac{\epsilon_{Si} \cdot kT}{qN_D \cdot q}}, \quad (B.1)$$

where $\epsilon_{Si} = 1.04 \cdot 10^{-10}$ F/m is the electrical permittivity of silicon and $N_D$ is the dopant concentration. The flatband capacitance can then be determined from the following relation:

$$\frac{1}{C_{FB}} = \frac{1}{C_{ox}} + \frac{1}{C_{Si}} = \frac{1}{C_{ox}} + \frac{\lambda_D}{\epsilon_{Si}}. \quad (B.2)$$
where the second term on the right side of the equation represents the semiconductor capacitance, given by the depletion layer with a width of $\lambda_D$. The application of the flatband capacitance method is limited to high frequency C-V measurements\cite{46}.

Our C-V measurements were done at a relatively low frequency (500 Hz - 1 kHz) a third method was used for $V_{FB}$ determination. The method, proposed by Winter et al, approximates the flatband voltage with the bias at which an inflection point occurs in the C-V curve\cite{46}. This point can be easily extracted by numerically calculating the second derivative of the measured curve and graphically determining the solution to the following equation:

$$\frac{d^2C}{dV^2} = 0.$$ \quad (B.3)

The inflection point method reportedly provides an accurate approximation of the flatband voltage for sufficiently thin films and low enough interface trap densities\cite{47}. A comparison between this and the flatband capacitance method for our measurements revealed an average difference in $V_{FB}$ of less than 20 mV, producing an acceptable fixed charge density difference of well under $5 \cdot 10^{11}$ cm$^{-2}$ for the samples with the highest $D_{it}$ values. All films deposited for C-V characterization had a thickness of 10 nm, which is well within the acceptable range of thickness, of up to 55 nm. The inflection point method has the advantage of not requiring any prior knowledge of the MOS structure, since the flatband voltage is determined directly from the C-V curve. Taking all this into consideration, and also noting that a precise determination of fixed charge values is not necessary to achieve a deeper understanding of the electrical properties of HfO$_2$, the chosen $V_{FB}$ determination method was the inflection point method.
Appendix C

EDS maps of HfO₂ layers

In this section, the chemical composition of the deposited HfO₂ films is shown, in EDS maps, as described in section 3.2. The maps are enlarged, in order to show the signal produced by each atomic species as well as possible (species such as C and N were barely detected in our samples). For the HyALD precursor, the maps for Hf, Si, O, C and N are shown, while for the HfCl₄ precursor only the Cl maps are added, as proof that its distribution is similar to the one described by Sreenivasan et al[22]. The Hf, O and Si distribution is qualitatively identical for the two precursors, such that it is only shown for the HyALD case.

C.1 HyALD precursor
Figure C.1: EDS maps of the Hf (green), O (red) and Si (cyan) content of the HfO$_2$-passivated Si surface imaged in Fig. 3.5. Hf presence in the substrate is due to the ion beam milling of the sample in a top to bottom direction. The interfacial layer is marked with a yellow box. It is most likely a SiO$_2$ layer, formed during the first cycles of the ALD process. The maps correspond to the as-deposited sample. Hf, O and Si content is similarly distributed after 400°C and 500°C anneals.
APPENDIX C. EDS MAPS OF HfO$_2$ LAYERS

Figure C.2: EDS maps of the N impurity content of the HfO$_2$-passivated Si surface imaged in fig. 3.5. The maps correspond to as-deposited (a), 400°C-annealed (b), and 500°C-annealed samples (c). The signal is almost undetectable, suggesting that the concentration of N is less than 1 at. % under all annealing conditions.
Figure C.3: EDS maps of the C impurity content of the HfO$_2$-passivated Si surface imaged in fig. 3.5. The maps correspond to as-deposited (a), 400°C-annealed (b), and 500°C-annealed samples (c). The signal is almost undetectable, suggesting that the concentration of N is close to, or less than 1 at. % under all annealing conditions.
C.2 HfCl$_4$ precursor
Figure C.4: EDS maps showing Cl impurity distribution in the Si substrate - HfO$_2$ thin film structure. The maps correspond to as-deposited (a), 400°C-annealed (b), and 500°C-annealed samples (c). A low intensity peak in the signal is registered in the interface layer, which is marked with a red box. Cl atoms are also detected in the bulk of the HfO$_2$ film.

Characterization of Hafnium Oxide Thin Films for Applications in High Efficiency c-Si Solar Cells
Appendix D

Tables of measurement averages

D.0.1 $Q_f$ and $D_{it}$ values

Table D.1: Average $Q_f$ and $D_{it}$ values, measured for the HyALD and HfCl$_4$ precursors, under all conditions discussed in chapter 3.

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<th>Precursor</th>
<th>Deposition temperature</th>
<th>Surface type</th>
<th>Annealing condition</th>
<th>$Q_f$ left (cm$^{-2}$)</th>
<th>$Q_f$ right (cm$^{-2}$)</th>
<th>$D_{it}$ (cm$^{2}$eV$^{-1}$)</th>
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<td>-6.27E+11</td>
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### D.0.2 $S_{\text{eff}}$ values

Table D.2: Average surface recombination velocities, determined for CMOS-type samples. The calculated Si bulk lifetime was $\sim 45$ ms.

<table>
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<th>Precursor</th>
<th>Deposition temperature</th>
<th>Surface type</th>
<th>Annealing condition</th>
<th>$S_{\text{eff}}$ (cm/s)</th>
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<td>$\infty$</td>
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Table D.3: Average surface recombination velocities, determined for PV-type samples. The calculated Si bulk lifetime was $\sim 19$ ms.

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<th>Annealing condition</th>
<th>$S_{\text{eff}}$ (cm/s)</th>
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