MASTER

Systematic design of a two-stage 30GHz MMIC power amplifier suitable for LMDS architecture terminated by coplanar matching networks, complemented employment of IF termination

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Two-stage 30GHz MMIC
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complemented employment of IF termination

J.P.B. Janssen

12 August 2005
Abstract

There is a growing need for high data-rate communication, which implies applications on higher frequencies with higher bandwidths. One of those applications is called Local Multipoint Distribution Service (LMDS), which is a first-mile-last-mile solution according to the IEEE802.16 standard.

LMDS is a fixed high speed wireless data network, which operates above 20GHz. A LMDS network has a point-to-multipoint topology, where the base-station is placed on a high building, with the subscriber-stations in the line of sight. The application recommends different complex modulation techniques for different distances, namely QPSK, 16-QAM and 64-QAM.

The goal of this project is the employment of a top-down approach for a systematic design for a two-stage power amplifier, which meets the specifications according to the IEEE802.16c standard, which covers this application. A fully implementation of the input matching (from 50Ω), interstage matching and output matching (to 50Ω) has to be realized, as well as the bias circuits.

The designed power amplifier operates at high frequency (30GHz). The main trade-off is linearity versus efficiency, because input-power back-off is needed, due to the complex modulation scheme. Simultaneously improvement of linearity and efficiency must be investigated through different methods e.g. IF-termination and input mismatch.

The used top-down approach has improved the speed up of the design procedure, through taking the right step at the right moment. Distinction is made in several (semi) independent building blocks, which are designed independently to reduce the complexity per design step.

Load-pull simulations are done based on an orthogonal approach, assuming that proper harmonic termination can be achieved independently. So every harmonic impedance is optimized separately and verified after every step.

The required output power single-tone and QAM is achieved, with the required linearity performance:

- Single tone: $P_{del} > 22$dBm, namely 23dBm
- 64QAM: $P_{del} > 15$dBm, namely 17dBm

The linearity requirements of the IEEE802.16c standard are achieved, when simulated with ADS 2003c:

- Error vector magnitude is 1.5%.
- Output spectrum is inside the defined spectrum mask.
On the other hand 25% efficiency with the 64-QAM signal determined in advance, is not achieved, because the focus was on linearity and the power amplifier operation is kept in class A.

Pseudo input mismatch is employed to improve the linearity of the input-stage, which has improved the error vector magnitude (EVM).

The results of the designed power amplifier shows that error vector magnitude is not dependent only on the output-stage, because the AM-to-PM distortion of the input-stage also has a significant impact on the final EVM.

Coplanar waveguides are used to match the power amplifier. Electro magnetic simulations are necessary to really understand the advantages of coplanar waveguide technology of the used process in microwave frequency design.

For the power amplifier designed in this project, IF-termination has no influence on error vector magnitude, due to the crest-factor of a complex modulated signal. When using IF-termination the biasing and DC decoupling of the circuit is critical. It has to be taken into account from the start of the design.
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Chapter 1

Introduction

1.1 Project background

There is a growing need for high data-rate communication, which implies applications on higher frequencies with higher bandwidths. One of those applications is called Local Multipoint Distribution Service (LMDS), which is a first-mile-last-mile solution according to the IEEE802.16 standard (see reference [19], [21]).

![LMDS network topology](image)

Figure 1.1: LMDS network topology ([21]).

LMDS is a fixed high speed wireless data network, which operates above 20GHz. A LMDS network has a point-to-multipoint topology, where the base-station is placed on a high building, with the subscriber-stations in the line of sight. The application recommends different complex modulation techniques for different distances, namely QPSK, 16-QAM and 64-QAM (see figure 1.1 and reference [19]).

1.2 Design goal

The goal of this project is to design a two-stage power amplifier suitable for LMDS applications. The linearity specifications have to be according to the IEEE802.16c standard, which covers this application. Other specifications are enumerated below:

- Operating frequency: 30GHz
• Output power 1-tone: 22dBm
• Efficiency 1-tone: 45%
• Efficiency 64-QAM: 25%
• Topology: 2-stage cascade

A fully implementation of the input matching (from 50Ω), interstage matching and output matching (to 50Ω) has to be realized, as well as the bias circuits.

The simulation results are got with Agilent Advanced Design System (ADS) version 2003c. A note has to be made for the error vector magnitude calculations. In the last month an error in this ADS calculation is found, so the EVM calculations will be done afterwards with ADS 2004a, which has correct EVM calculation.

1.3 Problem description

The designed power amplifier operates at high frequency (30GHz). The main trade-off is linearity versus efficiency (see reference [2], [8], [11]), because input-power back-off is needed, due to the complex modulation scheme.

Simultaneously improvement of the linearity and efficiency must be investigated through different methods e.g. IF-termination (see reference [11], [15], [16]) and input mismatch (see reference [12]).

1.4 Design approach

A systematic top-down approach is employed to upgrade the design speed of the power amplifier. A distinction is made in several (semi) independent building blocks, which are designed separately to reduce the complexity per design step.

Load-pull simulations are done based on an orthogonal approach, assuming that proper harmonic termination can be achieved independently. So every harmonic impedance is optimized separately and verified after every step.

1.5 Technologies in use

Two transistor models are available for this project and are verified and investigated:

• Omnic DH15IB Indium Phosphide based Double Heterojunction Bipolar Transistor
• Omnic D01PH Gallium Arsenide based Pseudomorphic High Electron Mobility Transistor

Due to the high frequency operation the matching networks are designed with coplanar waveguide technology, because of the good magnetic separation (see reference [7]).
1.6 Thesis overview

First of all the operation environment of the designed power amplifier is discussed. A 64-QAM modulator and demodulator are presented in chapter 2. In chapter 3, theoretical topics on power amplifier design is discussed, with some ADS simulations and a start of systematic design approach is presented. Here after the available transistor models are discussed in chapter 4. First some theory and afterwards some simulation results to verify the models. Subsequently a design procedure to design a two-stage power amplifier is discussed and the results of the design are presented chapter 5. Afterwards a method to improve the linearity-efficiency trade-off is presented in chapter 6. Finally the drawn conclusions and the recommendations are presented.
Chapter 2

IEEE 802.16c standard

This chapter describes the specifications of the standard IEEE 802.16c and the modulation technique 64-QAM.

2.1 Introduction

The designed power amplifier has to operate in an environment according to the IEEE 802.16c standard, called Air Interface for Fixed Broadband Wireless Access Systems. A first-mile-last-mile application according to this standard is local multipoint distribution service (LMDS).

LMDS is a broadband wireless point-to-multipoint communication system operating above 20GHz (depending on geographic distribution and required licenses). This system can be used to provide communication services e.g. digital two-way voice, data, Internet and video services.

Some specifications of the IEEE 802.16 standard and the properties of the modulation technique are presented in this chapter, as well as a designed modulator and demodulator.

2.2 Properties

This section describes some properties of the standard and the related topics of Quadrature Amplitude Modulation scheme (modulation and demodulation).

2.2.1 Modulation

The standard describes three modulations techniques (see reference [19]), which provides different bit-rates. The table below gives an overview of the possible modulation schemes and the corresponding bandwidths and bit-rates.

<table>
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<th>QPSK</th>
<th>16-QAM</th>
<th>64-QAM</th>
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<td>Channel bandwidth</td>
<td>20 MHz</td>
<td>25 MHz</td>
<td>28 MHz</td>
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<tr>
<td>Bit-rate</td>
<td>44.8 Mbit/s</td>
<td>89.6 Mbit/s</td>
<td>134.4 Mbit/s</td>
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The used modulation technique in this project is 64-QAM, because the restrictions, specially according to linearity are most critical.
2.2.2 General QAM system

Quadrature amplitude modulation (QAM) is a combination of amplitude modulation (AM) and phase shift keying (PSK). It is a quadrature modulation, because it uses two signals in quadrature (90° phase shift). In general a QAM signal can be described with formula 2.1 (see reference [4]).

\[ s(t) = x(t) \cos \omega_c t - y(t) \sin \omega_c t \]  
(2.1)

Another useful representation is the magnitude and phase of the signal:

\[ g(t) = x(t) + jy(t) = I(t) + jQ(t) = R(t)e^{j\Theta(t)} \]  
(2.2)

with magnitude:

\[ R(t) = \sqrt{I^2(t) + Q^2(t)} \]  
(2.3)

and phase:

\[ \Theta = \arctan \frac{Q(t)}{I(t)} \]  
(2.4)

The baseband waveforms I and Q are represented by:

\[ x(t) = \sum_n x_n h_1(t - \frac{n}{D}) \]  
(2.5)

\[ y(t) = \sum_n y_n h_1(t - \frac{n}{D}) \]  
(2.6)

Where \( D \) is the bit-rate "R" divided by the number of bits "I" for coding I and Q and \( (x_n, y_n) \) denotes the number of the permitted \( (x_i, y_i) \) values during the symbol time that is centered on \( t = nT = n/D \) seconds. And \( h_1 \) is the pulse shape that is used for each symbol.

A constellation diagram is a useful representation of the I and Q signals. Figure 2.1 shows an ideal constellation diagram of a 64-QAM signal. The dots represent the symbols.

![Figure 2.1: Constellation diagram of 64-QAM](image)
2.2 Properties

Modulator

Modulation is in principle a multiplication of two signals, with the goal to represent the data and to shift the transmitted signal into another part of the frequency spectrum. In most cases to a higher part of the spectrum.

As mentioned before, a quadrature modulated signal consists of two orthogonal signals. These signals have to be multiplied with a carrier signal, which is $90^\circ$ phase shifted in one case. Finally the signals are added and a QAM signal is generated. Figure 2.2 shows a general representation of a QAM modulator.

![Figure 2.2: General quadrature modulator](image)

Demodulator

Demodulation is the opposite of modulation, but with almost the same operation. In this case the QAM signal is multiplied with the carrier frequency. Before the multiplication the carrier is split into two orthogonal signals. After multiplication the signal is low-pass filtered to eliminate the summation components. The baseband components $I(t)$ and $Q(t)$ are left. In figure 2.3 a generalized schematic of a QAM demodulator is presented.

![Figure 2.3: General quadrature demodulator](image)

Raised-cosine filter

Intersymbol interference (ISI) occurs when the receiver of a digital transmission system cannot distinguish reliably between individual symbols received. It is produced...
by distortion, which is manifested in the temporal spreading and consequent overlap of individual pulses. At some point the transmitted symbols by the transmitter cannot be recovered in the receiver and information is lost.

To prevent ISI a raised-cosine filter is used (see reference [4]). The impulse response of this filter has the characteristic that zero-crossings occur exact on one symbol-time (see figure 2.4(a)). The absolute transmission bandwidth of the filter can be represented as:

\[ B_T = \left( \frac{1 + r}{l} \right) R \]  

(2.7)

Where "r" is the roll-off factor of the filter, "l" is the number of bits for coding and "R" the bit-rate.

![Fig. 2.4: Impulse responses of a RRC and a SRRC.](image)

Mostly raised-cosine filters are used as well as in the transmitter as in the receiver. When this is the case, two square root raised-cosine filters (SRRC) are used.
in the transmitter and one in the receiver. Together they fulfil the raised-cosine characteristic.

### 2.2.3 QAM and peak-to-average ratio

The peak-to-average ratio, also known as Crest factor, is the ratio between the peak instantaneous power and the average power.

Instantaneous power is defined as:

\[ p(t) = v(t) \cdot i(t) \]  

(2.8)

Average power is defined as:

\[ \langle p(t) \rangle = \langle v(t) \cdot i(t) \rangle = \frac{1}{N} \sum_{i=1}^{N} p_i(t), \]  

(2.9)

with \( n \) the number of samples

The crest-factor has an impact on the gain-compression curve of an amplifier. This impact is shown with some simulation results of the designed power amplifier with 1-tone, 2-tones and 64-QAM signals in figure 2.5. It can be seen that the compression occurs earlier with 2-tones simulation and even more with 64-QAM.

![Figure 2.5: Effect of the Peak-to-average ratio on power compression.](image)

### 2.2.4 QAM and linearity

Linearity of a QAM system is an important factor for the accuracy of recovering the data. It is also an important parameter for spectral contamination. Error vector magnitude (EVM) and adjacent channel power ratio (ACPR) are much used parameters to describe the linearity of a complex modulation system.

**Error vector magnitude**

To recover the data in the right way the data must be transmit correct. Error vector magnitude (EVM) measurement is a method to measure the accuracy of the transmission, which can be graphically explained with a constellation diagram. It
The EVM is defined as the square root of the ratio of the average error vector power to the average reference power expressed in percentage (see reference [13]). The calculation of the error vector is done for each symbol. The measured symbol, denoted as $Z_n$, consists of a signal which has been corrupted by noise, frequency offsets and other impairments. The ideal reference signal, denoted as $S_n$, is a signal free of noise whose magnitude has been normalized to one. $\hat{Z}_n$ is the modified version of the measured signal where the frequency, absolute phase, absolute amplitude and chip clock timing have been selected to have the minimum error vector. Each complex element is represented as $S_n$, $Z_n$ and $\hat{Z}_n$ respectively. The instantaneous error vector is obtained by subtracting the ideal reference from the modified version of the measured waveform. The root mean square value of the EVM is defined in equation 2.10.

\[
EVM_{RMS} = \sqrt{\frac{\sum_{n \in N} |\hat{Z}_n - S_n|^2}{\sum_{n \in N} |S_n|^2}} \tag{2.10}
\]

### Adjacent Channel Power Ratio

The adjacent channel power ratio (ACPR) is the ratio between the power in the fundamental zone ($P_{\text{out}}$) and the power of the lower and upper adjacent channel bands ($P_{\text{LA}}$ and $P_{\text{UA}}$) (see reference [8]).

\[
ACPR = \frac{P_{\text{out}}}{P_{\text{LA}} + P_{\text{UA}}} \tag{2.11}
\]

Figure 2.7 gives a representation of a power spectrum. The dashed part is the input spectrum with $\omega_0$ as center frequency and the lined part is the output spectrum after non-linear amplification. The upcoming upper and lower channels is called spectral regrowth, which is due to non-linear amplification of the signal.
2.3 Specifications

Relevant specifications according to the IEEE802.16c standard are described in this section (see reference [19], [21]).

2.3.1 Modulation accuracy

The allowed Error Vector Magnitude (EVM) in percentage versus modulation technique is given in the table below. As shown in the table, the higher the modulation density the more critical the EVM. This because the points in the constellation diagram are closer to each other at higher densities.

<table>
<thead>
<tr>
<th>Modulation technique</th>
<th>QPSK</th>
<th>16-QAM</th>
<th>64-QAM</th>
</tr>
</thead>
<tbody>
<tr>
<td>EVM</td>
<td>10%</td>
<td>3%</td>
<td>1.5%</td>
</tr>
</tbody>
</table>

2.3.2 Spectrum mask

There are different spectrum masks specified for IEEE802.16c standard. In Europe the mask according to the European Telecommunication Standards Institute (ETSI) is relevant and most critical, which is the guideline to determine the used mask. There are different versions specified (A, B and C) according to the ETSI (see reference [20]). The most critical mask is determined out of the different versions. The determined mask is shown in figure 2.8.

2.3.3 Power level

According to the standard the RMS power level of the transmitter, at maximum power level setting, has to be equal or higher than 15dBm at the antenna port.
2.4 64-QAM modulation in ADS

This section describes the designed 64-QAM modulator in ADS, which creates the environment for the power amplifier and presents the simulation results.

2.4.1 Designed modulator

As explained in section 2.2.2 QAM modulation is a multiplication of two orthogonal signals with a carrier. The modulator designed in ADS (figure 2.9) makes a 90° phase shift of the Q-data to create the orthogonal signals. The building blocks used for this modulator are mentioned below.

- Pseudo random bit-generators (to generate the I and Q data)
- Voltage source with single frequency (to generate the RF signal)
- Ideal amplifiers (to normalize the RMS value of the I and Q data to 1)
- Pulse generators (to provide the upsampling)
- Ideal multipliers (to provide the upsampling)
- square root raised-cosine filters (to filter the sampled I and Q data)
- I-Q multiplier (To multiply the I and Q data with the RF signal)
- Output impedance

The symbol-rate, generated by the pseudo random bit-generators is set on the bandwidth of the system, which is 28MHz. The bit-generators generate different amplitudes to create 8 different levels. The values of the amplitudes are determined in the way that it's not possible to get the value of zero.

The ideal amplifiers have a gain to normalize the RMS-value of the I and Q data to 1. So the output power is only dependent on the RF voltage source. This makes it easier to define the power and to use it with power sweeps.
Simulation of the modulator in ADS is dependent on the time-step of the simulator. Therefore important building blocks are the pulse generators and the ideal multipliers. These provide the upsampling of the I and Q data with $2^3$-time-step. This upsampling is necessary to see more than only the signal bandwidth.

The square root raised-cosine filters are set on the bandwidth of 28MHz. This means the filter response has a zero-crossing on every symbol-time. This prevents intersymbol interference (ISI). The delay of these filters is set on 15 times a symbol-time because the ads-model is not working properly with a lower delay time.

At the output of the modulator there is a terminal to create the right impedance, so the modulator can be matched optimally to another device.

![Diagram of QAM modulator in ADS](image)

**Figure 2.9: The designed QAM modulator in ADS**

### 2.4.2 Simulation results of the modulator

This subsection describes simulation results of the QAM modulator, which are relevant to power amplifier design.

**Constellation**

As mentioned before a QAM signal can be presented in a constellation diagram. In figure 2.10 the constellation diagrams of the ideal I and Q signals and the output of the QAM modulator are presented. The dot at (0,0) of the output constellation is a result of the way of upsampling, where interpolation of zeros is used.
Figure 2.10: Constellation diagrams (with different scaling) of the 64QAM modulator

Spectrum

The spectrum of the output of the modulator is shown in figure 2.11. Since the envelope simulator of ADS is used, the center frequency is normalized to zero, so the spectrum is shown as a function of frequency offset. The bandwidth is 28 MHz.

![Spectrum](image)

Figure 2.11: Output spectrum of the modulator

Power distribution

The power distribution of the QAM signal is an important fact for power amplifier design. Power distribution can be expressed as a probability density function (PDF), which indicates the probability that the signal has a determined power. The normalized PDF of the designed QAM modulator is shown in figure 2.12 and can be calculated in ADS with equation 2.12.

\[
PDF = \text{histogram} \left( \frac{P_{\text{instantaneous}}}{P_{\text{average}}} \right)
\]  

(2.12)

Crucial for linearity is the upper edge of the PDF histogram (±6 dB above average).
The symbols with these powers, the same as the corner dots in a constellation diagram are most sensitive for gain compression.

![Figure 2.12: The probability density function](image)

2.5 64-QAM demodulation in ADS

This section describes the 64-QAM demodulator in ADS.

2.5.1 Designed demodulator

In section 2.2.2 the basic principle of QAM demodulation is described. The designed demodulator first down-convert the signal to baseband with a phase shift in the Q-pad. After this, the I and Q signals are filtered with SRRCs and down sampled. A multi level signal is created.

The demodulator consists of the next building blocks.

- A phase shifter (to provide a 90° phase shift)
- Ideal multipliers (to provide down conversion and down sampling)
- Voltage sources with single frequency (to generate the RF signal)
- Square root raised-cosine filters (to filter the I and Q data)
- Pulse generators (to provide the downsampling)

First there is made a −90° phase shift to separate the I and Q data. Next the two data-pads are multiplied with the carrier frequency to bring the signal back to baseband.

Again the root raised-cosine filters are set on the bandwidth of 28MHz. Together with the SRRC-filters in the modulator, these filters fulfil the raised-cosine transfer function. Because of the same reason as in the modulator the delay time of these filters is set on 15-symbol-time.

Also this simulation is dependent on the time-step of the simulator. Therefore important building blocks are the pulse generators and the ideal multipliers. These provide the downsampling of the I and Q data with $2^3$-time-step.
2.5.2 Simulation results of the demodulator

This subsection describes the simulation results of the designed 64QAM demodulator.

**Constellation**

To check if the output of the demodulator is correct a constellation diagram is generated in ADS. In figure 2.14 the constellation diagrams of the ideal I and Q signals and the output of the QAM demodulator are presented.

The dot at (0,0) of the output constellation is a result of the interpolation of zeros due to the upsampling and downsampling.

Notable is the difference in amplitude of both constellations. This is due to the upsampling, upconverting and downsampling, downconverting of the signal, which is are not compensated.

![Figure 2.14: Constellation diagrams (with different scaling) of the 64QAM demodulator](image)
2.5 64-QAM demodulation in ADS

Spectrum

The spectrum of the output of the demodulator is shown in figure 2.15. Also here the spectrum is shown as a function of frequency offset. The bandwidth is 28 MHz. In comparison with the spectrum of the modulator (figure 2.11) it can be seen that the transmission is ideal. There is no spectral regrowth.

Figure 2.15: Output spectrum of the demodulator
Chapter 3

Power amplifier theory

This chapter describes some theoretical aspects of power amplifier design.

3.1 Introduction

To give a better insight in power amplifier design some power amplifier and microwave theory is discussed here. This chapter is separated in four main parts. Small-signal, large-signal, matching and biasing, and a start for a systematic design approach.

3.2 Small signal

Microwave small-signal signal subjects are discussed in this section.

3.2.1 S-parameters

In the theory of network analysis two-port networks (figure 3.1(a)) can be specified completely with a set of four parameters. This set can be y-, z-, h- or ABCD parameters. In high frequency design or characterization these parameters are rarely used, because of the following problems at high frequencies (see reference [3]):

- Total voltages and currents are difficult to measure.
- In the measurement of these two-port parameters, short and open circuits are required. These are difficult to realize over a wide range of frequencies.
- Most active devices or circuits are not open or short circuit stable.

At high frequencies s-parameters (scattering parameters) are used to characterize a circuit. S-parameters are based on forward and reflected (scattered) traveling waves.

The voltages $V_1$ and $V_2$, and the currents $I_1$ and $I_2$ of a general two-port network (figure 3.1(a)) can be expressed in terms of traveling waves (see reference [1], [3]), like in the equations 3.1 to 3.4.

$$V_1 = V_1^+ + V_1^-$$  \hspace{1cm} (3.1)
Where the + and - superscripts refer to whether the traveling wave is going into or coming out of the two-port network and $Z_0$ is the characteristic impedance of the system.

When defining $s$-parameters the two-port of figure 3.1(b) gives a better representation.

To define the $s$-parameters the voltages are divided by $\sqrt{Z_0}$ where $a_1$ and $a_2$ are the incoming waves and $b_1$ and $b_2$ the reflected waves.

$$I_1 = \frac{V_{1}^+ - V_{1}^-}{Z_0} \quad \text{(3.2)}$$

$$V_2 = V_{2}^+ + V_{2}^- \quad \text{(3.3)}$$

$$I_2 = \frac{V_{2}^+ - V_{2}^-}{Z_0} \quad \text{(3.4)}$$

Figure 3.1: Two-port networks
Now defining the s-parameters:

\[ s_{11} = \frac{b_1}{a_1} \bigg|_{a_2=0} \]  
(3.9)

This is the input reflection coefficient with the output port terminated by a matched load \((Z_L=Z_0)\)

\[ s_{22} = \frac{b_2}{a_2} \bigg|_{a_1=0} \]  
(3.10)

This is the output reflection coefficient with the input port terminated by a matched load \((Z_S=Z_0)\)

\[ s_{12} = \frac{b_1}{a_2} \bigg|_{a_1=0} \]  
(3.11)

Forward transmission (insertion) gain with the output port terminated in a matched load

\[ s_{12} = \frac{b_1}{a_2} \bigg|_{a_1=0} \]  
(3.12)

Reverse transmission (insertion) gain with the input port terminated in a matched load

### 3.2.2 Smith-chart

The Smith-chart is a really useful graphic representation of impedances and admittances, mapped on a complex reflection coefficient plane (figure 3.2). The reflection coefficient plane \((\Gamma-plane)\) consists of circles of constant reflection and has a couple of interesting points:

- The left side is short circuit impedance.
- The right side is open circuit impedance.
- The center is the normalization impedance \((Z_0)\).

The Smith-chart consists of an impedance plane (figure 3.3(a)) with circles for the real part and arcs for the imaginary part and in the same way an admittance plane (figure 3.3(b)). Together they form the Smith-chart (figure 3.3(c)). The derivation of the Smith-chart from the \(\Gamma\)-plane is based on the relation of equation 3.13 (see reference [1]).

\[ \Gamma = \frac{Z - Z_0}{Z + Z_0} \]  
(3.13)

\(Z_0\) is the characteristic impedance of a reference impedance or transmission line (usual 50Ω). Mostly the Smith-chart is used in normalized form with \(Z_0\) as center. The normalized relation is:

\[ z = \frac{Z}{Z_0} = \frac{R + j \cdot X}{Z_0} = r + j \cdot x \]

\[ \Gamma = \frac{z - 1}{z + 1} \]  
(3.14)

The complete Smith-chart is given in appendix A.
3.2.3 Gain

When there is a matter of gain, mostly in low frequency design it is voltage gain. In high frequency design power gain is the most important gain, because maximum power transfer has to be reached. Power gain can be distinguished in different types (see reference [1]).

- Transducer power gain \( (G_T) = \frac{\text{power delivered to the load}}{\text{power available from the source}} \)

- Operating power gain \( (G_P) = \frac{\text{power delivered to the load}}{\text{power input to the network}} \)

- Available power gain \( (G_A) = \frac{\text{power available from the network}}{\text{power available from the source}} \)

\[
G_T = \frac{1 - |\Gamma_s|^2}{|1 - \Gamma_{IN}\Gamma_s|^2} \frac{|s_{21}|^2}{|1 - s_{22}\Gamma_L|^2} \frac{1 - |\Gamma_L|^2}{|1 - s_{22}\Gamma_L|^2} \\
G_P = \frac{1}{|1 - s_{11}\Gamma_s|^2} \frac{|s_{21}|^2}{|1 - s_{22}\Gamma_L|^2} \frac{1 - |\Gamma_L|^2}{|1 - \Gamma_{OUT}|^2} \\
G_A = \frac{1 - |\Gamma_s|^2}{|1 - s_{11}\Gamma_s|^2} \frac{|s_{21}|^2}{|1 - s_{22}\Gamma_L|^2} \frac{1 - |\Gamma_L|^2}{|1 - \Gamma_{OUT}|^2}
\]
3.2 Small signal

\[ \Gamma_{IN} = s_{11} + \frac{s_{12}s_{21}\Gamma_L}{1-s_{22}\Gamma_L} \]  \hspace{1cm} (3.18) \\
\[ \Gamma_{OUT} = s_{22} + \frac{s_{12}s_{21}\Gamma_s}{1-s_{11}\Gamma_s} \]  \hspace{1cm} (3.19)

Often the reverse transmission gain \( s_{12} \) is very small and can be neglected, so \( \Gamma_{IN} \approx s_{11} \) and \( \Gamma_{OUT} \approx s_{22} \).

3.2.4 Stability

Not every found impedance or admittance on de Smith-chart is suitable, because of stability of the circuit. Stability on the Smith-chart means that the reflection coefficients on the input and output have to be smaller than one. A factor, to see if the transistor is unconditionally stable is called the k-factor (see reference [1]). When the k-factor is larger than one, the transistor is unconditionally stable. If it is smaller than one than there is always an area on the Smith-chart which is potential unstable.

\[ K = \frac{1-|s_{11}|^2-|s_{22}|^2-|\Delta|^2}{2 \cdot |s_{12}s_{21}|} \]  \hspace{1cm} (3.20)

Where \( \Delta = s_{11}s_{22} - s_{12}s_{21} \) and \( |\Delta| < 1 \)

Another crucial stability parameter is \( B1 \), which has to be larger then 0 to let be the circuit unconditional stable.

\[ B1 = 1+|s_{11}|^2-|s_{22}|^2-|\Delta|^2 \]  \hspace{1cm} (3.21)

Stability can be visualized with stability circles on the Smith-chart. These circles represent the place were the reflection coefficient is equal to one. Stability circles can be calculated with formulas 3.22 for the input and 3.23 for the output. Where \( C_s \) and \( C_L \) are the centers of the source and load stability circles and \( r_s \) and \( r_L \) are the radii.
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Power amplifier theory

3.3 Large signal

Large signal design subjects are discussed in this section.

3.3.1 Power

In high frequency design there are different definitions of power. The most important are the power available from the source ($P_{AVS}$) and the power delivered to the load ($P_{del}$). These powers are calculated as follows (see reference [1], [2]).

$$P_{AVS} = \frac{V_{source}^2}{8 \cdot R_{source}} \quad (3.24)$$

$$P_{del} = \frac{V_{load}^2}{2 \cdot R_{load}} \quad (3.25)$$

3.3.2 Efficiency

An amplifier is a device which converts energy from an available source of power (DC-power) into signal energy, so to add power to an input signal. Therefore efficiency should be measured as added efficiency to the input signal.

There are two major definitions of efficiency, namely drain efficiency ($\eta$) and power added efficiency (PAE). Most used is power added efficiency, because it takes the power added to the input signal in mind, so the power gain ($G_p$).

$$\eta = \frac{P_{out}}{P_{DC}} \quad (3.26)$$

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} = \frac{P_{out}}{P_{DC}} \cdot (1 - \frac{1}{G_p}) \quad (3.27)$$

According to the conduction angle of a power amplifier, PA's can be classified in different generic classes depending on the power added efficiency. The table below shows the classes of "linear" power amplifiers and the maximum theoretical efficiencies (see reference [2]).

<table>
<thead>
<tr>
<th>Class</th>
<th>Conduction angle</th>
<th>Efficiency</th>
<th>Operation mode</th>
<th>Linearity</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>$2\pi$</td>
<td>$\leq 50%$</td>
<td>&quot;Linear&quot;</td>
<td>Good</td>
</tr>
<tr>
<td>AB</td>
<td>$\pi - 2\pi$</td>
<td>50% - 78.5%</td>
<td>&quot;Linear&quot;</td>
<td>Moderate</td>
</tr>
<tr>
<td>B</td>
<td>$\pi$</td>
<td>78.5%</td>
<td>&quot;Linear&quot;</td>
<td>Moderate</td>
</tr>
<tr>
<td>C</td>
<td>$0 - \pi$</td>
<td>$\leq 100%$</td>
<td>&quot;Linear&quot;</td>
<td>Poor</td>
</tr>
</tbody>
</table>
3.3 Linearity

Linearity is a direct trade-off of power added efficiency (PAE). Linearity caused by gain compression of the amplifier (AM-to-AM) and the produced phase shift of the amplifier (AM-to-PM). A consequence is that mixing products appear. Most critical are the odd order mixing products, because these mixing products fall direct into the signal band. Most significant is the third order harmonic, which produces the third order mixing products, because it has the most power.

In a complex modulation environment like 64-QAM, linearity aspects as EVM and spectral regrowth are critical, which are explained in chapter 2.

3.3.4 Load-pull

At the output the power amplifier has to deliver a specified power, with the best possible efficiency and linearity. These three are the main trade-offs in the design procedure of the output-stage of a power amplifier and are dependent of the load, which the transistor sees at the output. To find the optimal load, load-pull simulation has to be done.

In this simulation the load is changed in a specified area on the Smith-chart. The delivered power, efficiency and third harmonic component (important for linearity) can be shown on the simulated place on the Smith-chart.

In this project load-pull simulation is not done by changing the load impedance, but by changing the reflection coefficient (Γ). This way of simulating is much more time efficient than the built-in simulation of ADS, which changes the load impedance. The built-in simulation of ADS sweeps the impedances in horizontal lines over the Smith-chart and makes the impedance circles afterwards. The used simulation setup is simpler. It creates circles over the Smith-chart and the impedances can be seen directly. Also every part of the Smith-chart can be swept separately or can be avoided (see figure 3.5). The main reason is to simulate only stable regions in the Smith-chart and avoid the unstable regions. This can not totally be done with the build in simulation setup of ADS.

The impedance can be calculated directly from the found reflection coefficients, with formula 3.28.

\[ Z = \frac{1 + \Gamma}{1 - \Gamma} \cdot Z_0 \]  

3.3.5 Load-line

The DC load-line is the line in a \( I_d - V_{ds} \) plot, which connects \( I_{d,max} \) with \( V_{ds,max} \), and goes through the class A bias point (see reference [2]). The value is a first prediction of the needed load to provide the specified output power.

\[ P_{opt} = \frac{1}{2} \cdot V_{DC} \cdot I_{DC} \]  

\[ R_{opt} = \frac{V_{ds} - V_{knee}}{I_D} \]  

This first prediction can reduce the simulation time of the load-pull simulations a lot. The simulation can be targeted at that point, so less simulation points are necessary to determine the optimal load. The AC load-line is an ellips with the DC load-line as axis. The AC load-line shows were compression occurs.
3.4 Matching and biasing

Matching and biasing are two aspects, which are discussed here together. The reason is that these two aspects are mostly realized in the same circuit.

3.4.1 Principle and purpose

The purpose of matching is to create the right impedance at each side of the circuit. Transistors have to see a dedicated impedance to produce the right output power or to get the highest gain. On the other side the input and output of a system must be $50\Omega$ to get the lowest insertion loss when the system is connected to another system. Here for dedicated circuits have to be designed.

A matching network is mostly designed with the help of the normalized Smith chart, which is based on

$$\Gamma = \frac{z - 1}{z + 1} \quad (3.31)$$

The purpose of bias circuits is to keep the transistors in the right operation area, that is determined when the used transistor is characterized. On the other hand a bias circuit has to be an open circuit for RF power to provide minimum insertion loss.
3.4.2 Matching methods

Matching networks can be designed in several ways. ADS has a matching utility tool to design matching networks. The matching in this project is done manually to understand the matching principle in a better way.

Three methods are investigated and discussed here. These methods are discussed with the same approach, namely two element matching (see reference [1]). The output impedance of the output-stage of the designed power amplifier is matched to a 50Ω impedance.

![Diagram of two element approach](image)

(a) Lumped elements
(b) Transmission line with a capacitor

Figure 3.6: General two element approach full lumped and with use of transmission lines

Lumped elements

Lumped element matching uses building blocks like coils and capacitors. To match a circuit with lumped components the impedance is shift to the desired place on the Smith-chart over impedance and admittance circles/arcs, like in figure 3.6(a).

Graphically the target (like intermediate in figure 3.6) can be determined. The impedance difference in the start-point and target-point can be established, with the help of the impedance and admittance circles. The value of the needed inductance or capacitance can be calculated from the needed complex impedance.

Micro-strip lines

A micro-strip line is a thin metal line on a substrate with a metal layer on the other side of the substrate. A cross-section is shown in figure 3.7.

![Diagram of micro-strip line](image)

Figure 3.7: Cross section of a Micro-strip line
The characteristic impedance of a micro-strip line can be determined by some empirical formulas. It depends on the ratio of the width of the conductor \((W)\) and the height of the substrate \((h)\) which formula has to be used (see reference [1]). For example when assumed that \(W/h \geq 1\) then formula

\[
Z_{0,\text{microstrip}} = \frac{120\pi/\sqrt{\varepsilon_{\text{eff}}}}{W/h + 1.393 + 0.667 \cdot \ln(W/h + 1.444)} \tag{3.32}
\]

Where

\[
\varepsilon_{\text{eff}} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2} \left(1 + 12 \frac{h}{W}\right)^{-\frac{1}{2}} \tag{3.33}
\]

is valid.

When matching is done with micro-strip lines moving on the Smith-chart is done it terms of wavelengths in the micro-strip line over constant \(\Gamma\) circles. The wavelength in a micro-strip line is expressed like

\[
\lambda = \frac{\lambda_0}{\sqrt{\varepsilon_{\text{eff}}}} \tag{3.34}
\]

In this project, matching with micro-strip lines the combination of micro-strip lines and capacitors are used. Now in stead of using the impedance lines on the Smith chart, the reflection coefficient circles are used.

Coplanar waveguides

A coplanar wave-guide (CPW) is a micro-strip line with ground planes on each side of the transmission line. Because of the top ground planes the magnetic separation between the CPWs is good (see reference [7]). A cross-section is shown in figure 3.8.

![Cross section of a coplanar waveguide](image)

The characteristic impedance of a coplanar waveguide is dependent on the ratio of the width of the transmission line \((W)\) and the gaps \((G)\) to the adjacent ground planes (see reference [7] and [14]).

\[
Z_{0,\text{CPW}} = \frac{a}{b} = \frac{W}{W + 2G} \tag{3.35}
\]

When matching the length of the CPW is used to move on the Smith-chart. This length is expressed in terms of wavelengths through the CPW.

\[
\lambda = \frac{\lambda_0}{\sqrt{\varepsilon_{\text{eff}}}} \tag{3.36}
\]
3.5 Systematic design approach

A top-down, systematic design procedure is employed in this project in order to improve the design speed and to guarantee a correct designed power amplifier. This method contains several design steps, which can be considered as independent from each other. In this way the overall trajectory is divided into smaller steps.

Initially a two-stage power amplifier system can be separated in different (semi) independent building blocks, which are shown in figure 3.10. When employing a
systematic design procedure, these building blocks are designed independently. The main building blocks are enumerated below in right design order:

- **Output-stage**
  - Output power
  - Efficiency
  - Linearity

- **Input-stage**
  - Gain
  - Output power

- **Output matching network**
  - Match to 50Ω
  - Minimum insertion loss

- **Interstage matching network**
  - Provide the right impedances for both stages
  - Minimum insertion loss

- **Input matching network**
  - Match from 50Ω
  - Minimum insertion loss

- **Bias networks**
  - Minimum high frequency power loss

The power amplifier in this project is designed by specifications according to a standard. So the output-stage is designed initially, because this stage has to provide the needed output power and has the most impact on linearity. The procedure to design the output-stage is divided in smaller steps, which are explained in chapter 5.

The input-stage is designed to achieve maximum gain and to provide the right input power for the output-stage. When designing the input-stage the insertion by the interstage matching network has to be kept in mind.

The matching networks are designed finally. First the output matching is designed, because of it's influence on the performance of the system. Subsequently back to the input the interstage matching and input matching are designed. Due to the possible influence of the bias networks on the matching performance, the bias networks are introduced during the matching network design.
Chapter 4

Technologies and models

This chapter describes the for this project available technologies to design the power amplifier.

4.1 Introduction

The first target was to design a power amplifier in Indium Phosphide (InP) based Double Heterojunction Bipolar Transistor (DHBT) technology of GCS. Available was the InP DHBT technology of Omnic and by a coincidence also Gallium Arsenide (GaAs) based Pseudomorphic High Electron Mobility Transistor (PHEMT) technology of Omnic. Both models were verified and discussed in this chapter.

The simulations of these models were done with the biasing settings for the power amplifier, assumed that the power amplifier will be designed with the InP DHBT technology of GCS. This means the transistor has a breakdown voltage of 10V, so the supply voltage is chosen safe at 3.5V. This supply voltage is used for both Omnic transistors.

4.2 InP based DHBT

A double heterojunction bipolar transistor (DHBT) is a variant of the (n-p-n) bipolar transistor. Normally a bipolar transistor is made from one material (homojunction), whereas a DHBT is made from different materials to increase the efficiency and the cut-off frequency of the device.

A DHBT has a higher emitter efficiency and has higher speed and frequency capability, hence the DHBT is often used in microwave applications.

4.2.1 Basic principle

The base of a DHBT is made from different material than the emitter and the collector. The emitter and collector are made from wide band-gap materials, whereas the base is made from small band-gap material (see reference [5]). Less energy is needed to transport the electrons from the emitter to the collector and less losses are there due to recombination of electrons with holes. The latter is because the holes are closed in the base zone.
The cross-section of a DHBT is roughly the same as a bipolar transistor, there is a difference in material between the base and the emitter and collector. The positive (small band gap) base is made from Indium Gallium Arsenide (InGaAs) and the negative (large band gap) emitter and collector are made from Indium Phosphide.

The cross-section of the Ommic InP DHBT is given in figure 4.1.

![Cross section of the Ommic DHBT](image)

Figure 4.1: Cross section of the Ommic DHBT

### 4.2.2 Characteristics verification

The characteristics of the Ommic D15IB InP DHBT model are verified with simulations in ADS. The simulation results according to DC and AC characteristics are presented here. The size of the simulated transistor is according to the needed power for the power amplifier (see chapter 5).

**DC characteristics**

The DC characteristic of the DHBT is presented here. This characteristic is shown with the supply voltage of 3.5V as reference. Notable is the flatness of the curve.

![DC characteristic curve](image)

Figure 4.2: The $I_e$ versus $V_{be}$ curve of the Ommic InP based DHBT
AC characteristics

Important for the operating of the transistor is the cut-off frequency ($f_T$). The $f_T$ of the device is defined as the frequency where the magnitude of the current gain of the transistor is reduced to one under consideration that the output terminal of the transistor is short-circuit (see reference [10]).

The cut-off frequency is calculated with extrapolation of the slope of the $h_{21}$ (current gain) versus frequency curve.

$$slope = \frac{h_2 - h_1}{\log f_2 - \log f_1}$$

The simulation of $f_T$ is done with constant $V_{eb} = 0V$, because of the frequency dependency of the $C_{eb}$.

The $f_T$ versus $I_e$ is normalized, because the best current per $\mu m^2$ area has to be found to let operate the transistor in the best conditions, according to bandwidth.

![Graph](a) $f_T$ versus normalized $I_e$  (b) $f_T$ versus $V_{be}$

Figure 4.3: $f_T$ curves of the InP DHBT, done with extrapolation.

Another useful figure of merit is the maximum frequency of oscillation versus collector current or basis-emitter voltage. $f_{max}$ is defined by the frequency where the power gain of the transistor becomes equal to unity (see reference [10]).

The $f_{max}$ curve versus the normalized $I_e$ and $V_{be}$ is presented in figure 4.4.

![Graph](a) $f_{max}$ versus normalized $I_e$  (b) $f_{max}$ versus $V_{be}$

Figure 4.4: $f_{max}$ curves of the InP DHBT, done with extrapolation.

The ratio of $f_{max}$ over $f_T$ is typically 1.5 or 2 (see reference [10]). In this case the ratio is 5, which is disputable.
Stability

The input and output stability of the DHBT is investigated, because it is a very important fact for microwave transistors. This DHBT transistor is not unconditionally stable at 30GHz, because the k-factor=0.872.

As seen in figure 4.6 the output stability gives problems at lower frequencies. These impedances on the Smith-chart have to be avoided. According to figure 4.5 only some parts of the edges of the input has to be avoided to keep the input stable.

![Figure 4.5: DHBT input stability circles on different frequencies.](image)

![Figure 4.6: DHBT output stability circles on different frequencies.](image)

4.3 GaAs based PHEMT

A pseudomorphic high electron mobility transistor (PHEMT) is a variation of a HEMT. This device is familiar to the metal semiconductor field effect transistor (MESFET). It has a lot of different names:

- Heterojunction Field Effect Transistor (HFET).
- Modulation Doped Field Effect Transistor (MODFET).
- Two-Dimensional Electron Gas Field Effect Transistor (TEGFET)

This section gives a basic description of this technology.
4.3 GaAs based PHEMT

4.3.1 Basic principle

The cross-section of a HEMT looks like that of a MESFET (Metal-semiconductor FET), which is shown in Figure 4.7. A MESFET is a type of junction-gate FET (JFET). With the following differences (see reference [6]):

- The gate is a Schottky contact, which has a shorter gate-length. This gives a lower gate to channel capacitance and a shorter gate transit time.
- The common material of a MESFET is GaAs, which provides a higher electron mobility than silicon.

![Figure 4.7: Cross-section of a MESFET](image)

In a HEMT the electrons achieve a higher mobility than in a MESFET. The result is higher transconductance, lower noise and a higher frequency range. The difference in structure is the heterojunction instead of the normal doped channel.

The heterojunction consists of an n AlGaAs layer immediately under the gate, an undoped spacer layer and an undoped GaAs layer. The spacer is very thin in the order of a few tens of angstroms. The discontinuity in the band gaps of the AlGaAs and the GaAs causes a thin layer of electrons under the gate, at the interface between the undoped GaAs layer and the spacer. These electrons are closed in a GaAs well and have a very high mobility, because they are on discrete energy levels and can move "free".

![Figure 4.8: Cross-section of a HEMT](image)

The pseudomorphic HEMT or PHEMT uses an extra InGaAs layer between the n AlGaAs spacer and the GaAs layer. The resulting larger band gap gives more charge in the electron layer, which increases the transconductance and the output power. Because the InGaAs layer is unnaturally compressed this layer is called the pseudomorphic layer.

4.3.2 Characteristics verification

The characteristics of the Omnig D01PH 0.13µm PHEMT model are verified with simulations in ADS. The simulation results according to DC and AC characteristics
are presented here. The size of the transistor is according to the needed power for
the power amplifier (see chapter 5).

DC characteristics

The DC characteristic of the PHEMT is presented here. This characteristic is shown
with the supply voltage of 3.5V as reference.

AC characteristics

Also here the cut-off frequency and maximum frequency of oscillation are calculated
with extrapolation.

\[ \text{slope} = \frac{h_2 - h_1}{\log f_2 - \log f_1} \quad (4.2) \]

Since the PHEMT is a symmetrical device, \( V_{dg} \) is not forced to 0V.
The \( f_T \) versus \( I_d \) is normalized, because the best current per \( \mu \text{m} \) gate length has to be found to let operate the transistor in the best conditions.
4.3 GaAs based PHEMT

Figure 4.11: $f_T$ curves of the PHEMT, done with extrapolation.

The $f_{\text{max}}$ curve versus the normalized $I_d$ and $V_{gs}$ is presented in figure 4.12.

Figure 4.12: $f_{\text{max}}$ curves of the InP PHEMT, done with extrapolation.

In this case the ratio of $f_{\text{max}}$ over $f_T$ is 7, which is disputable again. The best results are got with bias settings according to the $f_T$ curves (see chapter 5).

Stability

Also the input and output stability of the PHEMT are investigated. At the operating frequency the PHEMT is not unconditional stable at 30GHz, because the k-factor=0.92. Also lower and higher frequencies are investigated on stability.

As seen in figure 4.14 the output stability gives problems at lower frequencies. These impedances on the Smith-chart have to be avoided. According to figure 4.13 only some parts of the edges of the input has to be avoided, to keep the input of the transistor stable.
4.4 Convergence

However the first idea was that the power amplifier will be designed in the InP DHBT process technology, the power amplifier is designed with the Omnic D01PH 0.13µm PHEMT process. The reason is that the InP DHBT model is not convergent in load-pull simulations of ADS, especially in the two-tone and 64-QAM simulations. The decision is made to design the power amplifier with the PHEMT model, because the duration of the project limited and the goal of the project is to design a power amplifier.
Chapter 5

Design procedure for a two-stage power amplifier

This chapter describes the used design procedure and results of the designed 2-stage power amplifier.

5.1 Introduction

In this project a two-stage power amplifier is designed. The properties of the power amplifier have to be according to the IEEE 802.16c standard which is explained briefly in chapter 2.

- Operating frequency = 30GHz
- Bandwidth = 28MHz
- Output power (single tone) = 22dBm
- Output power (64QAM) ≥ 15dBm
- Efficiency (64QAM) = 25%
- Error Vector Magnitude = 1.5%
- ACPR = See spectrum mask in chapter 2.

In this chapter the used design procedure is presented with the achieved simulation results.

5.2 Procedure

The first distinction of the building blocks and an introduction to the top-down systematic design approach is discussed in chapter 3. For both stages separately the next design steps are taken, but with accents on different aspects, which will be explained later on in this chapter.

- Define operating frequency and the used technology.
• Scale the transistors to the needed output power.
• Carry out DC simulations.
• Carry-out AC simulations.
• Carry out small signal simulations.
• Carry out large signal simulations.
• Design of matching and biasing networks.

First of all the operation frequency and the modulation environment has to be known, so an impression of the target to reach is achieved. Subsequently the transistor has to be scaled to the needed output power, before the next simulations can be carried out.

With the DC simulations a first impression of the usable operating points can be found. With this data a pointed search to the optimum operating point can be started. A usable fact is the \( f_T \) of the device, which can be found with AC simulation. The exact operating point to start with can be defined.

The stability of the device is an important constraint. The device must not only be stable on the operating frequency, but also on the second and third harmonic frequencies, and on lower frequency oscillations, which are often present, due to a different network before the power amplifier.

The large signal simulation consists of load-pull simulations. With this simulation algorithm the optimum loads for the right output power, the highest possible efficiency and the best possible linearity can be found.

To keep as long as possible an ideal situation the matching and biasing networks are designed at the end.

### 5.3 Output stage design

A power amplifier is designed to deliver a specified power, mostly according to a standard. For this reason the output stage is designed first. This stage has to be optimized for

- Delivered power
- Efficiency
- Linearity

#### 5.3.1 Transistor’s size

Before starting simulations the transistor has to be scaled to the needed output power. The size is a result of the needed current to achieve the output power.

\[
P_{\text{del}} = \frac{1}{2} \cdot V_{\text{DC}} \cdot I_{\text{DC}}
\]

(5.1)

Where comes out \( I_{\text{DC}} = 90\text{mA} \).
According to the AC simulation results in chapter 4 the highest \( f_T \) is reached at \( I_d = 0.23mA/\mu m \). This means at least a gate width is needed of 392\( \mu m \). A gate width of 420\( \mu m \) is determined to be sure that 22dBm is reached.

The segmentation of the gate fingers and the amount of transistors is chosen "arbitrary", because simulation results have given no explanation for an optimum. Measurement data is needed.

The chosen segmentation is 6 transistors of 7 fingers with a gate width of 10\( \mu m \) per gate finger, which gives a total gate-width of 420\( \mu m \).

**5.3.2 Small signal**

In small signal a first impression of the transistor's operating point can be found. Gain and stability is a trade-off, which has to be investigated.

**Operating point**

As shown in chapter 4 the maximum \( f_T \) of the PHEMT transistor is at \( I_d = 0.25mA/\mu m \) and \( V_{gs} = -0.300V \). This gives an impression at which bias-point the transistor achieves the highest current-gain.

These bias settings are also checked with large signal DC-simulations (see chapter 4) and load-pull simulations (later on in this chapter) and is the best point to start the design.

**Gain**

To achieve a good efficiency, power gain is important. The achieved gain is dependent on the input impedance of the transistor. In ideal situation, the transistor has to see the conjugate impedance of the transistor's input impedance \( Z_{input}^* \) to be matched for maximum gain.

\[
Z_{\text{match}} = Z_{\text{input}}^* \tag{5.2}
\]

Unfortunately this can not be achieved, because of the input stability of the transistor. The best stable impedance has to be chosen. The determined input matching impedance is \( Z_0 \cdot (0.1 + j \cdot 0.1) \), which is shown on the Smith-chart of figure 5.1 with the stability circle at 30GHz.

The dashed circles are the constant gain circles. The smaller the circles the higher the gain, until the transistor is not stable anymore. The chosen impedance gives an available gain of 9.7dB.

**Stability**

Stability of the transistor is discussed in chapter 3. Stability is an issue in microwave power amplifier design. Especially low frequency stability is a problem, because most microwave transistors are less stable on lower frequencies.

The input stability circle with the input matching impedance, shown in figure 5.1 is at 30 GHz. As shown in chapter 3 the trend of the input stability circle at lower frequencies is that the circle is going to the inductive (upper) side of the Smith-chart. So the input impedance determined previous is suitable for input stability.
5.3.3 Large signal

Large signal simulations are most important to reach the properties of the output-stage. This means delivered power, efficiency and linearity. In this subsection the approach and results are discussed to carry out focussed load-pull simulations.

Load-pull simulations were done based on an orthogonal approach and with the method as explained in section 3.3.4. In this approach the assumption is made that the different harmonic loads do not influence each other, so every harmonic load is simulated separately with the other harmonic impedances fixed. A flow-chart for this approach is presented in appendix B. The load-pull simulation targets for the different harmonic loads are:

- 1st harmonic to optimize the load for output power and efficiency
- 2nd harmonic to optimize the load for power added efficiency
- 3rd harmonic to optimize the load for linearity

The 2nd harmonic impedance can improve the efficiency, because this harmonic affects the DC zone in the spectrum. The 3rd harmonic impedance affects the signal-band, so it affects the linearity of the system.

Load-line

The load-line is determined, because this line gives a first impression (lucky guess) of the needed load to get the right output power. When determined, more focused load-pull simulations can be done.

The first impression of $R_{\text{load}}$ is determined with

$$P_{\text{del}} = \frac{(V_{\text{ds}} - V_{\text{knee}})^2}{2 \cdot R_{\text{load}}} \implies R_{\text{load}} = 30\Omega$$

(5.3)
The knee voltage is determined in the $I_d$ versus $V_{ds}$ characteristic as the point where the curve goes to saturation at maximum $I_d$. The load-line is shown in figure 5.2.

**Load-pull simulation 1-tone fundamental**

First 1-tone simulations are done. Every harmonic is optimized separately to the previous mentioned goals. The circuit, which is simulated is shown in figure 5.3. Most important in this simulation setup is the load-tuner (square block) on the output of the transistor. This block changes the, to the transistor presented reflection coefficients.

The targets for the fundamental tone are to optimize the output power to 22dBm and to keep the power added efficiency (PAE) as high as possible. In figure 5.4(a) the simulation on the Smith-chart is shown. A low frequency stability circle is shown in the Smith-chart and that part is avoided by the simulations.

The levels of delivered power and PAE are shown in figure 5.4(b), where the dashed lines are the PAE lines. The best solution is to stay at the edge of the simulated
area, because it is the most far from the output stability circle with a good result. The best result is got at a phase of -2.5 radians.

(a) Fundamental swept on the Smith-chart

Figure 5.4: 1-tone fundamental harmonic simulation results.

Load-pull simulation 1-tone 2nd harmonic

With the second harmonic impedance the efficiency of the amplifier can be improved. So load-pull simulations were done for the second harmonic impedance. Only the edge of the Smith-chart is swept (see figure 5.5(a)), because then the reflection coefficient is the largest, and the 2nd harmonic is not amplified a lot. So the most effect can be obtained at the edge.

The result is not a big improvement on efficiency (see figure 5.5(b)), so the second harmonic impedance will be open circuit (point at 0.0 radians in figure 5.5(b)).

(a) 2nd harmonic swept on the Smith-chart

(b) Efficiency levels on the simulated part.

Figure 5.5: 1-tone 2nd harmonic simulation results.
5.3 Output stage design

Load-pull simulation 1-tone 3rd harmonic

Linearity is important for this design and is dependent on the third harmonic. To improve the linearity, load-pull simulation is done at the third harmonic impedance. Also in this case only the edge of the Smith-chart is swept, because then the reflection coefficient is the largest, so more results can be obtained.

As seen in figure 5.6(b) the power of the third harmonic is the lowest at 0.0 radians on the Smith-chart. To achieve the lowest third harmonic power, the 3rd harmonic impedance has to be an open circuit.

Figure 5.6: 1-tone 3rd harmonic simulation results.

Results after 1-tone load-pull

The results of the 1-tone load-pull simulations are verified with harmonic balance (frequency-domain) simulation in ADS and are given below.

Extracted from the 1-tone power curve in figure 5.7 the one dB compression point is above 22dBm at an input power of 14dBm. The power added efficiency (dashed line) on that point is ±40%. This can be better, but than the power amplifier has to be driven more into compression, which means the linearity is getting worse.

Figure 5.8 presents the spectrum at $P_{\text{ave}} = 14\, \text{dBm}$. In this case the 3rd harmonic distortion ratio is 65dB.

<table>
<thead>
<tr>
<th>Harmonic impedance</th>
<th>Value [Ω]</th>
<th>Achieved result</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fundamental 30GHz</td>
<td>$Z_0(0.295 + j \cdot 0.188)$</td>
<td>$P_{\text{del}}$ at 1dB compression ≥22dBm</td>
</tr>
<tr>
<td>Second harmonic 60GHz</td>
<td>open circuit</td>
<td>PAE of 40%</td>
</tr>
<tr>
<td>Third harmonic 90GHz</td>
<td>open circuit</td>
<td>$P_{3rd} = -42, \text{dBm}$</td>
</tr>
</tbody>
</table>
Figure 5.7: Power and PAE curves after 1-tone load-pull simulations

Figure 5.8: The spectrum of the output-stage after 1-tone load-pull simulations @ 14dBm

Load-pull simulation 2-tones fundamental

Two-tone load-pull simulations are done to get insight in the intermodulation distortions and are done to fine-tune or to confirm the loads, found in the one-tone load-pull simulations. Again the approach is to assume the harmonic impedances orthogonal. So every harmonic is optimised separately in the same way as in the one-tone simulations. The two-tone simulations are focused on the results of the one-tone simulations, which decreases the simulation time significantly.

The used circuit is almost the same as the circuit of the 1-tone simulations. Only here an "n-tone" power source is used to create the two tones. These tones have a spacing of 1MHz.

First the fundamental tone is swept to optimize the load to reach the delivered power and to keep the power added efficiency as high as possible. In figure 5.10(a) the simulation on the Smith-chart is shown. A low frequency stability circle is shown in the Smith-chart and that part is avoided by the simulations.

The levels of delivered power and PAE are shown in figure 5.10(b), where the dashed lines are the PAE lines. The best solution is to stay at the edge of the simulated area, at the phase of -3.5 radians. A problem is that this point is very close to the
5.3 Output stage design

Figure 5.9: The 2-tone load-pull simulation circuit

stability circle.

Figure 5.10: 2-tone fundamental harmonic simulation results.

**Load-pull simulation 2-tones 2nd harmonic**

Also with two-tone simulations, the power added efficiency can be optimized when tuning the second harmonic load. From the one-tone simulations is known that the best results can be got on the edge of the Smith-chart. In this case the edge of the Smith-chart is simulated with less simulation points than in the one-tone simulation to confirm the achieved result of the one-tone simulation.

No significant change is achieved in power added efficiency, so the second harmonic impedance will be open circuit.
Load-pull simulation 2-tones 3rd harmonic

The last two-tone load-pull simulation is sweeping the third harmonic impedance on the edge of the Smith-chart. Measured is the power of the third order intermodulation products, which fall into the signal band. This simulation is done, according to the one-tone simulation results with less points, to reduce the simulation time.

Also the third harmonic impedance will be open circuit. The ratio of the third order intermodulation products with the delivered power is not changing significantly.

Figure 5.11: 2-tone 2nd harmonic simulation results.

Figure 5.12: 2-tone 3rd harmonic simulation results.
5.3 Output stage design

Results after 2-tones load-pull

The results of the two-tone load-pull simulations are verified with harmonic balance simulations. The 2-tone power curve in figure 5.13 shows the one dB compression point of 21dBm at an input power of 11dBm. The power added efficiency (dashed line) on that point is ±30%.

Figure 5.14 presents the spectrum at $P_{in} = 11dBm$. In this case the worst-case 3rd order intermodulation ratio is 23dB.

<table>
<thead>
<tr>
<th>Harmonic impedance</th>
<th>Value [Ω]</th>
<th>Achieved result</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fundamental [30GHz]</td>
<td>$Z_0(0.180 + j \cdot 0.200)$</td>
<td>$P_{del}$ at 1dB compression ≥ 21dBm</td>
</tr>
<tr>
<td>Second harmonic [60GHz]</td>
<td>open circuit</td>
<td>PAE of 30%</td>
</tr>
<tr>
<td>Third harmonic [90GHz]</td>
<td>open circuit</td>
<td>$P_{3rdIMD} = -13dBm$</td>
</tr>
</tbody>
</table>

Figure 5.13: Power and PAE curves after 2-tone load-pull simulations

Figure 5.14: The spectrum of the output-stage after 2-tone load-pull simulations
Load-pull QAM-signal according to the standard fundamental

The power amplifier has to operate in a 64-QAM environment, so finally load-pull simulations are done with the 64-QAM modulator to optimize the load to this signal. Because of the 64-QAM source these simulations were done with the envelope simulator of ADS.

Again the same circuit is used to carry out the simulations. Only here the designed 64-QAM modulator (see chapter 2) is used to provide the input signal.

Figure 5.15: The 64-QAM load-pull simulation circuit

The fundamental tone is swept on the Smith-chart in the same way as in the 1-tone and 2-tone simulations. There are less simulation points used than in the previous simulations, because this simulation takes much more time than the others.

Figure 5.16: 64-QAM fundamental harmonic simulation results.

The best and most safe result is got at the simulation phase of -1.6rad, which as a
5.3 Output stage design

complex impedance value of $Z_0(0.295 + j \cdot 0.188)$. This is the same impedance as found in the one-tone simulations.

Load-pull QAM-signal according to the standard 2nd harmonic

The second harmonic impedance is swept at the edge of the Smith-chart, because of the same reasons as mentioned in the previous simulations. Again this simulation is done roughly, because there is already data available from the 1-tone and 2-tone simulations.

No significant change is achieved in power added efficiency by changing the load of the second harmonic. So the second harmonic load impedance is open circuit.

![Graph](image)

(a) 2nd harmonic swept on the Smith-chart  
(b) Efficiency levels on the simulated part.

Figure 5.17: 64-QAM 2nd harmonic simulation results.

Load-pull QAM-signal according to the standard 3rd harmonic

The 3rd harmonic impedance is swept in the same way as in the previous 3rd harmonic simulations, but in this case less simulation points are used. This simulation has to confirm the 1-tone and 2-tone simulations.

The result is as expected. When the third harmonic impedance is open circuit the power of the third harmonic is the lowest (see figure 5.18).

Results after QAM load-pull

The results are verified with the envelope simulator and are shown in the table below. More comprehensive results of the 64-QAM simulations are discussed in the next section.

<table>
<thead>
<tr>
<th>Harmonic impedance</th>
<th>Value [Ω]</th>
<th>Achieved result</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fundamental [30GHz]</td>
<td>$Z_0(0.295 + j \cdot 0.188)$</td>
<td>$P_{\text{del}}$ at 1dB compression ≥17dBm</td>
</tr>
<tr>
<td>Second harmonic [60GHz]</td>
<td>open circuit</td>
<td>PAE of 13%</td>
</tr>
<tr>
<td>Third harmonic [90GHz]</td>
<td>open circuit</td>
<td>See next section: Envelope verification</td>
</tr>
</tbody>
</table>
5.3.4 Envelope verification

In a multi-tone environment envelope verification is an important step. According to the IEEE802.16c standard the error vector magnitude (EVM) and the spectrum mask are verified (see chapter 2).

**Error vector magnitude**

The EVM is calculated in ADS with the "const.evm" function. The simulations were done with a dummy source to guarantee the ideal reference constellation for the EVM calculation. The EVM results are verified with different input back-off powers, to investigate the limit of the needed back-off to keep the EVM according to the standard. Figure 5.19 presents the constellation diagrams at the input and output of the output-stage at an input power of 9dBm, which gives an output power of 18dBm.

Notable is the distortion in the output constellation diagram. This distortion is not due to the gain compression, because this distortion affects every symbol. This distortion is due to the AM to PM conversion (see section 5.6.1).

The error vector magnitude at this level is 1.4%, which is in the limit of the standard.

**Spectrum mask**

The output spectrum of the output-stage is verified with the spectrum mask defined in chapter 2. This spectrum mask is put on top of the signal, because the mask is defined in relative levels (dBc).

No problems occur when considering the spectrum mask in the output spectrum of the output-stage.
5.4 Input-stage design

The input-stage is designed to achieve maximum gain and the right output power, which has to be high enough for the output stage, including the insertion loss of the interstage matching.

5.4.1 Gain

The main target of input-stage design is to achieve high gain. Mainly responsible for gain is the input impedance, which has to be conjugate matched in ideal case (see chapter 3).

To find the right input and output impedances s-parameter simulations have to be done. Targets are to create gain circles as function of the input and output reflection coefficients (so indirect impedance). This is presented in figure 5.21, where the solid lines are the gain circles at the input and the dashed lines the gain circles at the output.

The maximum gain is achieved in the middle of the circles, which is $\geq 10\text{dB}$ (see figure 5.25).
5.4.2 Stability

When achieving maximum gain, stability has to be taken in mind. Also in this case with s-parameter simulations the input and output stability circles have to be visualized.

On 30GHz there is no problem, according to the results in figure 5.21, where the solid line is the input stability circle and the dashed line the output stability circle. The lower frequencies can give problems, because the transistor is getting more unstable.

![Stability circles on the lower frequencies](image)

(a) Stability at the input (b) Stability at the output

The input stability circles are moving around the desired input impedance (black dot in figure 5.22(a), so the input stability gives no problem. The output stability gives problems at 12.5GHz and lower, which can be seen in figure 5.22(b) where the 12.5GHz stability circle crosses the load impedance. This can be avoided in the matching network design.
5.4.3 Pseudo input mismatch

The input-stage has to deliver the right output power, which is necessary to let operate the output-stage in the best way. This means that the input-stage transistor has to be big enough to deliver the needed power.

Figure 5.23: Matched input impedances when a power sweep is applied.

In first case the input-stage is designed to deliver the exact necessary 1dB compression point power to feed the output-stage. This affected the linearity performance of the total power amplifier a lot. For this reason the size of the transistor is determined twice as big, which gives a better result.

![Gain expansion](image)

Figure 5.24: Effect due to pseudo input mismatch.

Also pseudo input mismatch applied (see reference [12]). In this case the input impedance of the amplifier is fixed at 1dB compression of the output, determined after a power sweep with the input impedance fixed on the value at the lowest input power. This is shown in figure 5.23, where the input impedance is changing when the input power is swept. All the shown impedances are correct matched, but at different input power.

The result is a change in the $P_{in}$ versus $P_{out}$ curve, which is also explained in figure 5.24. The gain of the system is some lower, but there is a gain expansion near the
1dB compression point. The result is an improvement of the 1dB compression of the system, but with a lower gain.

![Image](image.png)

Figure 5.25: AM-AM curve of the input stage

The result in ADS is presented in figure 5.25. The change is not big in this case, because there is only a small input impedance change when the power is swept. This input impedance is applied in the input-stage.

The input and output impedance values of the input-stage are determined on:

- Input impedance = $Z_0(0.207 + j \cdot 0.416)$
- Output impedance = $Z_0(0.868 + j \cdot 0.550)$

The output power of the input-stage is 18dBm at 1dB compression. 14dBm is needed as input power of the output-stage.

5.5 Matching and biasing networks

The separate input-stage and output-stage have to be matched to the desired impedances, 50Ω and to each other. The approach is to start with the output matching and end up with the input matching, because the output impedance affects the most the output power and power added efficiency (see reference [10]).

Enumerated:

- Output impedance of the output-stage to 50Ω.
- Output impedance of the output-stage to the input impedance of the input-stage (interstage).
- 50Ω to the input impedance of the input-stage.

The matching networks are designed with coplanar waveguide technology. This technology provides a better magnetic separation between the transmission lines, due to the adjacent ground planes (reference [7]). The losses are quite similar to micro-strip lines, according to s-parameter simulations in ADS.
To go off-chip bond wires are necessary, so it has to be taken into account. The minimum bond-wire inductance is 0.1nH, according to Philips Semiconductors. This is the smallest value and is used at the input and output of the high frequency path. The biasing circuits are designed along with the matching circuits, because these circuits can affect the performance of the matching circuits.

5.5.1 Output matching network

The output matching network is designed to match the needed load of the output-stage \( (Z_o \cdot (0.295 + j \cdot 0.188)\Omega) \) to 50\( \Omega \). A 0.1nH inductance is taken into account, to keep the possibility to go off-chip. The used approach to match the output-stage to 50\( \Omega \) is shown in figure 5.26. A serie-C is used (see figure 5.27), instead of a shunt-C, due to the influence of the 0.1nH inductance.

![Figure 5.26: Matching approach for the output](image1.png)

![Figure 5.27: Designed output matching network](image2.png)

The solid lines in figure 5.28(b) are S11 and S22 parameters, which gives a suppress at 30GHz of \( \geq 25dB \). The dashed lines are S12 and S21 parameters, which gives the insertion loss of the network, which is 0.2dB at 30GHz.
Design procedure for a two-stage power amplifier

(a) Matching on the Smith-chart  
(b) S-parameters versus frequency

Figure 5.28: Matching results of the output matching network

5.5.2 Interstage matching network

The interstage matching network is designed to match the output of the input-stage transistor \((Z_0' : (0.868 + j \cdot 0.550) \Omega)\) to the input of the output-stage transistor \((Z_0' : (0.100 + j \cdot 0.100) \Omega)\). The insertion loss has to be taken into account, so enough power is available to feed the output-stage.

![Direct, without 50Ω intermezzo](image1.png)  
![Indirect, with 50Ω intermezzo](image2.png)

Figure 5.29: Matching approach for the interstage

Indirect

There are different possibilities to design the interstage matching. Often an intermezzo impedance (for example 50Ω) is determined (see figure 5.29(b)). Both impedances are matched to that intermezzo impedance and the two resulting networks are put together afterwards. This is explained in figure 5.30, where two (arbitrary) complex impedances \(Z_{in}\) and \(Z_{out}\) have to be matched together, via a 50Ω intermezzo impedance. When circuit 1 and circuit 2 are matched correct to the 50Ω impedance, the 50Ω impedances are removed and the circuits are connected together. The result is a matching network, which matches two complex impedances.
5.5 Matching and biasing networks

The solid lines in figure 5.32(b) are $S_{11}$ and $S_{22}$ parameters, which gives a suppress at 30GHz of $\geq 20\text{dB}$. The dashed lines are $S_{12}$ and $S_{21}$ parameters, which gives the insertion loss of the network, which is 0.5dB at 30GHz, according to s-parameter simulations.

(a) Matching on the Smith-chart  
(b) S-parameters versus frequency

Figure 5.32: Matching results of the interstage matching network indirect

Direct

Another approach is to match the two impedances direct together (see figure 5.29(a)). This is done in the ADS data-display. This can be tricky, because ADS normalizes the Smith-chart to the impedance at the determined impedance of the terminal, which is not 50\Omega in this case (seen from both sides).

The solid lines in figure 5.34(b) are $S_{11}$ and $S_{22}$ parameters, which gives a suppress at 30GHz of $\geq 20\text{dB}$. The dashed lines are $S_{12}$ and $S_{21}$ parameters, which gives the
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Figure 5.33: Designed interstage matching network direct

insertion loss of the network, which is 0.5dB at 30GHz, according to s-parameter simulations.

Figure 5.34: Matching results of the interstage matching network direct

The result is not a big difference in matching network, because the output impedance of the input-stage is close to 50Ω (see figure 5.29). Also the suppress and the insertion loss are roughly the same, when simulated with s-parameter simulation. The designed network, presented in figure 5.31 is used, because this network gives the best result when simulated with a power source in the AM-to-AM characteristic of the complete power amplifier.

5.5.3 Input matching network

The input matching network is designed to match the 50Ω to the input impedance of the input-stage, which is $Z_0 \cdot (0.207 + j \cdot 0.416)\Omega$. The used matching approach to go from 50Ω to the input impedance is shown on the Smith-chart in figure 5.35.

The needed serie capacitor has a value of 40fF. This value is too small for the used models, so two capacitors of 80fF are used in serie.

The solid lines in figure 5.37(b) are S11 and S22 parameters, which gives a suppress at 30GHz of $\geq 30$dB. The dashed lines are S12 and S21 parameters, which gives the insertion loss of the network, which is 0.2dB at 30GHz.
5.5 Matching and biasing networks

Figure 5.35: Matching approach for the input

Figure 5.36: Designed input matching network

Figure 5.37: Matching results of the output matching network

5.5.4 Biasing networks

The biasing networks are designed with a \( \lambda/4 \) coplanar waveguide and a capacitor to make a resonance at the operating frequency of 30GHz. The bias circuit is a short circuit for DC power from the supply and an open circuit for the high frequency signal from the transistor (see figure 5.38).

By designing the biasing networks a bond wire inductance of 0.5nH is taken into account to provide the possibility to go off-chip.
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5.6 Complete power amplifier

The final step is to assemble the designed parts of the power amplifier and verify the achieved results. This is done step by step, from the output to the input. The schematic of the designed two-stage power amplifier is presented in figure 5.39. The main blocks consist of the transistors and the matching networks, which are enumerated below.

- Input matching network + biasing
- Input-stage transistor
- Interstage matching network + biasing
- Output-stage transistor
- Output matching network + biasing

![Figure 5.38: A bias network with $\lambda/4$ transmission line](image)

![Figure 5.39: The schematic of the designed power amplifier](image)
5.6 Complete power amplifier

5.6.1 AM-to-AM and AM-to-PM

Important curves are the AM-to-AM distortion and AM-to-PM distortion curves of the power amplifier. AM-to-AM is the output power compression curve as function of the input power. AM-to-PM is the phase difference between the input and output signals as function of the input power.

These distortions give information about the amount of back-off, necessary to achieve good linearity with the 64-QAM signal.

AM-to-AM

AM-to-AM conversion or the gain curve of the complete power amplifier is presented in figure 5.40. It can be seen that the gain is linear and the 1dB compression point of the power amplifier is at almost 23dBm output power.

\[ P_{\text{ave}} \text{ versus } P_{\text{del}} \]

Figure 5.40: The $P_{\text{ave}}$ versus $P_{\text{del}}$

AM-to-PM

The AM-to-PM curve of the designed power amplifier is presented in figure 5.41. The non-linearity in phase is starting earlier than the gain compression of the power amplifier. The non-linearity in the phase is already starting at $P_{\text{ave}} = -5\text{dBm}$. This means that the AM-to-PM conversion is the dominant distortion for the needed back-off to achieve the conditions according to the standard.

5.6.2 Envelope verification

The power amplifier has to operate according to the standard, described in chapter 2. This means the error vector magnitude has to be $\leq 1.5\%$ and the output spectrum has to fit into the defined spectrum mask.

Because of the AM-to-PM the error vector magnitude will be more critical than the spectrum mask.
Error vector magnitude

Due to the AM-to-AM and AM-to-PM distortion the error vector magnitude (EVM) is dependent on the input back-off, because of the peak to average ratio of a 64-QAM signal. The EVM as function of input power an input back-off are presented in figure 5.42 and 5.43.

From figure 5.43 can be seen that an input back-off of 6.5dB is necessary to achieve an EVM of 1.5%. The back-off is determined with the 1dB compression point of the 1-tone simulations. The needed back-off can be verified by the probability density function of the power distribution of the 64-QAM signal in chapter 2, where the highest power is 7dB above average.

At the input back-off of 6.5dB the power amplifier achieves an output power of 17dBm.
5.6 Complete power amplifier

Figure 5.43: The EVM as function of input power back-off

The input and output constellation diagrams are shown in figure 5.44. Notable is the kind of distortion in the output constellation. No compression occurs, but there is distortion in all the symbols. This is due to the AM-to-PM distortion, which occurs earlier than the AM-to-AM nonlinear distortion, or gain compression.

Figure 5.44: Constellation diagrams (with different scales) of the power amplifier.
Spectrum mask

The output spectrum of the power amplifier at 6.5dB back-off operation is presented in figure 5.45. As can be seen the spectrum falls into the spectrum mask, according to the standard.

Figure 5.45: The output spectrum of the PA and the spectrum mask
Chapter 6

Linearity improvement by IF termination

To achieve a better performance and trade-off between efficiency and linearity a linearity improvement by IF-termination is investigated.

6.1 Introduction

The linearity of the designed power amplifier is very critical, when using complex modulated signals. Due to the demands of the standard, the power amplifier has to operate in back-off operation, therefore the achieved power added efficiency is low. According to the literature (reference [11], [15]) a better trade-off between efficiency and linearity can be achieved with IF-termination.

In this chapter some theory of this subject and the achieved results of the applied IF-termination are presented.

6.2 Theory

The principle of a linearity improvement by IF-termination and a non-linear FET model are presented.

6.2.1 Principle

A non-linear system can be described with a power series representation (see reference [2], [8], [11]), like

\[ y(t) = a_1 x(t) + a_2 x^2 + a_3 x^3 \]  \hspace{1cm} (6.1)

When a two-tone simulation is done, mixing products appear. Most important are the third order intermodulation products (IM3), because these products appear in the signal band (see figure 6.1). The point where the linear extrapolated fundamental compression curve crosses the linear extrapolated IM3 compression curve is called the 3rd order intercept point "IP3" (see equation 6.2), which is about 9.6dB above the 1dB compression point (reference [2], page 188).
Third order intermodulation products consist of direct mixing products, as a result of mixing of the third order signals \((2\omega_1 - \omega_2)\) and \((2\omega_2 - \omega_1)\). And also of indirect mixing products (see reference [11]), as a result of mixing of the fundamental tones with the baseband second order intermodulation \((\omega_2 - \omega_1)\) and the second harmonic \((2\omega_1 \text{ and } 2\omega_2)\).

The target is to determine an impedance for IM2 at low frequency, which gives a phase-shift to the indirect mixing product of the fundamental and IM2. So the contribution to the third order intermodulation products (IM3) is in opposite phase, which means a reduction of the IM3. The analysis of the effect of a base-band impedance can be done with Volterra series (reference [8]), which is done in reference [11] for a bipolar device and in reference [15] and [16] for a FET device.

### 6.2.2 FET model

The main non-linear elements in a FET are the gate-source capacitor \(C_{gs}\) and the drain current source \(i_d\). According to reference [11] and [15] the gate-drain capacitor \(C_{gd}\) can be neglected, because its effect to non-linear behavior is very small when compared to \(C_{gs}\) and \(i_d\).

The simplified model is presented in figure 6.2.

Figure 6.1: Impression of mixing products as a result of two-tone simulation ([11]).

\[
v_{IP3} = \sqrt{\frac{4}{3}} \frac{a_1}{a_3} \tag{6.2}
\]

Where the non-linear elements are modeled by a fifth-order Taylor expansion (see reference [11] and [15]).
The Taylor expansion of the non-linear elements is shown till fifth order, because the fifth order component affects the linearity of the third order component (see reference [8] and [11]).

\[ i_{C_{gs}} = C_{gs1}v_{gs}(t) + C_{gs2}v_{gs}(t)^2 + C_{gs3}v_{gs}(t)^3 + C_{gs4}v_{gs}(t)^4 + C_{gs5}v_{gs}(t)^5 \]  \hspace{1cm} (6.3)

\[ i_d(t) = g_{m1}v_{gs}(t) + g_{m2}v_{gs}(t)^2 + g_{m3}v_{gs}(t)^3 + g_{m4}v_{gs}(t)^4 + g_{m5}v_{gs}(t)^5 \]  \hspace{1cm} (6.4)

6.3 Simulation results

To verify the the possibilities of IF-termination, load-pull simulations were done with the output-stage in ideal case.

6.3.1 2-tone simulations

![Figure 6.3: The two-tone simulation setup.](image)

Two-tone load-pull simulations were done with the circuit of figure 6.3. An additional load-tuner and source-tuner is used. These two tuners provide the reflection coefficients at the IF frequencies and force the RF-impedances in these tuners to zero, to be sure that the higher frequency impedances are the same as without the additional tuners, which is verified with a reference circuit without IF-tuners.

<table>
<thead>
<tr>
<th>Reflection coefficient tuner</th>
<th>IF frequency</th>
<th>RF frequency</th>
</tr>
</thead>
<tbody>
<tr>
<td>Source: IF frequency</td>
<td>Dedicated IF impedance</td>
<td>Short circuit</td>
</tr>
<tr>
<td>Load: IF frequency</td>
<td>Dedicated IF impedance</td>
<td>Short circuit</td>
</tr>
<tr>
<td>Load: RF frequency</td>
<td>Short circuit</td>
<td>Dedicated RF impedances</td>
</tr>
</tbody>
</table>

All the lumped components are ideal in this case. DC-blocks and DC-feeds are used.
This load-pull simulation fixes all the harmonic impedances and sweeps the IF impedances on the edge of the Smith-chart, because there are the largest changes. When the source IF-impedance and the load IF-impedance are open-circuit, then the third harmonic intermodulation ratio is the largest. See the table below, where the results are presented at an input power of 14dBm, which is determined in chapter 5.

<table>
<thead>
<tr>
<th>Load IF impedance</th>
<th>Source IF impedance</th>
<th>3rd harmonic IMR</th>
</tr>
</thead>
<tbody>
<tr>
<td>Open circuit</td>
<td>Open circuit</td>
<td>21.5dB</td>
</tr>
<tr>
<td>Short circuit</td>
<td>Short circuit</td>
<td>19.3dB</td>
</tr>
<tr>
<td>Short circuit</td>
<td>50Ω</td>
<td>20.0dB</td>
</tr>
</tbody>
</table>

To verify the results of the load-pull simulations, a power sweep in harmonic balance is done. The result is presented in figure 6.4, where the AM-to-AM curve is shown in ideal case with IF-termination and without IF-termination. It can be seen clearly that the curve with IF-termination shows a higher 1dB compression point, so a linearity improvement is achieved.

Figure 6.4: The ideal curve without and with IF-termination

The phase-shift of the output-stage is shown in figure 6.5. Notable is that the AM-to-PM distortion is getting nonlinear at already 2dBm of input power and that the AM-to-PM distortion is the same for both cases.

Figure 6.5: The AM-to-PM curve of the output-stage

The bias networks and AC-coupling capacitors are critical to see the effect of IF-
termination in the designed output-stage of the power amplifier. The improvement effects were only observed with ideal DC-feeds or inductances of $\geq 1mH$, and with AC-coupling capacitors or capacitors of $\geq 1\mu F$. In the other situations the curve follows the reference curve, without IF-termination.

### 6.3.2 64-QAM simulations

In the 64-QAM environment the two-tones AM-to-AM linearity improvement is applied. Error vector magnitude (EVM) simulations were done, because this is the most critical constraint of the IEEE802.16c standard, so the most interesting.

![Figure 6.6: The EVM simulation setup with dummy circuit](image)

The EVM simulations were done with a dummy source to guarantee the ideal reference constellation for the EVM calculation. An overview of the results of different IF-impedances versus EVM in percentage is presented in the table on the next page, where the reflection coefficients of the IF tuners are presented versus the delivered power and EVM.

The simulations are done with the ideal output-stage circuit without any IF-tuners as a reference. The next settings with the accompanying results are used:

- $P_{in} = 9.5dB$
- $P_{del} = 18.7dB$
- EVM=1.6%

The IF-impedance is set on the frequency spacing, used by the two-tone simulations, which is 4MHz in this case, because 1MHz spacing (applied in chapter 5) has shown no effect in the 2-tone simulations of the previous section. The order of the harmonic balance simulator is set on 7, with a maximum of 11.
First everything in the IF-tuners is ideally short circuit to have a comparison with the reference. After that the RF impedances in the RF-tuners are set on $\Gamma = -0.99$, which is not ideal anymore. And subsequently the IF-impedances in the IF-tuners are set on $\infty$, which means $\Gamma = 1$.

<table>
<thead>
<tr>
<th>IF source $\Gamma$</th>
<th>RF source $\Gamma$</th>
<th>IF load $\Gamma$</th>
<th>RF load $\Gamma$</th>
<th>$P_{del}$ [dBm]</th>
<th>EVM [%]</th>
</tr>
</thead>
<tbody>
<tr>
<td>-1</td>
<td>-1</td>
<td>-1</td>
<td>-1</td>
<td>18.7</td>
<td>1.6</td>
</tr>
<tr>
<td>-1</td>
<td>-0.99</td>
<td>-1</td>
<td>-0.99</td>
<td>18.4</td>
<td>1.4</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>-1</td>
<td>18.7</td>
<td>1.6</td>
</tr>
<tr>
<td>$\Gamma_{source}$</td>
<td>$\Gamma_{load}$</td>
<td></td>
<td></td>
<td>18.7</td>
<td>1.6</td>
</tr>
</tbody>
</table>

The results according to the EVM simulations, which are shown in the table, are enumerated below.

- The short circuit value $\Gamma = -1$ of the RF impedances in the IF load is critical for a good simulation, which can be seen in the table were the RF reflection coefficients are -0.99.
- The different (extreme) values of IF source and load reflection coefficients have no effect on EVM.

As seen in the two-tone simulations in this chapter the AM-to-AM characteristic is improved by IF-termination in ideal case. Unfortunately the AM-to-PM characteristic starts getting non-linear earlier. The non-linearity in the AM-to-PM characteristic is strong (±10°) at the 1dB compression point in the AM-to-AM characteristic, so AM-to-AM is inferior to AM-to-PM in the presented power amplifier.
Chapter 7

Conclusions

A systematic design approach with small steps is employed to design the power amplifier. During the project the importance of an approach like this to design a system in limited time and to understand what steps to take is realized, as well as verification of simulation results.

The required output power single-tone and QAM is achieved, with the required linearity performance:

- Single tone: $P_{del} > 22\,dBm$, namely 23dBm
- 64QAM: $P_{del} > 15\,dBm$, namely 17dBm

The linearity requirements of the IEEE802.16c standard are achieved, when simulated with ADS 2003c:

- Error vector magnitude is 1.5%.
- Output spectrum is inside the defined spectrum mask.

On the other hand 25% efficiency with the 64-QAM signal, determined in advance is not achieved, because the focus was on linearity and the power amplifier operation is kept in class A.

Pseudo input mismatch is employed to improve the linearity of the input-stage.

The final linearity performance is not only dependent on the output-stage of this power amplifier, because also the AM-to-PM distortion of the input-stage has a significant impact.

Electromagnetic simulations are necessary to really understand the advantages of coplanar waveguide technology of the used process in microwave frequency design.

For the power amplifier designed in this project, IF-termination has no influence on error vector magnitude, due to the Crest-factor.

When using IF-termination the biasing and DC decoupling of the circuit is critical. It has to be taken into account from the start of the design.
Chapter 8

Recommendations

In this project the power amplifier operates in class A. To gain more efficiency class AB operation can be considered with additional linearity improvements to achieve the EVM criterium of the standard.

Measurements can be considered on real transistors to verify the characteristics of the transistor to find the optimum operating conditions. So a better symmetrical design can be achieved.

To be more sure the used models in the design are correct a verification of this design is necessary with newer versions of the Ommic models.

To verify the circuit simulation results the lay-out of the power amplifier has to be designed.

To place impedances just outside the stability circles is tricky and there can occur an input stability problem at 4GHz, so to improve the stability of the power amplifier dedicated input serie impedances can be considered (see reference [10]).

Other topologies, like a cascode input-stage, can be investigated to design a power amplifier for this standard.

Predistortion can be applied to achieve a better EVM.

The EVM calculations have to be done in the RF circuit simulator of ADS2004a and newer.

The coefficients of the differential equations of the non-linear FET model in chapter 6 can be calculated to verify the results with the theory.

Other models can be considered to verify the effect on EVM with IF-termination.
Appendix A

Complete Smith-chart

Figure A.1: The complete impedance/admittance Smith-chart.
Appendix B

Load-pull approach flow-chart

This appendix presents a flow-chart for the used load-pull simulation approach, assumed that harmonic impedances can be terminated properly independent from each other.

Figure B.1: The approach for load-pull simulation.
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