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Off-line Balanced Forward-Flyback Converter

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Abstract—Due to the flybacks’ indirect characteristic of energy transfer, the transformer size increases for high power levels. Providing an additional direct energy transfer path can decrease its size. Parallel forward-flyback converters offer such functionality and outperform forward converters with regard to PFC functionality. A balanced forward-flyback converter is a variation on this kind of parallel converter. The forward and flyback sub-converters share a transformer winding and an additional balancing capacitor enables even better AC line voltage utilization. This paper starts with an in-depth analysis of the balanced forward-flyback converter, and introduces ten operating modes in which this converter can operate. A boundary-conduction mode (BCM) controller for the magnetization current is developed and presented, and through simulations the PFC performance of the converter is tested with a constant switch on-time controller. Moreover, a prototype is designed and built with both a dissipative R-C-D snubber and two-switch clamp configuration. Experimental results from the 100W/120-373V AC/DC prototype were obtained to prove the converter operation and BCM controller concept. The balanced forward-flyback converter in BCM offers good PFC performance and manages a THD of input current between 1.69% and 4.38%.

Index Terms—AC-DC conversion, PFC, balanced forward-flyback converter, BCM

I. INTRODUCTION

Power supplies for grid-connected applications account for a significant part of the bill of material of electronic equipment. Single-switch converters, e.g. the flyback converter, are generally accepted for power levels up to approximately 150 Watt. Above this level other topologies, such as the 2-switch forward and half-bridge topology, become more attractive due to the flybacks’ indirect nature of energy transfer [1]. Topologies that combine direct and indirect energy transfer can lead to a gain in conversion efficiency and cost reduction.

To comply with international regulations regarding current harmonics [2] power factor correction (PFC) is required. An often used solution is adding a PFC boost stage to a conventional converter. However, this leads to an increase in component count and cost. As a result, single-stage PFC topologies are popular research topics [3]–[5].

A flyback converter offers good PFC performance, but due to its indirect energy transfer characteristic a large transformer is required for high output power levels. Providing a direct energy transfer path can decrease the amount of energy storage, thus decreasing transformer size. A forward converter is a typical topology with direct energy transfer. However, it requires a demagnetization snubber or winding [6], [7] and a large output filter. Moreover, in contrary to the flyback converter, a forward converter is not suitable for single-stage PFC, because it suffers from a dead-zone around the zero-crossings

of the sinusoidal input voltage [8], [9]. Paralleling a flyback and forward converter in principle can provide the best of both worlds. Not only does it lead to smaller transformer and output filter sizes, but also eliminates the forward converters’ demagnetization circuit. Parallel forward-flyback converters are proposed in [9]–[11]. These parallel operating converters share a primary switch and have a separate winding on a shared transformer. The forward conversion path still suffers from a dead-zone, but the flyback conversion path can transfer energy during these intervals. This makes the parallel forward-flyback more suitable for PFC than a conventional forward converter. The balanced forward-flyback converter proposed in [8] combines a conventional flyback and forward converter with a shared secondary transformer winding and shared primary switch. Energy transfer from primary to secondary occurs when the switch is turned on (forward action) and when the switch is turned off (flyback action). A secondary-side balancing capacitor prevents saturation of the magnetic core and lowers the minimum input voltage required for the forward converter to operate, as will be shown later in this paper. The latter makes this topology suited for integrated PFC functionality.

II. BALANCED FORWARD-FLYBACK CONVERTER

The balanced forward-flyback converter from [8] combines a conventional forward converter with a flyback converter and adds a balancing capacitor at the secondary side. Fig. 1 depicts a schematic representation of the topology. For the analysis, the transformer is modeled as an ideal transformer with a parallel inductance L_M representing the magnetizing inductance which is used for energy storage. The series leakage inductance is neglected for the conceptual analysis of the topology. All remaining components are also considered ideal. Capacitors C_b and C_o are assumed to be large enough such that their voltage ripples can be neglected.

The steady-state analysis is based on the assumption that switch S is either conducting, as shown in Fig. 2(a), or open, as depicted in Fig. 2(b), and that currents i_{L_M} and i_{L_o} are positive. While S is turned on, energy is transferred to the secondary side and the converter stores energy in the magnetic core i.e. magnetizing inductance L_M . When S is turned off, forward current freewheels through diode D_2 and magnetically stored energy is transferred to the secondary side through the transformer and D_3 .

The converter gain is derived from the steady-state analysis presented in [8] and is determined to be

$$V_o = \frac{\delta}{n(1 - \delta^2)} V_d \quad (1)$$

Fig. 1. Topology of the balanced forward-flyback converter.

where δ represents the switch duty-cycle, V_d the input voltage, V_o the output voltage, and n the primary to secondary turns ratio of the transformer.

An expression for the switch duty cycle δ can be obtained by rearranging (1), which results in

$$\delta = -\frac{V_d}{2nV_o} + \sqrt{\left(\frac{V_d}{2nV_o}\right)^2 + 1}. \quad (2)$$

The average bias capacitor voltage V_{C_b} is calculated to be $V_{C_b} = \delta V_o$ [8] thus C_b in series with the secondary transformer winding acts as a controllable DC voltage source. Under steady-state conditions the voltage across C_b is constant, which requires the average current to be zero. Therefore, average secondary winding current is zero as well. Consequently, current through the ideal primary transformer winding is zero on average, and the average current drawn from the input source equals the average magnetization current such that $I_d = I_{L_M}$ [8]. Both forward conversion current i_{D_1} and flyback conversion current i_{D_3} flow through C_b . The forward action current discharges the capacitor, while the flyback current recharges it. A constant capacitor voltage V_{C_b} under steady-state conditions implies that the forward and flyback action current are on average equal in magnitude i.e. $I_{D_1} = I_{D_3}$. Since

$$I_{L_o} = \frac{I_{D_1}}{\delta}, \quad (3)$$

summing the average output filter and flyback action current contribution results in the average output current

$$I_o = \frac{I_{D_1}}{\delta} + I_{D_3} = I_{L_o} + I_{D_3}. \quad (4)$$

When assuming 100% conversion efficiency i.e. $P_d = P_o$, then (1) can also be written as

$$I_d = \frac{\delta}{n(1 - \delta^2)} I_o, \quad (5)$$

which in turn can be rewritten to

$$I_{D_3} = nI_{L_M}(1 - \delta) = nI_d(1 - \delta). \quad (6)$$

Combining (4), (5) and (6) leads to an expression for the average output filter inductor current

$$I_{L_o} = I_o \left(1 - \frac{\delta(1 - \delta)}{(1 - \delta^2)}\right). \quad (7)$$

Equations (6) and (7) show that the flyback and forward action contribution depend on the duty cycle and, thus, vary with the input voltage level.

When S is conducting, as shown in Fig. 2(a), V_{C_b} is a voltage source in series with the primary transformed input voltage, which is advantageous for the forward power conversion. Conventional forward converters in AC-DC PFC applications suffer from a dead-zone around the zero-crossings of the AC mains source [8], [9], because the input voltage is insufficient to make D_1 forward-biased. In this scenario V_{C_b} increases the D_2 anode voltage, thus lowering the minimum required input voltage and increasing the portion of sinusoidal half-wave for which the forward power conversion stage is active. Secondly, a flyback converter ideally is able to operate from any input voltage and thus allows flyback energy conversion over the full rectified mains voltage waveform. Additionally, the flyback conversion current charges capacitor C_b causing V_{C_b} to rise around the AC input voltage zero-crossings. As a result, the required input voltage for forward energy conversion is automatically lowered around these zero-crossings. The balanced forward-flyback topology therefore allows for a better utilization of rectified mains voltage compared to the parallel forward-flyback converters proposed in [9]–[11], which suffer from a significant time interval with no forward action around the zero crossings. The balanced forward-flyback converter minimizes this interval.

A. Operation modes

A sequence of configurations is called an operating mode of the converter. One switching cycle ($T_{sw} = 1/f_{sw}$) is split in two or more intervals separated by switch actions of S or by one of the diodes starting or stopping to conduct. Each interval relates to one of the circuit configurations depicted in Fig. 2, in which the conducting components are indicated in the circuit topology. The active operating mode is determined by component parameters, average forward action current I_{L_o} , average flyback action current I_{D_3} , output power P_o and switching frequency f_{sw} . Each possible operating mode is discussed after introducing the eight circuit configurations.

- **Configuration 1:** First of the two configurations used for steady-state analysis. Switch S is turned on and energy is transferred to the load by means of a forward current through D_1 and, simultaneously, energy is stored in the magnetizing inductance by current i_{L_M} . Note that i_{L_M} can start at a negative value. If switch S turns on, V_d across L_M causes an increasing magnetization current.
- **Configuration 2:** Second of the two configurations used for steady-state analysis. Switch S is turned off and magnetically stored energy is transferred to the secondary side through the transformer and D_3 . Current i_{L_o} freewheels through D_2 . Note that i_{L_o} can reach negative values, but only if it is smaller in magnitude than i_{D_3} .
- **Configuration 3:** This current loop is formed if i_{L_o} is positive during a switching cycle and i_{L_M} reaches a negative value due to the average I_{L_M} level and the reflected secondary voltage across L_M .

Fig. 2. Eight circuit configurations of the balanced forward-flyback converter where the active components are highlighted and red represents forward action current, and green represents flyback action current.

- **Configuration 4:** Magnetizing current i_{L_M} can reach a negative value, which leads to diode D_1 becoming forward-biased and positive i_{sec} . L_M is clamped to the reflected secondary voltage level $-n \cdot V_{C_b}$ since D_2 is conducting current. Current i_{L_o} freewheels through D_2 , and D_1 flows in opposite direction through D_2 . Node current analysis shows that D_2 carries i_{L_o} plus the positive part of i_{sec} . This configuration is only possible if i_{L_M} remains smaller in magnitude than i_{L_o} .
- **Configuration 5:** With i_{L_M} being positive, i_{L_o} can reach a negative value during the time S is turned off. D_2 stops conducting. Because flyback action current i_{D_3} is flowing, L_M and L_o are now in series with bias capacitor voltage V_{C_b} . Load R_L is fed by the output capacitance C_o .
- **Configuration 6:** Forward conversion current is not possible if the sum of input voltage V_d/n and balancing capacitor voltage V_{C_b} is insufficient for forward-biasing D_1 . Energy is magnetically stored in L_M and the load is fed by the output capacitance C_o .
- **Configuration 7:** Switch S turns on while i_{L_M} is positive and i_{L_o} is negative. Current i_{L_o} flows through diode D_3 while the sum of reflected input voltage and V_{C_b} is across L_o . This causes i_{L_o} to increase until it reaches zero.
- **Configuration 8:** Forward and flyback conversion current have both reached zero amplitude and none of the diodes is in conduction. The load is purely fed by the output capacitance, and V_{C_b} does not change.

All operation modes i.e. sequences of configurations can be distinguished based on currents i_{L_M} and i_{L_o} . An overview of all modes and corresponding currents is presented in Fig. 3. Each interval is marked with a number, which corresponds to one of the circuit configurations depicted in Fig. 2.

a) Mode 1: This mode can be considered continuous conduction mode (CCM) of both magnetization and output inductor current. The steady-state analysis presented in section II applies to this mode. Boundary conduction mode (BCM) of magnetization current can be considered as a special case of operation mode 1, where the switching frequency f_{sw} is dynamically controlled such that i_{L_M} starts and ends at zero in one switching cycle T_{sw} .

b) Mode 2: Mode 2 can occur only for i_{L_M} in BCM. For some combinations of filter inductance value L_o and output current levels, the current ripple of i_{L_o} is larger than its average value, making i_{L_o} negative during a switching cycle. If the magnitude of i_{L_o} reaches that of the secondary magnetizing current $n \cdot i_{L_M}$, then the operating mode changes.

c) Mode 3: During BCM operation of i_{L_M} the input voltage may not be sufficient to forward bias diode D_1 . In this case, no direct power transfer occurs during the interval S is turned on. All output power is delivered through the flyback action and by output capacitor C_o .

In configuration 5 the inductors L_M and L_o form a series circuit, which causes a decreased rate of demagnetization of L_M and magnetization of L_o . The low rate of demagnetization of L_M restricts the switching frequency for BCM and thus

Fig. 3. Currents i_{L_o} , i_{L_M} , i_{sec} and i_{D_2} during one switching cycle of a specific mode. Each interval is marked with a number, which corresponds to a configuration. Note: signals are not drawn in the right proportions, the waveform shape is important.

decreases energy transfer around the zero crossings. This makes configuration 5 undesirable.

d) *Mode 4*: Mode 4 is an extension of mode 3 and can occur if a minimum T_{sw} is forced by the controller. The first three configurations of mode 3 and 4 are identical, but the circuit configuration changes to 8 when currents i_{L_M} and i_{L_o} reach zero and the minimum switching cycle time has not yet passed.

e) *Mode 5*: Mode 5 can occur for CCM operation of i_{L_o} . Current i_{L_o} is positive during a complete switching cycle. However, the amount of Volt-seconds across L_M causes i_{L_M} to end and start at a negative value.

f) *Mode 6*: An extension of mode 5 occurs if the magnitude of the negative magnetizing current $n i_{L_M}$ reaches the same level as current i_{L_o} at t_3 . In that case, a series circuit is formed and $i_{L_M} = n i_{L_o}$ during the remaining part of the switching cycle. In this last interval, no flyback or forward action current flows to the load.

g) *Mode 7*: Mode 7 is entered if current i_{L_M} is continuously positive or in BCM, and i_{L_o} has a ripple such that it becomes negative. Therefore, current i_{L_o} starts and ends at a negative value. This mode ends with configuration 2 if the magnitude of i_{L_o} is smaller than $n i_{L_M}$. Otherwise, D_2 stops conducting and circuit configuration 2 changes to 5, as in mode 8. During the interval from 0 to t_1 , i_{sec} is negative. This induces current at the primary side and contributes to the current i_{L_M} .

h) *Mode 8*: Mode 8 is an extension of mode 7 and is entered if current $n \cdot i_{L_o}$ reaches the same magnitude as i_{L_M}

during switch-off time. Diode D_2 then stops conducting, and L_M and L_o form a series circuit according to configuration 5. This mode can occur only if the magnetization current is not in BCM.

i) *Mode 9*: Mode 9 is a variation on mode 8 and can occur for i_{L_M} in BCM in combination with a minimum T_{sw} requirement. Again, the ripple on i_{L_o} makes the current smaller than zero which eventually leads to circuit configuration 5. However, after i_{L_M} and i_{L_o} reach zero, the requirement on T_{sw} is not yet met. Only after T_{sw} has passed, a new switching cycle is initiated.

j) *Mode 10*: This mode can be considered as the opposite of mode 9, because, instead of i_{L_o} , now i_{L_M} reaches a negative value. Mode 10 can occur only for non-BCM operation of i_{L_M} and with a minimum T_{sw} requirement.

It must be noted again that the steady-state analysis in section II only applies to operating mode 1. Therefore, only this mode is considered in the following sections, unless noted otherwise.

III. BALANCED FORWARD-FLYBACK CONVERTER DESIGN

A converter design is made based on a worst-case DC-DC conversion scenario. Minimum and maximum input voltage from a rectified mains voltage (120 V and 373 V for wide input voltage range), and maximum load are considered. An overview of design parameters is given in Table I and Table II lists the fixed parameters.

The converter is designed to have the flyback action current i.e. i_{L_M} in BCM. Compared to continuous conduction mode

TABLE I
DESIGN PARAMETERS

N_1	Number of primary turns	L_M	Magnetizing inductance
N_2	Number of secondary turns	L_o	Output inductance
n	Turns ratio (N_1/N_2)	C_o	Output capacitance
f_{sw}	Switching frequency	C_b	Balance capacitance

TABLE II
REQUIRED SPECIFICATIONS

Parameter	Description	Value
V_o	Output voltage	12 V
$P_{o,min}$	Minimum output power	15 W
$P_{o,nom}$	Nominal output power	60 W
$P_{o,max}$	Peak output power	100 W
$V_{d,min}$	Minimum DC input voltage	120 VDC
$V_{d,max}$	Maximum DC input voltage	373 VDC

(CCM) the magnetic core utilization is better in BCM (full quadrant vs. minor loop in B-H curve). Discontinuous current mode (DCM) offers equal core utilization, but current stress on components is higher than for BCM. Because the magnetization current i_{L_M} is forced into BCM, the set of possible modes is limited to 1, 2, 3, 6, 7 and 8. The output filter current i_{L_o} is designed to be in continuous conduction mode, because negative i_{L_o} leads to demagnetization of L_M at a low rate. This phenomenon can be observed in operating modes 2, 3, 4, 8, and 9. It is considered undesirable, because during this interval no power is delivered to the load.

BCM of flyback action current occurs if the current ripple $\Delta i_{L_M} = 2L_M$ where

$$\Delta i_{L_M} = \frac{V_d}{L_M} \delta T_{sw}. \quad (8)$$

Combining (8) with (5) leads to

$$I_{L_M} = \frac{\delta}{n(1-\delta^2)} I_o = \frac{V_d}{2L_M} \delta T_{sw}. \quad (9)$$

The switching cycle duration T_{sw} for BCM is obtained by calculating the time required for i_{L_M} to reach $2I_{L_M}$ (T_{on}) and, subsequently, decrease to zero again (T_{off}). This leads to an expression for the switching frequency as a function of output power

$$f_{sw}(P_o) = \frac{n(1-\delta^2)V_o}{2\delta L_M P_o \left(\frac{1}{V_d} + \frac{1}{n(V_o + \delta V_o)} \right)}. \quad (10)$$

Maximum input voltage and L_M determine the maximum switching frequency. The allowed frequency range is set from 20 to 200 kHz. An output power of 15 W at 373 V input voltage and $f_{sw}=200$ kHz would require a magnetizing inductance of 3.64 mH, according to (10). Since the magnetic core size increases with inductance, this high inductance value is undesirable. A compromise between functionality and reasonable magnetizing inductance value is reached by requiring the converter to operate in mode 1 at maximum input voltage for output power higher than 50 W. To satisfy this specification, $L_M=1.1$ mH. Fig. 4 depicts the dynamic

Fig. 4. Switching frequency f_{sw} for $L_M=1.1$ mH, $n=5$, DC input voltage of 120 to 373 V and output power between 15 and 100 W.

frequency for a range of input voltage and output power. In summary, each input voltage level has a minimum output power for which the converter works in operating mode 1. Below this limit other operating mode are active.

The turns ratio n of the primary and secondary transformer winding is chosen to balance the reverse voltage stress on switch S and diode D_2 . For decreasing n the reverse voltage across D_2 increases, while switch S suffers from an increasing reverse voltage. A winding ratio $n=5$ is chosen as a compromise. An iterative design process leads to a transformer design based on a ETD 34/17/11 core (3C90 material), winding ratio of 5 (60/12 turns), and L_M of 1.1 mH $\pm 10\%$ (0.203 mm airgap).

IV. PFC STUDY BASED ON SIMULATION RESULTS

The PFC functionality of the balanced forward-flyback converter has been simulated in software. A custom BCM controller implementation keeps the magnetizing current, i.e. flyback current, in boundary conduction mode by monitoring i_{D_3} . It also limits the switching frequency to the allowed range. A constant T_{on} controller regulates the switch on-time required to generate an output voltage of 12 V. The output voltage ripple due to lack of energy transfer during the AC zero-crossings is minimized by choosing $C_o=20$ mF.

Nominal load of 60 Watt at 12 V is simulated for a rectified sinusoidal input voltage. To analyze the wide input voltage range performance, this simulation has been performed with $v_d = 120 \sin(2\pi \cdot 60t)$ V and $v_d = 373 \sin(2\pi \cdot 50t)$ V. Results of the simulation are presented in Fig. 5 and Fig. 6. It is observed that i_{L_o} is in CCM, and i_{L_o} and i_{D_1} fall to zero around the zero crossings of the input voltage, which is in agreement with the theoretical analysis. Current i_{L_o} actually becomes negative and at that point operating modes other than mode 1 are active. Flyback action current i_{D_3} is almost a perfect sinusoidal, because i_{L_M} is linearly proportional to v_d . The input current i_d is a sum of i_{L_M} and i_{L_o} and, thus, cannot be a perfect sinusoidal. Furthermore, the switching frequency varies due to BCM of i_{L_M} and remains within the specified range. A low-frequent oscillation in i_{D_1} , i_{D_2} , i_{L_o} , i_d and V_{C_b} is observed in Fig. 6. This can be

TABLE III
PROTOTYPE COMPONENTS

Component	Type
S	Infineon IPA60R380C6 MOSFET (FullPAK)
D_1, D_3	ON Semiconductor MBR3320T3
D_2	ON Semiconductor NTSJ40120CTG (FullPAK)
MOSFET driver	ON Semiconductor NCP5181
C_b, C_o	Suncon HVH 56 μ F
L_o	Bourns PM2120-560K-RC 56 μ H
D_{sn}, D_h, D_l	STMicroelectronics STTH1R06A
R_{sn}	4.7 k Ω , 17 W
C_{sn}	82 nF, 520V PP film cap

explained by interaction between the secondary-side capacitors and inductors. Research is required to check if this effect is due to the applied control method and switching frequency limits, and whether an optimized controller in combination with feedback can suppress the oscillation. Empirically it is found that a smaller value of C_b can suppress the oscillatory behavior up to a certain level. An alternative component value selection can, thus, be a first step to a solution.

A Fourier analysis up to the tenth harmonic of the input current is used to calculate the total harmonic distortion (THD) of input current i_d . The results are a THD of 1.69% for 120V and 4.38% for 373 V. The latter result is expected to improve if the oscillations are suppressed.

Voltage V_{C_b} varies over a half-wave of the input voltage, as observed in Fig. 5 and Fig. 6, which can be explained by the varying contribution of forward and flyback conversion current. Around the zero-crossings of the input voltage, merely flyback action current flows. This current charges the balancing capacitor. However, once D_1 is forward biased and the forward conversion current can flow, V_{C_b} decreases. V_{C_b} reaches its maximum at the peak input voltage, where forward conversion current is maximal. As observed the average current through C_b over one switching cycle is zero on average.

Finally, the simulation results show that the balanced forward-flyback converter exhibits stable behavior when it leaves operating mode 1, as can be seen around the zero-crossings of the AC input voltage. Despite an unknown converter gain for these other operating modes, constant- T_{on} modulation seems an appropriate control method. Still, any mode other than 1 is actually undesirable, because it contains configurations where no energy is transferred to the load.

V. EXPERIMENTAL SETUP AND MEASUREMENT RESULTS

A prototype is built to verify the operation of the balanced forward-flyback converter. Components are chosen and manufactured according to the previously discussed design and are listed in Table III. Both an R-C-D snubber [12] and two-switch clamping circuit [13] have been implemented to allow for an efficiency comparison. The R-C-D snubber provides a clamp voltage of approximately 202 Volt using components R_{sn} , C_{sn} and D_{sn} . For the two-switch clamp a second, identical MOSFET is added in series with the primary winding and free-wheeling diodes D_h and D_l are added.

Fig. 5. Simulation results for a PFC application with $v_d = 120 \sin(2\pi \cdot 60t)$ V and nominal output power of 60 Watt. From top to bottom are depicted: i_{D1} , i_{D3} , i_{D2} , i_{L_o} , v_d , i_d , f_{sw} , v_o , v_{C_b} .

Fig. 6. Simulation results for a PFC application with $v_d = 373 \sin(2\pi \cdot 50t)$ V and nominal output power of 60 Watt. From top to bottom are depicted: i_{D1} , i_{D3} , i_{D2} , i_{Lo} , v_d , i_d , f_{sw} , v_o , v_{Cb} .

Fig. 7. Experimental result for $V_d=120V$, $P_o=60W$, flyback BCM, $f_{sw}=35.7kHz$, $\delta = 44.20\%$: MOSFET gate signal (20 V/div), MOSFET v_{DS} (500 V/div), i_{sec} (5 A/div), i_{D2} (5A/div), timescale 10 μs /div. This experiment corresponds to operating mode 1, as can be observed in Fig. 3(a).

Measurements are performed under two conditions i.e. minimum and maximum rectified input voltage (DC) and a nominal output power of 60 W. Additionally, other output power levels are tested to measure the conversion efficiency. The prototype operates in open-loop under conditions that, if not mentioned otherwise, the flyback current is in BCM.

The experimental result depicted in Fig. 7 shows the gate signal, MOSFET drain-source voltage, secondary transformer winding current i_{sec} and i_{D2} . The positive part of i_{sec} is the forward action current, which also flows through i_{D1} . The negative part is the flyback action current flowing through $D3$, which reaches zero before the next switching cycle (BCM). Diode $D2$ carries the freewheeling current i_{Lo} and flyback current i_{D3} while S is turned off. As can be seen in Fig. 3(a), this experiment corresponds to operating mode 1.

For verification of another operating mode, an experiment without BCM settings is conducted. In Fig. 8 the gate signal, V_{DS} , i_{sec} and i_{D2} are captured with non-BCM settings. As observed, i_{sec} does not end at zero current before the next switching cycle starts. This occurs if the magnetic core is fully discharged and the, theoretical, current i_{LM} switches polarity. Diode $D1$ comes into conduction again such that, in combination with $D2$ conducting, the secondary transformer winding voltage is clamped to V_{Cb} . This causes a positive secondary winding current and according to Kirchhoff's current law (KCL) an increased current i_{D2} . During this experiment the converter operated in mode 5, as can be observed in Fig. 3(e).

The experimental results of the efficiency measurement of the balanced forward-flyback converter with the R-C-D clamp and two-switch configuration are presented in, respectively, Table IV and Table V. Since a pre-prototype is used for experiments, the thermal design is not optimized.

With regard to improvement of the conversion efficiency

Fig. 8. Experimental result for $V_d=120\text{V}$, $f_{sw}=35.7\text{kHz}$, $\delta = 20.7\%$: MOSFET gate signal (20 V/div), MOSFET V_{DS} (500 V/div), i_{sec} (5 A/div), i_{D2} (5 A/div), timescale 10 $\mu\text{s}/\text{div}$. Non-BCM magnetization current. This experiment corresponds to operating mode 5, as can be observed in Fig. 3(e).

TABLE IV

INPUT, OUTPUT AND LOAD CONDITIONS FOR EFFICIENCY MEASUREMENT OF BALANCED FORWARD-FLYBACK CONVERTER IN BCM WITH R-C-D CLAMP

V_d [V]	Load [Ω]	P_{in} [W]	P_{out} [W]	Efficiency [%]
120	2.4	71.35	60.08	84.2
120	4.8	36.01	30.01	83.3
120	9.6	19.04	15.01	78.8
373	2.4	71.40	60.04	84.1

diode D_2 can be replaced by a synchronous rectifier MOSFET. This can almost reduce the conduction loss in the flyback action by half, because one diode is eliminated from this path. However, the effect of the switching loss of the synchronous rectifier requires additional research.

VI. CONCLUSION AND RECOMMENDATIONS

Boundary conduction mode of i_{LM} offers good transformer utilization, but requires a dynamically changing frequency. Therefore, it restricts the output power level if operation in mode 1 is required.

The simulation study of the PFC functionality has shown that the combination of the BCM and constant- T_{on} modulation actually offers good performance. Despite seven possible operation modes, which are considerably more than presented in [8], the converter exhibits quite linear behavior, also around the zero-crossings of the AC input voltage where it operates

in modes other than 1. However, a low-frequency oscillation appears for a 373 VAC input voltage. Empirically it was found that this oscillation can be suppressed by decreasing C_b . A controller with appropriate feedback may offer better suppression.

Finally, a dissipative R-C-D snubber and a two-switch clamp configuration were compared based on measurement results. Despite of a higher cost, at output power levels above 15 W a two-switch configuration is recommended. Compared to the R-C-D snubber it allows for a 4 to 9.4% higher overall efficiency.

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TABLE V

INPUT, OUTPUT AND LOAD CONDITIONS FOR EFFICIENCY MEASUREMENT OF BALANCED FORWARD-FLYBACK CONVERTER IN BCM WITH TWO-SWITCH CLAMP

V_d [V]	Load [Ω]	P_{in} [W]	P_{out} [W]	Efficiency [%]
120	2.4	68.12	60.05	88.2
120	4.8	33.55	30.0	89.4
120	9.6	17.08	15.06	88.2