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Citation for published version (APA):

Zheng, X., Raz, O., Calabretta, N., Zhao, D., Lu, R., & Yong, L. (2016). Multiport InP monolithically integrated all-optical wavelength router. *Optics Letters*, 41(16), 3892-3895. <https://doi.org/10.1364/OL.41.003892>

DOI:

[10.1364/OL.41.003892](https://doi.org/10.1364/OL.41.003892)

Document status and date:

Published: 15/08/2016

Please check the document version of this publication:

- A submitted manuscript is the version of the article upon submission and before peer-review. There can be important differences between the submitted version and the official published version of record. People interested in the research are advised to contact the author for the final version of the publication, or visit the DOI to the publisher's website.
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Optics Letters

Multiport InP monolithically integrated all-optical wavelength router

XIU ZHENG,¹ ODED RAZ,² NICOLA CALABRETTA,² DAN ZHAO,² RONGGUO LU,¹ AND YONG LIU^{1,*}

¹State Key Laboratory of Electronic Thin Films and Integrated Devices, School of Optoelectronic Information, University of Electronic Science and Technology of China, Chengdu 610054, China

²COBRA Research Institute, Eindhoven University of Technology, Eindhoven 5600 MB, The Netherlands

*Corresponding author: YongLiu@uestc.edu.cn

Received 17 June 2016; revised 21 July 2016; accepted 27 July 2016; posted 28 July 2016 (Doc. ID 268524); published 15 August 2016

An indium phosphide-based monolithically integrated wavelength router is demonstrated in this Letter. The wavelength router has four input ports and four output ports, which integrate four wavelength converters and a 4×4 arrayed-waveguide grating router. Each wavelength converter is achieved based on cross-gain modulation and cross-phase modulation effects in a semiconductor optical amplifier. Error-free wavelength switching for a non-return-to-zero $2^{31}-1$ ps pseudorandom binary sequence at 40 Gb/s data rate is performed. Both 1×4 and 3×1 all-optical routing functions of this chip are demonstrated for the first time with power penalties as low as 3.2 dB. © 2016 Optical Society of America

OCIS codes: (250.5300) Photonic integrated circuits; (060.4265) Networks, wavelength routing; (080.1238) Array waveguide devices; (250.5980) Semiconductor optical amplifiers.

<http://dx.doi.org/10.1364/OL.41.003892>

The exponential growth in network traffic is attracting growing research interest in photonic integrated circuits (PICs) in recent years [1,2]. By monolithically integrating multiple discrete components into a single PIC, an optical sub-system with reduced system footprint, power consumption, and enhanced efficiency is obtained [1,3]. Among the various materials for PIC fabrication, indium phosphide (InP), a direct bandgap material, processing matched lattice with ternary and quaternary compounds, is promising for the integration of active components such as lasers and amplifiers [4]. A number of photonic components with advanced functionalities on an InP platform have been realized in the past decades, such as transmitters, wavelength converters, receivers, and optical switches [5–8].

One of the key functionalities for future high-capacity wavelength division multiplexing networks is an all-optical router which can be integrated in a photonic network on chip implementation [9]. A wavelength router was realized with discrete semiconductor optical amplifier (SOA)-based wavelength converters and an arrayed-waveguide grating router (AWGR) [10]. The optical coupling losses and footprint of this router can be

significantly reduced by integrating these separate devices into a single PIC. An 8×8 SOA-based wavelength router chip was fabricated by combining the wavelength converters and an AWGR into a single InP chip [11]. Wavelength routing at a 40 Gb/s return-to-zero (RZ) signal was successfully demonstrated, where wavelength conversion was realized by using an SOA-based Mach–Zehnder interferometer (MZI) structure with an SOA in each arm of the MZI. Differential operation was used to overcome the slow recovery time of the SOA, thus enhancing the wavelength converting speed to 40 Gb/s for an RZ signal. The wavelength conversion had power penalties ranging from 4.5 to 7 dB.

In this Letter, we present a multiport monolithically integrated all-optical wavelength router chip based on an InP platform. To the best of our knowledge, this is the first structure to integrate a SOA-based wavelength converter, AWGR, and delay interferometer (DI) in a single PIC for the 40 Gb/s non-return-to-zero (NRZ) wavelength switching operation. The AWGR in the chip is also used as a blueshifted filter to compensate for the slow carrier recovery in the SOA, resulting in an optimized wavelength conversion. A similar wavelength conversion structure was demonstrated at 320 Gb/s using an SOA and other discrete components [12]. The details of the chip design are introduced and the operation principle is presented. Error-free operations of 1×4 and 3×1 wavelength routing at a 40 Gb/s line rate per port are finally demonstrated.

The schematic and the photonic integrated wavelength router is shown in Figs. 1(a) and 1(b), respectively. The wavelength router consists of several wavelength converters, an AWGR, and DIs. The function of the AWGR is to passively route the input signal from different ports to different destinations according to the input wavelength. The wavelength converter exploits nonlinear cross-gain modulation (XGM) and cross-phase modulation (XPM) effects in an SOA. The AWGR acts as a blueshifted filter, and the DI acts as a further filter. The fabricated integrated wavelength router in an InP/InGaAsP consists of an SOA array, a 4×4 AWGR, and two DIs with sizes of $4.6 \text{ mm} \times 1.85 \text{ mm}$, as shown in Fig. 1(b). After the AWGR, two waveguides are directly connected to the chip outputs, acting as monitoring ports to replace the other two DIs in Fig. 1(a). Besides, each of the two fabricated

Fig. 1. Multiport wavelength router. (a) Integrated wavelength router scheme. (b) Photograph of the fabricated $4.6 \text{ mm} \times 1.85 \text{ mm}$ chip, where the inset shows the SEM of the AWGR.

DIs has an additional monitoring output port, which is not shown Fig. 1(a). Each input port is designed to be 7-degree angled to reduce the facet reflection. This AR-coated PIC is fabricated by SMART Photonics B.V., the Netherlands, in a multi-project wafer (MPW) run of the JePPIX platform. This integration platform provides an active-passive integration technology, with a set of basic building blocks (BBBs) and standard fabrication processes. The PIC has three kinds of BBBs: passive waveguide devices, SOAs, and electro-optical phase modulators (EOPMs). For experimental stability, the fabricated chip is soldered to a copper block and wire bounded before experiments. During the operation, three tapered fibers are used to couple lights to and from the chip by utilizing two three-axis flexure platforms and one six-axis flexure platform. Coupling loss between fiber and chip is estimated at about 4.5 dB/facet.

The four input ports of the chip are first connected to four $2 \text{ }\mu\text{m}$ wide and 2 mm long shallow-etched SOAs, respectively. Here, each SOA active layer consists of an 84 nm thick layer with four quantum wells ($\lambda_{\text{bg}} = 1.55 \text{ }\mu\text{m}$; bg: bandgap) embedded between a 158 nm quaternary layer ($\lambda_{\text{bg}} = 1.25 \text{ }\mu\text{m}$) and a 208 nm quaternary layer ($\lambda_{\text{bg}} = 1.25 \text{ }\mu\text{m}$).

The input 40 Gb/s NRZ data signal at wavelength λ_i is combined with a continuous-wave (CW) probe light at λ_c and then injected into the integrated wavelength router. Then, the data signal depletes the carriers in the nonlinear SOA to make an inverted copy at λ_c based on the XGM effect, simultaneously modulating the refractive index which results in a phase change on the inverted copy via the XPM effect. As a result, a chirped converted signal with the inverted polarity is achieved.

The output of the SOA is connected to an AWGR with a channel spacing of 5 nm (625 GHz) and a free-spectral range (FSR) of 20 nm (2.5 THz). The AWGR is designed to be TE-polarized with the $4 \text{ }\mu\text{m}$ distance between the input waveguides, the $0.8 \text{ }\mu\text{m}$ gap between array waveguides at the star coupler, and the $1.5 \text{ }\mu\text{m}$ arrayed waveguide width.

The AWGR performance is measured by a forward biasing on-chip SOA with 80 mA to generate amplified spontaneous emission (ASE). Then, the output is fiber coupled to an optical spectrum analyzer (OSA) with a 0.06 nm resolution

Fig. 2. Output ASE response of the AWGR measured on 0.06 nm resolution bandwidth: (a) measured all outputs of the PIC by biasing only SOA2 and (b) measured only output 4 by biasing each SOA.

bandwidth. The spectral response measured at different outputs by biasing only one SOA2 is shown in Fig. 2(a). The split in the peaks shown in the ASE responses of the AWGR measured at output 1 and output 3 is due to the further filtering by the DIs. Figure 2(b) shows the resulting spectrum from one output by biasing the SOAs. The measured results show the AWGR with good performance of around 2 nm bandwidth, a crosstalk of -20 dB , and 20 nm FSR as designed.

After the SOA, the converted signal and the excess input signal are injected into the AWGR. Then, the converted signal is routed to a different output according to its wavelength, and the residual pump signal is filtered out. Meanwhile, by tuning the wavelength of the input probe light to the red side of one of the AWGR passbands, the AWGR is also used as a blueshifted filter to compensate for the slow gain recovery by utilizing ultrafast chirp dynamics of the SOA [12]. Thus, the pattern effect can be eliminated, resulting in an optimized converted signal. In our experiment, the converted 40 Gb/s signal has an optimized performance when the AWGR passband is blue-shifted 0.8 nm to the probe wavelength.

Then, the two outputs of the AWGR are directly connected to the chip output 2 and output 4, while the other two outputs are connected to two 1×2 DIs with different delay times. The DI configuration design is based on the scheme in [13]. Each DI consists of a 1×2 multi-mode interference (MMI) as a 3 dB splitter at the input, two 2 mm long EOPMs as phase shifter section on each arm and a 2×2 MMI as a 3 dB coupler at the output. The longer arm is designed to provide a 3.5 ps delay for DI1 and a 2.5 ps delay for DI2. As the two outputs of the DI transmit the same signal with a phase difference of π [13], only one output of the DI is required at each time, and the other output could be used as a monitor.

For the NRZ signal, the DI is used as a filter to further filter the excess pump signal. Thus, one DI transmission band is

Fig. 3. Experimental setup. TL, tunable laser; MOD, modulator; VOA, variable optical attenuator; PD, photodetector; BERT, BER tester.

centered at λ_c by adjusting the voltage of the DI, and the final converted signal out of the chip is still inverted.

The experimental setup for wavelength conversion and routing functions is sketched in Fig. 3. As the required four-channel fiber array for 4×4 wavelength routing is not available for the moment, only single-channel operation is realized in this Letter. The 40 Gb/s NRZ data is generated by the 40 Gb/s commercially available transmitter. A tunable laser at λ_s is modulated with a $2^{31}-1$ ps pseudorandom bit sequence. This 40 Gb/s data signal is further amplified with an erbium-doped fiber amplifier (EDFA) and filtered with a 2.92 nm bandpass filter (BPF). Then, the data signal is combined with a CW probe light at λ_c using a 3 dB optical coupler. The wavelength of the CW light is set to match with one of the AWGR transmission bands. Besides, as the employed four quantum wells for the SOA and AWGR are TE-polarization sensitive, polarization controllers (PC1 and PC2) are utilized to set proper polarizations of the input signal and the probe light, respectively, before injecting into the PIC. The output is then transmitted to a commercially available receiver for the 40 Gb/s bit error rate (BER) measurements. The power meter is applied to measure the output power of the converted signal.

The optical spectra and BER performance for 40 Gb/s wavelength switching from a single input to several outputs are shown in Figs. 4(a) and 4(b), respectively. The average powers at the chip input port are around 8.3 dBm for the data signal and 3.7 dBm, 3.6 dBm, 1.9 dBm, and 1.8 dBm for the CW light with the SOA current biased at 408 mA, 415 mA, 409 mA, and 410 mA when $\lambda_c = 1537.2$ nm, 1532.2 nm, 1547.2 nm, and 1537.2 nm, respectively. The results show the 1×4 routing function of the PIC by tuning the wavelength of the input probe light every 5 nm which is the same as the channel spacing of the AWGR to route the input data signal at 1549.2 nm from one constant input port (input 2) to different output ports. The power penalty at a BER of 10^{-9} with respect to the back-to-back input signal is 3.6 dB, 3.6 dB, 3.9 dB, and 3.6 dB when $\lambda_c = 1537.2$ nm, 1532.2 nm, 1547.2 nm, and 1537.2 nm, with a converted output power of 1.4 dBm, 0.1 dBm, -1.7 dBm, and 4.4 dBm, respectively.

Besides, the optical spectra and BER performance for wavelength switching from several inputs to a single output at 40 Gb/s are also obtained, shown in Figs. 5(a) and 5(b), respectively. The average powers at the chip input port are around 8.4 dBm, 8.9 dBm, and 8.6 dBm for the data signal and 2.6 dBm, 5.5 dBm, and 3.8 dBm for the CW light with the SOA current biased at 396 mA, 410 mA, and 400 mA when $\lambda_c = 1547.2$ nm, 1542.2 nm, and 1537.2 nm, respectively. In principle, 4×1 wavelength routing is possible based on the

Fig. 4. Measured (a) optical spectra on 0.16 pm resolution bandwidth and (b) BER performances of 40 Gb/s wavelength switching from input 2 to four different output channels. Insets: the associated eye diagrams for the converted signals and the original pump signal. Output 1, $\lambda_c = 1537.2$ nm; output 2, $\lambda_c = 1532.2$ nm; output 3, $\lambda_c = 1547.2$ nm; output 4, $\lambda_c = 1537.2$ nm.

device. Unfortunately, the input waveguide for input 4 was damaged during testing. Therefore, the measured results show the 3×1 routing function of the PIC by tuning the wavelength of the CW with 5 nm channel spacing to route the input data signal at 1550.1 nm from different input ports to one constant output port (output 4). Regarding $\lambda_c = 1547.2$ nm, 1542.2 nm, and 1537.2 nm, a power penalty of 3.7 dB, 3.6 dB, and 3.2 dB with the converted output power of 2.5 dBm, 1.3 dBm, and 4.4 dBm is achieved, respectively.

In our experiment, the BER performance of each converted signal is optimized by adjusting the input powers and polarizations of the pump signal and CW light, as well as the injection current of the SOA. In addition, the coupling loss of each port is not identical. As a result, the converted output powers are different.

Wavelength conversion at 40 Gb/s with a different pattern length is also investigated. The BER performance in Fig. 6 shows that the long pattern length of $2^{31}-1$ ps leads to over 1 dB power penalty compared with that of 2^7-1 ps pattern length.

The power penalties range from 3.2 to 3.9 dB, depending on the different CW wavelengths and input ports, which could be attributed to three main impairments. First, the extinction ratio (ER) is around 10.5 dB for the input pump signal and around 6 dB for the converted signal. According to the relationship between the power penalty and the ER shown in [14], the 4.5 dB ER degradation leads to around 1 dB power penalty. Second, the power penalties are also attributed to the influence

Fig. 5. Measured (a) optical spectra on 0.16 pm resolution bandwidth and (b) BER performances of 40 Gb/s wavelength switching from different inputs to output 4. Insets: the associated eye diagrams for the converted signals and one original pump signal. Input 1, $\lambda_c = 1547.2$ nm; input 2, $\lambda_c = 1542.2$ nm; input 3, $\lambda_c = 1537.2$ nm.

Fig. 6. BER performance of 40 Gb/s wavelength conversion from input 2 to output 4 with different pattern length.

of the residual pump signal. However, for the good performance of the AWGR with a crosstalk less than -20 dB, most of the residual pump signals are well filtered. However, there is still some residual pump signal. In fact, a higher power penalty

is observed when the wavelengths of the pump signal and the probe CW light are too close, as proved when wavelength conversion from input 2 to output 3 ($\lambda_s = 1549.2$ nm, $\lambda_c = 1547.2$ nm). Third, some unwanted noise is caused by the reflection between the angled input and straight output and other internal reflections caused by the fabrication defect inside the SOA, leading to an increased BER. All angled ports in future designs are expected to have better performance.

In summary, we report on a novel InP-based monolithically integrated chip for wavelength routing of 40 Gb/s NRZ data signals. Error free in 1×4 and 3×1 wavelength routing for $2^{31} - 1$ NRZ signal with an inverted operation is demonstrated with a power penalty as low as 3.2 dB. The obtained good performance makes the integrated wavelength router very promising for application in the future optical networks. In addition, this chip utilizes BBB-based integration technology and is realized on a generic InP integration platform, which gives the potential of fabricating a broad range of functionally advanced PICs with reduced fabrication cost.

Funding. KNAW The Netherlands China Exchange Program (12CDP008); National Natural Science Foundation of China (NSFC) (61090393, 61421002).

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