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Citation for published version (APA):

DOI:
10.1063/1.4960096

Document status and date:
Published: 25/07/2016

Document Version:
Publisher’s PDF, also known as Version of Record (includes final page, issue and volume numbers)

Please check the document version of this publication:

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Citation: Appl. Phys. Lett. 109, 043301 (2016); doi: 10.1063/1.4960096
View online: http://dx.doi.org/10.1063/1.4960096
View Table of Contents: http://aip.scitation.org/toc/apl/109/4
Published by the American Institute of Physics
Dielectric interface-dependent spatial charge distribution in ambipolar polymer semiconductors embedded in dual-gate field-effect transistors

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(Received 21 March 2016; accepted 17 July 2016; published online 28 July 2016)

The spatial charge distribution in diketopyrrolopyrrole-containing ambipolar polymeric semiconductors embedded in dual-gate field-effect transistors (DGFETs) was investigated. The DGFETs have identical active channel layers but two different channel/gate interfaces, with a CYTOP™ organic dielectric layer for the top-gate and an octadecyltrichlorosilane (ODTS) self-assembled monolayer-treated inorganic SiO2 dielectric for the bottom-gate, respectively. Temperature-dependent transfer measurements of the DGFETs were conducted to examine the charge transport at each interface. By fitting the temperature-dependent measurement results to the modified Vissenberg–Matters model, it can be inferred that the top-channel interfacing with the fluorinated organic dielectric layers has confined charge transport to two-dimensions, whereas the bottom-channel interfacing with the ODTS-treated SiO2 dielectric layers has three-dimensional charge transport.

Solution-processable organic ambipolar semiconductors, wherein both p- and n-type charge transport can occur, are attracting significant research interest because of their advantages that potentially allow easy fabrication of light-emitting transistors or inverting logic circuits.1–5 A promising class of organic materials for such ambipolar characteristics is based on diketopyrrolopyrrole (DPP)-containing copolymers that consist of DPP-acceptor and a large variety of donor blocks and exhibit a high mobility up to >10 cm2/V s, as has been reported by several groups.6 An improved understanding of the physical properties of ambipolar charge transport is required in order to expedite progress in the performance of DPP-based organic electronic applications. For this purpose, Kronemeijer et al. recently reported the confined two-dimensional charge-transport behavior in top-gated field-effect transistors, wherein organic gate dielectrics were located on the top of the semiconducting layers, and several polymeric semiconductors, including DPP-based polymers, were used as active channel materials.7 However, their results contradicted those reported by Brondijk et al., who observed that SiO2 bottom-gated field-effect transistors with polymer semiconductor films are well-described by the three-dimensional charge transport model.7,8

In order to address these conflicting observations, we study the charge transport properties of DPP-based ambipolar semiconducting polymers embedded in dual-gate field-effect transistors (DGFETs) comprising two separate dielectric/semiconductor interfaces in a single transistor.9,10 In fact, the DGFET structure is the best platform for studying the effects of different dielectrics upon device performance with minimal influence from external parameters, such as sample-to-sample variation, because the devices share an identical active semiconductor layer.9,10 In the present work, we perform temperature-dependent transfer-curve measurements on the DGFETs in the range of 120–260 K. Based on these measurements, we analyze the spatial charge-transporting behavior of holes in the active DPP-based semiconducting layer interfacing with the organic top-gate (TG) and SiO2 bottom-gate (BG) dielectric layers. We also correlate key charge-transport parameters with the dielectric layers that we have studied.

Figure 1(a) shows a schematic of the DGFETs and the chemical structure of poly[(diketopyrrolopyrrole)–alt–(2,2′-(1,4-phenylene)bisthiophene)] (PDPPTPT) used as an active channel material.11,12 Fabrication of the DGFETs starts with a heavily doped (n+++) Si substrate that also serves as a bottom-gate electrode. On the top of the Si substrate, a 200 nm-thick silicon dioxide (SiO2, εr = 3.9) dielectric layer with a capacitance of 17 nF/cm2 is thermally grown. For the source and drain (S/D) electrodes, a 30 nm-thick gold (Au) layer with a

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FIG. 1. (a) Schematics of the transistor and the chemical structure of the PDPPTPT used in this study. Deionized water contact angles with (b) ODTS-treated SiO2 and (c) CYTOP surfaces.
5 nm-thick titanium (Ti) adhesion layer is thermally evaporated onto the SiO₂ surfaces and photolithographically patterned. The width and length of the comb-shaped interdigitating S/D electrodes are 5 mm and 10 μm, respectively.

To passivate hydroxyl groups on the SiO₂ surfaces that are known to act as electron-trap sites, the substrate is immersed in a 10 mmol octadecyltrichlorosilane (ODTS)-concentrated n-hexane solution for 30 min after UV-ozone cleaning. The substrate is then rinsed with ethanol and baked for 30 min at 120 °C in ambient air to accelerate the surface reaction. The ODTS monolayer on top of the SiO₂ surfaces has a contact angle of >104°, as shown in Figure 1(b). Next, the PDPPTPT (synthesized according to a previously reported procedure) is spin-coated from a 10 mg/ml solution in hot chloroform, and the semiconducting polymer films are annealed at 200 °C for 30 min in the glove box with an atmosphere <0.1 ppm oxygen and water. The PDPPTPT-based polymer film’s thickness, as measured by atomic force microscopy, is ~50 nm. Subsequently, a fluorinated polymer, CYTOP™ (εr = 2.1, purchased from Asahi Glass Co.) is spin-coated and annealed at 150 °C in vacuum for 24 h to be used as a top-gate dielectric layer. The thickness of the CYTOP dielectric layer is ~750 nm, resulting in a capacitance of ~2.4 nF/cm², and the surface of the CYTOP layer has a contact angle of >110° (Figure 1(c)), which indicates the highly hydrophobic state of the CYTOP layer. Finally, the top-gate electrode is applied by thermally evaporating Au (50 nm) through a shadow mask. The DGFETs were characterized using a Keithley 4200-SCS semiconductor analyzer connected to a Desert Cryogenics vacuum probe station with a chamber pressure below 10⁻⁷ Torr at room temperature (RT).

The electrical characteristics of the DGFETs are shown in Figure 2. For both the TG and BG channels, the typical transfer and output characteristics of ambipolar operating behavior are observed. In particular, Figures 2(a) and 2(b) show the transfer characteristics of both channels for positive and negative drain biases (V_D), which have symmetric V-shaped curves indicating the transition from n- to p-type and vice versa. A large ON/OFF ratio of >10⁴ at |V_D| = 20 V for both channels is found in their transfer curves. From the slope of negative V_G vs. |V_D|, the hole-mobility of the saturation region is calculated to be ~0.39 and ~0.06 cm²/V s for the TG and BG channels, respectively, and the electron mobilities extracted from the slope of positive V_G vs. |V_D| are ~0.18 and ~0.06 cm²/V s for TG and BG, respectively. For both hole and electron transport, the charge-carrier mobility in the TG channel is more than three times higher than that in BG channel, although the thermally grown SiO₂ BG dielectric has a higher capacitance value compared with the CYTOP TG dielectrics, resulting in a substantially larger field-induced charge density in the BG channel. The origin of the different charge carrier mobilities will be discussed later. Figures 2(c) and 2(d) show the output characteristics with proper saturation at high gate biases. However, particularly for the electron-accumulation mode, we also observe a super linear drain current increase at low gate biases (|V_G| ≤ 50 V). In this bias condition, the minority carriers (i.e., holes in the n-type mode and electrons in the p-type mode) flow dominantly as the drain also works as a source when the |V_GD| is larger than |V_GS|.

In order to further examine the charge transport, temperature-dependent transfer-measurements were conducted on the PDPPTPT-based DGFETs in the range of 120–260 K. Figures 3(a) and 3(b) show the measured temperature-dependent transfer curves at a V_D of −40 V in the TG and BG channels, respectively. We note that the drain currents of the output curves shown in Figures 2(c) and 2(d) display a non-linearity at low drain-bias conditions (i.e., in the linear regime) due to poor charge injection that is generally found in DPP-containing polymer-based ambipolar transistors with single Au S/D contacts. Therefore, we measure the drain currents of the DGFETs in the saturation region of V_D = −40 V to minimize potential errors. As expected in thermally activated transport, the charge-carrier mobilities of both electrons and holes increase with increasing temperature. Figures 3(c) and 3(d) show plots of the charge-carrier mobility versus inverse temperature for both hole- and electron-accumulation modes with |V_GD| = 40 V, respectively. The hole mobilities of both channels are calculated to be 0.40 and 0.06 cm²/V s for the TG and BG channels, respectively. The electron mobilities extracted from the slope of positive V_G vs. |V_D| are ~0.18 and ~0.06 cm²/V s for TG and BG, respectively. For both hole and electron transport, the charge-carrier mobility in the TG channel is more than three times higher than that in BG channel, although the thermally grown SiO₂ BG dielectric has a higher capacitance value compared with the CYTOP TG dielectrics, resulting in a substantially larger field-induced charge density in the BG channel. The origin of the different charge carrier mobilities will be discussed later. Figures 3(c) and 3(d) show the output characteristics with proper saturation at high gate biases. However, particularly for the electron-accumulation mode, we also observe a super linear drain current increase at low gate biases (|V_G| ≤ 50 V). In this bias condition, the minority carriers (i.e., holes in the n-type mode and electrons in the p-type mode) flow dominantly as the drain also works as a source when the |V_GD| is larger than |V_GS|.

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density profile in the accumulation layer that decreases quadratically with distance from the dielectric.\textsuperscript{15} For the analysis of self-assembled monolayer transistors, however, Brondijk \textit{et al.} revised the analytical model with a two-dimensional carrier-distribution profile in the accumulation layer of the transistor, in which the charge density is constant up to a certain limited thickness from the dielectric.\textsuperscript{7,8} Recently, Kronemeijer \textit{et al.} modified the Vissenberg–Matters model again to be appropriate to the charge transport in the saturation regime of the transistors as follows:\textsuperscript{7}

\[
I_D^2D = A \frac{W}{L} d_{sc}^{-(T_0/T)} \left( \frac{C_i}{\varepsilon} \right) \frac{T}{T_0 + T} (V_G - V_i)^{(T_0/T)+1},
\]

\[
I_D^3D = A \frac{W}{L} \left( \frac{1}{2K_0 T_0 \omega L} \right) \left( \frac{T_0/T}{a} \right)^{T_0/T} C_i^{2T_0/T-1} 
\times \frac{T}{2T_0} \left( T + \frac{1}{T_0} \right) (V_G - V_i)^{2T_0/T},
\]

with

\[
A = \sigma_0 \left( \frac{T_0}{T} \right)^4 \sin \left( \frac{\pi}{2} \frac{T}{T_0} \right) \Gamma_{2D},
\]

where $T_0$ is the characteristic width of the exponential density of states, $\alpha^{-1}$ is the wave-function overlap localization length, $\sigma_0$ is a conductivity prefactor, and $B_c$ is the critical number for the onset of percolation. The parameter $d_{sc}$ is the thickness of the confined two-dimensional charge sheet. More importantly, the above complicated equations are reduced to an approximate power-law dependence of the source-drain current on the gate voltage without the Taylor expansion. Consequently, both the two- and three-dimensional models lead to direct power laws, i.e., $I_D \propto a (V_G - V_i)^\gamma$, where $a$ is a fitting constant that comprises several physical parameters (e.g., $A$ in Equation (3) and device geometry factors) and the exponent $\gamma$ is a function of temperature (e.g., $\gamma_{2D} = (T_0/T) + 1$ and $\gamma_{3D} = 2T_0/T$ in the saturation regime), which carries information about the spatial charge-transport behavior.\textsuperscript{7,8}

Figures 4(a) and 4(b) show plots of the temperature-dependent transfer curves on a double logarithmic scale for the TG and BG channels, respectively. We note that there are instabilities of the turn-on voltages and drain-gate leakage currents that are slightly greater than the source-drain currents at the elevated temperature for the electron-accumulation mode.\textsuperscript{19} For this reason, only hole-transport is analyzed using the modified Vissenberg–Matters model. Solid lines are obtained for all temperatures by fitting the measured data to the reduced power-law dependence of the source-drain current as a function of the gate-overdrive voltage ($V_G - V_i$), where the $V_i$ values were $-1.5$ V and $-11$ V for the TG and BG channels, respectively. The $\gamma$ value is also extracted from the measured transfer curve for each temperature and is then plotted against inverse temperature $(1/T)$.\textsuperscript{7,8,15} Figure 4(c) shows the $\gamma$ versus $1/T$ plots constructed for both the TG and BG channels. The extrapolated line of the TG channel crosses the exponential axis at a value of 1, indicating that the two-dimensional charge-carrier profile is presented in the top-channel, whereas the extrapolated line of
where we use fluorinated organic layers with a relatively low contact angle measurement (Figure 1(b)), we assume that the interfacial states of both channels have similar quality; thus, we infer that differences in the electrostatic interaction with the dielectrics, the fluorinated organic CYTOP layer with a low dielectric constant induces a relatively small number of charge carriers mobility of the TG channel with higher thermal activation energy could not be explained.

Compared with the ODTS-treated SiO2 dielectrics, the fluorinated organic CYTOP layer with a low dielectric constant induces a relatively small number of charge carriers in the TG channel under the same bias condition onto the BG dielectric layer. Although this small number of charges is insufficient to fill the adjacent trap sites and leads to a higher thermal activation energy, the narrow width of the density of the states resulting from the electrostatic interactions with the low-k organic TG dielectrics allows an efficient hopping process of the induced charges; this results in the higher charge-carrier mobility of the TG channel.

In summary, we have investigated the spatial charge transport properties in a PDPPTPT-based ambipolar polymeric semiconductor embedded in a DGFET consisting of two separate dielectric/semiconductor interfaces in a single transistor. Temperature-dependent measurement results on the TG channels interfacing with the low-dielectric constant organic fluorinated insulating layer are compared with the results obtained from the BG channel contact with ODTS-treated SiO2 dielectrics. The modified Vissenberg–Matters model indicates that the top-channel has a two-dimensional charge-distribution profile, whereas the bottom-channel has a three-dimensional charge distribution.

This work was supported by Holst Centre and the Basic Science Research Program through the National Research Foundation (NRF) funded by the Ministry of Science, ICT, and Future Planning of Korea (Code No. 2015R1C1A1A02037534). The authors wish to acknowledge the helpful comments of Dr. Auke J. Kronemeijer at Host Centre.


TABLE I. Summary of key charge transport parameters: room-temperature mobility $\mu_{RT}$, activation energy $E_a$, width of the density of localized states $k_0T_0$, and information about the dielectric layers.

<table>
<thead>
<tr>
<th>Channel</th>
<th>Dielectric ($\varepsilon_r$)</th>
<th>$\mu_{RT}$ (cm²/V s)</th>
<th>$E_a$ (meV)</th>
<th>$k_0T_0$ (meV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Top</td>
<td>CYTOP (2.1)</td>
<td>0.18</td>
<td>51</td>
<td></td>
</tr>
<tr>
<td>Bottom</td>
<td>SiO2 (3.9)</td>
<td>0.06</td>
<td>49</td>
<td>29.5</td>
</tr>
</tbody>
</table>

FIG. 4. Replotted transfer characteristics of (a) the TG channel and (b) the BG channel on a double-logarithmic scale. Black solid lines are fits to extract the parameter, $\gamma$, for each temperature. (c) Extracted values of $\gamma$ for the TG and BG channels plotted against inverse temperature. The extrapolated dashed linear fit yields the intersection with the exponential axis.


See supplementary material at http://dx.doi.org/10.1063/1.4960096 for the VG versus ID and IG curves of the dual-gate field-effect transistors at each temperature, ranging from 120 K to 260 K.
