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Ferroelectric phase separated memory diodes from morphology to electrical properties

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Ferroelectric phase separated memory diodes
from morphology to electrical properties

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Abstract

The ferroelectric phase separated blend diode is a novel non-volatile memory device which combines the properties of ferroelectrics and semiconductors. The polarization-modulated injection barrier for charge carriers allows convenient resistive readout of the ferroelectric switching. It is considered to be potentially an important component in future organic RFID devices.

We successfully fabricated the memory diode with F8BT as semiconductor and P(VDF-TrFE) as ferroelectric. Thin films of the polymer blend showed lateral phase separation influenced by the substrate, characterized by vertical F8BT columns in a P(VDF-TrFE) matrix. Due to the effect of the surface energy, the F8BT columns have shown a tendency to fall down and wet the Au substrate during the annealing. Via the study, a scheme has been proposed to describe the whole process for the formation of morphology. Numerical simulations have been done on the basis of observed morphology to analyze the carrier injection and transport. Proposed models take into consideration the surface morphology of the columns and possible subsurface features as well. It is discovered that the shape of the F8BT column determines the location of ferroelectric charges, which in turn directly influences the carrier injection. Analysis has been given regarding the optimum morphology for a device. Electrical characterization has also been performed. The electrical characteristics are found to be affected by the blend morphology as expected. The diode shows limited endurance and retention time. We also proposed and tried various ways to identify the root for such relatively poor performance.
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Chapter 1 Introduction

1. 1. Materials and related electrical properties

1. 1. 1 Ferroelectrics

A dielectric is an electrical insulator which can be polarized by an applied electric field [1]. The polarization is caused by a displacement of positive and negative charges. This induced polarization also creates a so-called depolarization field, an electric field in the opposite direction, which tends to bring the displaced charges back to their equilibrium position after removing the external field. Normally upon the withdrawal of the external electric field, polarization also disappears along with the electric dipoles.

Ferroelectrics refers to a special form of dielectric material which can retain the electric polarization even after the external field is withdrawn [2] [3]. The remnant polarization is reversible by an applied external electric field in the opposite direction. This critical electric field for reversing the polarization is called the coercive field. As a consequence, if the electric displacement ($D$) as a function of field strength ($E$) is drawn for a ferroelectric, a hysteretic curve ($D$–$E$ loop) will be formed between opposite polarities, which differs from most non-ferroelectric dielectrics whose polarization response is nearly linear. This difference is clearly demonstrated in Figure 1-1.

Ferroelectrics are all crystalline materials since only crystal structure is possible to give intrinsic dipole moments in highly ordered orientation, yielding a non-zero net polarization. For many ferroelectrics, a phase transition takes place at a certain temperature called the Curie temperature. Above the Curie temperature the ferroelectricity disappears due to a change of the crystalline structure from the low temperature polarized state to a high temperature unpolarized state.

![Figure 1-1](image)

Figure 1-1 Comparison between normal dielectric materials and ferroelectrics. (a) the D-E loop of a typical dielectric material (b) the D-E loop of a ferroelectric material. [4]
This electric bistability of ferroelectrics can be used for non-volatile memory elements. For example, ferroelectric random access memory (FeRAM) and ferroelectric field-effect transistors are subjects being studied for practical application. [4]

1.1.2 Ferroelectric polymers

Ferroelectric polymers have been the interest of a lot of studies and regarded as promising materials for use in nonvolatile data storage due to their low cost, high performance, chemical stability, and environmental compatibility. They can usually be solution-processed into a thin film, which is compatible to organic electronics devices processing.

Most of the research activity surrounding ferroelectric polymers is focused on PVDF [polyvinylidene fluoride; (CH2CF2)n] and its copolymer P(VDF-TrFE) [poly(vinylidene fluoride-trifluoroethylene); (CH2CF2)n-(CHFCF2)m].

![Structure of the PVDF and its copolymers](image)

**Figure 1-2** Structure of the PVDF and its copolymers (a) structure of all-trans conformation consisting of the carbon backbone with attached fluorine and hydrogen atoms (b) The crystal structure of the ferroelectric β phase polymer chains are viewed end-on, showing the quasi-hexagonal close packing of the polymer chains. [6]

As shown in **Fig 1-2(a)**, the VDF molecules in the polymer chains of PVDF and P(VDF-TrFE) have net dipole moments pointing from the electronegative fluorine to the electropositive hydrogen. These chains can crystallize in parallel rows [**Fig. 1-2(b)**] and, a macroscopic polarization appears when the dipoles of all chains are aligned along a twofold crystalline axis in a ferroelectric state. The polarization can be switched by applying a large reverse electric field.

Normally, PVDF that is processed from the melt or from a solution needs extra steps such as stretching to force the polymer in to the right conformation for ferroelectricity. For P(VDF-TrFE), these steps could be replaced by simply an annealing step at 140 °C, which enhances the crystallinity of the semicrystalline polymer, and hence its ferroelectric response.
An artistic illustration of the dipole switching in PVDF. On the left, the larger fluorine atoms are on top of and the dipole moment points upwards. Towards the right, with the opposite electric field, the molecule rotates around its axis, resulting in a downward dipole moment.

1.1.3 Organic semiconductors

A semiconductor has an unoccupied valence band and full conduction band, but its band-gap is relatively small, which accounts for its properties between an insulator and a metal. At absolute zero temperature, it behaves like a perfect insulator, while at room temperature it exhibits finite conduction due to thermal excitation of electrons. With their highly tunable conductivity and other attractive properties, semiconductor materials have found various applications in modern electronics.

Originally the semiconducting property was only found in inorganic elements or compounds, and organics were thought to be insulators. But a breakthrough came when it was discovered that some polymers could also be (semi)conductive. Now, different organic semiconducting materials found include single molecules, short chain (oligomers) and organic polymers. In this thesis, the major topics revolve only around polymers.

The origin of semiconducting behavior in some polymers is conjugation, which refers to a framework of alternating single and double carbon-carbon bonds. Ideally the overlap of adjacent p\textsubscript{z} orbitals of each carbon atom in such system can result in a \pi-band that consists of delocalized electrons and an empty \pi^* -band. The filled \pi -band is called the Highest Occupied Molecular Orbital (HOMO), and the empty \pi^* -band is called the Lowest Unoccupied Molecular Orbital (LUMO). The small bandgap (1-4eV) makes the polymer an intrinsic semiconductor of which the charge transport mechanism might be expected to resemble that of the inorganic ones.
However, in reality, a semiconducting polymer is not a perfect conjugated system due to the spatial and energetic disorder caused by twisted and kinked chains and chemical defects. The ideal of band conduction by delocalized charges doesn’t hold any more. Instead, charge carriers must travel between localized states (inter- or intra-chain transitions) via hopping, tunneling and other related mechanisms. This usually leads to very low carrier mobility. Despite the absence of “real” bands, the concepts of HOMO and LOMO are still kept to indicate the average position of the dispersed energy levels.

Apart from being an interesting subject in scientific study, organic semiconductors are also promising in terms of industrial application. They have many desirable features including easy fabrication, mechanical flexibility, and the potential of a low cost of the final product. As compared to crystalline inorganic semiconductors they remain strongly limited by their low carrier mobility and sometimes a short life-time. That is why they are expected to find a different role to play in electronics devices compared with conventional inorganic materials.

Rigid-backbone organic semiconductors have now already been used as active elements in optoelectronic devices such as organic light-emitting diodes (OLEDs), organic solar cells, organic field-effect transistors and more recently bio-sensors. With the advancement of technology, more novel applications and devices of lower cost would hopefully emerge in the future.

1.1.4 Charge injection and transport

For functional electronic devices, the most important issues include charge carrier injection and transport. For semiconductors with a low mobility like the conjugated polymers, the injection of carriers could be influenced by transport away from the metal contact as well as by the energy barrier at the interface.

The interface energy barrier of a metal-organic contact originates from the energy difference between the Fermi energy level of the metal and the molecular orbital energy level of the semiconductor (LUMO for electrons and HOMO for holes).

The charge carriers need to overcome such interface barrier to get into the bulk semiconductor material and drift away under applied electric field. There is a number of models that try to explain this injection process, including the classic Fowler-Nordheim tunneling and Richardson–Schottky thermionic emission, which describe the two types of basic behavior in simple scenarios, and some more advanced models based on hopping injection which takes the effect of disorder into account.
The metal-organic semiconductor contact can fall into two different types, considering its influence on charge transport. To make the case simple, the discussion is limited to unipolar transport. If the energy barrier is so large that the supply of carriers cannot achieve the maximum the semiconductor material can support, the contact is called an injection-limited contact, and the corresponding current injection-limited current. On the contrary, if the injection barrier is low or zero, the contact can be approximated as an infinite reservoir capable of providing unlimited number of charge carriers, which is called an Ohmic contact. In this case, the limiting factor for the charge transport in organic material is the built up of space charge which is setting up the electric field, and the current is called space-charge limited current (or bulk-limited current).

The classification above only considers two extreme cases. In reality, the distinction is not very sharp between bulk-limited and injection limited transport and there is always a grey area where both factors can be in effect. Normally polymer semiconductors have a high degree of disorder, which broadens the distribution of localized HOMO and LUMO levels and complicates the definition of an injection barrier. According to theoretical calculations, for a contact barrier $\phi_b < 0.3\text{eV}$, the current is mainly determined by the electrostatics due to the space charge rather than the energy barrier at the metal-semiconductor interface. In this case, the current can be regarded as space-charge limited current (SCLC), and the contact an Ohmic one. Naturally with $\phi_b > 0.3\text{eV}$, the current that the contact can supply is mainly limited by injection and smaller then SCLC and hence experimentally called injection-limited current.

1.2 Processing and related mechanisms

1.2.1 Polymer blends

Blending two or more polymers is a very established and useful technology to achieve special structural or physical properties. Polymers are generally immiscible because mixing only results in increased free energy (enthalpy of mixing is positive and entropy is small) and doesn’t occur spontaneously. As a result, when two polymers are blended together, they are most likely to demix to form separate co-
existing phases [8]. Such phase separation usually takes place when the system is cooled down or the amount of solvent is reduced (when dissolved in a common solvent). If the process is fast enough, the system may not reach its equilibrium but freezes into a solid while still in an intermediate state. That is why the final state of the blend is often depending on process conditions.

Spin-coating is a commonly used method to prepare a thin film polymer blend, a process in which solvent quenching induced phase separation happens. Lateral phase domains are expected to be formed when no blend component wets the surface or substrate. This could result in different morphologies depending on the relative ratio of two components. However, if interface energy plays an important role, surface-directed effects or stratification will occur. Very different blend morphologies can be obtained by varying the spin-coating conditions, the substrate and/or the composition of the solvent.

So far, the phase separated polymer blend has been used in organic electronic devices such as solar cells and diodes. A lot of interest has been devoted to controlling the blend morphology since it has proved to be an important factor for the device performance.

![Possible morphologies resulting from lateral phase separation of a two polymer system](image)

**Figure 1-6** Possible morphologies resulting from lateral phase separation of a two polymer system (a) an interpenetrating network of two different phases (b) Columns of one phase embedded in another phase

1.2.2 Spinodal decomposition

Spinodal decomposition is a mechanism of phase separation, by which a solution of two or more components can separate into distinct phases with distinctly different chemical compositions and physical properties [9]. Different from classical nucleation characterized by the discrete nucleation sites, spinodal decomposition occurs uniformly throughout the material.

As a special kind of phase transition, spinodal decomposition occurs under some certain conditions, which can be illustrated in a phase diagram. Usually, for a mixture of two or more components, different components do not mix in all proportions at all temperatures. Phase separation is found to occur within some temperature and proportion range. The area formed by points on the phase diagram where several phases co-exist is referred to as miscibility gap, the boundary of which is called coexistence curve, as shown in Figure 1-7(a).
Within the miscibility gap, another curve called spinodal divides the area into two regions. Inside the spinodal, the second derivative of free energy of the mixture is negative \( \frac{d^2 G}{dc^2} < 0 \). In this case, a homogeneous solution is unstable against fluctuation of density or composition, and a phase separation can automatically occur and, due to the lack of thermodynamic barrier to the growth of a new phase, is solely diffusion controlled. This case is called spinodal decomposition. Outside the spinodal where the second derivative of the free energy of the homogeneous phase is positive, small variation in composition only increases the total free energy and the system is thus metastable. In this case, phase transformation can only happen at the presence of nuclei that are very different from the whole environment. In this region, phase separation takes place by nucleation.

![Diagram](image)

**Figure 1-7** (a) A representation of the coexistence curve and the spinodal curve (b) a plotted free energy curve as a function of composition to illustrate how two points in the spinodal are defined by the inflection points in the curve [9]

Due to its inherent simplicity, spinodal decomposition is one of the few phase transitions in solids for which there is a plausible quantitative theory. The process can be treated as a pure diffusion problem because of the lack of thermodynamic barrier.

It is also of interest from a practical point of view, as it can be used as a method to make a very finely dispersed microstructure with well-defined phase segregation. The phase separation has a characteristic length determined by the appropriate intermediate wavelengths in the diffusion process. Too large wavelength components grow slowly because of the long diffusion distances, and too small wavelength fluctuations are suppressed to avoid the potential sharp increase of the surface energy that results from increased interface area.
Normally this sort of structure can significantly enhance the physical properties of the material or provide novel functionalities to devices, as for the memory diodes addressed in this thesis.

1.3. Ferroelectric phase separate blend memory diodes

Ferroelectric materials have long been recognized as promising materials for memory devices of non-volatile switching, since the two polarizations can be used as two binary levels. But the direct readout of the polarization state, for instance, in a ferroelectric capacitor is destructive, which is unfavorable for memory application. In principle, a resistive readout of the polarization state is non-destructive and can be realized in a ferroelectric Schottky diode [10]. However, the electrical conductivity and ferroelectricity of inorganic ferroelectrics used in such devices are not able to be tuned independently, with enhancement of one always leading to decline of the other, which results in the great difficulty in optimization [4].

In order to overcome this disadvantage, efforts have been made to combine a semiconductor and ferroelectric material into one device, in which the binary non-volatile memory states are provided by ferroelectric polarization and resistive switching is realized by tuning the conductivity of semiconductor part. Such devices are the subject of study in this project, ferroelectric phase separated blend memory diodes.

Such a memory diode is realized by blending the ferroelectric P(VDF-TrFE) and an organic semiconducting material. Spin-casting of a solution in which both polymers are dissolved can produce a thin film of phase-separated structures via spinodal decomposition [12], normally with semiconductor-rich columns embedded in a large ferroelectric-rich ambient environment due to the relatively low content of semiconducting material.

A memory diode consists of such a blend sandwiched between two electrodes. By applying a voltage that provides electric fields higher than its coercive field, the ferroelectric polarization can be switched into one of the two different states. The current response to a voltage lower than the coercive voltage of such a diode depends heavily on the state of ferroelectric polarization. In the “on-state” current is assisted by the polarization charge, thus larger than that of the “off state” by orders of magnitude(Figure 1-8). If the semiconductor is light-emitting, such a device can also be an OLED, which is called Mem-OLED, because whether the device gives light-emission depends on whether it has been programmed into its on-state, characterized by a larger current response.
It is generally agreed that the increased current in on-state compared to off-state current results from the reduction of the charge injection barrier by ferroelectric polarization at the semiconductor/metal interface, with the diode switched from injection-limited to space charge limited [13] [14]. However, the underlying mechanism for such modulation of injection barrier is still under investigation.

There are so far two different explanations about the mechanism related to the switching.

The first explanation proposes that as the ferroelectrics polarizes, the polarization charge close to the interface will be compensated by opposite charge in the semiconductor and the electrode. This in turn will result in band-bending and lower the injection barrier. In this scenario, it is assumed that an undercut exists in the ferroelectric phase for such charge compensation to take place. Also the amount of free charges for the compensation in the semiconductor plays a role in determining the level of the barrier modulation [6].

Figure 1-8  (a) Schematic representation of the on-state (left) and the off state (right) of a memory diode. (b) The J-V of the on-state and the off-state [5]

Figure 1-9  Schematic of a) the band bending that occurs at the electrode/semiconductor contact [13] b) The first explanation for the switching mechanism which requires the hole compensation and some particular morphology[6] c) the second explanation which is based on the influence of the polarization charge stray filed [14]
The other explanation states that simply the stray field originating from the ferroelectric phase is enough to modulate the charge injection. The lowering of the injection barriers can be caused by the polarization charge and the corresponding image charge in metal in combination. There is no special restriction on the interface morphology for such mechanism to work and the charge compensation by carriers in semiconductor is not required either. But the enhanced charge injection can only happen at the region close enough to the ferroelectric phase where the stray field is strong. The current will be also spatially confined due to the charge accumulation at the interface until it is affected by polarization charge at the other end [14].
Chapter 2 Study of blend morphology

2.1. Introduction

The polymer blend in a ferroelectric memory diode device is solution-processed via spin-coating. During this process, with rapid evaporation of solvent, a partially miscible polymer blend is quenched inside the unstable region of the phase diagram and spinodal decomposition takes place [8].

This chapter deals with the study of the influence of different process conditions on the final blend morphology. The study of the morphology has been done using atomic force microscopy measurements. The effects of the molecular weight of the semiconductor, solvent composition, spin time, substrate and thermal annealing are presented.

The morphological study carried out in this chapter is mainly for the purpose of optimization of device processing. It was necessary due to the fact that the semiconductor material originally purchased and used for previous experiments was no longer available, and old process conditions failed to apply to the new materials (of different molecular weight). Because of this, the study of different factors in processing is more practically oriented than strictly systematic. But still a lot of knowledge has been gained about the most important issues for making successful devices and also about the phase separation process, of which a scheme has been proposed at the end of the chapter.

2.2. Materials and experimental methods

For making a memory diode, one ferroelectric and one semiconducting polymer are blended. As introduced in Section 1.1.2, the ferroelectric material used is P(VDF-TrFE) (Poly(vinylidene fluoride-co-trifluoroethylene)). On the other hand, F8BT ( Poly[9,9-di-n-octylfluorenyl-2,7-diyl]-alt-(benzo[2,1,3]thiadiazol-4,8-diyl]) is used as the semiconductor. The chemical structures of both materials are shown in Figure 2-1. Previously, the memory diode has also been made with PFO as a semiconductor [13]. However, that device suffered from large surface roughness and poor retention time. With F8BT, these problems have been reduced significantly.

![Figure 2-1](a) chemical structure of P(VDF-TrFE)  (b) Chemical structure of F8BT
P(VDF-TrFE) with 77 mol% VDF was purchased from Solvay. A number of different types of F8BT were used in the whole optimization process. For a good comparison, the results presented include two purchased from Sigma-Aldrich and one synthesized by Holst Centre.

To fabricate the memory diode device, a blend of the two polymers was made by spin-coating. The solutions for processing were prepared by dissolving the 30 or 45mg/mL total amount of P(VDF-TrFE) and F8BT of 9:1 weight ratio into the solvent. As the solvent, a combination of cyclohexanone and tetrahydrofuran (THF) was chosen, with a volume ratio from 60/40 to 75/25 according to the type of F8BT used for a balance between solubility and blend roughness (More details included in Section 2.3).

As bottom electrode, Au was evaporated on cleaned glass substrate with a 5 nm Ti adhesion layer. Before spin-coating, the substrates are cleaned by wet-chemically followed by oxygen plasma treatment and then, be immersed in ethanol for one hour to lower the work function of the Au bottom electrode.

The prepared blend solution was filtered through a 0.45 µm filter and then spin coated onto the substrate in a nitrogen filled glove box, forming a thin film of roughly 200nm in thickness by choosing the appropriate spin speed and spin time. Then the stack was annealed on a hot plate in the same glove box for 1 hour at 135 °C in order to enhance the crystallinity of the P(VDF-TrFE) phase.

After the annealing step, AFM measurement were performed on the blend surface. These measurements were done with a Veeco Dimension 3100 AFM in tapping mode.

In order to make functional memory diode devices, the process mentioned above would be followed by more steps. After the annealing, a top electrode would be evaporated on top of the film through a shadow mask. Different materials have been used as the top contact to study the device physics, which is one of the subjects in Chapter 4. To prevent the devices from any sort of degradation (mainly the degradation of Ba when used as the top electrode), they would normally be encapsulated during the last step.

2.3. Blend morphology study

2.3.1 Surface topography of blends of different F8BT

Three different types of F8BT of different molecular weight have been used in the morphology study, including two purchased from Sigma-Aldrich and one synthesized by Holst Centre. The information of the F8BT materials is shown in Table 2-1, batch number indicated by I, II and III. The first purchased one (I) worked well in making blends for devices but is not available anymore, which is why the other two have been used for morphology study optimization. Because these F8BT batches have different properties, each resultant blend morphology also demonstrates various features. For different batches, the process conditions, such as the solid content in the solution and volume ratio of solvents, could also be different.
Due to the much higher molecular weight of F8BT II, its solubility in THF is significantly lower than the other two, resulting in a lower solid content in its solution and higher THF solvent composition. In order to achieve the same blend thickness, the process condition for F8BT II was also different. A spin speed of 2000 rpm was applied for F8BT II, instead of the 2500 rpm for the other two batches. The spin time was kept to 30 s for all three batches.

![Figure 2-2](image-url)  
**Figure 2-2** AFM height images of polymer blend surface made from different F8BT batches: (a) F8BT I (b) F8BT II (c) F8BT III

**Figure 2-2** shows the surface height profiles measured by AFM of the polymer blends. There are distinct differences among the surface topographies of the blends made from the three batches of F8BT. For F8BT I, which has a molecular weight of 14kD, the semiconductor columns are clearly visible as the bright circular domains and are nicely embedded in the ferroelectric matrix (**Figure 2-2(a)**). The columns are typically 100-400nm in diameter, slightly protruding out of the ferroelectric part with a height difference of roughly 0-20nm. The surface roughness of the blend is also relatively small, with a total height variation of around 70nm on a 3µm x 3µm scale.
For F8BT II, which has the largest molecular weight of 43kD, the blend surface is characterized by the presence of irregularly shaped pits instead of protruding semiconductor columns (Figure 2-2(b)). The depth of such pits exceeds 150nm. Consequently the surface roughness is significantly higher, indicated by the more than 300nm height spread. Another prominent feature is that the ferroelectric part exhibits a tendency of breaking into polygonal domains.

The surface topography of blend for F8BT III appears to be in a transitional state between I and II (Figure 2-2(c)). Firstly, similar to blend II, pits are found on the surface. The size of them is close to that of the columns found in blend I, and the average depth is around 50nm, much smaller as compared to the F8BT II blend. Moreover, a small number of protruding columns is also formed by the semiconductor phase, with a smaller average diameter compared to the pits. The ferroelectric part is as smooth as blend I, without any domain-like features.

### 2.3.2 Further study via partial removal by scotch tape

For the blend of F8BT II and III, there is an absence of clear F8BT-rich phase in the surface topography. But those conspicuous pits indicate that the semiconductor-rich phase is buried underneath. In order to probe further into the buried morphology, Scotch tape was used to remove the “upper” part of the blend II and blend III and the remaining substance on the bottom was studied - “scotch tape technique”.

![Figure 2-3](image_url)

**Figure 2-3** Optical microscopic images of the blend of F8BT II: (a) Before removal by scotch tape (b) After removal by scotch tape

The optical microscopy measurement has been done on the blend II before and after the partial removal of the blend and results are shown in **Figure 2-3**. Some island-like structures are observed at the bottom. The positions of the islands largely correspond to the area with high density of pits on the blend. If these previously buried islands are F8BT, it will provide evidence that the formation of the pits is related to the large areas of semiconductor that has sunken to the substrate.

A clearer message has been obtained from the study on the blend of F8BT III. The use of Scotch tape resulted in a complete removal of whole the ferroelectric
phase, so the possible remaining semiconductor structure on the bottom was directly measured by AFM. As demonstrated in Figure 2-4, the semiconductor columns have been found standing on the Au-substrate, mostly 150-200nm in height. This confirms that the phase separation did happen, only that the F8BT phase somehow went buried inside the layer. When these columns are embedded in a 200nm thick ferroelectric layer, they appear to be shallow pits in the surface topography. Compared to F8BT III, the F8BT II blend has even much deeper and more irregular pits. The explanation could be that the stratification effect in that blend is so prominent that the semiconductor phase is more like a “wetting layer” on the substrate.

![Figure 2-4](image)

**Figure 2-4** (a) The AFM height image of the blend of F8BT III after selective removal of ferroelectric phase  (b) The 3D image of the remaining F8BT columns  (c) the cross-section of a single column

### 2.3.3 The influence of the solvent composition ratio

The difference in the blend morphology could probably be attributed to the properties of different F8BT batches. However, it should be noted that other factors could also have an effect on the final morphology, since for blend II a different solvent ratio and solution concentration have been used. In fact, the solvent compositions do have an important influence, at least on the ferroelectric part of the blend, as found in another experiment as described below.
Two samples were made from P(VDF-TrFE) in solvents of different Cyclohexanone/THF composition ratios. One was 60/40 and the other was 75/25. With 60/40 solvent, the ferroelectric broke into domains with deep clefts on the boundaries while 75/25 resulted in a much smoother surface. Although the reason remains unclear, the choice of solvent does make a difference in the morphology of ferroelectric phase and is very likely to account for the ferroelectric domains found in blend II.

Whether the selected solvent could also have had an effect on the stratification of the layer is to be investigated. In this sense, if the effect of material batch itself is to be singled out, investigation should be focused on the comparison between the blends for F8BT I and F8BTII, for which the solvent ratio used in processing was exactly the same.

2.3.4 Substrate dependence of the phase separation

Through the ‘Scotch tape’ study of the buried structure, it is known that the cause for the large surface roughness and the formation of pits is the ‘descending’ of the semiconductor columns. In this section, the underlying mechanism for this tendency was further studied.

For a laterally phase-separated polymer blend of two or more components, it is common that there is a difference in height between each phase, resulting in a rough blend surface characterized by pits or protruding islands on the surface. It was proposed that formation of this typical structure for a binary blend could be caused by the different solubility of the two components in the common solvent [15]. During spin-coating, two different types of domains are formed due to the lateral phase separation, with each type rich in one component. The domains rich of the less soluble component solidify earlier than the other ones. These solidified domains form “walls” between which the remaining solution of the more soluble phase resides. As the solvent continues to evaporate, the second domains in liquid phase shrinks and collapses in the wells formed between the walls before turning into solids, because the polymer was swollen in the solvent. In our case, it could be that the F8BT-rich phase is more soluble and thus collapses to form all the pits. However, this argument was not clearly supported in our experiments. When solvents of different compositions (65/35, 70/30, 80/20) were used for the blend processing in order to change the solubility of F8BT, no obvious variation was observed of the blend.
morphology. This indicated that the solubility is not a decisive factor for the blend structure formation.

Apart from the previous explanation based on the material solubility, the influence of the surface energy remains as another possibly crucial factor. Generally surface-directed spinodal decomposition may take place when the difference in interfacial energies of the two blend components is large, with one of the blend components attracted to an external surface (either to the interface with air or with the substrate) [8]. This sometimes leads to a vertically phase-separated morphology. In our case, in view that the F8BT phase tends to stay close to the Au bottom electrode, it is expected that the relationship in (2.1) would exist

\[ \gamma_{F8BT/Au} + \gamma_{P(VDF-TrFE)/air} < \gamma_{P(VDF-TrFE)/Au} + \gamma_{F8BT/air} \tag{2.1} \]

\( \gamma_{F8BT/Au} \) refers to the surface energy for the F8BT-rich phase /Au interface and the same holds for the others. In this case, to minimize the total energy of the system, the F8BT-rich phase would be wetting the Au substrate. Although for the blend studied in our experiment a complete stratification was not observed, the fallen semiconductor phase still may have been caused by such surface-directed effect. In order to verify this assumption, the substrate dependency of the blend morphology was studied.

The F8BT III blend was used for the study. The first one was spin-coated on a glass substrate and the other two on a Au substrate. As already demonstrated before, the blend on the Au substrate featured of pits in the ferroelectric matrix caused by the fallen semiconductor phase. In contrary, for the blend on glass, droplet-like features (light color in AFM image) are found on the surface instead of holes (dark areas) , as shown in Figure 2-7(a). This means the semiconductor phase appears as protruding columns, with larger height than the surrounding ferroelectric phase.
The difference between the other two blends on Au is the thickness of the Au substrate. A comparison has been made between the blend morphologies on a 15nm-Au substrate and a 30nm-Au substrate, and a difference has also been found, as shown in Figure 2-7 (b) (c). The average depth of the pits on the 15nm Au is less than that on 30nm Au. On 15nm Au, the columns almost have the same height as the ferroelectric part while on 30nm Au, they are typically 30nm-50nm lower in height. We still don’t know the cause of this peculiar effect. Since the thickness of substrate is much larger than the atomic scale, the interface energy is not likely to be influenced by the thickness difference.

From these experimental results, it is clear that the choice of substrate has a significant effect on the morphology, mainly on the height difference between the two phases. It confirms that the trend of vertical segregation in the blend is triggered by the interface energy difference.

![AFM height image](image)

**Figure 2-7** The AFM height image of F8BT III blend (a) on glass with cross section on a F8BT column (b) on 15nm Au with cross section on a F8BT column (c) on 30-nm Au with cross section on a F8BT column
2.3.5 The role of annealing

Although it has been proven that the surface energy is directly responsible for the relative height difference of two phases in the blend, one peculiar fact still needs to be accounted for. In the blend formed on the Au substrates, two different types of semiconductor columns have been observed, roughly 80% of “normal” descending ones and 20% of protruding ones. It’s difficult to explain why the columns could appear in two very different forms considering that the effect of surface energy can only result in one preferential direction of movement.

The study on the effect of the annealing process can shed light on this puzzle. In Figure 2-8, the surface topography of the blend as measured by AFM is presented without being annealed, annealed for 5 min and annealed for 60 min respectively. The F8BT columns in the non-annealed blend are all sticking out above the surface by 100-200nm, contrary to the predominantly large fraction of pits or fallen down columns in the blend annealed for either 5 min or 60 min.

This result reveals that the annealing process is an important stage for shaping the final morphology. Before the annealing the semiconductor phase trends to stay away from the gold substrate, forming protruding “islands” on the blend surface. But this trend is completely reversed during the annealing process, with the floating “islands” collapsing into pits. It can be inferred that this process takes place within...
5min, since longer annealing time of 60min doesn’t bring in significant difference in either the typical shape or the depth of the pits compared to 5min annealing.

2.4. A scheme for the phase separation process

By integrating all the discoveries regarding the impacts on the blend morphology of the different factors studied, a scheme is proposed for the blend (F8BTIII) morphology evolution throughout the processing as described in the steps below:

Stage (a)(b): As the spin coating starts and goes on, the solvent evaporation reaches certain degree and the phase separation starts to take place. It is marked by the scattered regions of F8BT-rich phase (red) in a bulk P(VDF-TrFE)-rich phase (Blue).

Stage (c): During the later stages of spin-coating, the F8BT-rich regions have grown large enough clusters to be influenced by the substrate and the surface. In this case, the relationship of the surface energies below is valid

\[ \gamma_{F8BT/Au} + \gamma_{P(VDF-TrFE)/air} > \gamma_{P(VDF-TrFE)/Au} + \gamma_{F8BT/air} \]  \hspace{1cm} (2.2)
Due to the minimization of the interfacial energy, the F8BT will be dewetting the Au substrate, resulting in the droplets floating on the blend surface with no or little contact with the Au substrate.

\[ \gamma_{F8BT/Au} + \gamma_{P(VDF-TrFE)/air} < \gamma_{P(VDF-TrFE)/Au} + \gamma_{F8BT/air} \]

This reversal could be due to various reasons. First, the interfacial energy is related to temperature, and at a high temperature of 135 °C during annealing, all the values regarding the energies could be different from those at room temperature during the spin-coating. Second, in annealing, the remaining amount of solvent is much less than during spin-coating, which would certainly have an effect on the interaction at the interfaces. Moreover, the ferroelectric part of the blend also undergoes a phase transition to become crystalline and this may also have an impact on the interfacial energy related to P(VDF-TrFE).

At this annealing stage, because there is still a small fraction of remnant solvent which allows a certain degree of molecular mobility, the blend morphology will be driven to a new equilibrium, with the semiconducting phase attracted to the Au substrate. Most semiconductor droplets would descend to the bottom, which makes them appear as pits on the surface. However, some relatively smaller droplets are less affected by the energetic driving force because they are in a larger distance from the substrate. As a result, these small droplets still remain on the surface. Thus, the origin of two different sorts of F8BT columns in an annealed blend is explained.

So far, this proposed scheme has been supported by the conductive AFM measurement on a F8BT III blend. As shown in Figure 2-10, the smaller protruding F8BT columns are giving no current or very small current compared to the substantial amount of current provided by the descending ones. This implies that those protruded ones are not or only slightly in contact with the bottom electrode.
In this chapter, the influence of the process conditions on the final blend morphology has been presented and discussed. Phase separation of the blend has been found to be a very delicate process, which is easily influenced by a lot of factors. For instance, a variation in molecular weight of the semiconductor, solvent ratio, spin speed, spin time, or the substrate material can all result in significant differences in the morphology.

With different batches of F8BT, various blend morphologies have been obtained, characterized by the levels of falling down of the F8BT phase compared to the ferroelectric matrix. Via the study of the substrate dependence, it is found that the vertical segregation can attributed to the influence of interfacial energy. Also the annealing process is proved to be crucial to the morphology, because pits or droplets are found on annealed and non-annealed blends respectively. Based on the discovery above, a scheme is proposed to describe the whole process for the formation of the blend morphology.

In the future, more investigation could be done to reveal the complete process of blend morphology formation. More experimental methods could be figured out to study the structure of the F8BT columns, for instance by selectively dissolving the F8BT in the blend. Also, the morphology change during annealing should be probed and recorded. In this way, the proposed scheme could be further examined and refined.

The knowledge about the morphology formation mechanisms should be serving for realizing control over the blend morphology in the future. Many attempts can be made in this respect, such as changing the size of the F8BT columns by varying the composition ratio, or tuning the interfacial energy by surface treatment to modulate the vertical segregation. The morphology control can be combined with the nanoscale electrical characterization to search for the optimum blend morphology for device functionality.

2.5. Conclusion

Figure 2-10 (a) AFM height image of F8BT III blend, the protruding columns are highlighted (b) The conductive AFM on the same area of the blend. With +20V applied on the bottom electrode, most of the protruding columns are not showing current.
Chapter 3 Simulation of charge injection and transport

3.1. Introduction

For organic electronic thin film devices, the film morphology is an important subject to study since it’s closely related to many physical properties that directly determine the device performance [8], such as film conductivity, charge carrier injection at the polymer/metal interface, bulk transport and recombination.

As introduced in Section 1.3, although the underlying mechanism for switching the memory diode is not fully understood, the morphology does play an important role in different proposed schemes. Also, from the morphological study in Chapter 2, more complicated morphologies have been observed than assumed in early theories. It is interesting to study how the new morphology would affect the properties of the memory diode.

In this chapter, we extend the numerical model used in reference [14] to study the morphology dependence of the charge injection and transport in the polymer blend made for the memory diode. The simulation is done by calculation of the current density in the on-state of the diode when the ferroelectric polarization is assisting the carrier injection. The morphology model has been extended based on the results of AFM measurements. The influence of morphological details on the electrical transport properties have been presented for bulk measurements and for local measurements.

3.2. Methods

The whole simulation has been done with the DriftKicker program package in MatLab. To simulate the electrical transport and injection properties, a model has been employed in which the coupled drift-diffusion, Possion and current continuity equations (Equation 3.1-3.3) are numerically solved.

![Figure 3-1](image-url) Schematic representation of the grid points. Details around grid point I are shown, in contact with cells a-d. The arrows indicate current densities from point i-1 to i in cells a and c and from i to i+1 in cells b and d. From Ref. [DriftKicker user manual].

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\[ j^n = q \mu_n F + qD \nabla n \]  
\[ \nabla \cdot D = \varepsilon_0 (F \cdot \nabla \varepsilon_r \cdot F) = \rho = q(p - n + p_t - n_t) \]  
\[ q \frac{\partial n_x}{\partial t} = \nabla j^n + q(G - R_n) - qU_n \]  

The calculation is performed on a rectangular grid (Figure 3-1), where the grid points are at the corners of cells. The simulated device is defined in terms of these cells. Each cell has a material type (gate, contact, dielectric, semiconductor), which each has its specific defined properties. Different values for each of these defined properties can be set for each cell. The three equations are also discretized accordingly.

In order to perform the simulation, the 3D morphology in a phase separated blend needs to be reduced to a 2D structure, with the semiconductor columns standing in ferroelectric matrix replaced by alternating ferroelectric and semiconductor slabs. Since on the nano-scale the discussion of the physical mechanisms revolves around a single semiconductor column, the simulation is carried out on a single morphological unit, in which there is only one rectangular slab of F8BT phase (red) sandwiched between two P(VDF-TrFE) slabs (blue), with a top electrode above and a bottom electrode underneath (yellow), as shown in Figure 3-2. It is assumed that the system consists of many such repetitive units, implemented by periodic boundary conditions.

![Figure 3-2](image)

Figure 3-2 Schematics of the unit for simulation. Red slab represents F8BT and blue ones represent P(VDF-TrFE) phase. The arrows show the stray field at the interface in a polarized state.

For the ferroelectric phase, the carrier mobility is set to be zero, and a certain amount of surface polarization charge is fixed on the grid points at the interfaces, 2nm above bottom electrode and below top electrode. The surface polarization density \( \sigma_p \) is 70mC/m\(^2\) for a full polarization. A static relative dielectric constant \( \varepsilon_r \) of 10 is used.

The F8BT semiconducting slab is characterized by a HOMO level of 5.9eV and a LUMO level of 3.3eV. The hole mobility \( \mu_p \) is chosen to be 6.5\times10^{-11}m^2/Vs, the electron mobility \( \mu_e \) 6.5\times10^{-13}m^2/Vs and \( \varepsilon_r \) 2.5.

In the simulation, both the bottom electrode and the top electrode are Au, with a work function of 5eV. This gives an injection barrier of 0.9eV for holes and 1.7eV for electrons. In this case, the current going though the device is predominantly due to
hole transport, since only the barrier for holes can be overcome by the ferroelectric polarization. To simulate the current-voltage characteristics, the Emtage/O’Dwyer model is applied to account for the charge injection from electrodes into semiconductor. In this model, the charge injection is via thermal excitation over an lowered injection barrier due to the presence of image potential.

With this injection model, the mechanism for the lowering of the injection barrier by the polarization charges in an “on-state” can be explained in such a way: The polarization charges accumulate at the interface between the poled ferroelectric and the two electrodes, positive at the cathode and negative at the anode. Close to the anode, the electric field line points from the positive image charges to the negative polarization charges. This leads to an enhanced electric field that in turn can reduce the injection barrier for the holes in the vicinity of the interface with the ferroelectric, turning the injection limited contact into an Ohmic contact.

3.3. Simplified scenario and basic features for charge injection and transport

The simplified model only takes into account the simplest case where the semiconductor is in the form of completely straight columns. Mapped into a 2D structure, the edges of the slabs are straight and perpendicular to the electrodes.

The dimension of the morphology unit can be described by the values in Figure 3-4 (in nanometers). In this model, a basic picture for charge injection and transport can be clearly illustrated.

The calculated current density profile in the on-state of the diode is demonstrated in Figure 3-3 (a)-(b). As can be observed at the injecting bottom electrode, the hole injection is greatly enhanced at the semiconductor/ferroelectric interface locally due to the effect of prominent stray field. Consequentially the hole density at injection point is also significantly higher than elsewhere. At the injecting electrode, the lateral x-component of the electric field induces a strong accumulation of injected holes and posts a restriction to the current. The current remains confined in filaments close to the interfaces at either side and until it gets deflected out by the opposite lateral field at the collecting contact at the top electrode.
3.4. The carrier injection into concave and convex semiconductor slabs

The simplified model above only describes the ideal case. In reality, the semiconductor columns are not necessarily straight and the height of them is not exactly the same as the ferroelectric phase. According to the observation by the AFM measurements, the columns are divided in two types, one is protruding from the blend with a convex surface on the top of the column and the other is falling down and with a concave surface. By performing conductive AFM measurements, it is discovered that the conductivity of the these two types are very different.

Based on the result of AFM measurements, two additional morphological models are proposed, one with a convex semiconductor slab and one with a concave slab. As depicted in Figure 3-4. Although it is still controversial about how the protruding and convex columns look like beneath the surface, we assume that they are the
same as the simplified model. Thus the study would be simply on how the height difference of two phases and the shapes of the column surface affects the charge carrier injection. The width of the semiconductor slab is chosen to be 50nm and the height 150nm. Although the width is less than that of diameter of the typical column diameter measured by AFM, it is assumed that it already captures the basic transport properties at the interfacial region (more discussion in Section 3.5).

The calculated current densities for the on-state are presented in Table 3-1. Due to the broken morphological symmetry in the vertical direction, injection from both electrodes have been taken into account (+20V means for bottom and -20V for top).

Two different situations are considered for the model of concaved slab. In the first situation, the polarization charge only exists at the top and bottom surface of the ferroelectric phase. In the second situation, because of the lateral x-component of the electric field, the polarization charges are also induced at the part of vertical interface with semiconductor close to the contact. The height of the charged area corresponds exactly to that of the hollowed part of the semiconductor slab which is filled with the Au electrode.

<table>
<thead>
<tr>
<th>Model</th>
<th>Voltage</th>
<th>A1 Without lateral polarization</th>
<th>B1 Without lateral polarization</th>
<th>B1 With lateral polarization</th>
<th>C1</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>20V</td>
<td>2.5E-5</td>
<td>4.3E-5</td>
<td>2.6E-5</td>
<td>3.8E-5</td>
</tr>
<tr>
<td></td>
<td>-20V</td>
<td>-2.5E-5</td>
<td>-7.1E-6</td>
<td>-2.5E-5</td>
<td>-4.4E-5</td>
</tr>
</tbody>
</table>

**Figure 3-4** Three morphological models and relevant size parameters (units: nm) A1: the simplified model. B1: the concaved case. C1: the convex case.

**Table 3-1** Simulation results for the on-state current density (A/m) for the models A1 B1 and C1.
The calculated on-state current densities are shown in Table 3-1 in the semiconductor slab for all models mentioned above, of which the unit is A/m. Judging from the simulation result, when hole current is injected from the bottom electrode(+20V), the level of injected current for all different cases are close to each other. This result is reasonable since the condition for the injecting point is exactly the same for all cases, and the influence of the collecting point is relatively minor.

When injection takes place at the top electrode(-20V), the existence of the lateral polarization plays a very important role in the concave slab structure (B1). Without the lateral polarization, the current would be four times smaller. This result shows that the location of the polarization charge relative the injection point is a crucial factor for current injection. Since the slab is concave charge that comes from the vertical polarization along the y-axis is situated at a higher position than the injecting point at the electrode, and the resulting upward electric field could even impede rather than enhance the hole injection. The injection enhancement is mainly due to the polarization charge at the vertical interface with semiconductor and the current is also mainly injected laterally.

Another issue that needs to be addressed is why the convex case (C1) has the largest on-state current despite that it is largest in height. This could be attributed to the geometry of the injecting point. Qualitatively speaking, for the convex semiconductor surface, the current is injected at the edge, it has a larger “angle” to spread out rather than to stay more confined within a small angle as in the concave case. With the least space charge limiting effect, the injected current in this case is the largest.

3.5. The influence of possible morphological features beneath the surface

In the Section 3.4, the influence of different observable features on the surface has been studied. Apart from that, it is reasonable that the morphology buried beneath the surface or features close to the bottom electrode could also affect the injection and transport properties of the semiconductor columns. The actual shape of a typical column is not clear and still needs further investigation. However, based on the fact that the F8BT-rich phase is wetting the Au substrate, it can be speculated that an increasing composition ratio of F8BT can be found as it goes from the surface to the bottom. In this chapter, two other morphological models are proposed to account for this trend. As in Figure 3-5(b), in the first case, the F8BT slab is a trapezoid with a gradually increasing width from top to bottom. In the second case, as in Figure 3-5(c), the enrichment of the F8BT phase occurs in a more sudden way in the vicinity of the substrate, resulting in obvious undercuts of the P(VDF-TrFE) phase. For both cases, the top of the column is flat and of the same height as the ferroelectric phase. The simulation results are shown in Table 3-2.
Figure 3-5 Three morphological models and relevant size parameters (units: nm)  A2: the simplified model. B2: the trapezoid case. C2: the “undercut” case.

Table 3-2 Simulation results of on-state current density (A/m) for the models A2, B2 and C2.

<table>
<thead>
<tr>
<th>Model</th>
<th>Voltage</th>
<th>A2</th>
<th>B2</th>
<th>C2</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>+20V</td>
<td>2.5E-5</td>
<td>4.9E-5</td>
<td>2.7E-5</td>
</tr>
<tr>
<td></td>
<td>+6V</td>
<td>2.3E-7</td>
<td>3.0E-6</td>
<td>7.8E-8</td>
</tr>
<tr>
<td></td>
<td>-20V</td>
<td>2.5E-5</td>
<td>Inhibited</td>
<td>1.4E-5</td>
</tr>
<tr>
<td></td>
<td>-6V</td>
<td>2.3E-7</td>
<td>Inhibited</td>
<td>Inhibited</td>
</tr>
</tbody>
</table>

Due to those special geometries in case B2 and C2, polarization charges appear not only at the top and bottom surface in ferroelectrics, but could also at the inclined interface with the semiconductor slab. This new feature could bring some unusual results.

For the situation when positive voltage is applied at the bottom electrode, the additional polarization charges in the ferroelectrics at the inclined interface would be negative and could have a positive effect on the hole injection (Figure3-6(a)), reflected by a larger injection current than for the simplified geometry at case A2.
In contrast, when the holes are injected from top electrode and the diode is switched into an on-state, the charge at the inclined interface would be positive. Chances could be that these positive charges would have a repulsive effect on injected holes and thus inhibit the hole injection almost completely (Figure 3-6(b)). In this situation, although the injection barrier is lowered by polarization at the top surface, the interfacial charge inside the blend layer would create a potential barrier (Figure 3-6(c)), and the space limited charge would be many orders smaller than normal. This phenomenon has been observed in some cases in the simulation. As shown in Table 3-2, for case B2, with negative voltage on the bottom electrode, the inhibition mentioned above would happen, with current density lower than $10^{-16}$ A/m. For case
C2, this could also occur at low applied voltage (-6V) while at high voltage (-20V) the barrier could be overcome.

To conclude this section, another question needs to be addressed, namely to which degree these simulation results on a smaller geometry (50nm wide semiconductor slab) can describe what happens on more realistic dimensions (hundreds of nm in diameter for semiconductor columns) and whether the slab size effect is important or not. In the following study, the width of the semiconductor slab has been increased to 150nm.

Table 3-3 The simulation results of on-state current density (A/m) for the models A2, B2 and C2, with increased slab with of 150nm

<table>
<thead>
<tr>
<th>Voltage</th>
<th>Model</th>
<th>A2</th>
<th>B2</th>
<th>C2</th>
</tr>
</thead>
<tbody>
<tr>
<td>-20V</td>
<td></td>
<td>3.3E-5</td>
<td>6.7E-8</td>
<td>2.1E-5</td>
</tr>
<tr>
<td>-6V</td>
<td></td>
<td>7.1E-7</td>
<td>Inhibited</td>
<td>Inhibited</td>
</tr>
</tbody>
</table>

For the simplified model, the enlarged size of the semiconductor increases the on-state current slightly at both large voltage (20V) and small voltage (6V). Compared to at 20V, the level of increase is larger at 6V. Generally, the size of the slab does not influence the current level very much. So even if a slab of reduced size is used for simulation, the order of magnitude of the calculated current will still be correct. This is expectable since the injection of the current mainly takes place at the boundary and the effective injection area is more determined by the penetration length of the stray field from polarization charge and less related to the actual size of the semiconductor slab.

For the other two cases, the influence of the slab size could be more prominent. For the case B2, the inhibition of the injection from the top electrode imposed by the charge at the interface is relieved at -20V. Although the current is still the smallest in all the three cases, it has already seen an increase of 9 orders of magnitude compared to the value for the 50nm wide slab. This is because the energy barrier created by the polarization charge at the inclined interface effectively pinches off the semiconducting channel. Hence, the limiting effect is subject to the size and geometry related to the charge distribution. Increasing the width of the slab could supposedly allow more current to bypass the repulsive force from the side polarization charge.
3.6. Simulation of the local measurement by C-AFM

The nano-scale electrical characterization by conductive AFM measurement can provide a lot of knowledge about the injection and switching mechanism of the memory diode. However, what is measured by C-AFM should not be regarded as the same as the current in a real device. Since in a nano-scale measurement, the injection or extraction of charge carriers is done locally by a tiny metallic tip of a diameter smaller than that of a single F8BT column. This differs significantly from a bulk current measured in a diode device with a planar electrode on top. The study in this section is on the simulation of the local current probing done by C-AFM measurements and investigates the difference between nano-scale and the bulk current measurements.

The morphological models used in Section 3.4 are employed again, but the planar top electrode is replaced by a AFM tip. For the sake of easy comparison, the tip is assumed to be Au. The tip takes a circular shape when mapped in to the 2D geometry. The contact length with the slab is 10nm as was estimated from Hertz model for elastically deformed media.

To apply the Hertz model, the sample is approximated as an isotropic and linear elastic solid half space and the tip as a non-deformable sphere [16] [17]. Then the radius of the contact area can be calculated from the tip curvature radius, the Young’s modulus of the sample (F8BT) and the interaction force [16] as estimated from the deflection and a calibrated spring constant of the cantilever.

For all the three different types of morphology, the simulation was done for two different probing positions and two applied voltages at the bottom electrode. The two positions are respectively at the centre and at the edge of the semiconductor slab. For voltage applied to the bottom electrode, +20V means hole extraction by the tip and -20V corresponds to hole injection from the tip.

![Diagram](image-url)  
**Figure 3-7** Schematics of the local probing of conductive AFM measurement. A3: The simplified model probed in the centre  B3: The concaved model probed at the edge  C3: The convex model probed at the edge.
Table 3-4 The simulation results of on-state current density (A/m) for the models A3, B3 and C3, at two different probing locations

<table>
<thead>
<tr>
<th>Model</th>
<th>A3</th>
<th>B3</th>
<th>C3</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Edge</td>
<td>Centre</td>
<td>Edge</td>
</tr>
<tr>
<td>20V</td>
<td>9.7E-6</td>
<td>3.3E-6</td>
<td>3.3E-6</td>
</tr>
<tr>
<td>-20V</td>
<td>3.3E-5</td>
<td>9.4E-6</td>
<td>3.1E-5</td>
</tr>
</tbody>
</table>

For the case of hole injection from the tip (-20V), probing at two different positions, at the edge and at the centre, does result in different amounts of current. The probing at the boundary gives higher values of current density. This is consistent with the fact that the injection is enhanced at the boundary by the polarization charge. However, the difference between the values at two positions is not very large, ranging from several times to fifty times. This is less than the current density difference between these two locations when there is a planar top electrode. This could be explained by the current density map from the simulation. When the tip sits at the centre, the current can travel from centre to the edge along the surface due to the very large potential difference between two locations and then get into the bulk, as shown by the arrows in Figure 3-7 A1.

For the case of hole extraction (20V), the current is relatively low compared to tip injection, which is caused by different free charge densities and electrostatic potential profiles for these two cases. The difference in current density due to the probing positions is not as large either. This is because the conditions for injection at the bottom electrode are the same, and the current has already spread out from the filament shape to cover the whole cross section in the slab before reaching the collecting end.

In the simulation, the convex case can give similar level of the current as the concave case upon local probing. This is very different from the actual C- AFM measurement result in Figure 2-10, which shows that the protruding semiconductor columns are giving no or very little current. It means that there must be more difference than what can be seen at the surface morphology. This could be regarded as a further evidence to the argument that the protruding columns are floating droplets on top of the blend, with no or little contact with the bottom electrode.

When case B3 is compared with B1, we can see that the calculated current density level probed by the tip at the edge is not a far cry to the calculated bulk current when there is top electrode, with a difference with one order. This means the local conductive AFM measurement can provide useful information regarding the magnitude of current density for the planar electrode injection.
3.7. Conclusion

In this chapter, the results have been presented of the simulation for local charge injection and transport based on several proposed morphological models. More knowledge has been gained on the possible effects due to particular features in morphology on, for instance, injection and space charge limiting effect. The simulation on local probing also provides information about the real blend morphology combined with C-AFM results. It should be aware that the morphological models are still quite simplified. Thus the simulation result can only predict basic and limited phenomena and not necessarily reflect all the complex behavior seen in real experimental measurements. Based on the simulation results of the bulk injection with a planar top electrode, we can make some conclusions about the desirable morphology for the best injection in an on-state of the diode device. First, the surface structure of the F8BT columns doesn't result in a large difference in current density, especially when the hole injection is supposed to take place at the bottom electrode. But compared to others, the convex column gives a slightly larger current if the structures inside the film are the same. Moreover, the existence of a undercut of inclined interface would enhance the injection at the bottom electrode, but it could probably be inhibiting factor under some circumstance for an injection at top electrode, thus bringing in asymmetry in the electrical characteristics for the device. Since the effect of all the current enhancement is moderate (with difference within one order), we expect that the on-state current for the device could be increased by a factor of 10-20 by engineering the column structure and avoiding the disconnection of the F8BT phase from the bottom electrode as floating droplets.
Chapter 4 Electrical characterization of memory diodes

4.1. Introduction

A memory diode makes use of the hysteretic response of the ferroelectric polarization to an externally applied electric field to store information. A Boolean logic value “0” or “1” can be assigned to each of the binary states in the hysteresis. These logic states can be read out electrically as well, for the resistance of the diode is polarization-modulated. In this chapter, the electrical characterization of the memory diode devices is presented. First, the current density-voltage (J-V) characteristics have been measured. According to the typical hysteresis loop of the current, “on” and “off” states have been defined and studied. Then two other important properties for device performance, namely the endurance and the retention have also been studied. Some explanations are proposed for the results by combining to the blend morphology and relative mechanisms.

4.2. Experimental

The devices were processed in steps as described in Section 2-2, by blending the insulating ferroelectric P(VDF-TrFE) and semiconducting F8BT (The F8BT III in Chapter2) of ratio 9:1 together. The blend was spin-coated on a substrate with patterned 30-nm Au as the anode, which allows significant hole injection after modulation. Then different types of cathodes were evaporated on top of the blend, normally of 70-80nm in thickness. In our study, Au, Ag, Ba/Al and MoO$_3$ have been used as cathodes, resulting in an either an unipolar (hole-only) or ambipolar device depending on whether the contact is electron-blocking or not. On each patterned substrate, there are 44 diode pixels and the active device area is 0.44E-6m$^2$ for each device. Due to the electrical shorts, the yield of these devices is usually 65%-90%.

The electrical characterization was done with the setup called “Ferrorgan. With this setup, a series of electrical pulses of certain voltage and duration can be applied on a diode pixel by a Voltage Source Meter Unit according to the order from a written script. By giving the right combination of pulses, various measurement for different purposes, as mentioned in section 4.1 can be realized.
4.3. J-V characteristics

The typical thickness of the blend is 200nm for a memory diode. With a coercive field of 50MV/m for P(VDF-TrFE), the coercive voltage to switch the polarization state is 10V for the 200nm-thick layer. The absolute current density-voltage (J-V) characteristics has been measured by performing such a voltage sweep: first from 0 to 18.5V, than from 18.5V to -18.5V, then back to 0, as shown in Figure 4-3. In this way, if the measurement starts with an un-poled state, the diode will be switched twice during the sweep, once at 10V from off to on state, and then another at -10V from on to off state. A complete hysteresis loop can be recorded during the process.

![Figure 4-3 Schematic of the voltage scan for the J-V measurement](image)

Typical J-V characteristics of diodes with four different top electrodes are presented in Figure 4-4 (a)-(d). All four devices have a bottom electrode of Au, the top electrodes are Ba/Al, Au, Ag and MoO₃ respectively. Normally, a bottom electrode of Au is used as an anode, and the voltage is applied on it relative to the top electrode. In this case the hole injection is allowed at the anode when the
ferroelectric polarization is switched on. Different cathodes of various work functions can be either electron blocking or injecting, thus resulting in ambipolar or unipolar devices. The injection barrier of different electrodes for electrons and holes relative to F8BT (HOMO 5.9eV; LUMO 3.3eV) are listed in Table 4-1.

Table 4-1 Work function and injection barriers of different electrodes in a memory diode

<table>
<thead>
<tr>
<th>Electrode</th>
<th>Work function</th>
<th>Hole injection Barrier</th>
<th>Electron injection Barrier</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ba</td>
<td>2.6eV</td>
<td>3.3eV</td>
<td>no</td>
</tr>
<tr>
<td>Au</td>
<td>5.1eV</td>
<td>0.8eV</td>
<td>1.8eV</td>
</tr>
<tr>
<td>Ag</td>
<td>4.3eV</td>
<td>1.6eV</td>
<td>1.0eV</td>
</tr>
<tr>
<td>MoO₃</td>
<td>5.5eV</td>
<td>0.3eV</td>
<td>2.2eV</td>
</tr>
</tbody>
</table>

(a)  
![Graph](image_a.png)  
(b)  
![Graph](image_b.png)  
(c)  
![Graph](image_c.png)  
(d)  
![Graph](image_d.png)
Figure 4-4 The J-V characteristics of memory diodes with different top electrodes (a)Ba/Al (b) Au (c) Ag (d) MoO$_3$. (e) The lower branch in the positive region showing the switching on process of different devices.

A typical J-V curve features hysteresis in the positive half of the voltage sweep. This is because with different directions of ferroelectric polarization, the current could be either injection-limited or space charge-limited, which corresponds to the lower or the higher branch respectively.

In Figure 4-4(e), the lower branch of the curve is shown for a better study of the switching properties of the diode. This branch starts with injection limited off-state current, then transits into an intermediate region where the polarization is partially poled, before it finally converges to the upper branch of the bulk limited current. For all the devices the switching occurs at roughly 8V. This voltage is lower than that of the coercive voltage of the ferroelectric capacitor of the same thickness, which is around 10V. To account for this difference, two possible causes are proposed: First, the actual thickness of the semiconductor phase is less than the blend thickness of 200nm due to the falling down of F8BT columns. The effective thickness of the ferroelectrics at the interfacial region with the semiconductor may also be reduced as well. So the switching can occur at a lower voltage that the bulk part. Second, the interaction of the polarization charge and the charge carriers inside the semiconductor could play a role in the switching on process, which makes it different than that of a pure ferroelectric capacitor.

A diode of pure F8BT has also been made to compare with the blend diode. This diode is made of a spin-coated layer of F8BT of 200nm thickness on the same device substrate, with an anode of Au and a cathode of Ba/Al. This diode is supposed be injection-limited, but the current of it should be approximately an order of magnitude larger than that of the blend diode at the off-state, since it has about an order larger effective conducting area of F8BT than a blend memory diode. However, this is not supported by the measurement as shown in the Figure 4-4(e). The current density of this diode is less than of the blend diode in the injection-limited region. It’s very likely that the leakage current is dominant in the blend diode and accounts for the current larger than expected for a purely injection-limited current at low voltages. Despite of this speculation, more investigation needs to be carried out to identify the cause.
For each type of diode device, detailed discussions are carried out below regarding their individual characteristics.

**Au/blend/Ba/Al**

The diode is an ambipolar device. When a positive voltage is applied, holes can be injected from the Au anode and electrons from the Ba/Al cathode, giving considerable recombination and light emission. In this case, the memory diode can also be functioning as an OLED, namely the MEMOLED. When the applied voltage is negative, the injection barrier is much too high for holes at the Ba/Al anode, and the current is relatively low and mainly carried by a small amount of electrons injected from the Au cathode when the injection is assisted by the polarization charges. That is why the J-V is the most asymmetric of all.

**Au/blend/Au**

The Au contact is blocking for electrons and a small amount of electrons can still be injected with the assistance of the ferroelectric polarization. In principle this diode can be considered as a unipolar device. However, in reality, a small amount of light emission has been observed when the absolute value of the applied voltage exceeds 16V. Since the device structure is symmetric, holes can be injected from both electrodes and the J-V curve demonstrates a high level of symmetry. Still, there are very noticeable differences between positive bias and negative bias regions. At negative bias, the injection limited current in the off state is higher and increasing faster than at positive bias. There could be several reasons for this, for instance, the difference between the processing and the surface treatment of the bottom and the top electrode.

![Figure 4-5](image_url)  
**Figure 4-5** A dip in the negative voltage region of the Au/blend/Au diode showing the asymmetry of electrical properties
Another distinctive feature for the reverse bias is that the current has a small dip right before it is switched on as the voltage increases. This feature has also been observed for the diodes with Ba/Al and Ag as top electrode. As the voltage reaches roughly the coercive region (in regard of the top electrode) the current density will first drop over a small voltage period, then start to rise again, as opposed to the constantly increasing trend at positive bias. This feature might be related to the asymmetry of the semiconductor column morphology. As discussed in Section 3.5, when holes are injected from the top electrode, the current could be inhibited or even lowered by the positive polarization charge appearing at the possibly inclined interface as the diode is just switched on. This would then correspond to the suppressed region at the negative bias. When the applied voltage is high enough to overcome the energy barrier, the current will start to grow again.

**Au/blend/Ag**

This device closely resembles the one of Au/blend /Au structure, apart from a stronger electron injection at positive bias, which has also been proven by its slightly better light-emission. Similar to the Au/blend/Ba/Al device, the diode has a higher bulk limited-current. This is a characteristic due to the ambipolar transport in the diode. With Ag as a better electron injector, the current balance is also better. Thus there is less space charge limitation and therefore a higher current.

**Au/blend/ MoO₃**

MoO₃ was used as the top electrode in order to make an Ohmic contact for holes when the bias is negative so that the bulk-limited transport could be directly measured for the diode. To realize this, a Fermi level lower than the HOMO of F8BT is needed and, if successful, the hysteresis loop would disappear at the left half of the J-V curve. However, for the real devices that have been made, the hysteresis is still present. It could be the result of a higher than expected Fermi level of MoO₃, which is above the HOMO of F8BT. It has been shown that MoO₃ has a large window of work functions under different process conditions [18] [19]. Tuning the work function of MoO₃ will be one of the issues to address in future experiments.

**Table 4-2** The level of current in different diodes in the forward and reverse direction.

<table>
<thead>
<tr>
<th>cathode</th>
<th>Work function (eV)</th>
<th>hole current fwd</th>
<th>electron current fwd</th>
<th>hole current rev</th>
<th>electron current rev</th>
<th>Light emission</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ba/Al</td>
<td>2.6</td>
<td>Large</td>
<td>Large</td>
<td>No</td>
<td>Small</td>
<td>Yes</td>
</tr>
<tr>
<td>Ag</td>
<td>4.3</td>
<td>Large</td>
<td>Medium</td>
<td>Medium</td>
<td>Small</td>
<td>Yes</td>
</tr>
<tr>
<td>Au</td>
<td>5.1</td>
<td>Large</td>
<td>small</td>
<td>Large</td>
<td>Small</td>
<td>little</td>
</tr>
<tr>
<td>MoO₃</td>
<td>5.5</td>
<td>Large</td>
<td>No</td>
<td>Large</td>
<td>Small</td>
<td>No</td>
</tr>
</tbody>
</table>

The injection barrier for different current levels: Large Current <1.0eV; Medium Current: 1.0-1.6eV; Small Current:1.6eV-2.1eV; No Current: >2.1eV
The operation scheme of the memory diode is demonstrated in Figure 4-6(b). The erasing or programming of the memory state can be done by applying a pulse of 18.5V that is large enough to switch the ferroelectric polarization. A non-destructive read-out of the memory state can be performed by applying a pulse of 6V, which is lower than the coercive voltage of the memory diode. At this voltage, the memory has a relatively large ratio of on-state current over off-state current, making the two states easily distinguishable.

4.4. Endurance measurement
4.4.1 Introduction and methods

For a memory device, it is important that it can be easily read-out after many times of programming and erasing. An endurance measurement, allows one to investigate the effect of permanent polarization reversals (i.e. programming and erase cycles) on the On/Off current ratio. For the first envisioned practical applications an On/Off current ratio of $10^3$ after $10^3$ cycles is preferred. In this section, the result and analysis of the endurance measurements are presented. The scheme for the measurement is described below:

First a pulse of 18.5V is applied to program the memory diode into the on-state, and then a pulse of -18.5V to program it into the off-state. The duration of each pulse is 50ms and the interval between the pulses is 1s. Such a process is defined as one switch or cycle (Figure 4-6(a)).

After N ($N=0, 1, 2, 5, 10, 20, 50, 100, 200, 500, 1000,...$) switches, the current value in the on- and off-state is read by applying a write and read pulse of +/- 18.5 V and 6V respectively (Figure 4-6(b)). An additional IV sweep is performed after $N=1, 10, 100, 1000,...$ switches (Figure 4-3).

![Figure 4-6](image)

(a) The pulse scheme for the switching (b) The pulse scheme for the reading
The readability of the memory device is characterized by the difference between the on-state current readout and the off-state current readout at 6V. Normally a ratio of $10^3$ is desired for the on-state current over off-state current (On/Off ratio) to have two clearly distinguishable logic states for storing information.

4.4.2 Results: normal and abnormal behavior

In the endurance measurement of devices with various top electrodes, two types of behavior have been observed. The first type can be regarded as normal behavior while the second type shows abnormal characteristics.

In Figure 4-7(a), the measurement for the device of Ba/Al top electrode is shown. The on-state current density shows a rapid decrease within 1000 switches, starting from roughly 1A/m$^2$ and ending with around $5 \times 10^{-3}$A/m$^2$, experiencing a 95% drop. The off-state current has maintained more or less its original level during the 1000 cycles. This behavior is called “normal”, because it gives a reasonable outcome. The on-state current is assisted by the presence of ferroelectric polarization. It is expected that the consecutive switching diminishes the ability of the ferroelectric to polarize and the on-state current drops consequently. The off-state current is almost independent of the polarization state and thus stays almost unaffected. The only problem here is the unusual rapid degradation of the ferroelectric. Normally, P(VDF-TrFE) has remarkable endurance and for reported P(VDF-TrFE) capacitor memories, the polarization degradation is limited to a value of 15% after $10^7$ cycles [4], which is in contrast with the observation in our measurement. This rapid polarization degradation observed in the diode could be related to the interaction of the polarization charge and the injected charge carriers. More experiments need to be carried out to investigate what the possible interaction exactly is and how it possibly accelerates the degradation of the ferroelectric.

The abnormal behavior of the endurance is presented in Figure 4-7(b). This measured device is with the Au top electrode, but similar behavior has also been observed for Ag and MoO$_3$ devices. In contrast to the normal scenario, within the first 1000 switches the on-state current has increased by 10 times and the off-state current by 100 times. From 1000 switches on, both currents decrease rapidly. After 10000 switches, the on-state current is 100 times smaller and the off-state current 5 times smaller than their respective starting values. It is hardly possible that the ferroelectric polarization can be strengthened after switching to enhance the current in these devices. In order to probe the underlying mechanism for the obtrusive rise in current values, more investigation has been done and will be discussed in the next section.
4.4.3 More investigation into the abnormal endurance behavior and discussions

More studies have been performed on the intriguing increase of the current level in the endurance measurement. A Au/blend/Au memory diode was switched 1000 times and left in open circuit for one week. The J-V curves have been recorded in the pristine state, right after the switches and after one week. As shown in Figure 4-8, the current immediately recorded after 1000 switches has shown large increase and almost reached its maximum. After one week in open circuit at room temperature, the J-V curve has shifted downward just as what is measured after switching in the normal endurance behavior. This means the high current state that appears during the switching is a transitory state and relaxes over time. From one week on, both the
J-V curve and the readout current levels in on and off states don’t show any significant change anymore, meaning this state is stable. In this stable state, the low readout current levels can authentically reflect the polarization degradation in the ferroelectrics. In contrast, during the early stage of the switching, another unknown process takes place to enhance the charge injection and reverse the decreasing trend induced by the weakened polarization, which results in the temporary net current enhancement.

![Figure 4-8](image)

*Figure 4-8* The J-V curves for a Au/Blend/Au diode before, right after and one week after the endurance measurement

Two other ways of endurance measurement were performed on the same type of Au/blend/Au device. The first was to only apply a positive pulse instead of one positive and one negative for 1000 times. The second one was to apply only the negative pulses. The on-state and off-state current were still read by applying a positive pulse of 6V. In this way, the different effects of two opposite pulses in one switch can be separated from each other by comparing the results. It was supposed that one of the two pulses must be the cause for the abnormal current enhancement. However, as shown in *Figure 4-9*, the enhancement phenomenal were not observed in either of these measurements. The positive pulse series resulted in 90% degradation of the on-state current after 1000 cycles while the negative pulse series almost did not affect the current levels. This seems to suggest that the positive pulsing is somehow responsible for the ‘normal’ degradation behavior.
Figure 4-9 (a) The endurance measurement with only positive pulses on a Au/blend /Au diode (b )
The endurance measurement with only negative pulses on a Au/blend /Au diode

Although the underlying mechanism for the current enhancement found in the experiments is still unclear, some preliminary conclusions can be drawn. First, the enhancement is a temporary effect induced by the polarization switches. This state is unstable and relaxes over time. When the ferroelectric degrades to a certain degree after 1000 switches, the effect is also disappearing. Second, the enhancement results from the combined effect of alternating positive and negative pulses. Only repeating one single type of pulse will not lead to such enhancement. Third, whether it happens or not depends on the choice of the top electrode, since the Ba/Al top electrode prevents such an effect.

Based on the relaxation behavior observed in the abnormal endurance measurement as shown in Figure 4-8, we could speculate that some trapping has taken place. Charge trapping at the metal/semiconductor interface is indeed a common cause for enhanced charge carrier injection in electronic devices due to surface dipole induced band bending [20] [21]. The annealing in our device processing has been reported to create surface states that facilitate trapping.
Figure 4-10 (a) The normal band diagram in the F8BT diode (b) The modified band-diagram by trapped charges induced band bending (c) Schematic of the dipoles under a forward electric field (d) Schematic of reverse-bias enhancement effect induced by aligned interfacial dipoles.

Results of similar nature have been shown in a reference paper [20]. In the paper, it was reported that in an electrical characterization, a diode of only F8BT demonstrated significantly increased hole current and quantum efficiency with driving time. The effect was observed to be even more enhanced by apply a alternation of forward and reverse biases. This was explained by deep hole trapping at the anode/F8BT interface during the driving. The trapped non-recombinant holes were thought to have formed an interfacial layer of dipoles with the compensating electrons, causing band-bending that opened up a channel for hole tunneling (Figure 4-10(a)(b)). By applying an electric field in the reverse direction, the formed interfacial dipole could be aligned in one direction and thus further enhance the band-bending (Figure 4-10(d)). Under such a scheme, the reverse bias enhancement effect was explained.

This mechanism can help explain the current enhancement by driving of electrical pulses in our memory diode. In our devices, the hole trapping at the one electrode
could probably be induced by hole current injection at the other electrode during a reverse bias pulse. That is why the enhancement is only observed when both positive and negative pulses are applied. In a diode with a Ba/Al top electrode, the hole current at negative bias is prohibited by a high hole injection barrier of Ba, and the charge trapping cannot take place at the Au electrode, so no injection enhancement is observed at the Au bottom electrode. This charge trapping scenario can explain the off-state current enhancement in devices that allow hole injection in both electrodes because of the lowered injection barrier, but it fails to account for the more than two orders of increase in the on-state current, which is space-charge limited. It means that the real picture is more complicated than depicted here, which requires further investigation.

From an application perspective, the memory diode device will be much more affected by the polarization degradation, i.e. the decreasing on-current than by the trapping-induced off-state current enhancement. Since the latter is a accumulative effect, it requires continuous switches of quite high frequency. In daily use of such device, this effect is prevented by relaxation during the relatively large time interval between two switches.

4.4.4 Improvement achieved by an edge cover

In order to improve the endurance of the memory diodes, an edge cover has been deposited on the Au substrate. The edge cover is a 500µm-thick SU8 layer patterned on the Au bottom electrode. The central area, a circular shape of 400µm diameter remains open while the edge part of the electrode is covered. During the spin-coating, the polymer blend that forms within this well would make the active area of the diode.

With this edge cover, the endurance of the devices has seen notable improvement. For a normal endurance behavior of a Ba/Al device, the decrease of the on-state current has been slowed down and the on/off ratio is roughly 50 after 1000 switches,10 times higher than without the edge cover. For a Au device, the current enhancement is also reduced. The results are presented in Figure 4-12.

The purpose of the edge cover is to prevent the poor quality of the polymer bend resulting from the boundary defect during the spin-coating to affect the device performance. The blend close to the edge of the electrode (interfacial area with glass) supposedly has a smaller thickness than average and thus becomes the weak point of the diode under the same electrical bias. That is why the endurance can be improved by adding an edge cover.
4.5. Retention time measurement

The concept of retention time for a memory device is relatively simple, namely the length of time the memory can store the information after being programmed. To measure the typical retention time of the memory diode, first the diode is programmed into either the on-state or the off-state at the beginning, and then after \( t=0s, 1s, 10s, 100s, 1000s \) and so forth, the current value for this particular state is measured. By plotting the current versus time, it be can be found out to what extend the stored information has diminished.
The typical result for retention time measurement is shown in Figure 4-13. The measured on-state current has shown a decrease of 2 orders of magnitude in $10^5$ seconds while the off-state current has only decreased slightly as expected. If a ratio of 1000 is needed for on-state current over off state current to store information, the retention time for the one state is less than 1000s. This value is much less than that for a ferroelectric capacitor. Although what is shown here is for a Au/blend/Au diode, this is universal for all the devices that have be made, regardless of the top electrode.

The decreased on-state current has been attributed to the depolarization of the ferroelectric in the blend [22]. Ferroelectric thin films depolarize largely due to the minimization of depolarizing field energy. The depolarizing field can be reduced by formation of screening charges at the film-electrode interfaces [23]. So normally the presence of two electrodes is crucial for maintaining the polarization when the ferroelectric has been switched on.

![Figure 4-13](image)

**Figure 4-13**  Typical result of retention time measurement, showing the evolution of on-state or off-state current density after switching.

In a blend sandwiched between two electrodes, the depolarization in the ferroelectric phase usually happens due to the lack of effective screening or a reduced interface capacitance effect. Since the short retention time is universal for devices of different electrodes, it can be inferred that the rapid depolarization is more related to morphological issues of the polymer blend. More study is underway to detect the possible root for the problem. In a reference paper it has been demonstrated that an semiconductor ad-layer between the blend and one electrode can cause depolarization in a short time [22]. This could also have been the reason for short retention time in our device. As found in the morphological study on the blend, the F8BT phase has a tendency to wet the Au substrate during the heat treatment. A partial wetting layer of F8BT could have formed on the bottom electrode and prevent the effective screening of the depolarization field by the metal electrode. Efforts are being made to detect the existence of such a layer by
performing AFM measurement on blends from which the ferroelectric part is selectively removed by solvent treatment.

4.6. Conclusion

In this chapter, the J-V characteristics have been presented for devices with different top electrodes. An analysis has been given of the results in relation to the carrier injection properties and the blend morphology. Different materials have been used as the top electrode of the memory diode while the bottom electrode has been kept as Au. The Au bottom electrode can provide good hole injection as an anode, while the choice of cathodes determines whether electrons can be injected. With Ba/Al or Ag as the cathode we can make a good ambipolar device, with either strong or relatively weak light emission. For the expected unipolar devices, a Au cathode still gives a small amount of undesired electron injection while MoO$_3$ is blocking for electrons. The level of on and off state current is also slightly influence by the cathode. Ba/Al and Ag can give roughly 2 or 3 times higher on-state current and thus higher on/off ratio, which is desirable for a memory device.

The results of the endurance and retention time measurement have also been presented. An abnormal current enhancement phenomenon has been found. Some evidence shows that it might be related to charge trapping, but more study needs to be carried out to complete the picture. For instance, the temperature dependence of the relaxation behavior could be studied in the future to probe the release of the trapped charges. Also pure F8BT diodes could be used to the experiment to disentangle the influence of the ferroelectric polarization and the charge-trapping.

The performance of the memory diode has been shown to be limited by the poor endurance and short retention time, Future study should be focused on pinning down the root of such issues. For the retention time, it has been proposed to study the possible morphological feature such as a F8BT wetting layer that could speed up the depolarization. For endurance, the priority should be on checking possible degradation of P(VDF-TrFE).
Summary

The ferroelectric phase separated blend memory diode is a memory device which employs the properties of both ferroelectrics and semiconductors. The diode consists of a blended thin film of a semiconducting and a ferroelectric polymer (normally P(VDF-TrFE)), sandwiched between two properly chosen electrodes. The ferroelectric can provide the binary logic states for storing information via two polarization directions. The semiconductor provides the means for non-destructive readout via resistive switching, which depends on the ferroelectric polarization - modulated injection barrier for charge carriers. In this project, a memory diode is made from P(VDF-TrFE) and F8BT, which also allows light emission and thus makes a memory organic light emitting diode.

First, the study has been carried out on the blend morphology via AFM measurements and the optimization of the fabrication process. It was demonstrated that the blend morphology was strongly influenced by the interfacial energy between the components and the substrate. The minimization of the total energy would result in a relative vertical movement of the laterally phase separated structures. Also the commonly employed annealing step was found to have an important role to play in the formation of the final morphology. A scheme for the morphology evolution has been proposed to account for the two different types of F8BT columns observed, which shows different nano-scale conductivities.

Based on the measured blend morphology, numerical simulations have been done to study how the charge injection and transport are influenced by morphology. Several cases were studied in regard of the different surface morphology and presumed subsurface structures and their effect on current transport was revealed. In order to explain the result of conductive AFM measurement, the local probing by a tip was also simulated. We discovered that in order to enhance the carrier injection from the bottom electrode in an on-state, an inclined semiconductor/ferroelectric interface is most helpful, while a convex surface gives larger current than other surface features. But these two features are mutually exclusive. In practice, we prefer to have descending semiconductor columns with an inclined interface with the ferroelectrics in the blend morphology. A enhancement of roughly a factor of 10 is expected compared to the case of straight columns.

Finally, the electrical characterization was done on the diodes devices. The results of J-V, endurance and retention time measurements were presented. Discussions have been carried out to explain the observed features and to account for the limited device performance in electrical characterizations in relation to the film morphology. The choice of anode can influence the on/off ratio and the behavior in the endurance measurement. In an ambipolar device with a top electrode of Ba/Al or Ag, roughly 2 or 3 times higher on-state current and thus higher on/off ratio can be achieved, which is desirable for a memory device. Abnormal current enhancement has been seen in endurance measurement and found to be relieved by adding a edge cover. Future experimental plans were proposed based on the current findings.
References

[17] Using Atomic Force Microscopy to Determine Elastic Properties of Biological Samples , JPK Instruments


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