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Citation for published version (APA):

DOI:
10.1587/elex.14.20170674

Document status and date:
Published: 25/04/2017

Document Version:
Publisher’s PDF, also known as Version of Record (includes final page, issue and volume numbers)

Please check the document version of this publication:
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Download date: 05. Jan. 2022
A novel complementary push-push frequency doubler with negative resistor conversion gain enhancement

Yang Liu¹, Zhiqun Li¹a), Hao Gao¹², Qin Li¹, and Zhigong Wang¹
¹ Institute of RF-Œ OE-ICs, Southeast University
Nanjing 210096, People’s Republic of China
² Eindhoven University of Technology; Delft University of Technology, The Netherlands
a) zhiqunli@seu.edu.cn

Abstract: This letter presents a 48 GHz frequency doubler in a 65 nm CMOS technology. The proposed frequency doubler is composed of a complementary push-push structure with negative resistance circuit for conversion gain enhancement. The maximum measured conversion gain reaches −6.1 dB at 48 GHz output frequency, and the 3-dB bandwidth is 40 ~ 54 GHz. The fundamental rejection is above 29.5 dB. The size of the proposed frequency doubler chip is 0.72 × 0.36 mm². The total power consumption is 16 mW.

Keywords: frequency doubler, CMOS, complementary push-push, negative resistor

Classification: Microwave and millimeter wave devices, circuits and systems

References

1 Introduction

Frequency doubler (FD) is a critical component for microwave and millimeter-wave frequency generation. It could be employed to generate high frequency signal from low frequency oscillator. It can be divided into categories such as single-transistor FD, distributed FD, doubler-balanced FD, Gilbert FD and push-push FD. Single-transistor FD is composed of a single transistor with matching network [1][2], but the conversion gain (CG) is low. Distributed FD [3] and Distributed FD with current-reuse technical [4] have been demonstrated, which provides higher CG. Both single-transistor and distributed FD provide low fundamental rejection (FR) and require extra filters for FR improvement. Differential structure FD can provide high FR. Double-balanced diode FD is demonstrated with high operation frequency and excellent FR [5][6], but this passive structure requires high input power and provides low CG. Balanced distributed FD is proposed with good CG and good FR [7], but also uses single-balanced structure. Double-balanced Gilbert structure is demonstrated with both high CG and high FR [8], however the power consumption is also high. Push-push structure is widely used due to simple structure, acceptable CG and good FR [9][10]. However, conventional push-push FD uses single-balanced structure and suffers from the imbalance of input and output and the low CG.

In this paper, a frequency doubler with complementary push-push structure and negative resistance is proposed. The proposed frequency doubler provides differential, balanced input and output structure. With this structure, it can also achieve high conversion gain with negative resistance circuit for conversion gain enhancement. The circuit design and measurement results are presented.
2 Design Methodology

2.1 Complementary Push-push Frequency Doubler

The push-push effect of a PMOS pair and a NMOS pair can be combined to enhance the FD performance. In a single NMOS or single PMOS pair, the push-push effect is stronger in drain node compared with source node, as shown in Fig.1.a and Fig.1.b. Combining a PMOS pair and a NMOS pair, the push-push effect can be enhanced at both source and drain nodes in the combined structure, as is shown in Fig.1.c.

Fig. 1. Principles of a. PMOS pair, b. NMOS pair and c. complementary push-push FD

Fig. 2. a. Schematic and b. Equivalent circuit of complementary push-push frequency doubler
Fig. 2 presents the schematic of complementary push-push FD. The input signal is $V_i = A_i \sin(\omega t)$, the output current of the transistors ($M_1 \sim M_4$) are

$$
\begin{align*}
I_1 &= k_p \left( \frac{V_i}{2} + V_{BP} - V_{DD} - V_{thp} \right)^2 \\
I_2 &= k_p \left( -\frac{V_i}{2} + V_{BP} - V_{DD} - V_{thp} \right)^2 \\
I_3 &= k_n \left( \frac{V_i}{2} + V_{BN} - V_{thn} \right)^2 \\
I_4 &= k_n \left( -\frac{V_i}{2} + V_{BN} - V_{thn} \right)^2
\end{align*}
$$

(1)

Where $k_p = \frac{\mu_p C_{ox} W_p}{2L_p}$ and $k_n = \frac{\mu_n C_{ox} W_n}{2L_n}$. The total current $I_{tot}$ from the complementary structure is the sum of $I_1 \sim I_4$.

$$
I_{tot} = \frac{k_p + k_n}{2} V_i^2 + 2k_p (V_{BP} - V_{DD} - V_{thp})^2 + 2k_n (V_{BN} - V_{thn})^2
$$

(2)

Since $V_i^2 = A_i^2 \sin^2(\omega t) = A_i^2 \frac{1 - \cos(2\omega t)}{2}$, Eq. (2) could be rewritten as below.

$$
I_{tot} = -(k_p + k_n) \frac{A_i^2}{4} \cos(2\omega_0 t)
$$

+ $(k_p + k_n) \frac{A_i^2}{4} + 2k_p (V_{BP} - V_{DD} - V_{thp})^2 + 2k_n (V_{BN} - V_{thn})^2$

(3)

From Eq. (3), $I_{tot}$ is a combination of a RF part and a DC part. Due to the DC-block capacitors, the output current at the load $R_L$ ($I_o$) is only the RF part of $I_{tot}$.

$$
I_o = -(k_p + k_n) \frac{A_i^2}{4} \cos(2\omega t)
$$

(4)

From Eq. (4), the output voltage ($V_o$) is

$$
V_o = (k_p + k_n) \frac{A_i^2}{4} \cos(2\omega t) \cdot (R_{DS} || \frac{1}{j\omega C_P} || j\omega L_P || R_P || R_L)
$$

(5)

Where $R_{DS}$ is the combined on-resistance and $C_P$ is the combined source-drain capacitor of the transistors and parasitic capacitors, $L_P$ is the equivalent inductance and $R_P$ is the equivalent parallel resistance of $L_1$ and $L_2$, $R_L$ is the load resistance.

Comparing Eq. (5) and $V_i$, the CG could be expressed as

$$
CG = (k_p + k_n) \frac{A_i}{4} (R_{DS} || \frac{1}{j\omega C_P} || j\omega L_P || R_P || R_L)
$$

(6)

The peak CG when $L_P$ resonates with $C_P$ is

$$
CG_{P} = (k_p + k_n) \frac{A_i}{4} (R_{DS} || R_P || R_L)
$$

(7)

And the peak-gain frequency is

$$
\omega_{PG} = \frac{1}{\sqrt{L_P C_P}}
$$

(8)
2.2 Using NR for CG Enhancement

Eq. (7) shows that the larger the output load, the larger the $CG_P$. Conversion gain can be enhanced by parallelling a negative resistance (NR) circuit with the output load, as is shown in Fig.3.a. The NR circuit could be implemented by complementary cross-coupled MOSFETs and an inductor ($L_N$). The equivalent circuit of NR is a parallel network of $L_N$, MOSFETs’ capacitor $C_N$ and negative resistance $-R_N$. The CG of FD with NR is

$$CG' = (k_p + k_n) \frac{A_i}{4} \left[ R_{DS} || \frac{1}{j\omega(C_P + C_N)} || j\omega \frac{L_P L_N}{L_P + L_N} || R_P || R_L || (-R_N) \right]$$ (9)

And the peak CG is enhanced to

$$CG'_P = (k_p + k_n) \frac{A_i}{4} \left[ R_{DS} || R_P || R_L || (-R_N) \right] \frac{R_N}{R_N - R_{DS} || R_P || R_L}$$ (10)

However, the value of $R_N$ should be kept larger than $(R_{DS} || R_P || R_L)$ for stability consideration. The peak-gain frequency of FD with NR is

$$\omega'_{PG} = \frac{1}{\sqrt{(L_P L_N) / (L_P + L_N)}} \sqrt{(C_P + C_N)}$$ (11)

Let $\omega'_{PG} \geq \omega_{PG}$, it can derived that $L_N \leq \frac{L_P C_P}{C_N}$. Consequently, the NR circuit could raise the peak-gain frequency if $L_N \leq \frac{L_P C_P}{C_N}$.

By contrast, the classical common-source buffer attaches a capacitive load $C_{buf}$ to the frequency doubler, as is shown in Fig.3.b. And $C_{buf}$ reduces the peak-gain frequency.
2.3 Proposed Frequency Doubler Design

The schematic of proposed FD is shown in Fig. 4. The PMOS ($M_1$, $M_2$) and NMOS ($M_3$, $M_4$) form a complementary push-push FD core. The transistors are biased in the sub-threshold region with $V_{BP} = 0.8V$ and $V_{BN} = 0.4V$. Inductors $L_1$ and $L_2$ are used for input impedance matching. $C_1 \sim C_4$ are DC-blocking capacitors. $TL_1$ and $TL_2$ are slow wave shielded transmission lines used as inductors. The complementary cross-coupled transistor pair ($M_5 \sim M_8$) form the negative resistor. $L_3$ is used to cancel the parasitic capacitors. $C_5 \sim C_8$ are DC blocking capacitors. The supply voltage is 1.2V.

![Schematic of proposed complementary push-push FD with NR for CG enhancement](image)

Fig. 4. Schematic of proposed complementary push-push FD with NR for CG enhancement

If $V_{in^+}$ and $V_{in^-}$ are a pair of differential input signals, there are only even-mode harmonics in node $A$ and $B$. Fig. 5 present the simulated transient voltage waveform of the proposed FD with 24 GHz, 0 dBm differential input signal. Since the even-mode harmonics have low amplitude, the voltage swing between node $A$ and $B$ is small, as the blue line. Since the breakdown voltage of 65nm CMOS is about 1.6 V, the risk of device-break-down is very low.

![Simulated transient voltage waveforms with 24GHz, 0 dBm input signal](image)

Fig. 5. Simulated transient voltage waveforms with 24GHz, 0 dBm input signal
The simulated input and output return loss curves are shown in Fig. 6. The input ports’ return loss reaches $-10$ dB at around 23 GHz. The output ports’ return loss is below $-20$ dB at around 46 GHz.

![Fig. 6. Simulated ports’ return loss](image)

The simulated CG of the FD core and FD with NR are shown in Fig. 7. The CG of the FD core circuit reaches $-7.21$ dB at the input frequency of 20 GHz. And the CG of FD with NR reaches $-5.23$ dB at 23 GHz. The NR circuits improves the CG by 2 dB and the input peak-gain frequency by 3 GHz.

![Fig. 7. Simulated CG of FD with and without NR with input power of 0 dBm](image)

The simulated output amplitude imbalance and phase difference with input power of 0 dBm are shown in Fig. 8.

![Fig. 8. Simulated output amplitude imbalance and phase difference with input power of 0 dBm](image)
The output amplitude imbalance is defined as the difference of signal amplitude between port 3 and 4 with 50Ω loads in dB. The phase difference is defined as the difference of signal phase between port 3 and 4 with 50Ω loads in degree. The simulated amplitude imbalance and phase difference of the output 2nd harmonic is shown in Fig.8. The amplitude imbalance is less than 0.3 dB and the phase difference error is less than 3.5 degree.

3 Measurement results

The proposed FD was fabricated using a 65 nm CMOS technology. The CG and FR measurement setup diagram and micrograph of the chip is shown in Fig.9. The size of the proposed FD with NR is 0.72 × 0.36 mm² without pads. On chip measurements were performed using a Cascade SUMMIT 11000 high frequency probing system. The differential input signals were generated by Rohde-Schwarz SMP04 signal generator and KRYTAR 4060265 3-dB 180-degree hybrid couplers. The output signal under 50 GHz were measured by Agilent E4448A spectrum analyzer, and for the output above 50 GHz, Agilent 11974 down-mixer is used together with E4448A. The power supply and bias voltage were provided by two Agilent 66309D DC source.

The simulated and measured CG with 0 dBm input power is shown in Fig.10. The maximum simulated CG is −5.2 dB at 23 GHz input frequency, and the maximum measured CG achieves −6.1 dB at 24 GHz input frequency.
The 3-dB bandwidth is approximate 40 ~ 54 GHz of output frequency.

The simulated and measured output amplitude imbalance with 0 dBm input power is shown in Fig.11. The measured output amplitude imbalance is less than 0.5 dB.

The measured FR with 0 dBm input power is shown in Fig.12. The minimum measured FR is 29.5 dB. The FD core draws 11.5 mA and the NR circuit draws 1.8 mA from the 1.2 V DC supply. The power consumption of the whole chip is 16 mW.

![Fig. 10. Simulated and measured CG with input power of 0 dBm](image1)

![Fig. 11. Simulated and measured output amplitude imbalance with input power of 0 dBm](image2)

![Fig. 12. Measured FR with input power of 0 dBm](image3)
Table I compares the performance of the proposed FD with other state-of-art active CMOS FDs. This work presents the highest CG and competitive FR and power consumption in millimeter-wave frequency band.

Table I. Summary of proposed FD’s performance and comparison with previous recently published designs

<table>
<thead>
<tr>
<th>Reference</th>
<th>1</th>
<th>4</th>
<th>9</th>
<th>This work</th>
</tr>
</thead>
<tbody>
<tr>
<td>Structure</td>
<td>Single-transistor</td>
<td>Current-reuse distributed</td>
<td>Push-push</td>
<td>Complementary push-push with NR</td>
</tr>
<tr>
<td>Output Frequency (GHz)</td>
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<td>50∼69</td>
<td>18 ∼ 26</td>
<td>15 ∼ 36</td>
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<tr>
<td>Bandwidth (%)</td>
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<td>82.4</td>
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<td>Peak Conversion Gain (dB)</td>
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<td>−15.3</td>
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<td>Fundamental Rejection (dB)</td>
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<td>∼ 18</td>
<td>30 ∼ 40</td>
<td>&gt; 33</td>
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<tr>
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<tr>
<td>Size (mm²)</td>
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<td>0.65</td>
<td>0.28</td>
<td>0.33</td>
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<tr>
<td>P₀DC (mW)</td>
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<td>4</td>
<td>10.5</td>
<td>4 ∼ 11</td>
</tr>
<tr>
<td>Technology</td>
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<td>65 nm CMOS</td>
<td>0.18 µm CMOS</td>
<td>65 nm CMOS</td>
</tr>
</tbody>
</table>

1 Two frequency doublers with same structure are presented in [1].
2 Two frequency doublers in different process with same structure are presented in [9].

4 Conclusion

A full-differential frequency doubler employing complementary push-push structure with negative resistance for conversion gain enhancement is presented. The proposed FD chip is fabricated using 65 nm CMOS process, and the core scale of the proposed FD chip is 0.72 × 0.36 mm². Measurement results of the proposed frequency doubler show very good conversion gain of −6.1 dB at 48 GHz output frequency with 3-dB bandwidth of 40 ∼ 54 GHz. The output amplitude imbalance is less than 0.5 dB. The fundamental rejection is above 29.5 dB and the power consumption is about 16 mW.

Acknowledgments

The authors would like to thank the National Science Foundation of China (No.61474021) for financially supporting this research.