

A Low-Voltage Chopper-Stabilized Amplifier for Fetal ECG Monitoring With a 1.41 Power Efficiency Factor

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A Low-Voltage Chopper-Stabilized Amplifier for Fetal ECG Monitoring with a 1.41 Power Efficiency Factor

Shuang Song, *Student Member, IEEE*, Michaël Rooijackers, *Student Member, IEEE*,
Pieter Harpe, *Member, IEEE*, Chiara Rabotti, *Member, IEEE*, Massimo Mischi, *Senior Member, IEEE*,
Arthur van Roermund, *Senior Member, IEEE* and Eugenio Cantatore, *Senior Member, IEEE*

Abstract—This paper presents a low-voltage current-reuse chopper-stabilized frontend amplifier for fetal ECG monitoring. The proposed amplifier allows for individual tuning of the noise in each measurement channel, minimizing the total power consumption while satisfying all application requirements. The low-voltage current reuse topology exploits power optimization in both the current and the voltage domain, exploiting multiple supply voltages (0.3, 0.6 and 1.2V). The power management circuitry providing the different supplies is optimized for high efficiency (peak charge-pump efficiency = 90%). The low-voltage amplifier together with its power management circuitry is implemented in a standard 0.18 μ m CMOS process and characterized experimentally. The amplifier core achieves both good noise efficiency factor (NEF=1.74) and power efficiency factor (PEF=1.05). Experiments show that the amplifier core can provide a noise level of 0.34 μ Vrms in a 0.7 to 182Hz band, consuming 1.17 μ W power. The amplifier together with its power management circuitry consumes 1.56 μ W, achieving a PEF of 1.41. The amplifier is also validated with adult ECG and pre-recorded fetal ECG measurements.

Index Terms—fetal electrocardiography, frontend amplifier, low-voltage, low-power, current-reuse, NEF, PEF.

I. INTRODUCTION

HIGH-RISK pregnancies are becoming more and more prevalent because women choose to have children at progressively higher age. Nowadays, over 10% of all pregnancies are seriously complicated [1], resulting in rising numbers of perinatal morbidity and mortality. Regular recording of the fetal electrocardiogram (fECG), which enables fetal heart beat rate (fHR) measurement, has been demonstrated to be useful for fetal health monitoring [2, 3]. To give an example, observing the fetal heart response to uterine contractions, which can be extracted from non-invasive measurements of the electrohysterogram (EHG), is a widely used procedure to recognize fetal distress [4, 5].

State-of-the-art fetal monitoring systems [6] are larger than a smart phone. To improve user comfort and make fetal-monitoring solutions more appealing to a large public, we propose a patch-like wearable system which integrates electrodes, electronics and a coin battery, as shown in Fig. 1 (a).

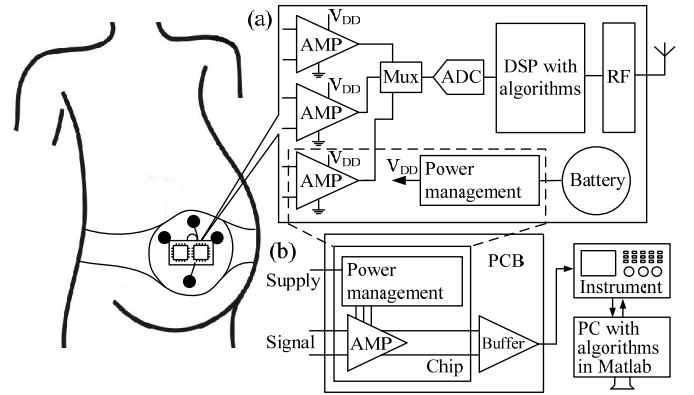


Fig. 1 (a) The system concept and (b) the taped-out frontend amplifier chip with test board and experimental setup

Ultra-low power consumption is paramount in such a wearable system, to enable miniature battery size and prolong the operational lifetime. To give an example, a 1.4V zinc-air button battery with a capacity of 620mAh [7] is able to provide about 350 μ W of continuous power when used for three months. Current biomedical monitoring systems usually include frontend amplifiers, a multiplexed ADC and a radio that sends raw data. In this case the power consumption is dominated by the radio. Recent advances employ on-body signal processing to extract the physiological information before transmission [8], reducing the RF transmission power to a negligible level and achieving a lower total consumption. Accordingly, in our system we envisage three amplification channels, a DSP to implement the fetal monitoring algorithms, power management circuitry and a radio - Fig. 1 (a). In this case, the system power consumption is usually dominated by the signal processing power in the DSP, while the frontend amplifier consumes the majority of the rest. Therefore, the power optimization on the analog circuitry should focus on the frontend amplifier.

Most of the power in the amplifier is needed to keep a suitably low input-referred noise, ensuring fetal heart rate detection. Several bipolar measurement directions are typically needed in fetal ECG systems, because the position of the fetus is unknown and changes in time [9]. The total system power could thus be minimized by assigning dynamically most of the power (and thus the lowest noise level) to the measurement direction that captures the largest fECG signal. The noise specifications on all other measurement directions can then be relaxed, strongly decreasing the power consumption in these channels. A trial and error approach is used to find the measurement direction that yields the best signal. Meanwhile,

the system is still enabling on the other channels maternal ECG measurement (mECG—which is typically 10 to 20 times larger than the fECG) and fECG peak amplitude detection, to follow the movement of the fetus and trigger possible changes in the optimum measurement direction.

Summarizing, a frontend amplifier for wearable fECG monitoring should have excellent power efficiency and a tunable noise range. Extensive circuit research in recent years has resulted in amplifier designs for biomedical sensing applications reaching a noise efficiency factor (NEF) as low as 1.52 [10, 11]. The research towards further optimization on the NEF begins to saturate. However frontend amplifiers exploiting power optimization in both current and voltage domain are not fully explored yet.

In this paper, two approaches for fECG monitoring amplifiers achieving state-of-the-art NEF are presented: a stacked current-reuse multi-channel amplifier [12] and a low voltage chopper-stabilized current-reuse amplifier. The latter topology is implemented in a standard 0.18 μ m CMOS technology and experimentally characterized. Fig. 1 (b) shows a block diagram of the frontend amplifier chip, which includes the low-voltage amplifier and power management circuitry. Measurement results show that this low-voltage amplifier consumes 1.17 μ W in the core (thus excluding the power management circuitry), achieving an NEF of 1.74 and a power efficiency factor (PEF) of 1.05 in low noise configuration. In this work all signal processing algorithms are implemented in Matlab® running on a PC.

The paper is organized as follows. In Section II the system for fECG monitoring is described in detail. In Section III the stacked current-reuse multiple-channel frontend amplifier [12] is described. In Section IV, the novel low-voltage frontend amplifier is presented and analyzed. In Section V, the two topologies are compared and the advantages of the low-voltage amplifier for a fECG system are discussed. The power management circuitry to perform voltage conversion is analyzed in Section VI. Measurement results of the low-voltage amplifier are presented in Section VII, and conclusions are drawn in Section VIII.

II. FETAL ECG MONITORING SYSTEM

The amplitude of the fECG strongly depends on gestational age, inter-electrode distance, and measurement orientation with respect to the moving fetal heart [9, 13]. In the last 12 weeks of pregnancy, when the fetus is usually head-down, the fECG measurement direction that offers maximum SNR is typically one of the three shown in Fig. 2(a) [9]. In this picture the electrodes defining the three bipolar fECG measurement directions are shown in dark and are placed at a distance of 16cm. An additional ground electrode is introduced to connect the body to the electric ground and reduce power line interference. This 5-electrode configuration can be embedded in a comfortable patch. Measurements with this patch provide typical fECG amplitudes between 3 and 20 μ V and enable also recording of the EHG [9].

The algorithm for fECG monitoring described in [14] consists of three steps: maternal ECG (mECG) peak detection,

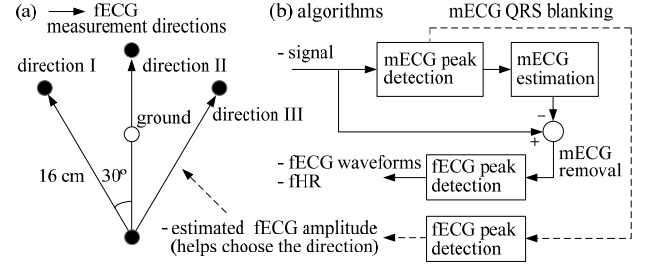


Fig. 2 (a) Electrode grid for fECG measurement and (b) combination of algorithms used for fECG measurement

accurate mECG estimation/removal, and fECG peak detection, as shown in Fig. 2(b) with continuous lines. The computational complexity of the algorithm is usually dominated by the mECG waveform estimation. In [14], a dynamic mECG template is matched to the time stamps of each wave provided by the first step. This approach minimizes the residual maternal component after mECG removal, enabling an accurate extraction of the fECG, but is computationally intensive (10 times more complex than the mECG peak detection). Alternatively, the simple algorithm described in [15] can be used just to evaluate the amplitude of the fECG signal. In this algorithm the QRS-waves in the mECG are simply blanked after peak detection, as shown in Fig. 2(b) with dashed lines, leaving a subset of fECG peaks from which the fECG amplitude can still be estimated. This simple algorithm consumes only 10% of the computational power needed for the complex algorithm in [14].

To minimize computational power while maintaining fECG signal quality, we propose to run the complex algorithm [14] only on the channel with the best signal quality. The largest frontend current will also be assigned to this channel, to minimize added electronic noise. At the same time the simple algorithm [15] runs on the other two channels, to monitor the fECG amplitude, helping to choose the optimal measurement direction. Frontend power will be kept in these channels to a much lower level, which is still sufficient to keep a meaningful evaluation of the fECG amplitude. In this way, almost 2/3 of the total system power can be saved [16, 17]. The system dynamically assigns the complex algorithm and minimum frontend noise (by increasing the biasing current of the amplifier) to the channel with highest signal quality, monitoring the signal quality available in the other channels with the low-complexity algorithm [15] to follow the fetal movements.

In the analog frontend the equivalent input noise level for the best channel is chosen to be 0.3 μ Vrms, ensuring sufficient SNR to run the high-accuracy algorithm. For the other two channels the allowed input noise can be increased to 1.0 μ Vrms.

III. STACKED MULTIPLE-CHANNEL FRONTEND AMPLIFIER

The frontend amplifier defines the noise level of biomedical acquisition systems. It usually applies a capacitive feedback as shown in Fig. 4(a) to define an accurate gain without introducing noise due to the feedback components [18]. Power optimization of the frontend amplifier in the current domain to improve the efficiency becomes increasingly difficult [10, 11], while optimization in the voltage domain can still achieve

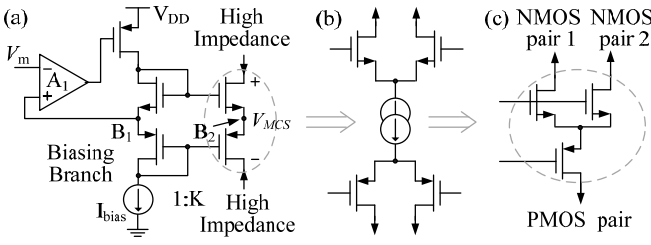


Fig. 3 (a) The proposed mid-rail current sink/source (MCS), (b) connection of two differential pairs and (c) split of the NMOS [12]

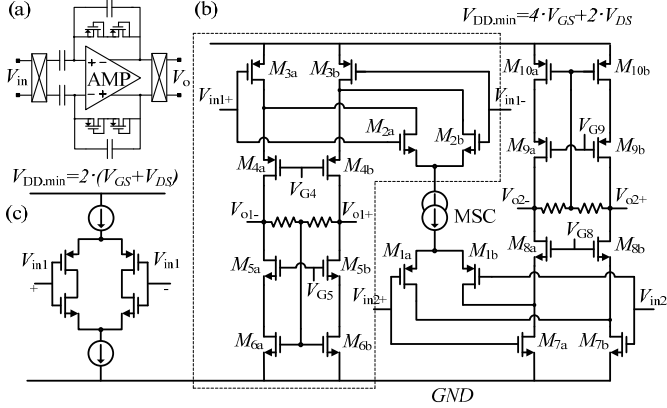


Fig. 4 Proposed current reuse folded-cascode amplifier with MCS [12]

Table I Transistors sizing for the folded-cascode amplifier with MCS

Transistors	$M_{1a,b}$	$M_{7a,b}$	$M_{8a,b}$	$M_{9a,b}$	$M_{10a,b}$
W/L ($\mu\text{m}/\mu\text{m}$)	600/0.3	240/0.3	10/1	20/1	2/6
Transistors	$M_{2a,b}$	$M_{3a,b}$	$M_{4a,b}$	$M_{5a,b}$	$M_{6a,b}$
W/L ($\mu\text{m}/\mu\text{m}$)	240/0.3	600/0.3	20/1	10/1	1/6
Transistors	M_{MSCP} (p-transistor in MSC)		M_{MSCN} (n-transistor in MSC)		
W/L ($\mu\text{m}/\mu\text{m}$)	12/0.5		6/0.5		

significant savings. This is because the input and output signal swings of the frontend amplifier are small, allowing for an aggressive reduction of the supply voltage. For this reason, more than one amplifier can be stacked between the rails, enabling reuse of the current among different channels, as further described in this Section.

A. Current reuse with mid-rail current sink/source

A mid-rail current sink/source (MCS) enabling current-reuse among different channels is proposed in Fig. 3 (a) to provide a power efficient frontend system with a single power supply. The MCS consists of an NMOS and a PMOS transistor with their sources connected. The gate voltages are provided by the biasing branch on the left side.

All transistors (N and PMOS) in the MCS and in the amplifiers that are discussed in following sections are biased in weak inversion. To ensure that these transistors are also in saturation, the minimum V_{DS} ($V_{DS,min}$), for both N and PMOS, should be larger than 4 times the thermal voltage, i.e. about 100mV. Therefore, the voltage across the MCS (V_{MCS}) should be sufficiently high ($V_{MCS} \geq 2V_{DS,min}$). The voltage at B_2 is kept equal to the one at B_1 by amplifier A_1 , which is implemented by a simple differential pair with active load.

The MCS features high impedance at both output terminals (drains). Therefore, it allows for connection of two independent differential pairs at both outputs as shown in Fig. 3 (b): an NMOS pair on the top and a PMOS pair at the bottom, which are driven separately by two different inputs. Based on this technique, a stacked amplifier with current reuse technique for fECG monitoring applications can be proposed.

B. Stacked current-reuse folded-cascode topology

A stacked current-reuse folded-cascode amplifier topology exploiting a MCS [12] is shown in Fig. 4 (b). The transistor dimensions are given in Table I. Compared with a conventional folded-cascode topology, the current source transistors $M_{3a,b}$ and $M_{7a,b}$ are driven together with the input pairs $M_{1a,b}$ and $M_{2a,b}$ to reuse the current and thus double the effective g_m . Still as shown in Fig. 4 (b), the input stages of two folded-cascode amplifiers can share the same bias current and the same MCS, taking advantage of the limited supply voltage needed for the input stage in fECG applications.

Summarizing, in the current domain, the current through the MCS is reused four times and, therefore, the equivalent NEF for one channel is reduced to half of the one for a single differential pair (NEF_0 in eq.1). More in detail, the voltage noise for one channel is reduced to $1/\sqrt{2}$ of the original value because $M_{3a,b}$ and $M_{7a,b}$ are driven together with the input pairs. At the same time, the current consumed per channel is reduced to half because the MCS enables sharing the same bias for two channels. One should observe that the current in the output stage is typically just 5% of the one in the input stage of folded-cascode amplifiers for biomedical applications, and thus it will not substantially deteriorate the NEF. The NEF of each channel in the stacked current-reuse topology can thus be calculated to be:

$$NEF_{stacked} = \frac{V_{rms}}{\sqrt{2}} \sqrt{\frac{2 \cdot (I_{tot}/2)}{\pi \cdot V_t \cdot 4kT \cdot BW}} = \frac{NEF_0}{2} \quad (1)$$

As all transistors in this design are in weak inversion and the thresholds for P and N type are similar in absolute value ($\approx 300\text{mV}$), the gate-source bias voltage V_{GS} is basically the same for all transistors. Therefore, in the voltage domain, the minimal supply voltage of the proposed amplifier is $4V_{GS} + 2V_{DS,min}$ ¹, as shown in Fig. 4 (b). In comparison, the current reuse amplifier [11] shown on the left in Fig. 4 (c) needs a minimal supply voltage of $2V_{GS} + 2V_{DS,min}$ (the voltage across the current source and current sink is also equal to one $V_{DS,min}$ in its implementation) but provides only one channel rather than two. Considering that two channels with identical noise level will be provided, the power consumption of these topologies can be compared in Eq. (2), neglecting the current in the second stage of the amplifier in Fig. 4 (c) and the current in the output stage of the stacked current-reuse folded-cascode amplifier in Fig.4 (b).

$$\frac{P_{MCS,FC}}{P_{reuse}} = \frac{I \cdot (4V_{GS} + 2V_{DS})}{2I \cdot (2V_{GS} + 2V_{DS})} = \frac{2V_{GS} + V_{DS}}{2V_{GS} + 2V_{DS}} \quad (2)$$

¹ $V_{GS3} + V_{GS2} + V_{MCS,min} + V_{GS1} + V_{GS7} = 4V_{GS} + 2V_{DS,min}$

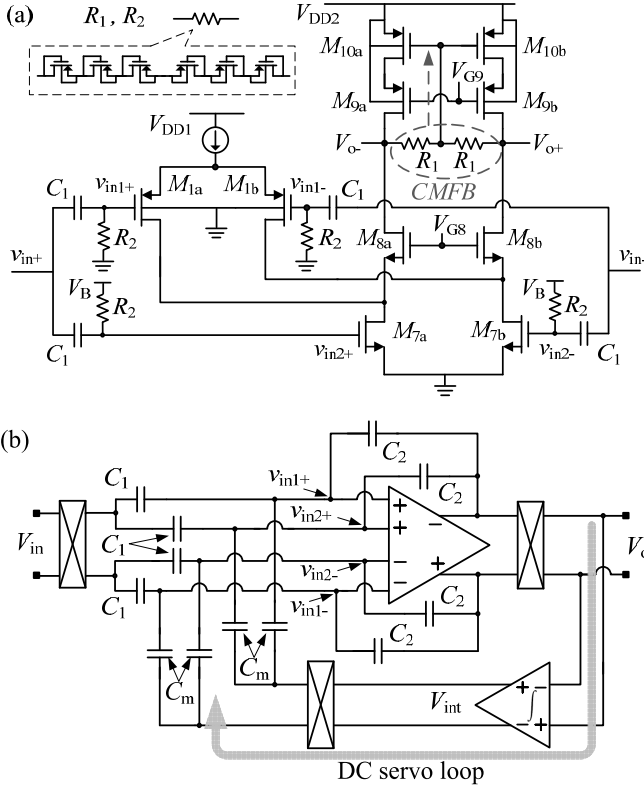


Fig. 5 (a) Proposed low-voltage amplifier and (b) The amplifier with feedback network and DC servo loop

Table II Transistor sizing for the low voltage amplifier core

Transistors	M _{1a,b}	M _{7a,b}	M _{8a,b}	M _{9a,b}	M _{10a,b}
W/L (μm/μm)	500/0.5	200/0.5	10/0.5	20/0.5	2/12

In this formula $P_{MCS,FC}$ is the consumption of the amplifier with MCS and P_{reuse} the power needed for the amplifier in Fig. 4(c). Plugging in eq. 2 the actual values of the bias voltages V_{GS} and V_{DS} , a 20% reduction in power can be estimated for the amplifier with MCS compared to the current-reuse solution of Fig. 4 (c).

Finally, the NMOS transistor in the MCS can be split in 2 identical ones as shown in Fig. 3 (c), providing two channels above the MCS, each with half current (in this case there are two copies of the amplifier in the dashed block in Fig. 4 (b)). This configuration provides one low-noise amplifier (below the MCS) and two low-power amplifiers (above the MCS), each using half of the current consumed in low-noise amplifier. **A more detailed discussion on this topology can be found in [12].**

C. Drawbacks of the stacked multiple-channel amplifier

The proposed stacked current-reuse amplifier can provide three channels with excellent power efficiency. As discussed in Section II, for fECG one amplifier with a noise level of $0.3\mu V_{rms}$ and two amplifiers with a noise level of $1\mu V_{rms}$ should be provided. Assuming the same NEF , the current consumed in the low power amplifier should be 10% of that in the low noise amplifier [19]. However, the current in the two low power amplifiers (above MSC) is always 50% of that in the low noise amplifier, hence the noise levels of the three channels cannot be tuned individually. This results in unnecessary high power consumption at system level.

IV. LOW VOLTAGE FRONTEND AMPLIFIER

According to the discussion in Section III.C, an amplifier with high power efficiency which allows for individual tuning of the noise level [13, 20] in each channel would be the most suitable choice for our fECG application. Therefore, a novel low-voltage current-reuse folded-cascode topology is suggested.

A. Low voltage current-reuse folded-cascode topology

The proposed low-voltage current-reuse folded-cascode topology is shown in Fig. 5 (a). The transistor dimensions are given in Table II. Current reuse is still exploited as the NMOS and PMOS pairs are driven together. The MCS is not used: instead, power management circuitry including charge pumps and LDOs (low dropout regulators) is employed to scale down aggressively the supply voltage V_{DD1} for the input stage of the folded-cascode amplifier, saving power. In order to further reduce the supply voltage in the input stage, the biasing voltage of the NMOS pair $M_{7a,b}$ and the PMOS pair $M_{1a,b}$ are provided separately. This measure reduces the theoretical value of the minimum supply voltage for the input stage from $2V_{GS} + V_{DS,min}^2$ to $3V_{DS,min}^3$. Besides, the bulk terminals of both PMOS input transistor $M_{1a,b}$ are connected to ground to reduce V_{TH} , avoiding the need for a negative voltage to bias their gates. As a result, V_{DD1} can be as low as 0.3V. The simulated value of leakage current from the PMOS wells is negligible, being below 10pA.

Since the biasing voltages of the NMOS pair $M_{7a,b}$ and the PMOS pair $M_{1a,b}$ are provided separately, two capacitive feedback networks (with $C_1=48pF$, $C_2=1.06pF$, $C_m=2pF$) are required in close loop configuration, as shown in Fig 5 (b). The common mode feedback circuit is implemented with two pseudo-resistors made with PMOS transistors in series as shown in Fig 5 (a), which provides 10GOhm simulated resistance. The supply voltage of the amplifier is designed at 0.3V for the input stage (V_{DD1}) and 0.6V for the output stage (V_{DD2}). For these supply voltages the maximum simulated output swing of the amplifier reaches 530mV. A 1.2V supply is used for the amplifier in the DC servo loop to enable there a large output swing and decrease the size of C_m as discussed in Section IV.B. The power management circuitry that performs voltage conversion will be discussed in Section VI.

Compared with the two-stage amplifier in Fig. 6 (a) [11], the proposed low-voltage current-reuse amplifier has only one dominant pole at the output, providing good stability when used in close loop. The two stage amplifier with two poles is usually compensated by exploiting Miller effect, which makes the pole at the first stage dominant [10]. This may result in an increase in current needed in the second stage to provide enough phase margin. Compared to the telescopic amplifier with current reuse in Fig. 6 (b) [10, 20], this topology allows $3V_{DS,min}$ supply on the main current path, which is typically 50% of the minimum supply ($2V_{GS}+2V_{DS,min}$) required by the telescopic topology. The noise tuning is realized by changing the bias current of the input stage of the proposed amplifier.

² $V_{GS1} + V_{GS7} + V_{DS,min} = 2V_{GS} + V_{DS,min}$

³ $V_{DS1} + V_{DS7} + V_{DS,min} = 3V_{DS,min}$

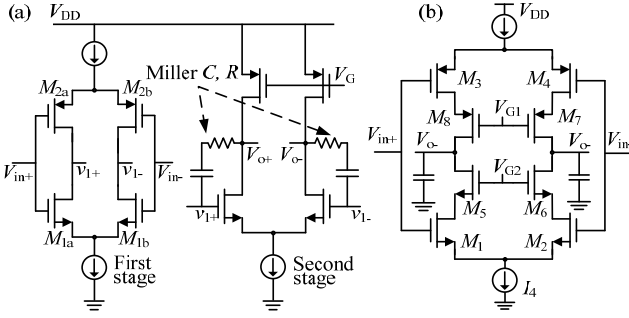


Fig. 6 (a) The two stage topology with current-reuse and (b) the telescopic topology with current-reuse

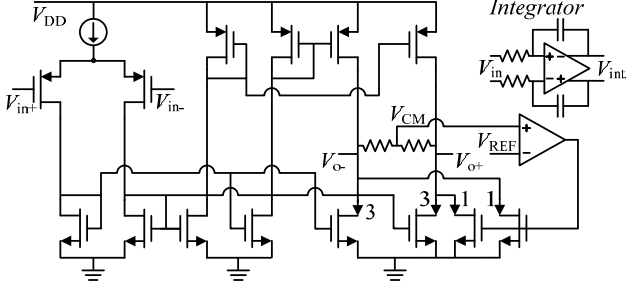


Fig. 7 Amplifier in the DC servo loop

B. DC servo-loop

Chopper stabilization is used in the low-voltage amplifier to cancel offset and $1/f$ noise. Chopping is preferred to auto-zeroing as it avoids noise aliasing [21]. The choppers are implemented by transmission gates. Clock feed-through appears at the chopping frequency, but being this outside the signal band, it can be easily filtered out. A DC servo loop is needed to create a high pass filter that cancels the modulated electrode DC offset and part of the motion artifacts, to prevent saturation of the amplifier [18]. The relation between the maximum DC offset (V_{DEO}) that can be cancelled and the voltage swing of the amplifier in DC servo loop can be expressed as $V_{DEO} \cdot C_1 = V_{int} \cdot C_m$, where V_{int} is output voltage of the integrator in the DC servo loop, C_1 is the input capacitor and C_m is the capacitor connected to the servo loop as shown in Fig. 5(b). The ratio C_m/C_1 should be made large to provide sufficient V_{DEO} cancellation (e.g. 50mV). However, the general input referred noise of the amplifier increases with the ratio C_m/C_1 as shown in Eq. (3). Therefore a relatively high supply voltage (1.2V) is chosen for the amplifier in the DC servo loop in order to increase V_{int} . In this way the ratio C_m/C_1 can be kept less than 1/20, avoiding any significant increase of the input referred noise level, according to the equation:

$$\overline{v_{in,noise}^2} = \left(\frac{C_1 + C_2 + C_m}{C_1} \right)^2 \cdot \overline{v_{amp,noise}^2} \quad (3)$$

The schematic of the amplifier in DC servo loop is shown in Fig 7. Since the output common mode voltage of the main amplifier is 0.3V, a PMOS input pair is used. The first stage and the second stage use both diode-connected loads. Their outputs drive a push-pull output stage to achieve rail to rail output swing and increase V_{int} . The amplifier has only one dominant pole at the output stage. The common mode feedback (CMFB) is applied to the output stage. The current ratio between the CMFB branch and the main branch is 1:3 (Fig. 7), to reduce the gain of the open loop transfer function of the CMFB and

improve stability, while keeping the current consumption low. The amplifier in the CMFB is implemented with a differential pair with active load and the resistors are implemented with PMOS transistors as discussed in section IV. A. The whole servo-loop amplifier consumes only 150nA.

V. COMPARISON OF THE TWO PROPOSED TOPOLOGIES

The proposed low-voltage amplifier topology suits the fECG application better than the stacked current-reuse amplifier since it allows individual tuning of the noise in each channel of the system. The NEF is widely used for comparison of the power efficiency of frontend amplifiers, however only the current consumption is considered in this figure of merit. A power efficiency factor (PEF) that also includes the supply voltage V_{DD} is introduced as $PEF = NEF^2 \cdot V_{DD}$ to allow better comparison of power efficiency for amplifiers with different supply voltages [22]. For an amplifier with multiple supply voltage we suggest to calculate the PEF as in eq. (4), where I_{tot} is the total current consumption used to calculate the NEF , and P_{tot} is the total power consumption of the circuit considered.

$$PEF = NEF^2 \cdot \frac{P_{tot}}{I_{tot}} \quad (4)$$

According to the approach discussed in Section II, for the fECG system should be provided one channel with $0.3\mu V_{rms}$ noise level and two channels with $1.0\mu V_{rms}$ noise. The power efficiency of the proposed low-voltage topology and the stacked current-reuse topology can then be compared in Table III based on simulation results. In this Table the core power per channel is the power consumed by the close loop amplifier (including DC servo) tuned to the specified channel noise level, and results in a core NEF/PEF per channel. The core power of all channels is the total power consumed by the two closed-loop amplifiers in low-power mode and the one in low-noise mode. The total power for all channels is the total power of the three amplifiers together with the power management circuitry.

As it can be seen in Table III, the stacked current-reuse amplifier achieves a better NEF than the low-voltage topology in both modes, because the current is reused four times. However, the low-voltage current-reuse topology achieves lower PEF in low-noise mode because of its lower supply voltage (0.3V) in the input stage compared to the 1.0V supply needed for the stacked current-reuse amplifier.

When providing three channels with the different noise specifications described above, the total core power of the low-voltage amplifiers is less than 50% of the core power consumed by the stacked multiple channel amplifier. This is because the proposed topology allows individual tuning of the noise level in each channel, while the stacked multiple-channel topology fixes the relation between the noise level in the low-noise channel and that in the low-power channels. When the power consumed in the power management circuitry is included in the simulation of the low-voltage amplifiers and one LDO (1.2 to 1.0V) is included for the multiple-channel amplifier, the simulated total power of the fECG system based on the low-voltage amplifiers is still 37% lower than the one exploiting the stacked multiple-channel amplifier.

Table III Simulated current consumption of the frontend system

Performances	Topology & mode		Low-voltage current-reuse amplifier				Stacked multiple-channel amplifier			
			Low-noise channel		Low-power channels		Low-noise channel		Low-power channels	
			Current	Supply	Current	Supply	Current	Supply	Current	Supply
Input stage			3.1 μ A	0.3V	0.35 μ A	0.3V	3.1 μ A	1.0V	1.55 μ A	1.0V
Output stage			50nA	0.6 V	50nA	0.6 V	50nA	1.0V	50nA	1.0V
DC-servo amplifier			150nA	1.2 V	150nA	1.2 V	150n	1.0V	150nA	1.0V
Noise level (0.5~180Hz band) \dagger			0.32 μ V _{rms}		1.0 μ V _{rms}		0.32 μ V _{rms}		0.47 μ V _{rms}	
NEF of channel			1.66		2.12		1.17		1.24	
Core power per channel			1.14 μ W		0.31 μ W		1.65 μ W		0.98 μ W	
Core PEF per channel			0.95		2.79		1.37		1.54	
Core power of all channels*			1.76 μ W				3.60 μ W			
Total power for all channels			2.72 μ W				4.32 μ W			

* includes one low-noise channel and two low-power channels \dagger Corner simulations predict a max.5% variation of the input noise

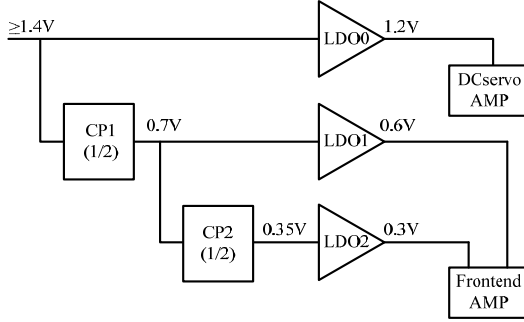


Fig. 8 Scheme of the power management circuitry

VI. POWER MANAGEMENT CIRCUITRY

A. The power management system

The power management circuitry performs on chip all voltage conversions needed for the proposed low-voltage current-reuse amplifier including the DC-servo loop. The design goal is to maximize power efficiency. According to the block diagram in Fig. 8, the circuitry includes two 1/2 step-down charge pumps (CP1, 2) and three LDOs. Three supply voltages are generated for the frontend amplifier (input and output stage of the folded-cascode gain stage) and the DC-servo amplifier. A minimum input supply voltage of 1.4V is required to allow enough dropout voltage in the LDOs.

B. Charge pumps & LDOs

The power efficiency of charge pumps is analyzed and optimized. There are three main contributions to the losses in a charge pump [23]: (1) charge redistribution losses (P_{RL}) that are inversely proportional to the switching frequency f_{sw} ; (2) conduction losses from the switches (P_{CL}) that are frequency independent; (3) switching losses from switches, switch drivers and from the parasitic capacitance at the bottom plate of the capacitors (P_{SL}) that are proportional to f_{sw} . A modified version of the model in [24], which includes also the switching losses P_{SL} and models all power losses by the output impedance R_o (Fig. 9(a)), is used to optimize the power efficiency of the charge pumps. The qualitative behavior of R_o for varying switching frequency is plotted in Fig. 9 (a) (black curve). Due to the sum of the different loss contributions, the minimum R_o (and thus the optimal efficiency of the charge pump) can be

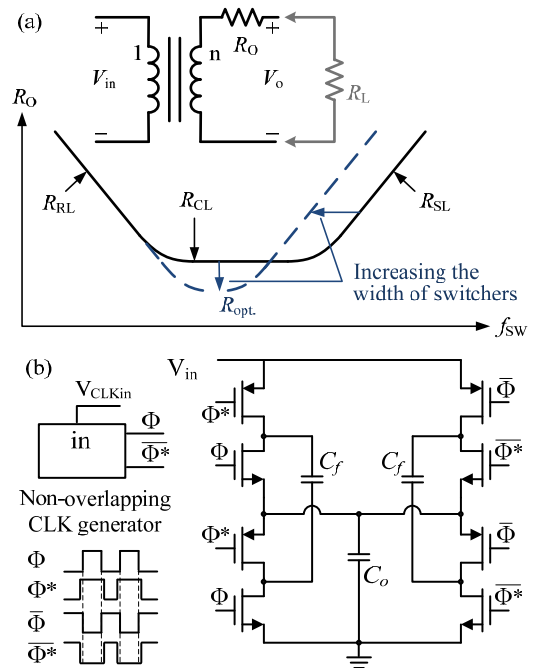


Fig. 9 (a) the model of a charge pump and its output resistance R_o and (b) the schematic of the chosen ladder charge pump with $C_f=100$ pF and $C_o=25$ pF expected at medium frequencies, where the conduction loss is dominant. As shown in Fig. 9 (b), a two-phase implementation of a simple parallel-series topology including two flying capacitors (C_f) is chosen for its good efficiency and low ripple in this region [25].

The power efficiency of the charge pump is maximized following a suitable optimization procedure, which exploits the proposed model of all losses (based on [24]). First, the maximum total on-chip capacitance $C_{tot} = C_o + 2C_f$ is fixed because of the limited chip area. Second, the maximum allowed amplitude of the output voltage ripple V_{rp} is specified. Accordingly, the minimum f_{sw} can be obtained based on C_{tot} , V_{rp} and the load current: $f_{sw} = I_{load}/(2C_{tot} \cdot V_{rp})$. In order to reduce the conduction losses, the width of the switches should be increased, reducing the on-resistance. As shown by the dashed curve in Fig. 9(a), this will result in the increase of the switching losses, since the capacitance of the switches increases with their width, and a decrease of the conduction

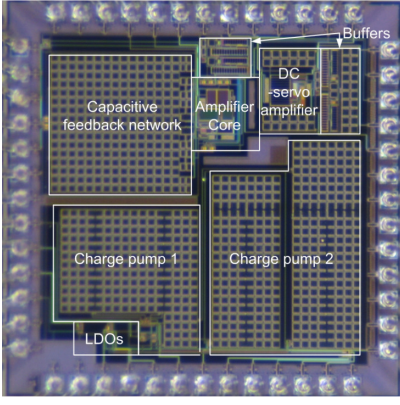


Fig. 10 Die-photo of the prototype amplifier

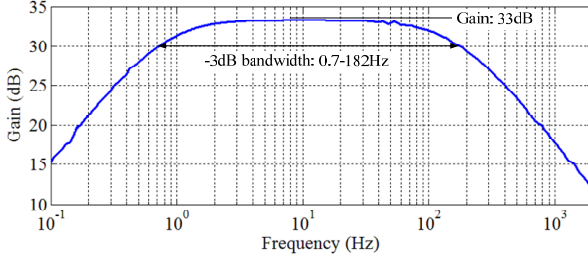


Fig. 11 Measured AC transfer of the amplifier

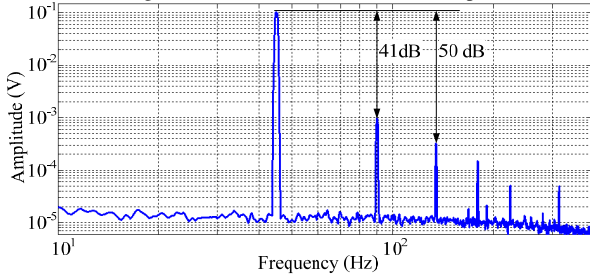


Fig. 12 Measured output spectrum of the amplifier for a 2.3 mV 45Hz signal (a)

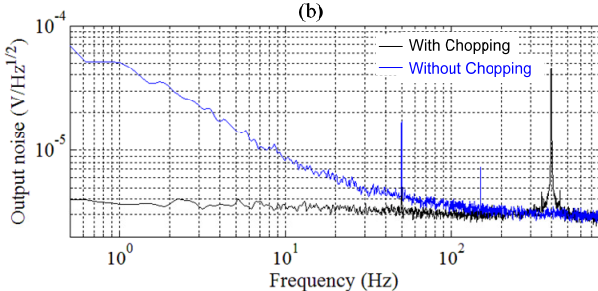
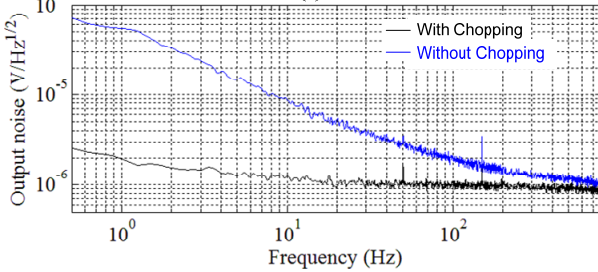


Fig. 13 (a) Output noise spectrum in low-noise mode ($f_{\text{chop}}=4\text{kHz}$) (b) Output noise spectrum in low-power mode ($f_{\text{chop}}=400\text{Hz}$)

losses. The minimum loss is achieved when the corner frequency between conduction and switching losses equals to the minimum f_{sw} calculated before. In this implementation, the f_{sw} is generated off-chip. A Matlab® model is implemented to verify the calculation results. The LDOs are designed for

minimum voltage dropout and minimum current consumption in the loop amplifier.

VII. MEASUREMENT AND BENCHMARKING

The proposed low-voltage amplifier is implemented in a standard $0.18\mu\text{m}$ CMOS process together with the power management circuitry. The amplifier, the feedback capacitors, the DC servo loop, the charge pumps, LDOs and buffers to drive the off-chip load are shown in the die-photo (Fig. 10). These buffers are implemented using an amplifier (differential pair with active load) in unity gain feedback configuration. These buffers limit the signal bandwidth to the desired value by appropriate off-chip loading. The chip occupies an area of 1.6 mm^2 . The performance of this design is verified by suitable measurements.

A. Electric characterization

Fig. 11 shows the measured AC transfer of the amplifier obtained with an Agilent 35670A signal analyzer. The small signal gain is 33dB (45V/V). The -3dB bandwidth is 0.7~182Hz. The linearity is tested by a 45Hz sinusoidal signal with 2.3mV amplitude, to obtain a 1% total harmonic distortion (THD) at the output. This test signal is generated by an Agilent 33250A function generator, which has a measured noise floor of $500\text{nV}/\sqrt{\text{Hz}}$. The chip output is acquired with an Agilent 54642D oscilloscope and processed using Matlab® to apply a second-order 50Hz notch filter and obtain the output spectrum shown in Fig. 12. The second and third harmonics are respectively 41dB and 50dB lower than the fundamental. Fig. 13 shows the output noise spectrum measured with an Agilent 35670A signal analyzer.

The noise performance of the amplifier is measured for two power settings. In the low-noise high-power mode, the chopping frequency is 4kHz and an output noise floor of $1.1\mu\text{V}/\sqrt{\text{Hz}}$ is measured, corresponding to an input-referred noise floor of $24.4\text{nV}/\sqrt{\text{Hz}}$. This results in a V_{rms} of $0.34\mu\text{V}$ in the signal band. In the high-noise low-power mode, the chopping frequency is 400Hz and an output noise floor of $3.3\mu\text{V}/\sqrt{\text{Hz}}$ is measured, corresponding to an input-referred noise floor of $73.3\text{nV}/\sqrt{\text{Hz}}$. This results in a V_{rms} of $1.01\mu\text{V}$ in the signal band. It can be observed that the $1/f$ noise component is effectively removed by the chopper-stabilization. Some 50Hz interference can be observed in the noise spectra. The amplifier core consumes $1.17\mu\text{W}$ ($\text{NEF}=1.74$, $\text{PEF}=1.05$) and $0.30\mu\text{W}$ ($\text{NEF}=2.04$, $\text{PEF}=2.50$) for the two settings, while the whole circuit including power management consumes $1.56\mu\text{W}$ ($\text{PEF}=1.41$) and $0.52\mu\text{W}$ ($\text{PEF}=4.33$) in the two modes.

The charge pumps are measured at $5\mu\text{A}$ current load, which is the total current consumption of the three amplification channels (one in low-noise mode and two in low-power mode). The efficiencies of CP1 and the cascaded CP1/CP2 are plotted in Fig. 14 (a) as a function of the switching frequency. The graph follows a concave shape, as it would be expected looking at the convex shape of the output resistance R_o (Fig. 9 (a)). At low frequencies P_{RL} dominates, and the efficiency increases with f_{sw} ; at high frequency P_{SL} dominates, and the efficiency

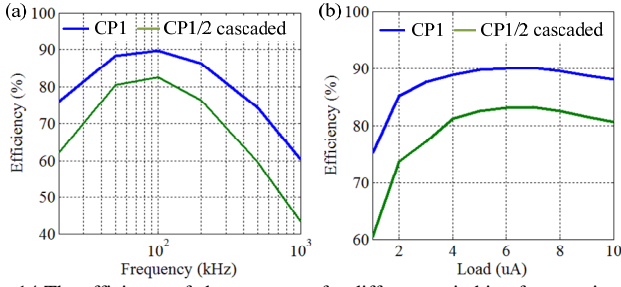


Fig. 14 The efficiency of charge pumps for different switching frequencies (a) and load conditions at a constant $f_{sw}=100\text{kHz}$ (b)

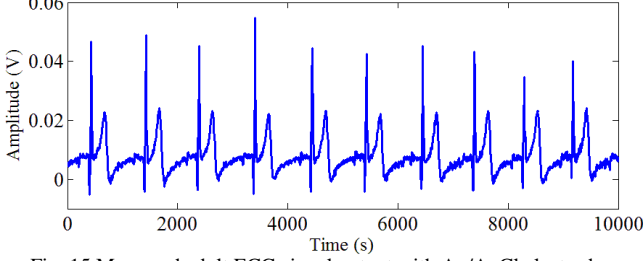


Fig. 15 Measured adult ECG signal output with Ag/AgCl electrode

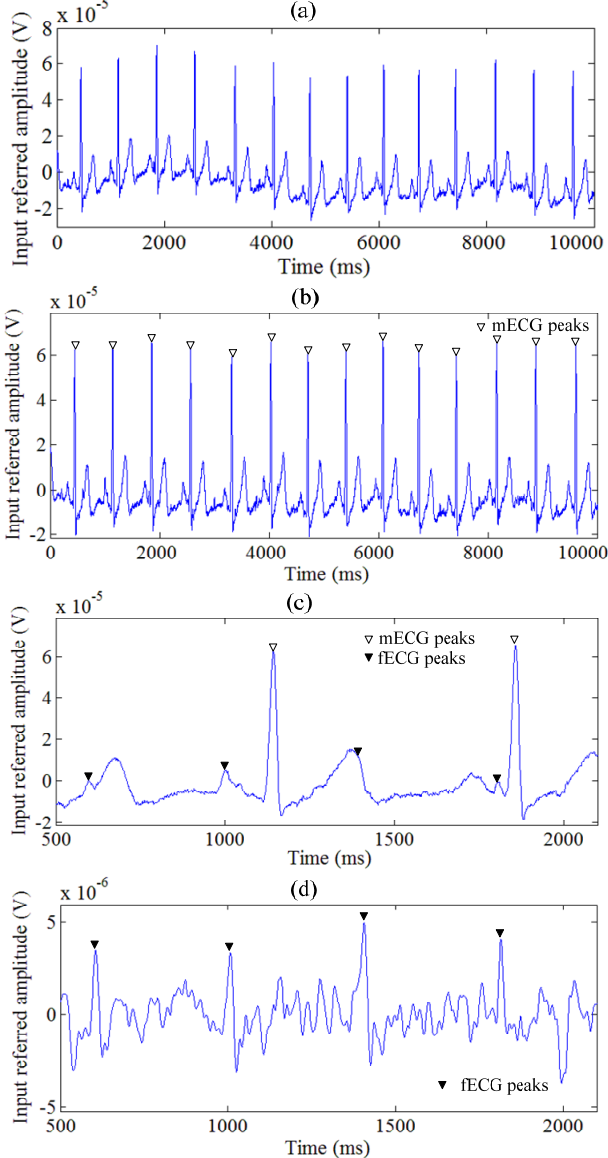


Fig. 16 (a) Original pre-measured signal (b) Measured signal with amplifier in low-noise mode and (c) its zoom-in (d) fECG waveform after mECG removal

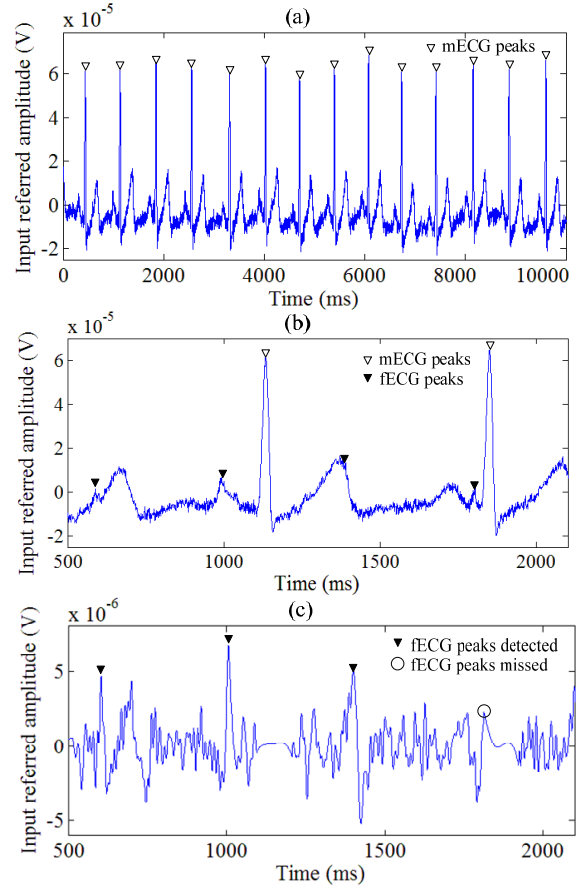


Fig. 17 (a) Measured signal with amplifier in low-noise mode (b) Zoom in of the signal (c) Waveform after running the simple algorithm

decreases with f_{sw} ; as foreseen in the design phase, the efficiency reaches a maximum around 100kHz , where the P_{CL} dominates. In Fig 15 (b), the measured efficiency of the charge pumps at different load conditions is plotted at the chosen $f_{sw}=100\text{ kHz}$. Peak efficiencies are 90% for CP1 and 83% for the cascaded CP1/CP2. The overall efficiency of the power management circuit supplying one low noise and two low power channels is measured to be 68.1%. This figure is calculated as the total output power divided by the input power including the LDOs.

B. Biologic measurements

The proposed low-voltage amplifier is validated measuring an adult ECG in lab environment with commercial Ag/AgCl wet electrodes. With two electrodes placed at only 3cm distance on the chest, an output ECG signal of $45\text{-}50\text{mV}_{pp}$ (corresponding to an input amplitude of $\sim 1\text{mV}_{pp}$) is recorded with the proposed amplifier in low-power mode. The result in Fig. 15 shows a clean ECG waveform.

The amplifier is also verified with pre-recorded signals measured in the 26th week of pregnancy with the electrode configuration of Fig. 2(a). This signal is replayed by an Agilent arbitrary waveform generator 33250A and suitably attenuated to obtain the correct signal amplitude at the input of the chip. In this signal, the maternal ECG (mECG) has $80\mu\text{V}_{pp}$ amplitude, and the fECG amplitude is $5\mu\text{V}_{pp}$, as shown in Fig. 16 (a). An off-chip amplifier INA217 is used to provide 20dB additional gain, the signal is then digitalized with an oscilloscope and processed on a PC using Matlab®. This INA minimizes the

Table IV Benchmarking of the proposed low-voltage amplifier with other works

	[22]	[26]	[20]	[27]	[28]	[29]		[30]	This work	
						BPA2	BPA3		Mode1	Mode2
Year	2013	2013	2014	2011	2012	2012		2013	2014	
Technology	0.18 μ m	0.13 μ m	0.35 μ m	0.5 μ m	0.18 μ m	0.5 μ m	0.13 μ m	0.18 μ m	0.18 μ m	
Supply [V]	0.45	1.5	2.5	2.0	1.0	1.0	1.0	1.0*/1.2**	0.3,0.6,1.2*/ 1.4**	
Gain [dB]	52	40.9	40.7	50	34/40	36	40	54.8	33	
THD @input amplitude	0.53% 2mV	1% 8.25mV	1% 2.5mV	N.A.	N.A.	7.1% 0.5mV	1% 0.5mV	1% 1.6mV	1% 2.3mV	
Bandwidth [Hz]	1-10k	45-20k	0.5-1k	0.2-170	0.2-5.8k	0.3-4.7k	0.1 -10.5k	0.4-5.1k	0.7-182	
Noise BW [Hz]	1-10k	N/A	0.05 -200k	0.2-400	0.2-10k	0.3-4.7k	0.1 -10.5k	0.4-10k	0.7-182	
Noise [μ V _{rms}]	3.2	3.06	2.8	1.7	5.71	3.6	2.2	4.0	0.34	1.01
NEF	1.57	1.64	2.01	4.0	2.59	1.9	2.9	1.9	1.74	2.04
PEF	1.12*	4.03	10.1	32	6.7	3.6	8.4	3.6*	1.05*/1.41**	2.50*/4.33**
Power [μ W]	0.73*	3.9	0.86	3.0	0.8	0.8	12.1	0.8*/1.0**	1.17*/1.56**	0.30*/ 0.52**
CMRR [dB]	73	78	>70	>105	>60	N/A	80	>60	>70	
PSRR [dB]	N/A	80	>70	N/A	>70	5.5	>80	>70	>70***	
Noise Tuning	No	No	Yes	No	No	No	No	No	Yes	

* excluding the power management circuitry

** including power management circuitry

***measured with the LDO

impact of oscilloscope noise on the measurement. The resulting signals (input referred) are shown in Fig. 16 and Fig. 17. The positions of the detected mECG and fECG peaks are annotated.

The waveforms in Fig 16 (b) and (c) are measured with the amplifier in low-noise mode (0.34 μ V_{rms} noise): the fECG peaks are well preserved. The waveform obtained after running the high-accuracy mECG removal algorithm [14] on the signal in Fig. 16 (c) is shown in Fig. 16 (d). The fECG peaks and the fHR are well detected.

The waveforms in Fig. 17 (a) and (b) are measured with the amplifier in low-power (1.01 μ V_{rms} noise) mode. In this case higher noise is visible. The waveform obtained after running the simple algorithm [15] (which blanks the mECG QRS waves) on the signal in Fig. 17 (b) is shown in Fig. 17 (c). It can be observed that the last peak is missing since it overlaps the QRS region of a mECG signal. However, the fECG amplitude can still be estimated from Fig. 17 (c) knowing the position of the fECG peaks which is determined by observing the low-noise channel.

C. Benchmarking

The proposed low-voltage current-reuse folded-cascode amplifier together with power management circuitry is compared to previous related works in Table IV. The supply voltage of this amplifier is the lowest for the amplifier core (0.3V and 0.6V). In spite of the aggressive supply scaling, the measured input amplitude for which a 1% THD is achieved (2.3mV), is similar to the one reported by other designs with comparable gain and 1V supply [29]. The bandwidth and noise level suits well the fetal monitoring application. The PSRR and CMRR are well in line with other works. The gain of this work only includes the preamplifier, and it can be easily increased by

changing the feedback ratio or including a second stage amplifier with little power penalty. The noise level of the low-voltage amplifier can be tuned from 0.34 μ V_{rms}, (1.17 μ W power), to 1.01 μ V_{rms}, (0.30 μ W power), by changing the bias current in the input stage. The measured NEF of 1.74 is among the lowest published, the core PEF of 1.05 improves previous achievements [22], and the PEF including the power management circuitry is 1.41.

VIII. CONCLUSION

A low-voltage chopper-stabilized amplifier is presented in this paper as a further improvement on the stacked multiple-channel frontend discussed in [12]. The low-voltage amplifier allows for individual tuning of the noise level in each channel. Therefore it achieves lower power consumption in a fetal ECG system than the stacked multiple-channel amplifier. The proposed low-voltage current-reuse folded-cascode topology enables a supply voltage of 0.3V in the input stage and 0.6V in the output stage, resulting in significant reduction of the power consumption. The aggressively scaled supply in the input stage is made possible using a suitable bias for the input devices, together with bulk biasing of the PMOS devices and a modified DC servo-loop. The power management circuitry performing on-chip voltage conversion is designed and optimized for high efficiency. The measured power consumption of the amplifier in low noise mode is 1.17 μ W for the core and 1.56 μ W including the power management circuitry, corresponding to a PEF of 1.05 and 1.41, respectively. The amplifier is validated with on-body adult ECG measurements and with a pre-measured mECG+fECG signal.

ACKNOWLEDGEMENT

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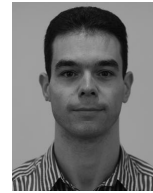
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Shuang Song (S'12) was born in 1983 in Hangzhou, China. He received the B. S. and M.S. degree in electrical engineering from Zhejiang University, Hangzhou, China in 2006 and 2008, respectively. In 2008 he joined a poster-master program in information and communication technology at Eindhoven University of Technology, the Netherlands. Since 2011, he is working towards the Ph.D. degree at the same university. His research interests include low-power analog and mixed signal circuits and systems for biomedical applications, interface circuits for MEMS device and low-power power management circuits.



Michiel Rooijakkers (S'11) was born in 1982 in 's-Hertogenbosch, The Netherlands. In 2009 he started an internship at Philips Research in Eindhoven, where he did research on ultra-low power R-peak detection, obtaining the MSc degree at the University of Technology Eindhoven (TU/e), in 2010. Since September 2010 he is a PhD-student at TU/e, researching the development of a low power wearable system by using abdominal electrodes to determine fetal health.



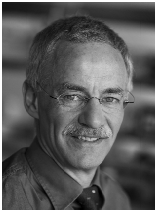
Pieter Harpe (M'11) received the M.Sc. and Ph.D. degrees from the Eindhoven University of Technology, The Netherlands. In 2008, he started as researcher at Holst Centre/imec, The Netherlands. In April 2011, he joined Eindhoven University of Technology as assistant professor on low-power mixed-signal circuits. He is co-organiser of the yearly workshop on Advances in Analog Circuit Design and a member of the Technical Program Committees for ISSCC and ESSCIRC.



Chiara Rabotti (M'08) received the M.Sc. degree in electrical engineering from the University of Florence, Italy, in 2004. In 2010 she received the Ph.D. degree from Eindhoven University of Technology on characterization of uterine activity during pregnancy. She is currently Assistant Professor at the Signal Processing Systems Group at the Electrical Engineering Department of the same university. Her research interests include biomedical signal processing and modeling with specific focus on electrohysterography, electro-myography, and electrocardiography.



Massimo Mischì (M'02-SM'10) received the M.Sc. degree in Electrical Engineering at La Sapienza University of Rome, Italy, in 1999. In 2004, he received the Ph.D. degree from the Eindhoven University of Technology (TU/e), the Netherlands. In 2007, he became assistant professor, and since 2011 he is an associate professor at the Electrical Engineering Department of TU/e. Since 2012, he is director of the Biomedical Diagnostics Research Lab. His research focuses on model-based quantitative analysis of ultrasound, MRI, and electrophysiology signals. He was awarded with the STW VIDI Grant in 2009 and the ERC Starting Grant in 2011 for his research on angiogenesis imaging. He has co-authored over 150 papers, 6 book chapters, and 6 patent applications. Massimo Mischì is vice-Chairman of the IEEE EMBS Benelux Chapter, Secretary of the Dutch Society of Medical Ultrasound, and a board member of the EAU (European Association of Urology) Section of Urological Imaging.



Arthur H.M. van Roermund (SM'95) was born in Delft, The Netherlands, in 1951. He received the M.Sc. degree in EE in 1975 from Delft University of Technology and the Ph.D. degree in Applied Sciences from K.U.Leuven, Belgium, in 1987. From 1975 to 1992 he was with Philips Research Laboratories in Eindhoven. From 1992 to 1999 he has been a full professor at the EE department of Delft University of Technology. In 1999 he joined Eindhoven University of Technology as a full professor, chairing the Mixed-signal Microelectronics Group. From Sept. 2002

to Sept. 2012 he has been director of research of the Department of Electrical Engineering. From 2009 to 2012 he has been a member of the supervisory board of the NRC Photonics research centre. He is chairman of the board of ProRISC, the microelectronics platform in the Netherlands, and vice chair of the ICT-research platform for the Netherlands (IPN). Since 2001, he is standing co-organiser of the yearly workshop on Advanced Analog Circuit Design (AACD). In 2004 he achieved the Simon Stevin Meester award, coupled to a price of 500.000 €, for his scientific and technological achievements. In 2007 he was member of an international assessment panel for the Department of Electronics and Information of Politecnico Milano, Italy; in 2009 for Electronics and Electrical Engineering for the merged Aalto University Finland; and in 2012 for KTH, Stockholm, Sweden. He authored and co-authored about 500 articles and 30 books.



Eugenio Cantatore (M'98, SM'14) received his Master and Ph.D. Degree in Electrical Engineering from Politecnico di Bari, Bari, Italy in 1993 and 1997 respectively. From 1994 to 1999 he was first a Ph.D. student and then a fellow at the European Laboratory for Particle Physics (CERN) Geneva, Switzerland. In 1999 he moved to Philips Research, Eindhoven, The Netherlands as senior scientist and in 2007 joined the Eindhoven University of Technology where he is associate professor.

His research interests include the design and characterization of electronic circuits exploiting emerging technologies as well as the design of ultra-low power micro-systems for medical applications. Dr. Cantatore (co-)authored more than 120 papers in journals and conference proceedings, and 13 patents or patent applications. He is active in the Technical Program Committees of ESSDERC, ESSCIRC and ISSCC and has been member of the Executive Committee of ISSCC. Since 2013 he is chair of the Technology Directions subcommittee of ISSCC. In 2006 he received from ISSCC the Beatrice Winner Award for Editorial Excellence and was nominated in the Scientific American top 50 list. He received the Philips Research Invention Award in 2007 and in 2012 the Best Paper Award from ESSDERC.

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Reviewer: 1

Comments to the Author

Thank you very much for your detailed response. The manuscript and its strength have been improved significantly. A couple of very minor things need to be added in the text. These are things you have addressed in your response but you haven't included in the manuscript, unless I missed them, in which case I apologize. I refer below to Reviewer 1 comments, as numbered in your response.

In 6: Please mention in the text that the algorithms are currently implemented in Matlab on a PC and refer the reader to Fig. 1(b).

Thank you. We added a sentence to clarify this at the end of the paragraph in section I where Fig. 1(b) is introduced (second page, mid of left column):

"In this work all signal processing algorithms are implemented in Matlab® running on a PC."

In 16: Mention at that point in the manuscript that a detailed discussion of this circuit is presented at your ISCAS paper.

We added one sentence to point out this at the end of section III.B:

"A more detailed discussion on this topology can be found in [12]."

In 21. Add in the main text what you say in your response in (1) regarding alternatives for noise reduction and reference the classic Enz and Temes paper from the IEEE Proceedings, which covers most techniques. Add in the text also what you mention in (2) regarding the buffer used with the load for low pass filtering. Mention briefly what the topology of the circuit is (is it a simple transconductor? have you linearized this?, What is the value of the load capacitance and transconductance setting the 182Hz cut-off? (that is if it is a gm-c filter)). The DC servo loop details are already in the text and (3) is perfectly fine.

(1) The chopping technique is indeed widely used for 1/f noise cancellation in biomedical amplifiers for its advantage (no noise aliasing) over auto-zero technique. Therefore we explained it briefly this reason and referred to the suggested paper at the beginning of IV.B:

"Chopper stabilization is used in the low-voltage amplifier to cancel offset and 1/f noise. Chopping is preferred to auto-zeroing as it avoids noise aliasing [21]."

(2) The buffer is implemented with a differential pair with active load, closed in unity gain feedback. The linearity is improved by the unity gain connection. At a cut off frequency of 182Hz, the g_m is $\sim 12\mu S$ and the load capacitor is 10nF off-chip. We added one sentence to explain the buffer at the beginning of section VII:

"These buffers are implemented using an amplifier (differential pair with active load) in unity gain feedback configuration. The buffers limit the signal bandwidth to the desired value by appropriate off-chip loading."

In 23: Please mention in the text if you don't already do so, that f_{sw} is generated off-chip.

This information is added to the text in section VI:

"In this implementation, the f_{sw} is generated off-chip."

One last thing, are any other resistors implemented with pseudo-resistors (e.g. the CMFB of Fig. 7)? If yes, just highlight it in the text. Also briefly mention in the text what is the topology of the CMFB amp of Fig. 7 (I guess it is a simple differential pair with active load).

Indeed the resistors in Fig. 7 are also implemented with pseudo-resistors. The topology of the amplifier there is indeed implemented with differential pair with active load. The above information is added to the text at the end of section IV:

"The amplifier in the CMFB is implemented with a differential pair with active load and the resistors are implemented with PMOS transistors as discussed in section IV.A."

References [6] and [7] may not be the appropriate IEEE way to reference websites. Please amend accordingly if this is the case. In [1] you are missing a dot after 2010. In [8] and [14] there may be a space missing between "no." and "1" and "no." and "3," respectively. In [3], [19], [20], [21], [27], [28] and [29] you refer to "no." as "issue:". Please change this to be consistent with the IEEE style and the rest of your references. You are missing dots after pp in references [12] and [13].

Thank you very much for pointing out this problem. We modified all website references to be consistent with IEEE style.

Once again thank you for revising the document.

Reviewer: 2

Comments to the Author

The authors have addressed most issues properly and improved the writing. A few more comments.

1. The 0.07% THD is given under 1 mV input, which corresponds with 45-50 mV output. This is much less than the maximum 530 mV. The paper should provide the THD under 530 mV output, or maximum output for 1% THD. Does 1% THD occur at 530 mV?

Thanks for your comments. As you suggest we did a new measurement, which shows that with 2.3mV input (~100mV output), the THD is 1%. We updated Fig. 12 and table IV accordingly. The text in sections VII A and C has also been modified to discuss this new result:

"The linearity is tested by a 45Hz sinusoidal signal with 2.3mV amplitude, to obtain a 1% total harmonic distortion (THD) at the output".

"The second and third harmonics are respectively 41dB and 50dB lower than the fundamental. "

"In spite of the aggressive supply scaling, the measured input amplitude for which a 1% THD is achieved (2.3mV), is similar to the one reported by other designs with comparable gain and 1V supply [29]."

2. Since the PSRR is measured with the LDO, it does not show the performance of the amplifier. Please mark it in Table IV.

We added a comment to Table IV: ****measured with the LDO*

3. The conclusion on page 9 line 50 is incorrect. PEF 1.05/1.41 does not include the charge pump and the LDO.

The PEF 1.05 does not include the charge pump and LDO, the number 1.41 does include the charge pump and LDO. This has also been indicated in Table IV.

4. The authors mentioned the reason for using PMOS input pair in Fig 7 is because of the input common mode of 0.3 V. This is not very clear. As discussed, the threshold for N/P are almost the same.

The supply voltage of the amplifier in Fig. 7 is 1.2V. At a 0.3V input common mode voltage, a PMOS pair allows more headroom (0.3V to 1.2V supply) for the V_{GS} of the differential pair and the V_{DS} of the current source than a NMOS pair (which would only allow 0.3V to ground).

5. Page 2 line 25: "the core" (the part excluding power management) is vague and remains unclear until very late of the paper. Consider explaining the "core" explicitly. Also please check the remaining uses in the paper.

We added an explanation the very first time that we mentioned the word "core" in the sixth paragraph of the main text (Section I):

"Measurement results show that this low-voltage amplifier consumes 1.17μW in the core (thus excluding the power management circuitry), achieving an NEF of 1.74 and a power efficiency factor (PEF) of 1.05 in low noise configuration."

6. Page 2 line 55: the sentence is incomplete.

This sentence is modified as follows:

"This 5-electrode configuration can be embedded in a comfortable patch. Measurements with this patch provide typical fECG amplitudes between 3 and 20μV and enable also recording of the EHG [9]."

7. Page 7 line 34: the sentence "The noise performance of ... " fits better in the beginning of the next paragraph.

Thank you very much. We moved the sentence to the beginning of next paragraph.

Reviewer: 3

Comments to the Author

The authors have carefully considered the comments made in the first review. Most issues have been fully satisfactorily solved.

There are only a few very minor points left, which are listed below with respect to the comments from the first review and the authors' replies.

Reviewer's comment:

Abstract + a few times in the manuscript:

Frequently, expressions like "individual tuning of the noise" are found. Although it is clear what is meant, the expression sounds a little confusing, as power / voltage / current are tuned resulting in related noise levels.

Maybe, a better way to express this can be found.

Authors' reply:

The first time we mention noise tuning we, at the end of Section II, we added "The system will dynamically assign the complex algorithm and minimum frontend noise (by increasing the biasing current of the amplifier) to the channel with highest signal quality, monitoring the signal quality available in the other channels with the low complexity algorithm [15] to follow the fetal movements." At the end of Section IV.A, we added "The noise tuning is realized by changing the bias current of the input stage of the proposed amplifier."

Reviewer's new comment:

It is proposed to use present tense instead of future, i.e. "The system dynamically assigns ..." instead of "The system will dynamically assign ..."

Thank you very much for your comments. We changed the sentence as suggested.

Reviewer's comment:

Page 2, column 1, line 31:

"... as shown in Fig. 1(b) with gray lines".

These lines do not appear in my paper, but that may be a pdf artifact. Please check.

Authors' reply:

Thanks, indeed there was a problem. It is fixed now.

Reviewer's new comment:

As the meaning of these lines (now black) is clear without extra comments, maybe you can shorten the sentence and simply write "... as shown in Fig. 1(b)".

We say now "continuous lines" instead of "black lines". Later in this section, we use the dashed lines in the same Fig. 1(b) to visualize the simple algorithm (reference [15]). We thus think that it is wise to keep a difference between continuous and dashed lines.

Reviewer's comment:

Page 3, column 1, line 13:

Please explain "effective gm".

Authors' reply:

The effective gm is the trans-conductance from the input voltage to total output current in small signal model.

Reviewer's new comment:

gm is clear. But why "effective"?

Effective g_m means that both the g_m of the NOMS pair and PMOS pair are included. This, in our view, is a widely used term in literature.

Reviewer's comment:

Page 7, column 1, line 13:

Why is the characterization done at 5 μ A? This condition differs from the operating conditions of your circuits (cf. Table I), so that this does not seem to be a really appropriate condition to evaluate the related circuits in the context of a system view.

Thus, if that comment applies, please provide comparisons and related data in forthcoming figures etc. at more representative conditions. If the comment does not apply, please explain and clarify.

Authors' reply:

The final system should include three amplifiers for three measurement channels. The total current including three amplifiers and the LDOs can reach a maximum of 4.6 μ A. Though this chip only includes one amplifier channel, we designed the charge pumps for the total foreseen load.

Reviewer's new comment:

Understood. However, please provide this information also explicitly in the manuscript!

According to this suggestion, we provided this information in Section VII.A:

"The charge pumps are measured at 5 μ A current load, which is the total current consumption of the three amplification channels (one in low noise mode and two in low power mode)."

Reviewer: 4

Comments to the Author

Thanks a lot to authors for cleaning my concerns. I agree that the THD @ input = 1 mV is pretty good.

1- If THD in table IV was calculated from the Fig. 12, there is some inconsistency. From Fig. 12, ignoring other higher harmonics, the two harmonics, -67 dB and -74 dB, contribute about 0.05%, right? Do I miss something? Please double check it.

2- If PMOS is used as something like a resistor, its nonlinearity would go to worse quickly after the voltage across it is larger than the certain range. 2003-Harrison-JSSC paper shows that. It is better to test THD with a larger output amplitude. Or, it can argue that the tested signal maximum amplitude is smaller than 1 mV.

Thanks a lot. Indeed, your remark 1 is correct, thank you for pointing this out, we address this issue in our answer. For remark 2, we did a new measurement at larger output voltage, as suggested. The measurement shows that with 2.3mV input amplitude (~100mV output), the THD is 1%. We updated Fig. 12 and table IV to include this new measurement. We also modified the text in section VII. A and C to describe this new result:

"The linearity is tested by a 45Hz sinusoidal signal with 2.3mV amplitude, to obtain a 1% total harmonic distortion (THD) at the output."

"The second and third harmonics are respectively 41dB and 50dB lower than the fundamental".

“In spite of the aggressive supply scaling, the measured input amplitude for which a 1% THD is achieved (2.3mV), is similar to the one reported by other designs with comparable gain and 1V supply [29].”