Device engineering for high-performance, low-voltage operating organic field effect transistor on plastic substrate

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DEVICE ENGINEERING FOR HIGH PERFORMANCE, LOW VOLTAGE OPERATING ORGANIC FIELD EFFECT TRANSISTOR ON PLASTIC SUBSTRATE

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Abstract

Various aspects in device engineering were tackled to realize high performance, low voltage operating organic field effect transistor on plastic substrate. Contact resistance between the active layer and metal electrodes was decreased employing oxide interfacial layers. Anodization of Al gate served as high capacitance dielectric layer enabling low voltage operation of the devices. Several polymers were investigated in passivating the surface of the oxide dielectric to decrease the interfacial trap densities and to enhance surface smoothness. Finally using these optimum conditions, devices on plastic substrate were fabricated, which yielded mobility higher than 2 cm²/Vs, without hysteresis, operating below 5 V, current on/off ratio higher than 10⁶ with the prospect of various applications in organic electronics.

1. Introduction

Devices utilizing organic semiconductors have huge potential in the future electronics market with a number of advantages over traditional devices.[¹] They can be cheap and flexible and there is no technological hurdle in fabricating large area devices. Among them, organic field effect transistors (OFET) have been attracting extensive research attention as being the main backbone of electronic circuits.[²-⁵] Impressive achievements have been realized over the last years thanks to the advancements in both chemical and device engineering.[⁶,⁷] Nowadays,
reports with mobility higher than 1 cm$^2$/Vs are quite common for OFETs employing polymer or small molecule active layers.$^{[8,9]}$ However, only few works dealt with the operational stability of the OFETs in the air.$^{[10,11]}$ One of the most promising molecules in terms of mobility and air stability reported so far is Dinaphtho[2,3-b:2’,3’-f]thieno[3,2-b]thiophene (DNTT).$^{[12,13]}$ Low voltage operating, air stable OFETs with DNTT as active layer has been reported showing mobility over 1 cm$^2$/Vs, making them almost ready for some market applications.$^{[11,13]}$ However, for mass production in industrial scale, simplification of the fabrication process is essential. In these studies, which have reported low voltage operating devices, either costly time consuming atomic layer deposition (ALD) or oxygen plasma method has been used for the oxide dielectric fabrication. Another time consuming process, self assembled monolayers (SAMs), has been applied for dielectrics surface passivation.$^{[11,13]}$ Indeed, developing alternative approaches is needed for the simplification of these processes.

In this work, we present our efforts in device engineering of DNTT based OFETs with main focus on process simplification. For this purpose, we first addressed an important issue in OFETs, which is the contact resistance. Although oxides, such as MoO$_3$ have been applied in a number of systems for hole injection/extraction layers, systematic study has not been carried out for DNTT based devices.$^{[14,15]}$ Here, we applied WO$_3$ and MoO$_3$ in combination with Ag and Au contacts for observing detailed contact resistance behavior of these devices. Then we fabricated our dielectric oxide using anodization, which is basically a solution based process for oxide growth.$^{[16]}$ Moreover, anodization allows for well controlled stoichiometry of the oxide. Third step of optimization process concerns oxide dielectric surface passivation. Various polymers were investigated through simple spin coating. Apart from passivating interface traps, polymers can have additional smoothening effect on the oxide surface, while SAMs only follow the surface structure. Finally, anodization of the gate, together with best performing dielectric surface passivation and optimum oxide/metal source/drain contacts
allowed us to achieve high performance OFET device on plastic substrate. These devices showed almost no hysteresis. Mobility reached above 2 $\text{cm}^2/\text{Vs}$ and current on/off ratio surpassed $10^6$ while operating below 5V.

2. Materials and methods

DNTT (sublimed grade, 99%; see Fig.1 (a) for molecular structure) and Poly (methyl methacrylate) (PMMA) were purchased from Sigma-Aldrich. Polystyrene (PS) was obtained from Pressure Chemical. Poly(1-vinyl-1,2,4-triazole) (PVT) was synthetized by collaborating partner.[17] Three different substrates were used for specific studies (see Figure 1).

For contact resistance studies, highly n-doped silicon substrate with thermally grown SiO$_2$ (200 nm) was used as both gate and dielectric layer. After cleaning with acetone, ethanol and isopropanol for 10 mins each, PVT was spin coated (2000 rpm/60 sec) from a solution in water (3 mg/ml), and subsequently dried in low vacuum oven at 80 °C for two hours forming about 10 nm of passivation layer[17]. 30 nm of DNTT was thermally evaporated at a rate of 0.01 nm/s under vacuum. Au, Ag, MoO$_3$/Au, WO$_3$/Au, MoO$_3$/Ag and WO$_3$/Ag were thermally evaporated through shadow masks as source/drain contacts. 0.1 nm/s of deposition rate for first 20 nm, then 0.5 nm/s of deposition rate for the rest of the thickness was used. Oxide thickness was fixed to 10 nm. Different channel lengths of 60 $\mu$m, 80 $\mu$m, 100 $\mu$m, 120 $\mu$m, and 140 $\mu$m were used for quantitative contact resistance analysis with channel width of 1 mm. Device structure is shown in Fig.1(b). In order to have a statistical approach, 40 devices were fabricated for each type of contact.

For low voltage operating devices, glass substrates were used. After cleaning, 100 nm of aluminum gate was deposited by e-beam evaporation through shadow mask. Al gate was partially anodized to obtain 35 nm of Al$_2$O$_3$ dielectric, with a capacitance of 210 nF/cm$^2$. Details of the anodization process were given in reference [17]. Briefly, constant current was
applied between the Al contact and the Pt counter electrode in citric acid electrolyte solution. Final voltage was fixed to control the thickness of the anodized oxide. The thickness was measured using Rutherford Backscattering Spectroscopy. PVT was prepared as mentioned earlier. PMMA and PS were dissolved in chlorobenzene with 3 mg/ml concentration. These polymer solutions were spin coated (2000 rpm/60 sec) to form very thin passivation layers on Al₂O₃ surface and dried in vacuum oven at 80 °C for two hours. Then, DNTT active layer were evaporated as mentioned above. Finally, Au source/drain contacts were deposited through shadow mask. Device channel length was 50 µm and channel width was 1 mm. See Fig.1(c) for device structure. 32 devices were fabricated for each condition for statistical approach. The measured thicknesses for PVT, PMMA and PS with AFM are 7, 13 and 17 nm respectively. MIM structure such as Al/oxide/polymer/Al was prepared to measure the total capacitance of the dielectric bilayer using Agilent network analyzer. The capacitance values taken at the frequency of 10 Hz are respectively 149, 126 and 93 nF/cm² for PVT/Al₂O₃, PMMA/Al₂O₃ and PS/Al₂O₃.

For plastic devices, 50 µm thick polyethylene naphthalate (PEN, from Goodfellow) was used as substrate with proper cleaning and surface treatment. Polydimethylsiloxane (PDMS) acted
as support. The processes of Al anodization, deposition of PS, evaporation of DNTT and WO\textsubscript{3}/Au were the same as described above. Device structure is given in Fig.1(d). Devices were tested using Keithley 4200 Semiconductor Characterization System.

3. Results and discussion

a. Contact resistance

We first used Si/SiO\textsubscript{2}/PVT/DNTT/Au configuration for our OFETs. Typical transfer (in saturation regime) and output characteristics of the device are shown in Fig. 2(a) and 2(b). The device did not show any hysteresis, thanks to PVT acting as passivation layer.\textsuperscript{[17]} Current on/off ratio was higher than \(10^6\). Low threshold voltage of about -3 V and subthreshold slope of 0.2 V/dec and maximum mobility of 0.4 cm\textsuperscript{2}/Vs were obtained. Output curves displayed proper linear and saturation characteristics. Despite all these excellent device parameters obtained, mobility was lower than those of the reported values,\textsuperscript{[12,13]} mainly due to this specific configuration which is open for further optimization.

![Figure 2](image_url)

Figure 2. (a) Transfer characteristics of a typical OFET in saturation regime with a device configuration of Si/SiO\textsubscript{2}/PVT/DNTT/Au. Dashed line shows the gate current; (b) corresponding output characteristics.

Contact resistance is one major limiting factor for achieving intrinsic mobility of an organic active layer in OFET devices.\textsuperscript{[18]} One of the origins of contact resistance is charge injection
barrier between the metal electrode and active layer. \cite{19} Suitable interfacial layers can be applied to minimize it through either doping or facilitated charge transfer. \cite{20} Metal oxides, thanks to their energy level alignment properties at the interfaces, have been applied in organic photovoltaic devices as electron or hole extraction layers. \cite{21} Here we investigated two oxides, namely MoO$_3$ and WO$_3$ as such interfacial layers for efficient hole injection so as to decrease the contact resistance of our OFET devices. Optimum thickness of the oxides was found to be 10 nm, where we compared the OFET performances with 5 nm, 10 nm and 15 nm. It should be noted that this thickness does not form a compact layer but rather large chunks of islands evidenced by AFM (see Figure S1 in Supporting Information).

Transfer curves of the devices with these top electrode combinations are presented in Fig. 3(a). Noticeable difference can be seen in the threshold voltages of the devices, which can be seen from the $V_{GS}$ vs. $I_{DS}^{1/2}$ curves in the inset. Device with Au contacts (Au only, MoO$_3$/Au and WO$_3$/Au) showed higher threshold voltages than devices with Ag contacts (Ag only, MoO$_3$/Ag and WO$_3$/Ag), which can probably be due to higher structural defects at the interface between DNTT with Au contacts comparing to the ones with Ag or charge transfer complex formed with Ag due to stronger metal/organic interactions comparing to Au. \cite{22} A further investigation is necessary to unravel such kind of behavior. We present in Fig. 3(b) the linear part of the output curves ($V_{GS}$=-9 V) of these OFETs with different contact materials. One can clearly observe that the differential output resistance gets smaller with the addition of the oxide layer, which is the case for both Au and Ag top layers. However, for Ag and oxide combination, the effect is much more pronounced, in line with our earlier observation in the transfer curves, where smaller threshold voltages were obtained for the devices with Ag contacts. However, total resistance is the sum of contact and channel resistance, therefore low total output resistance does not necessarily indicate low contact resistance.
In order to quantitatively analyze the contact resistances under these electrode combinations, we fabricated OFETs with different channel lengths: 60 µm, 80 µm, 100 µm, 120 µm and 140 µm and used transfer length method (TLM) to derive the contact resistances ($R_C$), using the following correlation between total output resistance ($R_t$) and channel length ($L$):

$$R_t = R_C + \frac{L}{W \cdot \mu \cdot C_i \cdot V_{DS} \cdot (V_{GS} - V_{th})}$$

where $W$ is the channel width, $\mu$ is the transistor effective mobility, $C_i$ is the dielectric capacitance and $V_{th}$ is the transistor threshold voltage.\textsuperscript{[23]} The intercept at the origin ($L=0$),
after the linear fit of $R_t$ vs. $L$, yields $R_C$ of these different electrode combinations, as shown in Fig. 3(c). It’s interesting to note that the device with Ag contacts showed highest contact resistance even though it yielded relatively low total resistance as previously shown. Clearly, it was due to relatively low channel resistance of the device coming from low threshold voltage. With a work function of 4.6 eV, Ag has high charge injection barrier with respect to the HOMO level of DNTT (5.4 eV).

Our finding infers that contact resistance is mainly dominated by the charge injection barrier. Oxide interfacial layer are expected to decrease such injection barrier. Indeed, with all electrodes of oxide/metal combination, clear decrease in contact resistance was achieved as displayed in Fig. 3(d).

We carried out Kelvin probe measurement to compare the work function of the electrode combinations, and the results are shown in Fig. 4. Much reduced energy level difference was observed for the oxides as compared to Ag and Au only contacts with regard to HOMO level of DNTT (5.4 eV), which led to more efficient charge transfer between active layer and the electrode and consequently lower contact resistance.

Figure 4. Kelvin probe measurement of various electrodes, 10 nm of oxide layers were deposited on top of Ag and Au thin layers
b. Low voltage operating devices

For practical application of OFETs, the operating voltage has to be decreased. Since the mobility of organic active layer is relatively low, increasing the capacitance of the dielectric layer provides a feasible approach. High dielectric constant oxides, such as Al₂O₃, have been applied in OFETs for this purpose.¹²,¹⁷ For high performance OFETs with DNTT as active layer, generally oxygen plasma or atomic layer deposition are used.¹¹,¹³ Both methods use vacuum processing, which are rather costly and time consuming processes. Therefore, in this work, we opted for applying anodization, which is a solution processed approach. Besides, anodization provides flexibility in terms of oxide thickness control comparing to oxygen plasma treatment. Furthermore, stoichiometry of oxide is well controlled by anodization. As oxides have intrinsic charge trapping species, such as oxygen deficient sites and non-bridging oxygen, dielectric surface passivation is critical for optimum performance of OFETs. Passivation with SAMs is commonly used.¹¹, ²⁴ One monolayer thickness indeed does not compensate much the total dielectric capacitance. However, self-assembling of these monolayers on oxide surface generally takes quite long time (over 12 hours). Besides they are strongly reliant on the surface morphology of the oxides. Here, we have chosen an alternative approach by using polymers instead. Deposition and drying of these layers can be completed in rather short period of time (within 2 hours). Dielectric constant, impurities and film forming properties of polymers can all affect OFET device performance. Therefore, we investigated three different polymers, namely PVT (ε : 5~6), PMMA (ε : 3~4) and PS (ε : 2~3) and compared their passivation efficiencies. They were chosen as to investigate also the effect of the dielectric constant on the device performance. In order not to decrease much the total capacitance, very thin layers (~10 nm) were deposited on anodized Al₂O₃ surface. Total capacitances measured from metal/insulator/metal (MIM) structure are 210 nF/cm² for Al₂O₃,
149 nF/cm² for Al₂O₃/PVT, 126 nF/cm² for Al₂O₃/PMMA and 93 nF/cm² for Al₂O₃/PS respectively.

Surface roughness plays also significant role in charge transport in thin film transistors. AFM of Al₂O₃ and polymer coated surfaces are compared in the Fig. 5. As predicted, polymers all manifested smoothening effect on the oxide, underlining the additional advantage of using polymers as passivation layer. Root mean square (RMS) roughness of Al₂O₃ is 0.52 nm, while PVT/Al₂O₃, PMMA/Al₂O₃ and PS/Al₂O₃ are 0.29 nm, 0.28 nm, 0.38 nm respectively.

Transfer characteristics of OFETs with bare Al₂O₃ and the ones passivated with these polymers are shown in Fig. 6(a). Comparison of the output characteristics can be seen in Fig. 6 (b). Device performance parameters are summarized in Table 1.
Figure 6. Transfer characteristics of OFETs in saturation regime with a configuration of glass/Al/Al₂O₃/polymer/DNTT/Au. Polymers are PVT, PS and PVT; (b) Output characteristics of corresponding devices

Device with bare Al₂O₃ evidenced clear hysteresis, which can be attributed to the trapped charges at the surface. Such a hysteresis behavior disappeared in all the devices with PS, PMMA and PVT spin coated on Al₂O₃, indicating efficient oxide surface passivation.

Subthreshold slope (SS) of bare Al₂O₃ device was relatively high (0.19 V/dec) comparing to other devices which had values of around 0.15 V/dec, another indication of the reduction of interface trap densities following polymer treatment of oxide surface. This is despite the fact that total capacitance of polymer passivated dielectrics are smaller than that of bare oxide.

Interface trap densities were calculated based on the correlation below, where \( C_i \) is the dielectric capacitance:

\[
D_{it} = C_i \left( \frac{SS}{(\ln 10)_q} \right) - 1
\]

Table 1 OFET device performance parameters of bare Al₂O₃ and with surface passivation layers on Al₂O₃.

<table>
<thead>
<tr>
<th></th>
<th>( \mu_{lin} ) (cm²/V.s)</th>
<th>( \mu_{sat} ) (cm²/V.s)</th>
<th>( V_{th} ) (V)</th>
<th>SS (V/dec)</th>
<th>( I_{on}/I_{off} )</th>
<th>( D_{it} ) (cm².eV⁻¹)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Al₂O₃</td>
<td>0.20±0.09</td>
<td>0.19±0.07</td>
<td>-0.6±0.1</td>
<td>0.20±0.02</td>
<td>1.7x10⁵</td>
<td>3.1x10¹²</td>
</tr>
<tr>
<td>PVT</td>
<td>0.32±0.08</td>
<td>0.33±0.07</td>
<td>-1.2±0.1</td>
<td>0.17±0.02</td>
<td>5.0x10⁵</td>
<td>1.7x10¹²</td>
</tr>
<tr>
<td>PMMA</td>
<td>0.63±0.22</td>
<td>0.88±0.11</td>
<td>-1.7±0.1</td>
<td>0.15±0.01</td>
<td>3.0x10⁶</td>
<td>1.2x10¹²</td>
</tr>
<tr>
<td>PS</td>
<td>0.91±0.15</td>
<td>1.05±0.12</td>
<td>-1.7±0.1</td>
<td>0.14±0.01</td>
<td>2.1x10⁶</td>
<td>0.8x10¹²</td>
</tr>
</tbody>
</table>
Threshold voltage \( (V_{th}) \) is determined by various factors, such as intrinsic charges, trap densities, charge injection barrier, interfacial dipole moment and dielectric capacitance etc. Bare Al\(_2\)O\(_3\) device gave relatively low \( V_{th} \) at -0.5V, probably coming from shallow traps present at oxide surface which are the source of intrinsic charges released under the operation of OFETs. This was also evidenced by the high off current in Al\(_2\)O\(_3\) device. Further proof could be drawn from the \( V_{th} \) value (-1V) of the back-scan curve that was in the range of \( V_{th} \) in PVT and PS devices.

Maximum saturation mobility achieved from Al\(_2\)O\(_3\), PVT, PMMA and PS devices in average are respectively 0.19 cm\(^2\)/Vs, 0.33 cm\(^2\)/Vs, 0.88 cm\(^2\)/Vs and 1.05 cm\(^2\)/Vs. Improvement in polymer passivated devices comparing to bare oxide can be attributed to the decrease in surface traps. Smoother surface also contribute to better charge transport in organic field effect transistors.\(^{[25]}\) Correlation of dielectric constant and charge transport behavior can be observed from the performances of PVT, PMMA and PS. The smaller is the dielectric constant the higher the mobility. The strength of the dipole moment at the interface is proportional to the dielectric constant. High dipole moment hinders charge transport.\(^{[26]}\) High mobility coupled with low off current allowed us to achieve higher than \( 10^6 \) current on/off ratio in the devices with PMMA and PS.

c. Plastic devices

Applying optimal interfacial layer WO\(_3\)/Au and dielectric surface passivation layer PS, we fabricated OFETs on PEN substrate. Transfer and output characteristics of a typical device operating below 5 V are shown in Fig. 7(a). Gate voltage dependent mobility is also shown. Maximum mobility reached 2.4 cm\(^2\)/Vs. Current on/off ratio was above \( 10^6 \). Current scan did not show clear hysteresis. Output characteristics (Fig. 7(b)) show the high quality of our
devices with nice linear and saturation curves. Device performance parameters are reported in Table 2. Considering that the active layer did not go through annealing treatment during the deposition process, these performances are comparable to the best reported ones based on DNTT, where mobility of 2.1 cm$^2$/Vs was reported. These characteristics indicate the viability of our device engineering approach and show practical application prospects of these devices in some areas of flexible electronics.

![Figure 7](image.png)

Figure 7. (a) Transfer characteristics of a typical OFET in saturation regime with a device configuration of PEN/Al$_2$O$_3$/PS/DNTT/WO$_3$/Au. Gate voltage dependent mobility is shown; (b) corresponding output characteristics of the device.

<table>
<thead>
<tr>
<th>PEN devices</th>
<th>$\mu_{\text{lin,max}}$ (cm$^2$/V.s)</th>
<th>$\mu_{\text{sat,max}}$ (cm$^2$/V.s)</th>
<th>$V_{\text{th}}$ (V)</th>
<th>SS (V/dec)</th>
<th>$I_{\text{On}}/I_{\text{Off}}$</th>
<th>$D_{\text{f}}$ (cm$^2$.eV$^{-1}$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>PEN devices</td>
<td>1.92±0.12</td>
<td>2.38±0.19</td>
<td>-1.3±0.1</td>
<td>0.35±0.05</td>
<td>2 x10$^6$</td>
<td>4.5×10$^{12}$</td>
</tr>
</tbody>
</table>

**Conclusions**

In this work, we report low voltage operating, high performance organic field effect transistor on plastic substrate fabricated through simplified processing conditions. Oxide interfacial layers were included to decrease the contact resistance between the active layer and the
electrodes. Both MoO$_3$ and WO$_3$ led to the decrease of the contact resistance comparing to Au or Ag only electrodes, which has been determined by transfer-length-method. Kelvin probe measurements confirmed better energy level alignment for charge injection when using these interfacial layers. Solution processing process, anodization, was used to form Al$_2$O$_3$ as gate dielectric for achieving high capacitance and consequently low voltage operating devices. Passivation layers using polymers with varying dielectric constants (PVT, PMMA and PS) were compared. AFM analysis evidenced smoothening effect of polymers on the bare oxide surface. All of them passivate the interfacial trap states deduced by hysteresis free and sharp subthreshold slope transfer characteristics of OFET devices. However, lower dielectric constant polymer (PS) tends to yield higher carrier mobility, which can be attributed to detrimental effect of strong dipole moment on carrier transport. Finally, applying WO$_3$/Au as electrodes, Al$_2$O$_3$ as dielectric, PS as dielectric surface passivation layer, we have fabricated OFET devices on plastic PEN substrate. Maximum mobility of these devices reached 2.4 cm$^2$/Vs, operated below 5 V, current on/off ratio surpassed $10^6$ with sharp subthreshold slope, validating our approach in device engineering for this promising air stable organic semiconductor (DNTT).

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